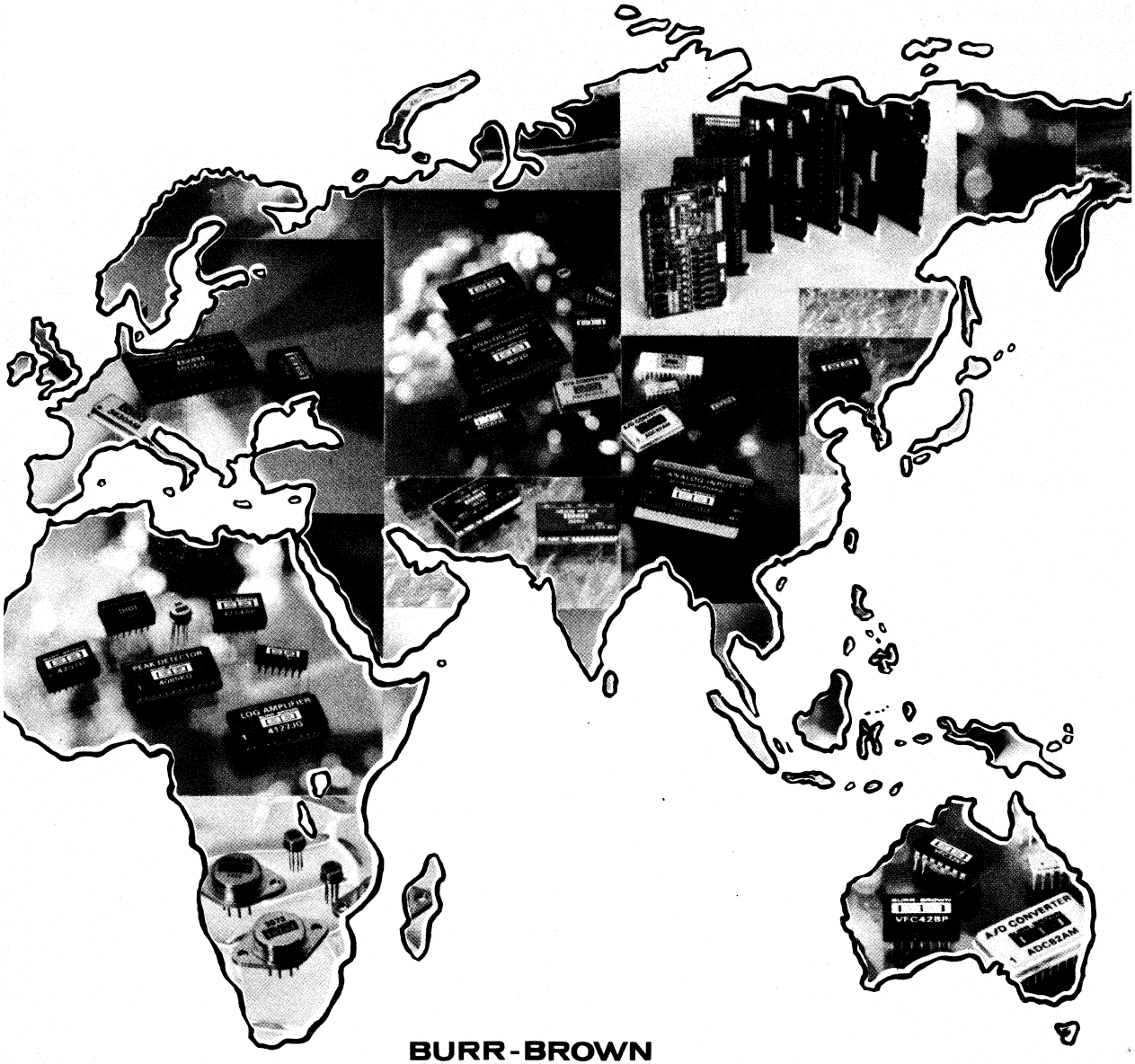
1979 General Catalog



BURR-BROWN

Putting Technology To Work For You

BURR-BROWN

GENERAL CATALOG

BURR-BROWN ...

Building an Unequalled Reputation, Worldwide, for Quality, Performance, Reliability

Data acquisition, signal conditioning, and computer I/O components and systems from Burr-Brown are recognized and used worldwide. Over the past two decades these products have earned a reputation for superior quality, exceptional performance, and consistent reliability - perhaps the best reputation for workmanship in our industry.

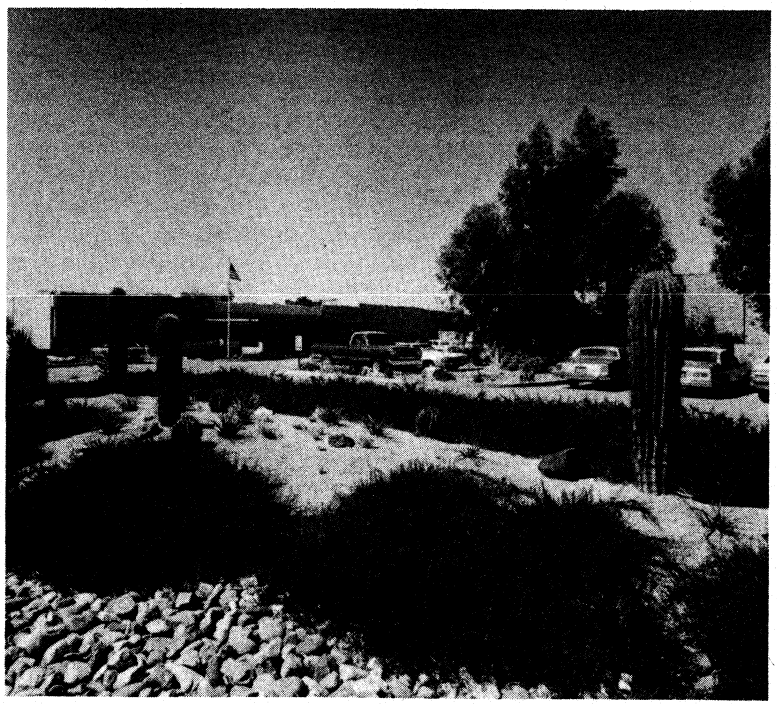
Cost effectiveness of our products has been proven in a host of applications: in industrial and process control, test instrumentation, aerospace systems, environmental monitoring, medical-clinical, and analytical instrumentation.

We have built our credibility by being totally responsive to our customers' requirements. Knowing the problems encountered in the real world, we apply the best, most appropriate, and proven technologies to achieve practical solutions.

Our components have become more complex, more sophisticated as we continue to combine and vertically integrate multiple functions into smaller, space-saving packages. When you select these versatile "mini-systems" your design and assembly time is decreased while your products' performance and reliability are increased. And today you pay less, per function, as these microcircuits and subsystems work more efficiently for you.

At Burr-Brown, quality and reliability are built-in by conservative designs, carefully selected components and manufacturing processes, by intensive, thorough testing, and stringent quality control.

Customers also give Burr-Brown high marks for service and support. Our technical literature is among the best in the industry and our global applications and sales force is factory trained ... highly qualified to help you in product selection and use. Wherever in the world you contact us, you can be assured of prompt, courteous, efficient service - and superb product performance.



BURR-BROWN GENERAL CATALOG

The Burr-Brown General Catalog contains product data sheets for one of the industry's broadest selections of circuits and systems for data acquisition, signal conditioning, and control. The products described range from high-technology integrated circuits to sophisticated and cost-effective systems based upon microcomputers.

For your convenience, the catalog is separted into nine major sections: Operational Amplifiers, Instrumentation Amplifiers, Isolation Amplifiers, Analog Circuit Functions, Data Conversion and Acquisition, Microcomputer Input/Output Systems, Industrial Measurement and Control Products, Power Supplies, and Accessories. Each section has a margin tab on the outer edge of each page which indicates both product function and model number. The tab index on page V provides a visual guide to the major sections.

At the beginning of each section you will find a selection guide which contains a summary of performance characteristics of the products within that section to assist you in selecting the product most suitable for your application. The selection guide also contains page numbers for individual product data sheets. Also included in each product data section is a glossary of terms.

The table of contents for the catalog and an index of the products listed alpha-numerically by model are found on page IV and VI respectively.

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MODEL INDEX

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STILL AVAILABLE ...

The following list incudes the more popular Burr-Brown models that are not listed elsewhere in this catalog. We realize that these models are "designed into" a great number of applications. We also realize that it is usually not economical for you to re-design in order to take advantage of newer products, even though they offer lower cost. Consequently, we want to assure you of the continuing availability of these older models.

However, we feel obligated to remind you that in many cases, these models may not be the best choices for your new designs. For your convenience, we have suggested newer models giving similar performance at lower cost.

Model Series	Nearest Equivalent	Model Series	Nearest Equivalent	Model Series	Nearest Equivalent	Model Series	Nearest Equivalent
ADC40	ADC80, ADC85	1557/15	3522K	3116/12C	3522K	3421K	3523K
ADC50	ADC80	3003/15	3500C	3117/12C	3500B	3421L	3523L
ADC55	ADC60	3004/15	3500B	3118/12C	3500B	3440J	3510BM
DAC12QZ	DAC80	3005/15	3500B	3119/12C	3500A	3440K	3510CM
DAC20	DAC85	3006/15	3500A	3129/15	3521K	3440L	3510CM
DAC40	DAC80	3007/15C	3500A	3138/25	3581J, 3582J	3460	3580J
DAC45	DAC70	3008/15C	3500B	3161/25	3626	3503A	3542J
DAC50	DAC85	3009/15C	3500B	3241/12C	3521K	3503B	3522J
MPM8S	MPC8S	3010/25	3291/14	3263/14	3626	3503R	3542S
MXP320	MPC16S	3011/25	3292/14	3264/14	3626	3503S	3522S
MXP321	MPC16S	3016/25	3329/03	3266/12C	3508J	3620J/16	3620J
SDM850	SDM853	3038/25	3581J, 3582J	3267/12C	3508J	3620K/16	3620K
SDM851	SDM853	3050/01	3500T	3268/14	3500B	3620L/16	3620L
SHC23	SHC80	3051/01	3500T	3269/14	3500A	3622	3620
SHM40	SHC85	3052/01	3500T	3307/12C	3522K	3625	3626
SHM41	SHC85	3053/01	3500S	3308/12C	3522K	4013	SHC85
UAF15	UAF41	3054/01	3500C	3341/15C	3554BM	4035/15	SHC85
UAF25	UAF41	3055/01	3500C	3342/15C	3554AM	4095/15	4213
501	553	3056/01	3500B	3348/03	3521J	4096/15	4213
1503	3500A	3057/01	3500A	3349/03	3521H	4118/25	4301
1506/15	3500B	3058/01	3500A	3350/03	3522J	4126/15C	4301
1507/15	3500A	3061/25	3626	3400	3554AM	4128	4341
1516/15	3500A	3064/12C	3550K	3401	3550K	4130	4341
1517/15	3500C	3064/15	3550K	3402	3550K	4131	4341
1520/15	3329/03	3069/49	3553AM	3420J	3521J	4201J	4213
1538A/25	3293/14	3112/12C	3542J	3420K	3521K	4202	4205
1541/25	3580J	3114/12C	3521J	3420L	3521L	4290	4291
1556/15	3521J	3115/12C	3521H	3421J	3523J		

PURCHASING AND

Burr-Brown operates from several worldwide locations to provide you with competent assistance in product selection, purchasing, product applications, literature, and other services as needed. These Burr-Brown subsidiaries are primarily intended to serve the countries in which they are located. Services and information for Eastern Europe are provided from our Sales Center for Eastern Europe, located in England. Other areas of the world are served by a network of Burr-Brown representatives, listed on the opposite page.

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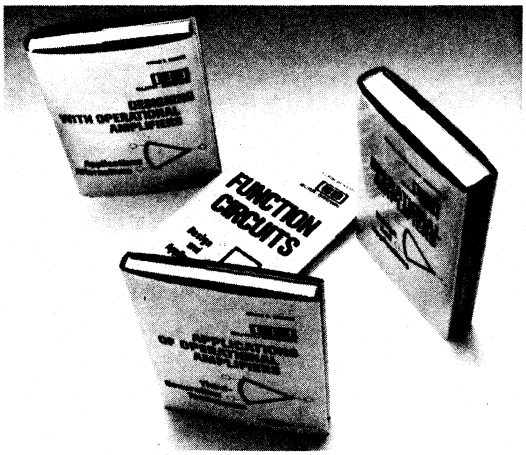
BURR-BROWN TECHNICAL LIBRARY

The Burr-Brown engineering staff, in cooperation with McGraw-Hill have authored the world's most extensive and authoritative library dealing with the art of analog signal conditioning, conversion, and computation. These books, respected and referenced throughout the international engineering community, are available to you directly from Burr-Brown.



FUNCTION CIRCUITS
Design and Applications

This new volume in the growing Burr-Brown series is the first to deal with the multi-faceted area of analog function circuits. FUNCTION CIRCUITS explores in depth both the design theory and numerous applications for such analog functions as Multipliers, Dividers, Logarithmic Amplifiers, Exponentiators, RMS Converters, and Active Filters. It also shows clearly how to specify and test these functions, which are increasingly becoming available in the form of integrated circuits. As in previous Burr-Brown books, the emphasis is on practicality while maintaining a rigorous treatment of theory. Numerous graphs and formulas are presented to allow the user to obtain optimum circuit performance (over 300 pages and 200 illustrations).

DESIGNING WITH OPERATIONAL AMPLIFIERS
Applications Alternatives

This latest volume in Burr-Brown's well-known series on Operational Amplifiers presents a wealth of new applications and circuit techniques which have evolved since publication of the previous two books. The applications are presented in a manner that will aid the user in developing further circuits. In addition to providing completed designs, the applications include explanations of circuit operation. Practical limitations are discussed and pertinent design equations presented to allow adaptation to specific application requirements.

New applications include amplifier performance improvement techniques, signal analyzers, signal conditioners, absolute-value circuits, signal generators, computing circuits, data transmission circuits, and test an measurement circuits (approximately 270 pages and 200 illustrations).

OPERATIONAL AMPLIFIERS
Design and Applications

Covering basic theory, test methods, amplifier design techniques, and applications, this pioneer work provides *practical* information which can be directly applied to instrumentation design.

The book is divided into two principal parts and two appendices. Part I considers the design of operational amplifiers, offers insight into the factors determining performance characteristics, and outlines the techniques available for their control. Part II presents a wide range of practical operational amplifier applications, and provides sufficient descriptions of operation to permit design adaption from the specific circuits described. In Appendix A the basic theory of operational amplifiers is reviewed to provide an accompanying reference. Appendix B gives concise definitions of the performance parameters used to characterize operational amplifiers, and provides associated test circuits (over 470 pages and 300 illustrations).

APPLICATIONS OF OPERATIONAL AMPLIFIERS

Third Generation Techniques

This is the second volume in the operational amplifier series. More than just a collection of circuit or theoretical analysis, the book presents numerous applications of operational amplifiers in a variety of electronic equipment: specialized amplifiers, signal controls, processors, waveform generators, and special purpose circuits. It is a storehouse of detailed practical information, featuring numerous circuit diagrams, circuit values, pertinent design equations, error sources, and test-based comments on the efficiency of the arrangements and devices (over 230 pages and 170 illustrations).

ORDERING INFORMATION FOR BURR-BROWN BOOKS

All prices are postpaid. Western European orders should be sent to Burr-Brown Literature Center, B.P. 7735, Schiphol Oost, Holland, Orders from all other areas should be sent to our Tucson address.

Make payable to Burr-Brown Research Corporation in U.S. dollars (or equivalent in local currency). Postal money orders NOT accepted.

PRICE LIST

Title	U.S.A. Canada	W. Europe	Elsewhere
FUNCTION CIRCUITS - Theory & Applications	$21.00	$21.25	$28.50
DESIGNING WITH OPERATIONAL AMPLIFIERS Applications Alternatives	$17.50	$18.75	$22.50
OPERATIONAL AMPLIFIERS Design & Applications	$21.25	$23.25	$29.05
APPLICATIONS OF OPERATIONAL AMPLIFIERS Third Generation Techniques	$18.65	$19.90	$22.65

APPLICATION NOTES. . .

Burr-Brown engineers have compiled a library of Applications Notes to assist you in your designs. These notes are listed below and are available on request.

AN-51	"A Primer on Analog Multiplier Specs"
AN-54	"Programmable Data Amplifier"
AN-55	"ANalog Modules Multiply User's Options"
AN-58	"D/A Converter Differential Linearity Error - It Really Shows Up!"
AN-59	"Don't Forget D/A Converter Tempco!"
AN-60	"Protect Op Amps from Overloads"
AN-62	"Varying Comparator Hysteresis w/o Shifting Initial Trip Point"
AN-63	"Electronic Controller With An Equilibrium Sustaining Mode"
AN-64	"Combine Two Op Amps to Avoid the Speed Accuracy Compromise"
AN-65	"Check Five Op Amp Specs in One Test"
AN-67	"A Noninverting Differentiator"
AN-68	"Using Op Amps in Low Noise Applications"
AN-70	"Analog Shaping"
AN-74	"Design of a Unique Precision Controlled Current Source"
AN-75	"Instrumentation Amplifiers"
AN-79	"Principles of Data Acquisition and Conversion"
AN-80	"Remote Multiplexing"
AN-81	"Distributed Data Processing"
AN-83	"How to Determine What Heatsink to Use"
AN-84	"Intrinsically Safe Data Acquisition"
AN-85	"Optical Coupling Extends Isolation Amplifier Utility"
AN-86	"Squeeze High Performance Out of Low Cost Hybrid Data Converters"
AN-87	"Analog I/O for Microprocessors Made Easy"
AN-88	"Software Conversion of Analog Outputs to Analog Inputs"

HIGH RELIABILITY PROGRAMS

Quality and reliability are major Burr-Brown commitments. It begins with "design-in" conservative design practices. Quality and reliablity are then "built-in" by careful choices of components and processes, comprehensive testing procedures, thorough quality control practices, and programs of military screening. We've earned our reputation for reliable products and we intend to maintain it by offering only high-quality products.

THE Q PROGRAM

The Burr-Brown Q Program offers increased reliability of the standard Burr-Brown integrated circuit at a reasonable cost. The Q Program is applicable to military and aerospace programs, as well as the control of industrial processes, medical patient monitoring, and other applications where failure may be expensive or hazardous. The Q Program consists of screening standard Burr-Brown integrated circuits in accordance with applicable test methods of Mil-Std-883. The screening sequence shown below details the mechanical, electrical, and thermal stresses applied to 100% of the Q products to identify and remove any potentially failure-prone devices.

Q SCREENING SEQUENCE

STEP	SCREEN	PROCEDURE
Routinely performed 100% on all Burr-Brown products	INTERNAL VISUAL INSPECTION (precap)	Burr-Brown QC4118 (copies available on request)
	ELECTRICAL TEST, 100% (postcap)	Per appropriate Burr-Brown product data sheet
①	STABILIZATION BAKE	Mil-Std-883, Method 1008
②	TEMPERATURE CYCLING	Mil-Std-883, Method 1010
③	HERMETICITY, GROSS LEAK	Mil-Std-883, Method 1014
④	HERMETICITY, FINE LEAK	Mil-Std-883, Method 1014
⑤	BURN-IN	Mil-Std-883, Method 1015
⑥	CONSTANT ACCELERATION (centrifuge)	Mil-Std-883, Method 2001
⑦	FINAL ELECTRICAL TEST	Per appropriate Burr-Brown product data sheet

Explanation of Screening Steps ...

- **INTERNAL VISUAL INSPECTION**
  This is a microscopic examination of the product performed prior to capping in order to verify conformance to Burr-Brown standards of quality for material, methods of construction, and workmanship. Its purpose is to detect and eliminate devices with internal defects which could lead to failures under the thermal, mechanical, and electrical stresses of extended operation.
- 100% **ELECTRICAL TEST**
  Each product is tested in accordance with the appropriate Burr-Brown product data sheet. These tests will normally include static and dynamic tests at +25°C, as well as drift tests over the operating temperature range.

① STABILIZATION BAKE
In this step the product is stored at an elevated temperature without electrical stress applied. The purpose is to stabilize circuit parameters through accelerated aging.

② TEMPERATURE CYCLING
The product is alternately exposed to extremes of high and low temperature such as would be experienced when parts or equipment are transferred to and from heated shelters in arctic areas. The purpose is to check for permanent changes in operating characteristics and physical damage resulting principally from variation in dimensions and other physical properties.

③ ④ HERMETICITY - GROSS AND FINE LEAK
The purpose of these two tests is to verify the hermeticity of the seal of integrated circuits having internal cavities which are evacuated or filled with gas. The test is intended to determine those devices which, when exposed for long periods to atmospheres containing high concentrations of water vapor or other gaseous contaminants, would degrade in performance and become latent failures.

⑤ BURN-IN
During burn-in the device is subjected to a high temperature for an extended period of time, with power applied. The burn-in screen is performed in order to eliminate marginal devices with inherent defects. In the absence of burn-in, these defective devices would be expected to result in infant mortality or early lifetime failures under use conditions.

⑥ CONSTANT ACCELERATION
This test subjects the product to a constant acceleration force in a centrifuge. The purpose is to detect and eliminate devices having structural and mechnaical weaknesses that could lead to failure when subjected to mechanical stresses during application.

⑦ FINAL ELECTRICAL TEST
This is a repetition of Step 2 with the purpose of verifying that the product still meets its specified performance. Devices which pass this test, after successfully passing the previous 8 steps, are qualified as Q parts.

DETAILED SCREENING PROCEDURES

The following table shows the Burr-Brown Q products presently available. The test conditions, as appropriate from product to product, are detailed. Only those devices which 100% pass the screening and meet all electrical specifications are marked with a Q suffix after the model number.

Other Burr-Brown hermetically-sealed monolithic and hybrid integrated circuits can be made available as Q products. These are quoted only by special request.

MODELS AVAILABLE	HIGH TEMP. STORAGE (Mil-Std-883)	TEMPERATURE CYCLING (Mil-Std-883)	HERMETICITY GROSS LEAK (Mil-Std-883)	HERMETICITY FINE LEAK (Mil-Std-883)	BURN-IN* (Mil-Std-883)	CENTRIFUGE (Mil-Std-883)
OPERATIONAL AMPLIFIERS (TO-99) 3500R, 3500S, 3500T 3521R 3522S 3523J 3542J, 3542S 3550S 3551S	Method 1008 Condition C +150°C 24 Hours	Method 1010 Condition C -65°C to +150°C 10 Cycles	Method 1014 Condition C Step 1 Fluorocarbon	Method 1014 Condition A Helium 5 x 10^{-8}cc/sec	Method 1015 Condition B 168 Hours	Method 2001 Condition D 20,000 G Y_1 Axis
OPERATIONAL AMPLIFIERS (TO-3) 3582J	Method 1008 Condition C +150°C 24 Hours	Method 1010 Condition B -55°C to +150°C 10 Cycles	Method 1014 Condition C Step 1 Fluorocarbon	Method 1014 Condition A Helium 5 x 10^{-7}cc/sec	Method 1015 Condition D 168 Hours	Method 2001 Condition A 5000 G Y_1 Axis
3583AM	Method 1008 Condition B +125°C 24 Hours	Method 1010 Condition B -55°C to +125°C 10 Cycles	Method 1014 Condition C Step 1 Fluorocarbon	Method 1014 Condition A Helium 5 x 10^{-7}cc/sec	Method 1015 Condition D 168 Hours	Method 2001 Condition A 5000 G Y_1 Axis
MULTIPLIERS (TO-100 ONLY) 4203S 4205S	Method 1008 Condition C +150°C 24 Hours	Method 1010 Condition C -65°C to +150°C 10 Cycles	Method 1014 Condition C Step 1 Fluorocarbon	Method 1014 Condition A Helium 5 x 10^{-8}cc/sec	Method 1015 Condition B 168 Hours	Method 2001 Condition D 20,000 G Y_1 Axis
MULTIPLIERS 4204S	Method 1008 Condition B +125°C 24 Hours	Method 1010 Condition B -55°C to +125°C 10 Cycles	Method 1014 Condition C Step 1 Fluorocarbon	Method 1014 Condition A Helium 5 x 10^{-7}cc/sec	Method 1015 Condition B 168 Hours	Method 2001 2,000 G Y_1 Axis
SAMPLE/HOLDS SHC23 Series SHC85 Series SHC80BM	Method 1008 Condition B +125°C 24 Hours	Method 1010 Condition B -55°C to +125°C 10 Cycles	Method 1014 Condition C Step 1 Fluorocarbon	Method 1014 Condition A Helium 5 x 10^{-7}cc/sec	Method 1015 Condition D 168 Hours	Method 2001 2,000 G Y_1 Axis
D/A CONVERTERS DAC85 DAC85C	Method 1008 Condition B +125°C, 24 Hours	Method 1010 Condition B -55°C to +125°C 10 Cycles	Method 1014 Condition C Step 1 Fluorocarbon	Method 1014 Condition A Helium 5 x 10^{-7}cc/sec	Method 1015 Condition D 168 Hours	Method 2001 2,000 G Y_1 Axis
D/A CONVERTERS DAC90BGQ DAC90SGQ	Method 1008 Condition C +150°C 24 Hours	Method 1010 Condition C -65°C to +150°C 10 Cycles	Method 1014 Condition C Step 1 Fluorocarbon	Method 1014 Condition A Helium 5 x 10^{-7}cc/sec	Method 1015 Condition B 168 Hours	Method 2001 20,000 G Y_1 Axis
A/D CONVERTERS ADC85 ADC85C ADC82AM	Method 1008 Condition B +125°C, 24 Hours	Method 1010 Condition B -55°C to +125°C 10 Cycles	Method 1014 Condition C Step 1 Fluorocarbon	Method 1014 Condition A Helium 5 x 10^{-7}cc/sec	Method 1015 Condition D 168 Hours	Method 2001 2,000 G Y_1 Axis
UNIVERSAL ACTIVE FILTERS UAF11H UAF21H	Method 1008 Condition B +125°C, 24 Hours	Method 1010 Condition B -55°C to +125°C 10 Cycles	Method 1014 Condition C Step 1 Fluorocarbon	Method 1014 Condition A Helium 5 x 10^{-7}cc/sec	Method 1015 Condition B 168 Hours	Method 2001 2,000 G Y_1 Axis
V/F-F/V CONVERTERS VFC32BMQ VFC32SMQ	Method 1008 Condition C +150°C 24 Hours	Method 1010 Condition C -65°C to +150°C 10 Cycles	Method 1014 Condition C Step 1 Fluorocarbon	Method 1014 Condition A Helium 5 x 10^{-8}cc/sec	Method 1015 Condition B 168 Hours	Method 2001 Condition D 20,000 G Y_1 Axis

*Burn-in is performed at the maximum specification temperature for each mode. See product data sheet for the model of interest.

/MIL PROGRAM

The Burr-Brown /MIL Program offers extremely-high product reliability - even beyond that offered by standard Burr-Brown products. The /MIL Program is applicable to military, aerospace, and government programs. The devices usually find applications as "nonstandard parts." The devices are high-reliability-manufactured, screened, and then inspected for quality conformance. They are available at higher cost. These devices exceed "Mil-Std-883, Class B, screened" requirements. The complete data sheets contain all the necessary information of Mil-M-38510 slash sheets thereby providing for easier nonstandard parts approval by the government procuring activity.

/MIL products may be used when a failure could be very expensive or hazardous. The table below describes the /MIL processing.

/MIL PROCESSING

SEQUENCE	METHOD	REQUIREMENTS*
Manufacture		Burr-Brown high reliability manufacture includes traceability, rework and rebonding provisions, product and process change controls, date coding, etc.
Screening (Class B only)	Mil-Std-883 Method 5004	Class B, 100% • Internal visual (Method 2010/2017) • Stabilization bake • Temperature cycle • Hermeticity, gross leak • Hermeticity, fine leak • Interim electrical • Burn-in • Constant acceleration • Final electrical • External visual
Qualification Conformance Inspection	Mil-Std-883 Method 5005/5008	Groups A & B plus periodic groups C & D • Group A - electrical tests • Group B - mechanical tests • Group C - die-related tests • Group D - package related tests
Qualification	Mil-Std-883 Method 5005/5008	Groups A, B, C, & D upon special request (Most recent data available)

*See the detailed product data sheet for each product.

The line of Burr-Brown /MIL products is growing. The following are the first products which will be available.

Model Number	Description
DAC85-CBI-V/MIL	12-bit digital-to-analog converter (voltage output model)
DAC85-CBI-I/MIL	12-bit digital-to-analog converter (current output mode)
3510VM/MIL	Precision bipolar operational amplifier
4213VM/MIL	1% multiplier
3554VM/MIL	Wideband, differential operational amplifier

NEW PRODUCTS

During the past year Burr-Brown has introduced many new products including operational amplifiers, instrumentation amplifiers, isolation amplifiers, multiplier-dividers, A/D-D/A-V/F converters, data acquisition systems, sample/hold amplifiers, microcomputer input/output systems, industrial measurement and control systems, and power supplies. These products are listed in the selection guides and are indicated by asterisks.

Other Burr-Brown products soon to be introduced will appear in electronic trade journals. Some of these are listed below:

High Speed Operational Amplifiers (Models 3529 and 3530)

Common features:
- 0.5pA bias current at 25°C
- 250uV offset voltage
- 5uV/°C offset voltage drift

Model 3529
- High gain applications
- 100MHz gain-bandwidth product at A_{CL} = 100
- 20V/usec slew rate
- 1usec settling time to 0.1% at A_{CL} = 1000

Model 3530
- Low gain applications
- 20MHz gain-bandwidth product at A_{CL} = 10
- 80V/usec slew rate
- 200nsec settling time to 0.1% at A_{CL} = 1

High Resolution D/A Converters (Models DAC71 and DAC72)
- 16-bit binary or 4-digit BCD resolution
- ±0.003% linearity
- Small 24-pin dual-in-line ceramic or hermetic metal package
- Voltage or current output
- Very low cost

Low Cost IC D/A Converter (Model DAC863)
- Internal reference
- Small 24-pin hermetic ceramic package
- ±1/4 LSB linearity
- -55°C to +125°C model with Mil-Std-883 screening available
- Pin-compatible with "563" converters

Low Level Data Acquisition System (Model SDM858)
- Highly accurate internal instrumentation amplifier
- ±0.1% system accuracy with ±10mV inputs
- Programmable input gain ranges from +10mV to +10V
- Reliability assured by 168-hour burn-in at factory

Wide Temperature Range, Enhanced Reliability, 12-bit D/A Converter
- -55°C to +125°C specification temperature range
- Complete with internal reference and output amplifier
- Compact 24-pin dual-in-line hermetic package
- Manufactured with military-level processes

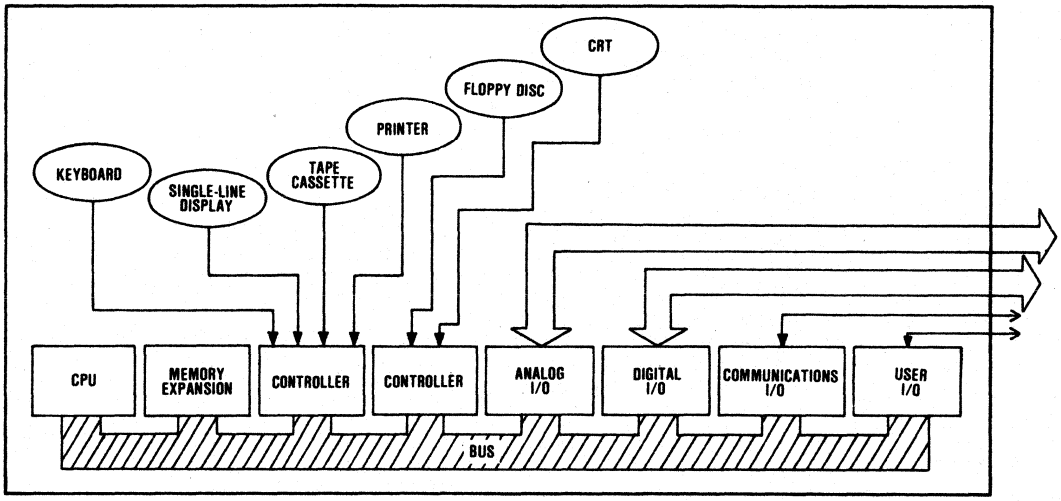
Microcomputer Analog Input Expander (Model MP8418-Expander)
- Intel SBC80-compatible PC board
- Allows MP8418 to be expanded to 127 input channels on two cards

Microcomputer Analog Input System (Model MP1216)

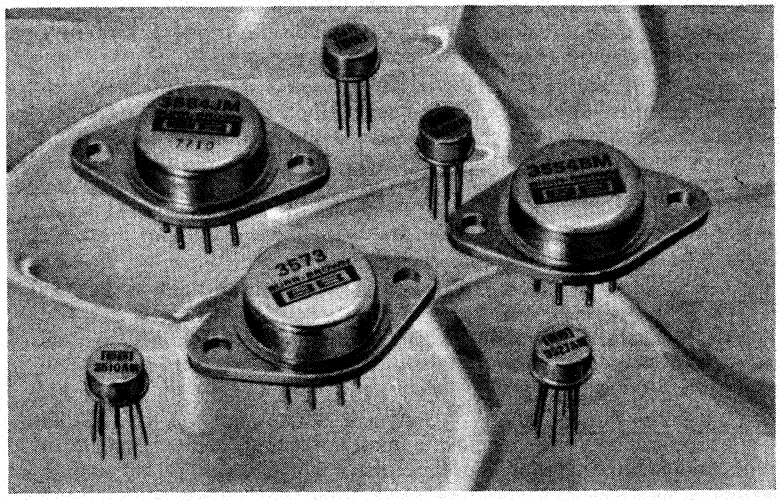
- 12-bit resolution
- 32 channels
- Software programmable-gain amplifier (gains of 1 to 1024)
- DEC LSI-11/2-compatible PC board (MP1216)

Intelligent Desk Top Data Acquisition and Control System

- Based on Burr-Brown analog and digital I/O boards
- Multi-task operating system
- Programmed in BASIC
- Multi-processor bus configuration
- All I/O programmable in high level language
- Complete system no larger than a terminal
- Communicates with operator via keyboard and display
- Optional printer, tape cassette, and floppy disc available
- Serial ASCII communication port
- IEEE-488 interface



1. OPERATIONAL AMPLIFIERS



Burr-Brown operational amplifiers are listed in seven applications groups and are described below. This enables the user to determine and select the best operational amplifier available for a design requirement. Instrumentation amplifiers and isolation amplifiers are described in sections 2 and 3 respectively.

General Purpose - General purpose operational amplifiers are suited for a wide variety of applications. They give moderately good performance over a wide range of parameters at moderate cost. This applications group contains both FET and bipolar input models with frequency responses from 0.5MHz to 1.5MHz and offset voltages as low as 1mV. Models 3500 and 3527 are particularly worth consideration in general purpose designs.

Low Temperature Drift - Low drift operational amplifiers are best suited for applications where accuracy must be preserved over a substantial temperature range. These amplifiers are optimized to minimize the initial input offset voltage and input offset voltage change with temperature. Input offset drifts from 0.1μV/°C to 10μV/°C are available within this group. Chopper-stabilized operational amplifiers represent the best available in overall accuracy and long term stability. In addition, integrated circuit models 3510 and 3527 are particularly worth consideration because of their small size, moderate cost, and differential inputs.

Low Bias Current - Low bias current operational amplifiers consist of a group of varactor diode and FET input designs. This group includes amplifiers with input bias currents from 0.01pA to 1nA. Applications with large feedback resistances or large source resistances (long time constants, integrators, current sources, etc.) and buffer applications will benefit by the use of low bias current amplifiers. Models 3582, 3527, and 3430 are particularly worth consideration.

Wideband - Wideband operational amplifiers have bandwidths greater than 10MHz. This group also contains fast settling and high slew rate amplifiers. These amplifiers reduce phase errors at high frequencies and accurately reproduce

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complex waveforms. These amplifiers are well suited for pulse, video, fast settling, and multiplexing applications. Model 3554, an outstanding product in this applications group, features 1.7GHz gain-bandwidth product, 1000Vμsec slew rate, 150nsec settling time and differential input.

High Voltage - The amplifiers in this group are designed to provide large output voltage swings and to operate on wide ranges of supply voltage. Output voltages greater than ±10V and up to ±145V are available in this applications group (up to 290V, single supply). These amplifiers provide good frequency response and performance in other parameters. Most models have electrically isolated packages and automatic thermal sensing and shutdown. All units have FET inputs to minimize bias current errors when the amplifier is used with the large resistances usually found with high voltage amplifiers.

High Current - These amplifiers provide output currents from ±10mA to ±2A (±5A peak). They are used with small load resistances, coax cable impedances, and with power booster applications. Many units have self-contained thermal sensing and shutdown to automatically protect the amplifiers from overheating and damage. All of these units have electrically isolated packages.

Unity-Gain Buffer (Power Booster) - Unity-gain buffer amplifiers have a wide variety of applications. They are used to boost the output current capability of another amplifier, to buffer an impedance that might load a critical circuit or to be an input impedance converter from an input which must not be loaded. These amplifiers may also be used inside the feedback loop of another operational amplifier to form a current-boosted, composite amplifier.

SELECTION GUIDE
Operational Amplifiers

These give moderately good performance over a wide range of parameters.

GENERAL PURPOSE

Description	Model	Rated Output ±V	Rated Output ±mA	Offset Voltage at 25°C mV	Offset Voltage Temp. Drift µV/°C	Bias Current nA (at 25°C)	Frequency Response Unity Gain MHz	Frequency Response Slew Rate V/µsec	Package		Page
Bipolar	3500A	10	10	5	20	±30	1.5	0.6	TO-99*		1-23
	3500B	10	10	2	5	±20	1.5	0.8	TO-99*		1-23
	3500C	10	10	1	3	±15	1.5	1.0	TO-99*		1-23
	3500R	10	10	5	20	±30	1.5	0.6	TO-99		1-23
	3500S	10	10	2	10	±20	1.5	0.8	TO-99		1-23
	3500T	10	10	1	5	±15	1.5	1.0	TO-99		1-23
	3501A	10	5	5	20	±15	0.5	0.1	TO-99		1-38
	3501B	10	5	2	10	±7	0.5	0.1	TO-99		1-38
	3501C	10	5	2	5	±3	0.5	0.1	TO-99		1-38
	3501R	10	5	5	20	±15	0.5	0.1	TO-99		1-38
	3501S	10	5	2	10	±7	0.5	0.1	TO-99		1-38
FET	3527AM**	10	10	0.50	10	-0.005	1.0	0.6	TO-99		1-69
	3527BM**	10	10	0.25	5	-0.002	1.0	0.6	TO-99		1-69
	3527CM**	10	10	0.25	2	-0.005	1.0	0.6	TO-99		1-69
	3542J	10	10	20	50	-0.025	1.0	0.5	TO-99		1-79
	3542S	10	10	20	50	-0.025	1.0	0.5	TO-99		1-79

0.1µV/°C to 10µV/°C input offset voltage change with temperature.

LOW TEMPERATURE DRIFT

	Description	Model	Rated Output ±V	Rated Output ±mA	Offset Voltage at 25°C mV	Offset Voltage Temp. Drift µV/°C	Bias Current nA (at 25°C)	Frequency Response Unity Gain MHz	Frequency Response Slew Rate V/µsec	Package		Page
CHOPPER-STABILIZED	Inverting Only	3291/14	10	5	0.02	0.10	±0.05	3	6	Module		1-9
		3292/14	10	5	0.05	0.30	±0.05	3	6	Module		1-9
		3293/14	10	5	0.10	1.0	±0.10	3	6	Module		1-9
	Differential	3354/25	10	5	0.03	0.10	±0.02	6	6	Module		1-9
		3355/25	10	5	0.05	0.25	±0.05	6	6	Module		1-9
		3356/25	10	5	0.10	1.0	±0.05	6	6	Module		1-9
	High Voltage	3271/25	110	20	0.05	1.0	±0.08	1	20	Module		1-7
Bipolar		3510AM	10	10	0.15	2	±35	0.4	0.5	TO-99		1-50
		3510BM	10	10	0.12	1	±25	0.4	0.5	TO-99		1-50
		3510CM	10	10	0.06	0.5	±15	0.4	0.5	TO-99		1-50
		3500A	10	10	5	20	±30	1.5	0.6	TO-99*		1-23
		3500B	10	10	2	5	±20	1.5	0.8	TO-99*		1-23
		3500C	10	10	1	3	±15	1.5	1.0	TO-99*		1-23
		3500R	10	10	5	20	±30	1.5	0.6	TO-99		1-23
		3500S	10	10	2	5	±20	1.5	0.8	TO-99		1-23
		3500T	10	10	1	3	±15	1.5	1.0	TO-99		1-23
		3500E	10	10	0.50	1	±50	1.5	0.8	TO-99		1-27
		3500MP	10	10	0.20[2]	1[2]	±50	1.5	0.8	TO-99		1-33
		3501A	10	5	5	20	±15	0.5	0.1	TO-99		1-38
		3501B	10	5	2	10	±7	0.5	0.1	TO-99		1-38
		3501C	10	5	2	5	±3	0.5	0.1	TO-99		1-38
		3501R	10	5	5	20	±15	0.5	0.1	TO-99		1-38
		3501S	10	5	2	10	±7	0.5	0.1	TO-99		1-38
FET		3521H	10	10	0.50	10	-0.02	1	0.6	TO-99		1-56
		3521J	10	10	0.25	5	-0.02	1	0.6	TO-99		1-56
		3521K	10	10	0.25	2	-0.015	1	0.6	TO-99		1-56
		3521L	10	10	0.25	1	-0.01	1	0.6	TO-99		1-56
		3521R	10	10	0.25	5	-0.02	1	0.6	TO-99		1-56
		3527AM**	10	10	0.50	10	-0.005	1	0.6	TO-99		1-69
		3527BM**	10	10	0.25	5	-0.002	1	0.6	TO-99		1-69
		3527CM**	10	10	0.25	2	-0.005	1	0.6	TO-99		1-69
		3528AM**	10	5	0.50	15	-0.30pA	0.7	0.3	TO-99		1-73
		3528BM**	10	5	0.25	5	-0.15pA	0.7	0.3	TO-99		1-73
		3528CM**	10	5	0.50	10	-0.075pA	0.7	0.3	TO-99		1-73

1) Prices for quantities (1-9) (10-24) (25-99). 2) These specifications apply to the match between two devices. The 3500MP is a matched pair of amplifiers.

*Add suffix "N" to model number for 8 pin mini-DIP package.

**New

LOW BIAS CURRENT

0.01pA to 1nA bias current.

	Description	Model	Rated Output ±V	Rated Output ±mA	Offset Voltage at 25°C mV	Offset Voltage Temp. Drift µV/°C	Bias Current pA (at 25°C)	Frequency Response Unity Gain MHz	Frequency Response Slew Rate V/µsec	Package		Page
VARACTOR	Inverting	3430J	10	5	Adj. to 0	30	±0.01	2kHz	0.4V/msec	Module		1-17
	Only	3430K	10	5	Adj. to 0	10	±0.01	2kHz	0.4V/msec	Module		1-17
	Noninverting	3431J	10	5	Adj. to 0	30	±0.01	2kHz	0.4V/msec	Module		1-17
	Only	3431K	10	5	Adj. to 0	10	±0.01	2kHz	0.4V/msec	Module		1-17
FET INPUT	Ultra-Low	3528AM**	10	5	0.50	15	-0.300	0.7	0.3	TO-99		1-73
	Bias	3528BM**	10	5	0.25	5	-0.150	0.7	0.3	TO-99		1-73
	Current	3528CM**	10	5	0.50	10	-0.075	0.7	0.3	TO-99		1-73
		3523J	10	10	1.0	50	-0.50	1	0.6	TO-99		1-65
		3523K	10	10	0.50	25	-0.25	1	0.6	TO-99		1-65
		3523L	10	10	0.50	25	-0.10	1	0.6	TO-99		1-65
	General	3522J	10	10	1.0	50	-10	1	0.6	TO-99		1-61
	Purpose	3522K	10	10	0.50	10	-5	1	0.6	TO-99		1-61
		3522L	10	10	0.50	10	-1	1	0.6	TO-99		1-61
		3522S	10	10	0.50	25	-5	1	0.6	TO-99		1-61
	Ultra-Low	3527AM**	10	10	0.50	10	-5	1	0.6	TO-99		1-69
	Drift	3527BM**	10	10	0.25	5	-2	1	0.6	TO-99		1-69
		3527CM**	10	10	0.25	2	-5	1	0.6	TO-99		1-69
		3521H	10	10	0.50	10	-20	1	0.6	TO-99		1-56
		3521J	10	10	0.25	5	-20	1	0.6	TO-99		1-56
		3521K	10	10	0.25	2	-15	1	0.6	TO-99		1-56
		3521L	10	10	0.25	1	-10	1	0.6	TO-99		1-56
		3521R	10	10	0.25	5	-20	1	0.6	TO-99		1-56
	Low Cost	3542J	10	10	20	50	-25	1	0.5	TO-99		1-79
		3542S	10	10	20	50	-25	1	0.5	TO-99		1-79
	Chopper-Stabilized	3291/14	10	5	0.02	0.1	±50	3	6	Module		1-9
		3292/14	10	5	0.05	0.3	±50	3	6	Module		1-9
		3293/14	10	5	0.10	1	±100	3	6	Module		1-9
		3271/25	110	20	0.05	1	±80	1	20	Module		1-7
	Wideband	3550J	10	10	1	50	-100	10	65	TO-99		1-83
		3550K	10	10	1	50	-100	20	100	TO-99		1-83
		3550S	10	10	1	50	-100	10	65	TO-99		1-83
		3551J	10	10	1	50	-100	50[3]	250	TO-99		1-87
		3551S	10	10	1	50	-100	50[3]	250	TO-99		1-87
		3554AM**	10	100	2	50	-50	1000[3]	1000	TO-3		1-95
		3554BM**	10	100	1	15	-50	1000[3]	1000	TO-3		1-95
		3554SM**	10	100	1	25	-50	1000[3]	1000	TO-3		1-95
	Buffer	3553AM	10	200	50	300	-200	300[4]	2000	TO-3		1-91
	High Current	3571AM	35	1A	2	40	-100	0.5	3	TO-3		1-103
		3572AM	35	2A	2	40	-100	0.5	3	TO-3		1-103
	High Voltage	3580J	30	60	10	30	-50	5	15	TO-3		1-113
		3581J	70	30	3	25	-20	5	20	TO-3		1-113
		3582J	145	15	3	25	-20	5	20	TO-3		1-113
		3583AM	140	75	3	25	-20	5	30	TO-3		1-117
		3583JM	140	75	3	25	-20	5	30	TO-3		1-117
		3584JM	145	15	3	25	-20	20[3]	150	TO-3		1-121

WIDEBAND

Bandwidths greater than 100MHz.

Description	Model	Rated Output ±V	Rated Output ±mA	Offset Voltage at 25°C mV	Offset Voltage Temp. Drift µV/°C	Frequency Response A-BW MHz	Frequency Response Slew Rate V/µsec	t_s ±0.1% nsec	Compensation	Package		Page
Differential	3554AM**	10	100	2	50	1000, A = 1000	1000	120	ext.	TO-3		1-95
	3554BM**	10	100	1	15	1000, A = 1000	1000	120	ext.	TO-3		1-95
	3554SM**	10	100	1	25	1000, A = 1000	1000	120	ext.	TO-3		1-95
	3551J	10	10	1	50	50, A = 10	250	400	ext.	TO-99		1-87
	3551S	10	10	1	50	50, A = 10	250	400	ext.	TO-99		1-87
	3550J	10	10	1	50	10, A = 1	65	400	int.	TO-99		1-83
	3550K	10	10	1	50	20, A = 1	100	400	int.	TO-99		1-83
	3550S	10	10	1	50	10, A = 1	65	400	int.	TO-99		1-83
	3508J	10	10	5	30	100, A = 100	20	-	ext.	TO-99		1-46
	3507J	10	10	10	30	20, A = 10	80	200	ext.	TO-99		1-42
Unity-Gain Buffer	3553AM	10	200	50	300	32[5]	2000	-	-	TO-3		1-91

HIGH VOLTAGE

Output voltages > ±10V to ±145V.

Description	Model	Rated Output ±V	Rated Output ±mA	Offset Voltage at 25°C mV	Offset Voltage Temp. Drift µV/°C	Bias Current pA (at°C)	Frequency Response Unity Gain MHz	Frequency Response Slew Rate V/µsec	Package		Page
FET	3584JM	145	15	3	25	-20	20[3]	150	TO-3		1-121
	3583AM	140	75	3	25	-20	5	30	TO-3		1-117
	3583JM	140	75	3	25	-20	5	30	TO-3		1-117
	3582J	145	15	3	25	-20	5	20	TO-3		1-113
	3581J	70	30	3	25	-20	5	20	TO-3		1-113
	3580J	30	60	10	30	-50	5	15	TO-3		1-113
	3571AM	35	1A[6]	2	40	-100	0.5	3	TO-3		1-103
	3572AM	35	2A[7]	2	40	-100	0.5	3	TO-3		1-103
	3573AM**	29	2A[7]	10	65	40nA	1	1.5	TO-3		1-109
Chopper-Stabilized	3271/25	110	20	0.05	1	±80	1	20	Module		1-7

HIGH CURRENT

Output currents > ±10mA to ±2A.

Description	Model	Rated Output ±V	Rated Output ±mA	Offset Voltage at 25°C mV	Offset Voltage Temp. Drift µV/°C	Bias Current pA (at°C)	Frequency Response Unity Gain MHz	Frequency Response Slew Rate V/µsec	Package		Page
High Power	3573AM**	29	2A[7]	10	65	40nA	1	1.5	TO-3		1-109
	3572AM	35	2A[7]	2	40	-100	0.5	3	TO-3		1-103
	3571AM	35	1A[6]	2	40	-100	0.5	3	TO-3		1-103
Wideband	3554AM**	10	100	2	50	-50	1000[3]	1000	TO-3		1-95
	3554BM**	10	100	1	15	-50	1000[3]	1000	TO-3		1-95
	3554SM**	10	100	1	25	-50	1000[3]	1000	TO-3		1-95
High Voltage	3584JM	145	15	3	25	-20	20[3]	150	TO-3		1-121
	3583AM	140	75	3	25	-20	5	30	TO-3		1-117
	3583JM	140	75	3	25	-20	5	30	TO-3		1-117
	3582J	145	15	3	25	-20	5	20	TO-3		1-113
	3581J	70	30	3	25	-20	5	20	TO-3		1-113
	3580J	30	60	10	30	-50	5	15	TO-3		1-113
Booster (Buffer)	3553AM	10	200	50	300	-200	32[5]	2000	TO-3		1-91
	3329/03	10	100	50	-	bipolar	1[5]	-	DIL		1-15

UNITY GAIN BUFFER (Power Booster)

Description	Model	Rated Output ±V	Rated Output ±mA	Frequency Response -3dB MHz	Frequency Response Full Pwr BW MHz	Frequency Response Slew Rate V/µsec	Gain V/V	Input Impedance Ω	Package		Page
Noninverting	3553AM	10	200	300	32	2000	≃ 1	10^{11}	TO-3		1-91
	3329/03	10	100	5	1	-	≃ 1	10k	DIL		1-15

3) Gain-bandwidth product. 4) -3dB bandwidth. 5) Full power bandwidth.

6) 2A peak. 7) 5A peak.

GLOSSARY OF TERMS AND DEFINITIONS
Operational Amplifiers

COMMON-MODE INPUT IMPEDANCE
The effective impedance (resistance in parallel with capacitance) between either input of an amplifier and its common, or ground terminal.

COMMON-MODE REJECTION (CMR)
When both inputs of a differential amplifier experience the same common-mode voltage (CMV), the output should, ideally, be unaffected. CMR is the ratio of the common-mode input voltage change to the differential input voltage (error voltage) which produces the same output change.

$$CMR\ (in\ dB) = 20\ \log_{10}\ CMV/Error\ Voltage$$

Thus a CMR of 80dB means that 1V of common-mode voltage will cause an error of 100μV (referred to input).

COMMON-MODE VOLTAGE (CMV)
That portion of an input signal which is common to both inputs of a differential amplifier. Mathematically it is defined as the average of the signals at the two inputs:

$$CMV = (e_1 + e_2)/2$$

COMMON-MODE VOLTAGE GAIN
The ratio of the output signal voltage (ideally zero) to the common-mode input signal voltage.

COMMON-MODE VOLTAGE RANGE
The range of input voltage for linear, nonsaturated operation.

DIFFERENTIAL INPUT IMPEDANCE
The apparent impedance, resistance in parallel with capacitance, between the two input terminals.

FULL POWER FREQUENCY RESPONSE
The maximum frequency at which a device can supply its peak-to-peak rated output voltage and current, without introducing significant distortion.

GAIN-BANDWIDTH PRODUCT
A product of small signal, open-loop gain and frequency at that gain.

INPUT BIAS CURRENT
The DC input current required at each input of an amplifier to provide zero output voltage when the input signal and input offset voltage are zero. The specified maximum is for each input.

INPUT BIAS CURRENT VS SUPPLY VOLTAGE
The sensitivity of input bias current to the power supply voltages.

INPUT BIAS CURRENT VS TEMPERATURE
The sensitivity of input bias current to temperature.

INPUT CURRENT NOISE
The input current which would produce, at the output of a noiseless amplifier, the same output as that produced by the inherent noise generated internally in the amplifier when the source resistances are large.

INPUT OFFSET CURRENT
The difference of the two input bias currents of a differential amplifier.

INPUT OFFSET VOLTAGE
The DC input voltage required to provide zero voltage at the output of an amplifier when the input signal and input bias currents are zero.

INPUT OFFSET VOLTAGE VS SUPPLY VOLTAGE I/PSRR
The sensitivity of input offset voltage to the power supply voltages. Both power supply magnitudes are changed in the same direction and over the operating voltage range.

INPUT OFFSET VOLTAGE VS TEMPERATURE (DRIFT)
The rate of change of input offset voltage with temperature. At Burr-Brown, this is the change in input offset voltage from 25°C to the maximum specification temperature, plus the change in input offset voltage from 25°C to the minimum specification temperature, this quantity divided by the specification temperature range.

INPUT OFFSET VOLTAGE VS TIME
The sensitivity of input offset voltage to time.

INPUT VOLTAGE NOISE
The differential input voltage which would produce, at the output of a noiseless amplifier, the same output as that produced by the inherent noise generated internally in the amplifier when the source resistances are small.

MAXIMUM SAFE INPUT VOLTAGE
The maximum, peak value, continuous voltage that may be applied at, or between, the inputs without damage.

OPEN-LOOP GAIN
The ratio of the output signal voltage to the differential input signal voltage.

OPERATING TEMPERATURE RANGE
The temperature range, ambient unless otherwise indicated, over which the amplifier may be safely operated.

OUTPUT RESISTANCE
The open-loop output source resistance with respect to ground.

POWER SUPPLY RATED VOLTAGE
The normal value of power supply voltage at which the amplifier is designed to operate.

POWER SUPPLY VOLTAGE RANGE
The range of power supply voltage over which the amplifier may be safely operated.

QUIESCENT CURRENT
The current required from the power supply to operate the amplfiier with no load and with the output at zero.

RATED OUTPUT
The peak output voltage and current which can be continuously, simultaneously supplied.

SETTLING TIME
The time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

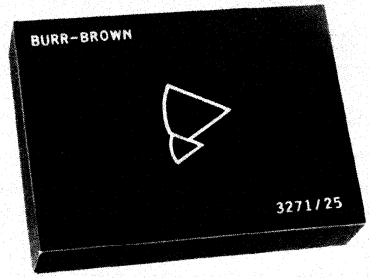
SLEW RATE
The maximum rate of charge of the output voltage when supplying rated output.

SPECIFICATION TEMPERATURE RANGE
The temperature range over which the "versus temperature" specifications are specified.

STORAGE TEMPERATURE RANGE
The temperature range over which the amplifier may be safely stored, unpowered.

UNITY-GAIN FREQUENCY RESPONSE
The frequency at which the open-loop becomes unity.

BURR-BROWN



3271/25

High Voltage - Chopper-stabilized OPERATIONAL AMPLIFIERS

FEATURES

- LOW DRIFT
- OPERATES OVER WIDE SUPPLY RANGE
- HIGH OUTPUT VOLTAGE UP TO 110V
- SMALL, ENCAPSULATED PACKAGE
- ALL SOLID-STATE DESIGN

DESCRIPTION

The Model 3271/25 is a high voltage, chopper-stabilized operational amplifier in a small, encapsulated package. The module can be soldered directly on a circuit board, or may be plugged into a 1500MC connector for chassis mounting. The epoxy encapsulation insures ruggedness and resistance to environmental stresses, while the all-solid-state design, including self-contained MOSFET chopper and driver, guarantees reliable operation.

The amplifier is designed for operation on external supplies ranging anywhere from ±60VDC to ±120VDC. Output voltage range depends on the supply voltages. A low-noise chopping technique insures ultra-low DC drift as a function of temperature and time, while eliminating the noise spikes usually associated with chopper amplifiers.

The 3271/25 has input protection up to the value of supply voltage. The output stage may be shorted to common without damage to the amplifier. These features are particularly desirable when the amplifier is used in a patchable simulator.

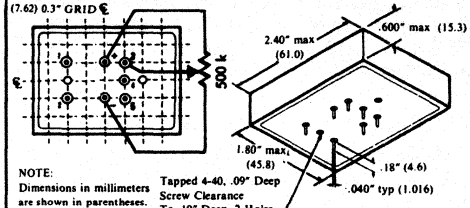
The open-loop gain exhibits a high frequency rolloff of approximately 6dB/octave, which insures stability at all feedback gain levels, or when driving capacitive loads. At the same time, the fast slewing rate and relatively wide bandwidth guarantee fast step response, with low overshoot, and low phase shift, when the 3271/25 is used as an inverter or summing amplifier.

APPLICATIONS

Typical areas of application for the 3271/25 are: integrators, summing amplifiers, inverters, sample/hold units, D/A converters, precision function generation, data amplifiers, and DC preamplifiers. The wide supply voltage tolerance and stable design enable the 3271/25 to be used as a replacement for vacuum tube amplifiers and older, solid-state amplifiers in simulators, data acquisition systems, and other systems where it is desired to increase reliability and improve performance at modest cost.

Because of the rugged construction techniques and use of silicon semiconductors, the 3271/25 is not limited to laboratory applications, but may also be used in relatively severe environments. Examples are shipboard, airborne, high vibration industrial, and remote monitoring stations.

MODEL 3271/25 ENCAPSULATED PACKAGE



NOTE: Dimensions in millimeters are shown in parentheses.

PIN CONNECTIONS

Pin 1	Inverting Signal Input
Pin 2	Common
Pin 4	Signal Output
(+)	Positive Power
(-)	Negative Power
Pin 3	External Zero Control
Pin 5	Overload Signal

MATERIAL

Case - Black Epoxy
Pins - Gold-Flashed
Header - Alum., Hard Black Anodized
Mating Connector
Model 1500MC

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LI-227-2D

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SPECIFICATIONS

Performance at 25°C and ±120 VDC supply unless otherwise noted.

* See discussion of output characteristics below.
Operating Temperature Range, -25°C to +85°C; Storage -55°C to +100°C.

MODEL	RATED OUTPUT		DC GAIN	BANDWIDTH		SLEW RATE	INPUT OFFSET VOLTAGE					INPUT BIAS CURRENT				INPUT NOISE	OPEN LOOP IMPEDANCES		POWER SUPPLY	
	V_o	I_o		Unity Gain	Full Power		At +25°C	Over Range -25°C to +85°C	Versus Temp.	Versus Supply	Versus Time	At 25°C	Over Range -25°C to 85°C	Versus Temp.	Versus Supply	10Hz to 10kHz	Input	Output	Range	Quies. Current
	Volts min	mA min	dB min	MHz min	kHz min	V/μs min	μV max	μV max	μV/°C max	μV/V max	μV/mo typ	pA max	pA max	pA/°C max	pA/V max	μV rms max	MΩ typ	kΩ typ	Volts	mA max
3271/25	Supply less ±10V	±20	140	1.0	30*	20	±50	±110	1.0	1.0	+1	±80	±200	±2	±10	25 10(typ)	0.5	25	±60 to ±120	±20mA @±120VDC

OPEN-LOOP RESPONSE

The DC gain of the amplifier is typically 160dB because of the additional gain contributed by the DC chopper channel. This chopper channel gain rolls off at very-low frequency after which the amplifier gain is determined by the AC channel. The high frequency gain decreases at very nearly 6dB/octave. Figure 1 illustrates the open-loop gain response of a typical unit.

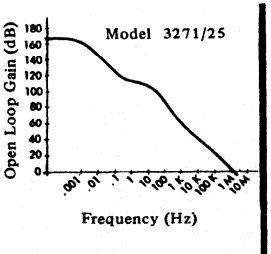

FIGURE 1. Open Loop Gain vs. Frequency.

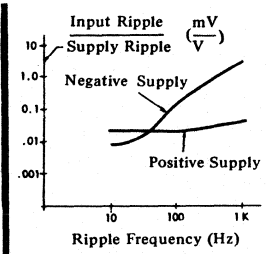

FIGURE 2. Supply Ripple Rejection vs. Frequency.

OUTPUT CHARACTERISTICS

The output stage of the amplifier is a balanced class B design which insures a minimum of quiescent drain from the power supply. The output current rating is +20mA and -20mA, regardless of the power supply level. Rated output voltage swing in either direction is 10V less than the supply voltage of the same polarity, whether equal or unequal values of supply voltage are used. For example, supply voltages of +75VDC and -90VDC could legitimately be used. The output voltage rated swing in the positive direction would be +(75-10) = +65V, while the negative rated output voltage would be -(90-10) = -80V. Full power frequency is measured with ±100V swing and ±20mA of output current, on ±120VDC supplies.

POWER SUPPLY CONSIDERATIONS

The 3271/25 will operate quite satisfactorily over a range of power supply voltages from ±60VDC to ±120VDC. In addition the supplies may have unequal values, so long as each is between 60V and 120V. Amplifier noise and drift will be minimized if the power supplies are balanced, well regulated, and have low output ripple. High frequency performance will be best, and crosstalk between adjacent amplifier channels will be least, if the supply impedance at the amplifier pins is low at all frequencies from DC to above 100kHz. If the supplies incorporate provisions for remote voltage sensing, the sense leads should be connected to the positive and negative supply buses as close as possible to the amplifier pins. The common lead should be as short as possible. Heavy gauge bus wire should be used if long supply and common leads are necessary. The addition of bypass capacitors from the supply bus to common, at the amplifier pins, will reduce the equivalent supply impedance and may be required if supply leads are long. Figure 2 illustrates the ripple induced at the amplifier input as a result of supply ripple.

INSTALLATION RECOMMENDATIONS

The input lead to the amplifier summing junction should be shielded to avoid pickup of spurious signals, particularly signals at the chopper drive frequency of 100Hz. In integrator applications, a shielded wire may be used to connect the feedback or integrating capacitor to the amplifier input terminals. The center conductor should be connected to the amplifier input, while the shield is connected to the amplifier output. The lead employed should have high insulation resistance to prevent capacitor discharge.

OFFSET VOLTAGE ZERO CONTROL

The Model 3271/25 operates with low DC input offset voltage, without the use of a zero control. An optional external zero control may be employed to accurately null the amplifier offset. This control is shown in the package drawing.

EXTERNAL OVERLOAD INDICATOR

Electrical overload signals may be detected in the chopper stabilizing channel and applied through pin 5 to an external overload indicating circuit. In the suggested circuit of Figure 3, D1 and D2 are silicon diodes; Q1 is an NPN silicon switching transistor while Q2 is a PNP silicon switch. Lamp DS1 is a 10V, 15mA indicator, G.E. #1869 or equivalent. The circuit may be adapted for latching operation by including the 100kΩ resistor and the reset switch shown in dotted lines. The indicator will then remain lighted, after the amplifier comes out of saturation, until the reset switch is closed.

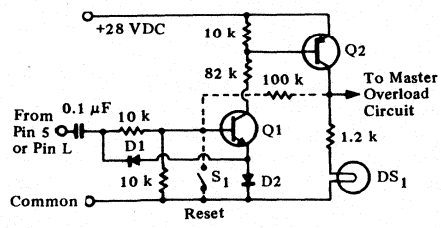

FIGURE 3. Overload Indicating Circuit.

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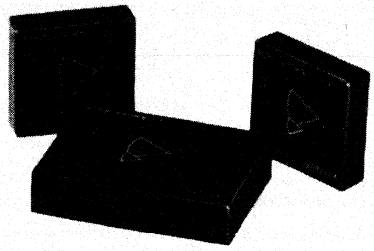

3291
3292
3293
3354
3355
3356

Chopper-Stabilized OPERATIONAL AMPLIFIERS

FEATURES

- DIFFERENTIAL INPUT OR SINGLE-ENDED
- VOLTAGE DRIFT AS LOW AS 0.1μV/°C
- CURRENT DRIFT AS LOW AS 0.5pA/°C

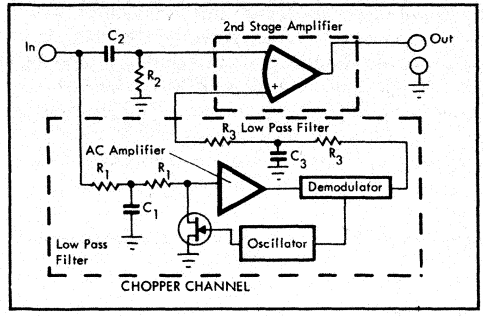

FIGURE 1. Single-ended Chopper-stablized Amplifier.

DESCRIPTION

Chopper-stabilized amplifiers achieve their ultra-low DC offset voltage and bias current by "chopping" the low frequency component of the input signal, amplifying this chopped signal in an AC amplifier and then demodulating the output of the AC amplifier. This output is then further amplified in a second stage of DC amplification. High frequency signals, which are filtered out at the input of the chopper channel, are coupled directly into the second stage amplifier. The net result of this technique is to reduce the DC offsets and drift of the second amplifier by a factor equal to the gain of the chopper channel. The AC amplifier introduces no offsets. Minor offsets and bias currents exist due to imperfect chopping, but these are extremely small.

The great strength of the chopper-stabilized amplifier is its insensitivity to component changes due to aging, temperature change, power supply variation or other environmental factors. Thus it is usually the best choice where both offset voltage and bias current must be small over long periods of time, or under significant environmental changes, and where external adjustment of offsets is undersirable or impossible. Both bias current and offset voltage can be nulled, if desired, by optional external controls. Figure 1 shows a simplified diagram of a single-ended chopper-stabilized op amp. Since the chopper channel, including switches and switch-driving oscillator, is built into the amplifier, only the DC power is supplied externally.

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ELECTRICAL SPECIFICATIONS

SPECIFICATIONS Typical at 25°C and rated supply unless otherwise noted.		MODELS	RATED OUTPUT V_o Volts min	RATED OUTPUT I_o mA min	DC GAIN dB min	BANDWIDTH Unity Gain MHz min	BANDWIDTH Full Power kHz min	SLEW RATE V/μsec min	INPUT NOISE Voltage 0.01 Hz to 10 Hz μV p-p	INPUT NOISE Voltage 10 Hz to 10 kHz μV rms	INPUT NOISE Current 0.01 Hz to 10 Hz pA p-p	INPUT NOISE Current 10 Hz to 10 kHz pA rms
	Low Cost Inverting Only	3291/14 3292/14 3293/14	±10	±5	140	3 typ	100	6.0	2	3	10	80
	Differential Input	3354/25 3355/25 3356/25	±10	±5	140	3	100	6.0	8	2	30	400

DIFFERENTIAL INPUT TYPES

Until the introudction of Burr-Brown Models 3354/25, 3355/25, and 3356/25, high performance chopper-stabilized operational amplifiers were always single-ended. In other words, they could only be used in inverting circuits. Now, with these units, the same ultra-low drift and low offset characteristics can be obtained for noninverting amplifiers, differential feedback amplifiers, sample/hold circuits, peak/hold circuits and many other applications where the amplifier must function with both differential and common-mode signals. These amplifiers are ideal for amplification of low level signals since the low drift and noise result in low input signal uncertainty. In addition, the gain and common-mode rejection ratio are very high, insuring excellent linearity of feedback gain (CMR for common-mode voltage of ±10V is typically 140dB at DC and 100dB up to 100Hz).

When the amplifier is used as a buffer for high impedance signal sources, the $10^{13}\Omega$ common-mode input impedance results in negligible loading of the source. Also, this causes the small DC input bias current to be virtually independent of input voltage - a very desirable characteristic for buffering of the memory capacitor in sample/hold and peak/hold circuits.

In general, these differential chopper-stabilized units can be used anywhere that a differential op amp would normally be used - but where both voltage and current drift must be very low.

LOW COST SINGLE-ENDED TYPES

For most inverting applications, Models 3291/14, 3292/14, or 3293/14 will be found to be the best choice. These units represent the state-of-the-art in single-ended chopper-stabilized amplifiers, featuring the lowest drift, lowest noise, lowest profile (1.5" x 1.5" x 0.4"), and the lowest prices available. Frequency response and slew rate are more than adequate for most applications.

Typical applications for these single-ended amplifiers are integrators, precision reference sources, D/A and A/D converters of high accuracy, precision comparators, current to voltage converters and high gain amplifiers for low level, low impedance signal sources.

Where a differential input is not required, these are the units to use for those applications where both low voltage drift and low bias current drift are required.

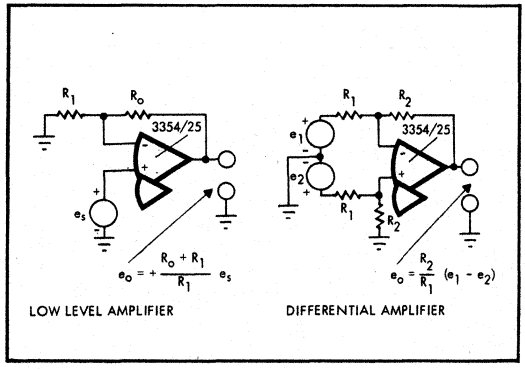


FIGURE 2. Typical Applications of Differential Chopper-stabilized Amplifiers.

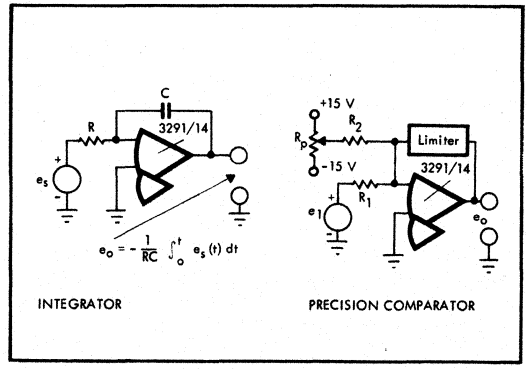


FIGURE 3. Typical Applications of Single-ended Chopper-stabilized Amplifiers.

INPUT OFFSET VOLTAGE		INPUT VOLTAGE DRIFT			INPUT BIAS CURRENT		BIAS CURRENT DRIFT		OPEN LOOP IMPEDANCES			POWER SUPPLY			PKG. DWG.	
At 25°C	Over Range -25°C to +85°C	Versus Temp. -25°C to +85°C	Versus Supply	Versus Time	At 25°C	Over Range -25°C to +85°C	Versus Temp. -25°C to +85°C	Versus Supply	Input Diff.	Input CM	Output	Nom. Rated	Range	Quies. Current	See Page 1-14	
µV max	µV max	µV/°C max	µV/V	µV/day	pA max	pA max	pA/°C max	pA/V	MΩ	Ω	kΩ	Volts	Volts	mA max	Fig. No.	
±20 ±50 ±100	±26 ±68 ±160	±0.1 ±0.3 ±1.0	±5	1 µV/mo	±50 ±50 ±100	±80 ±110 ±220	±0.5 ±1.0 ±2.0	±10	0.5	-	1.5	±15	±12 to ±18	±10	/14	
±30 ±50 ±100	±36 ±80 ±160	±0.1 ±0.25 ±1.0	±10	1 µV/mo	±20 ±50 ±50	doubles / +10°C		±1	1.0	10^{13}Ω	2.0	±15	±12 to ±18	±10	/25	

INSTALLATION, OPERATION AND APPLICATIONS INFORMATION

DRIFT CONSIDERATIONS

The best overall drift performance of an amplifier circuit will be achieved by minimizing impedance levels in the feedback network. The effect on output offset and drift of feedback and source impedances is illustrated in Figure 4. For very large resistances, input bias current becomes the major contributor to output voltage offset and drift. Where high input impedance and high gain are needed simultaneously, it may, therefore, not be feasible to use a single-ended inverting chopper-stabilized amplifier, because of this bias current factor. The differential input chopper-stabilized amplifier, used in the noninverting mode, then becomes the best choice. This allows the use of low impedance feedback networks while still retaining very high input impedance to prevent source loading. Note that input bias current doubles (approximately) for every +10°C temperature rise for these units.

The circuit of Figure 5 illustrates the effects of offset voltage and input bias current on integrator performance. Both parameters cause output errors which increase at a constant rate as a function of time. Additional offset voltage and input bias current caused by temperature drift will cause the output rate errors to increase with temperature. Note that the output rate error due to bias current diminishes as capacitance, C_F, increases. Usually, however, there is not much point in going beyond 10µF because of capacitor dielectric leakage. Also, as C_F is increased, R_i must decrease to maintain a given $R_i C_F$ product and there will usually be a lower limit on desirable values of R_i, since this represents the input impedance of the integrator. Also, R_i determines the amount of input and feedback current flowing for a given input level. The amplifier, and the signal source, must be capable of supplying this current. Thus a compromise set of R_i and C_F can usually be reached which takes into account these factors.

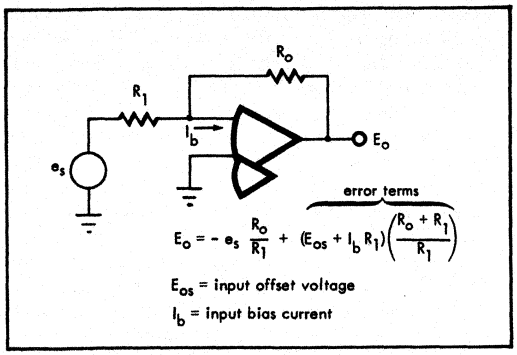


FIGURE 4. Output Drift Components.

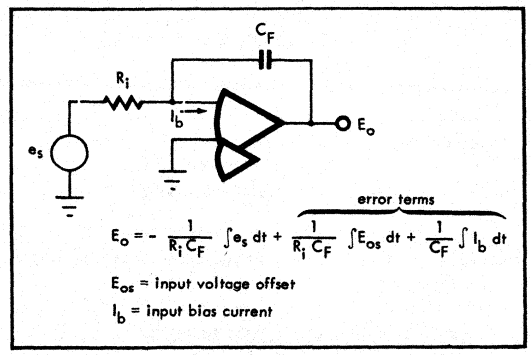


FIGURE 5. Integrator Errors Due to Offset Voltage and Bias Current.

NOISE CONSIDERATIONS

Because of the extremely low DC offset and DC drift associated with the chopper-stabilized amplifier, noise is often found to be the remaining limit on signal resolution. Thus it is desirable to design the feedback networks and external wiring to minimize the total circuit noise. This includes the proper grounding and noise decoupling as described under Wiring Recommendations. In addition it is desirable to minimize the levels of feedback impedance as a means of reducing noise "pickup" and the effects of amplifier current noise. When the full bandwidth of the amplifier is not required, it is recommended that a feedback capacitor be used to

limit the overall bandwidth and eliminate as much high frequency noise as possible.

When one of the differential input, chopper-stabilized amplifiers is used with a high impedance source, the input current noise will be the limiting factor on signal resolution. For source impedances of 1kΩ or greater it is recommended that a compensating resistance, R_C, be inserted in series with the inverting input (see Figure 6). This resistor will minimize the effect of current noise at the chopper frequency.

Shielding of feedback components is desirable and may be necessary in electrically noisy environments. Use of shielded wire for summing junction leads is also

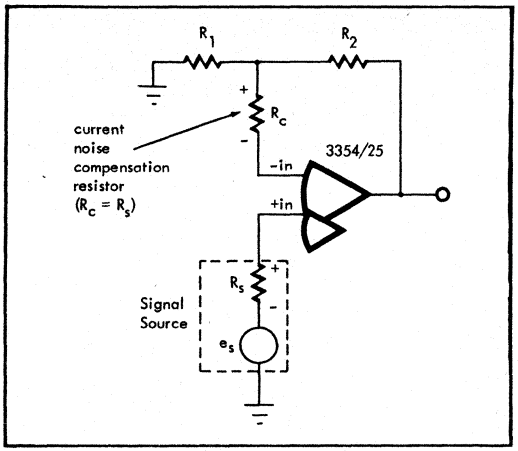


FIGURE 6. Use of a Current Noise Compensating Resistor with Differential Chopper-stabilized Operational Amplifier.

recommended in high noise environments. The shield should then be connected to the output terminal of the amplifier.

POWER SUPPLY REQUIREMENTS

The amplifiers described in this brochure are specified for operation on the rated supply voltages (±1%). They will operate with some degradation over the specified range

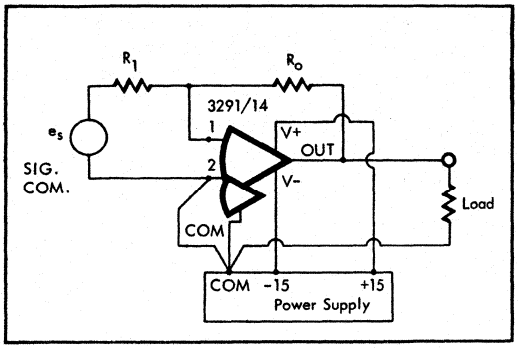


FIGURE 7. Proper Grounding of Models 3291/14, 3292/14 and 3293/14.

of supply voltages (±12VDC to ±18VDC for ±10V amplifiers).

Supply drain current is specified under quiescent conditions (no output current from the amplifier). When the amplifier is supplying current to a load, this current must be added to the quiescent current of the proper supply to determine total supply current.

WIRING RECOMMENDATIONS

Models 3291/14, 3292/14 and 3293/14 are designed with separate pins for power supply command and signal common. The diagram of Figure 7 illustrates the proper grounding techniques for these amplifiers. It is important that the signal common and power common leads be connected only at pin 2 of the amplifier. A separate lead is required from the power supply common to the COM pin of the amplifier.

Figure 8 illustrates proper grounding for noninverting circuits using the differential amplifiers (3354/25, 3355/25, 3356/25).

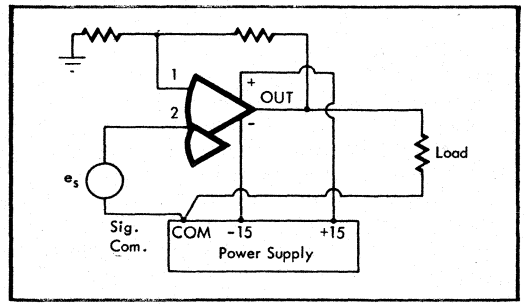


FIGURE 8. Proper Grounding of Differential Models (Noninverting Mode).

OVERLOAD CHARACTERISTICS

Because the chopper-stabilized amplifier consists of two amplifying channels, one fast and the other very slow, the overload behavior is different from that of nonchopper-stabilized op amps. If the chopper channel becomes overloaded due to a large error voltage at the summing junction, recovery may require as much as a few seconds. There are three ways in which such overloads may occur - output voltage saturation, output current limiting, and transient overload induced when power supply voltages are applied. The first of these three possible conditions arises when the amplifier output voltage is driven to its limits. When the output voltage can no longer follow the input signal, the summing junction voltage rises from its virtual ground potential. This relatively large potential is then amplified by the high gain of the chopper channel to a level of several volts, a much larger value than is encountered in the chopper channel during normal operation. Because of the very large time constants of the chopper channel filters, decay of this overvoltage, and consequently amplifier recovery, may take several seconds after removal of the overdrive signal. When the

amplifier reaches one of its output current limits, under the proper combination of loading and signal, a condition much like that of voltage saturation occurs. The output voltage fails to follow the input signal and chopper channel overload occurs.

In general, the amplifier will recover quickly from transient or short duration overloads since the relatively slow chopper channel will not become charged to high levels.

Overloads due to output voltage limiting (not current limiting) may be prevented by use of a feedback limiter such as that of Figure 9. Because the amplifier summing junction is always held at virtual ground, even when the limiter is active, the chopper channel does not overload and recovery from limiting is very rapid (1.0μsec or less is typical). The limits must, of course, be set below the output saturation levels of the amplifier itself.

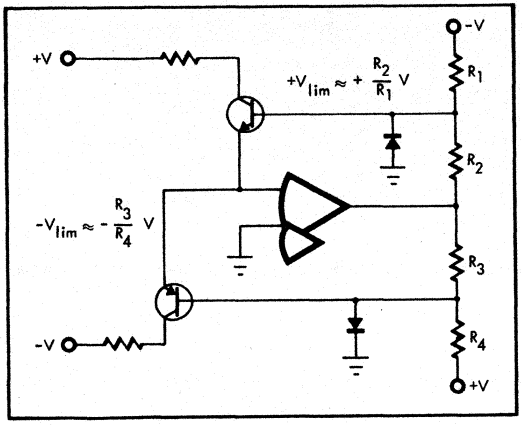


FIGURE 9. Feedback Limiter Circuit.

Overloads which occur during the application of DC power to the amplifier are a result of transient imbalances within the circuit. Recovery time from this type of overload is a function of circuit design. Where rapid recovery from such initial overloads is important, Models 3354/25, 3355/25 and 3356/25 are the best choices. These amplifiers typically recover to specified operation in less than one second. They recover equally fast from extended overload due to signal overdrive conditions for simple resistive feedback.

DC NULLING TECHNIQUES

The proper connections for nulling of the DC offset voltage are shown in the Mechanical Specifications. Note that in all cases these offset controls are optional and need not be used if the small offset voltage of the amplifier can be tolerated. The differential chopper-stabilized models (3354/25, 3355/25 and 3356/25) can be nulled as shown in Figure 10. However, the inherent offset voltage of these amplifiers is acceptably low (typically less than 10μV) for many applications and the null control may be unnecessary.

The input current of the amplifier may be nulled as in Figure 11 (for inverting circuits).

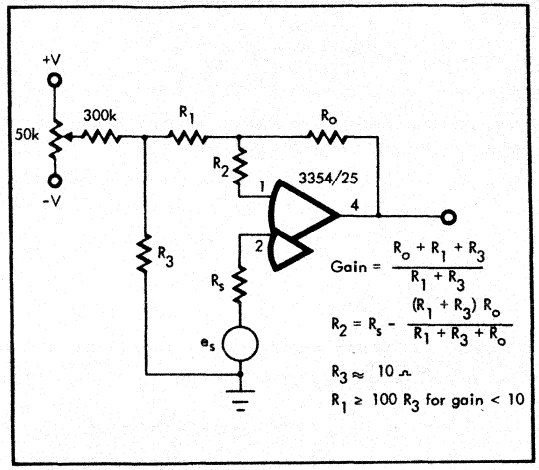


FIGURE 10. Offset Voltage Adjustment for Noninverting Circuits.

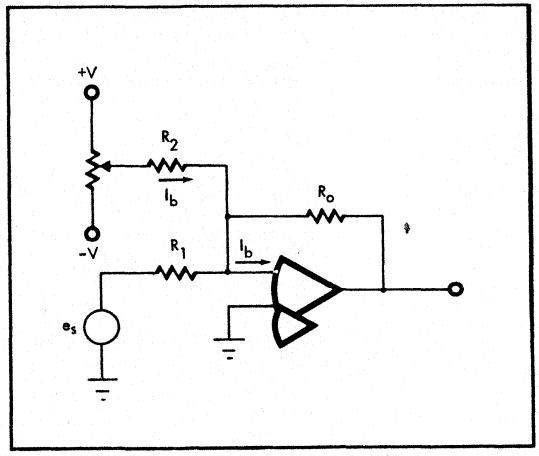


FIGURE 11. Null Adjustment of Input Current.

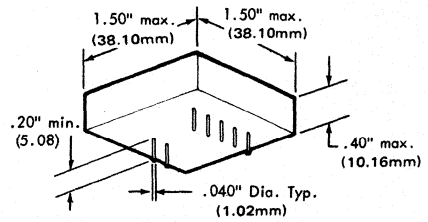
INPUT/OUTPUT PROTECTION

The various amplifiers described here are designed such that any voltage up to the value of power supply voltage may be applied directly to the amplifier input pin without damage to the amplifier.

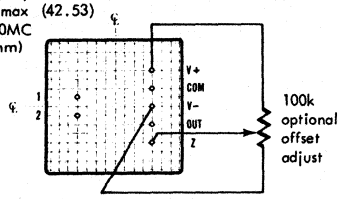
Output stages of the amplifiers are current limited to prevent damage should the output pin be shorted to common. Permanent damage to the amplifier may occur, however, if the output pin is connected to a voltage of the same order of magnitude as the supply voltages.

MECHANICAL SPECIFICATIONS

/14 MODULES



PIN - Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
MATERIAL - Black Epoxy
WEIGHT - 1.50 oz. max (42.53)
CONNECTOR - 1400MC
GRID - 0.1" (2.54mm)

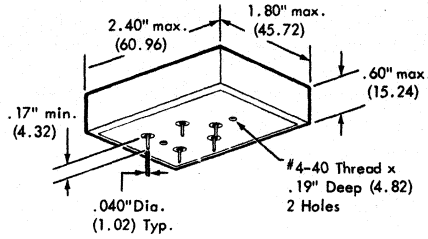


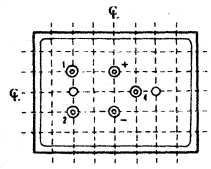
PIN CONNECTIONS - are as follows unless otherwise noted.

Pin	Connection
1	inverting input
2	signal common or noninverting input
3	(not used)
4 (OUT)	output
5	(not used)
+ (V+)	positive supply
- (V-)	negative supply
COM	power common
Z	optional offset adjust

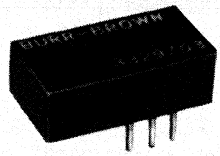
/25 MODULES

PIN - Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
MATERIAL - Black Epoxy
WEIGHT - 4.00 oz. max (113.40)
CONNECTOR - 1500MC
GRID - 0.3" (7.6)





BURR-BROWN

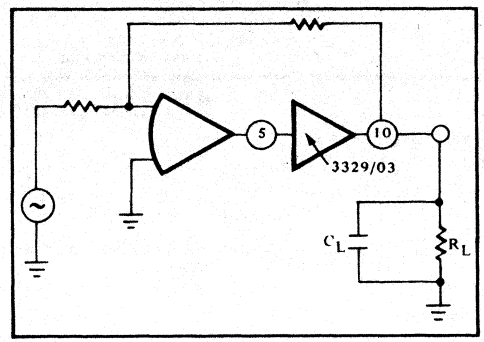


3329/03

HYBRID IC POWER BOOSTER

FEATURES

- ±100mA OUTPUT
- SHORT CIRCUIT PROTECTED
- NO HEAT SINK REQUIRED
- DUAL-IN-LINE PACKAGE



DESCRIPTION

The Model 3329/03 is a power booster amplifier designed for use in cascade with IC or discrete component operational amplifiers inside the feedback loop. Current output of up to ±100mA at ±10VDC is provided without the need for a heat sink. The unit is short circuit protected over the full temperature range or -40°C to +85°C. Output current is limited to ±15mA by internal circuitry. No external components are required. The high full power frequency (1MHz) and small signal bandwidth of 5MHz insure that the unit will not degrade the frequency response of the operational amplifier used.

The class B output stage provides high output current with a minimum of quiescent power supply drain. The low open loop output impedance (10Ω) insures stable operation with large capacitive loads, and virtually eliminates the closed loop gain loading effect of low impedance loads such as 50Ω terminated lines. Because of the 10kΩ input impedance of the booster, the current output requirements of the operational amplifier are minimal.

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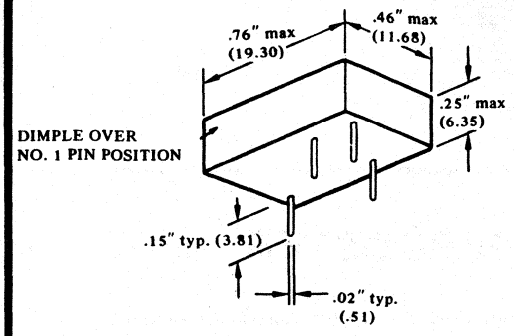
PDS-225E

Printed in U.S.A. July, 1978

MECHANICAL SPECIFICATIONS

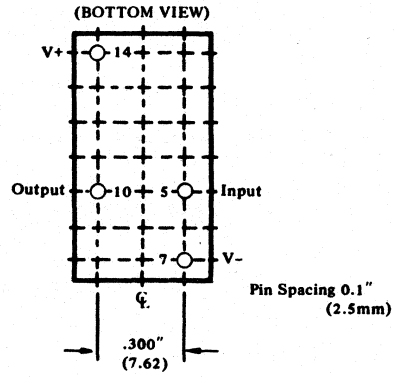
Dimensions in millimeters are shown in parentheses.

PHYSICAL DIMENSIONS



Weight: 0.12 Oz. (3.40 grams) max.
Material: Black Epoxy
Pins: Tin plated nickel
Connector: Fits any commercial dual-in-line connector

CONNECTION DIAGRAM



APPLICATIONS INFORMATION

Power Supply Requirements

The Model 3329/03 is designed to operate over a power supply range of ±12 VDC to ±18 VDC. Output voltage swing is guaranteed to be in excess of ±10 volts at full load, when operating on supplies of ±15 VDC. For other values of supply voltage, the output swing varies in proportion.

Gain and Stability

The voltage gain of the 3329/03 is approximately 1.0. The accuracy of this gain is relatively unimportant, since the booster is used inside the feedback loop of an operational amplifier. The booster by itself is completely stable under all conditions of capacitive loading. Because of it's very low output impedance, the 3329/03 tends to isolate the associated operational amplifier from the effects of capacitive load.

The input impedance of the booster is approximately equal to 100 x (load impedance). Thus, for a 100 ohm load, the input impedance is approximately 10 k ohms. The effective output impedance of the booster is approximately equal to the output impedance of the operational amplifier, divided by 100.

For most general purpose operational amplifiers the dynamic output impedance is on the order of 1 kΩ. When a low impedance load (e.g. 50Ω) is being driven, a severe loading effect occurs which greatly reduces the effective open loop gain and bandwidth. Effectively, the unloaded gain and bandwidth of the operational amplifier would be multipled by the loading factor $\frac{50}{1050} \approx .05$, if the load is 50Ω.

When the 3329/03 booster is used, however, the effective open loop output impedance is 10Ω. The loading factor now is $\frac{50}{60} = .866$, and the gain and bandwidth are reduced only slightly by this loading.

Input and Output Protection

The output stage of the 3329/03 is current limited to insure survival of the booster if the output is shunted to ground. The unit is safe even under continuous short circuit at +85°C. No heat sink is required.

The input circuitry will withstand overvoltage up to the value of supply voltage.

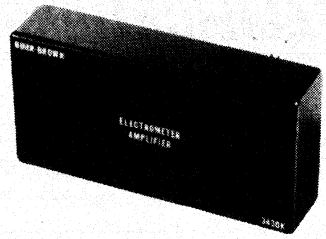
Temperature Range

The 3329/03 will operate over the -40°C to +85°C temperature range. Storage temperature range may vary from -55°C to +100°C.

3329/03 POWER BOOSTER SPECIFICATIONS

Rated Output		Full Power Response	-3dB Response	Input Signal Range	Input Offset Voltage	Input Impedance	Output Impedance	Power Supply Requirements			
V_O Volts (min)	I_O mA (min)	kHz (min)	MHz (min)	Volts (min)	mVolts (max)	kΩ (typ.)	Ω (typ.)	Nom. Rated Volts	Range Volts	Quies. Current mA (max)	
±10	±100	1000	5	±10	±50	10	10	±15	±12 to ±18	±15	

BURR-BROWN



3430
3431

ELECTROMETER AMPLIFIERS

FEATURES

- ULTRA-LOW INPUT CURRENT, .01pA, max
- LOW INPUT CURRENT NOISE, .001pA, p-p
- HIGH INPUT IMPEDANCE, $10^{14}\Omega$
- INVERTING OR NONINVERTING OPERATION

DESCRIPTION

Models 3430 and 3431 are designed to minimize input bias current and input noise current through the use of a varactor diode bridge technique. Models 3430J and 3430K are intended for meaurement of very-low-level currents, long-term integrators and analog memory applications. The 3431J and 3431K are designed for measurement of sub-millivolt signals from very high source impedances such as pH and other electrochemical cells, and in long-term track/hold applications where charge stored on a capacitor is the input signal source.

The varactor bridge technique uses the voltage variable capacitance and extremely low leakage current of the two zero-biased varactor diodes to achieve input bias current and input current noise 10 to 100 times less than that of FET amplifiers.

The 3430 and 3431 out-perform amplifiers that use electrometer tubes or MOSFET input stages. Primary areas of advantage over these other devices are in voltage drift, common-mode rejection, and lower cost. An additional advantage over MOSFET's is the inherent input protection of the varactor bridge input configuration.

Operation of the 3430 and 3431 are simply explained. The amplifier input voltage, e_{in}, varies the capacitance of the varactor diodes, causing a bridge unbalance and developing a bridge output signal at the carrier frequency. This carrier frequency signal, which is proportional in amplitude to the input signal level, is amplified by the low-noise AC amplifier, phase-sensitivity demodulated to restore correct polarity and filtered to eliminate the carrier components. Additional amplification is provided by a conventional DC amplifier stage. The output is equal to the product of input signal and open-loop gain.

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PDS-258C

Printed in U.S.A. July, 1978

SPECIFICATIONS

(Typical @ 25°C and ±15 VDC unless otherwise noted)

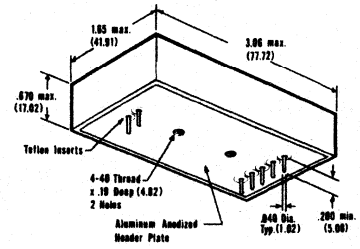
MODEL	3430J/K	3431J/K
OPEN LOOP GAIN		*
2k Ω load, min.	100 dB	
RATED OUTPUT		*
Voltage, min	±10 V	
Current, min	±5 mA	
Load Capacitance	0 to .01 µF	
Output Impedance @ DC	2 k Ω	
FREQUENCY RESPONSE		
Unity gain, small signal	2 kHz	*
Full power response, min	7 Hz	
Slewing rate, min	0.4 V/ms	
Overload recovery	10 ms	
INPUT OFFSET VOLTAGE		
External trim pot	100 k Ω	*
Avg. vs. temp (10°C to 70° C) max	±30 µV/°C (J) ±10 µV/°C (K)	±30 µV/°C (J) ±10 µV/°C (K)
vs. supply voltage	±500 µV/V	*
vs. time	±100 µV/mo.	*
Warm-up drift	75 µV (15 min)	*
INPUT BIAS CURRENT		
Initial bias, 25°C, max		
Inverting input	±0.01 pA	±1 nA
Non-inverting input	±1 nA	±0.01 pA
Avg. vs. temp (signal input only)**	x2/10°C	*
vs. supply voltage (signal input only)	±0.01 pA/V	*
INPUT IMPEDANCE		
Differential	-	3×10^{11} Ω || 30 pF
Inverting input (to common)	3×10^{11} Ω || 30 pF	10^9 Ω || .02 µF
Non-inverting input (to common)	-	10^{14} Ω || 35 pF
INPUT NOISE		*
Voltage, .01 to 1 Hz, p-p	10 µV	
1 to 100 Hz rms	5 µV	
Current, .01 to 1 Hz, p-p	.001 pA	
1 to 100 Hz, rms	.002 pA	
COMMON MODE CHARACTERISTICS		
Max safe input voltage	±300V	±300V
Max common mode	NA	±200V
Common mode rejection @ ±25V	NA	100 dB
POWER SUPPLY		*
Voltage, rated specification	±15V	
Voltage, operating	±(12 to 18)V	
Current, quiescent	+15, -6 mA	
TEMPERATURE RANGE		*
Operating, rated specifications	0° to +70°C	
Operating, derated specifications	-25° to +85°C	
Storage	-55° to +85°C	
MECHANICAL		*
Case style	28	
Mating connector	2800MC	
Weight	6 oz.	

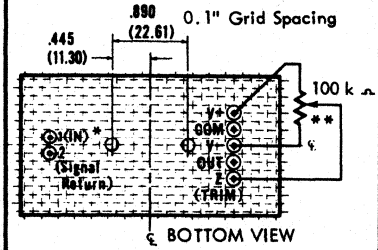
* Specification same as 3430.

** Negative input for Model 3430; positive input for Model 3431.

PACKAGE CONFIGURATION

NOTE: Dimensions in millimeters are shown in parentheses.

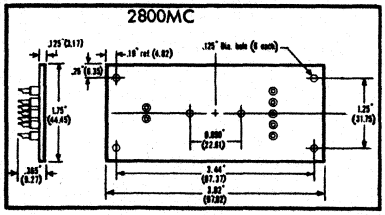




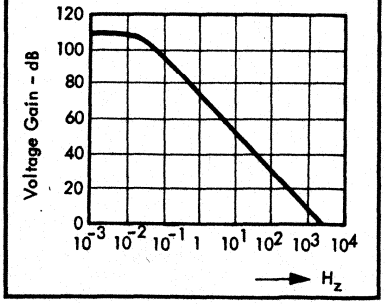
*-IN, 3430 **Optional Offset Adjust
+IN, 3431

PINS - Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
MATERIAL - Aluminum Case
Aluminum Anodized Header
WEIGHT - 6 oz max (170)

2800MC



OPEN LOOP FREQUENCY RESPONSE



APPLICATIONS INFORMATION

The varactor bridge amplifiers presented in this brochure are the best choices where the performance requirements are for low input bias current, low input noise current or high input impedance and where response speed is not important. The primary circuit applications of such amplifiers are shown in Figures 1 through 4.

For inverting applications, such as those of Figures 1 and 2, either Model 3430J or Model 3430K (inverting types) should be chosen.

In Figure 1, the varactor amplifier is being used to convert an input current signal to output voltage. The inverting input of the amplifier remains at "virtual ground" potential and input signal current flows through the feedback resistor, generating the desired output voltage. Input impedance presented to the current source is near zero, a desirable loading condition (for a current source). The input signal resolution is limited only by the input bias current and input noise current of the amplifier.

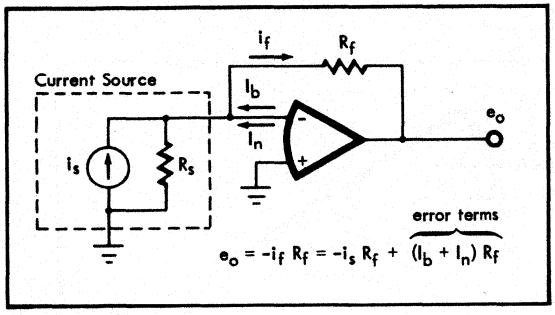


FIGURE 1. Current to Voltage Converter (Current Amplifier).

In the integrator circuit of Figure 2, the low bias current permits long term integration or holding capability. The bias current of the amplifier flows into C_F and causes the time dependent error

$$\epsilon_1 = \frac{1}{C_f} \int_o^t I_b \, dt \quad , \text{thus the}$$

need for low bias current in such applications. Offset voltage of the amplifier (V_{os}) contributes the additional error,

$$\epsilon_2 = \frac{1}{R_1 C_f} \int_o^t V_{os} \, dt + \frac{1}{R_d C_f} \int_o^t V_{os} \, dt.$$

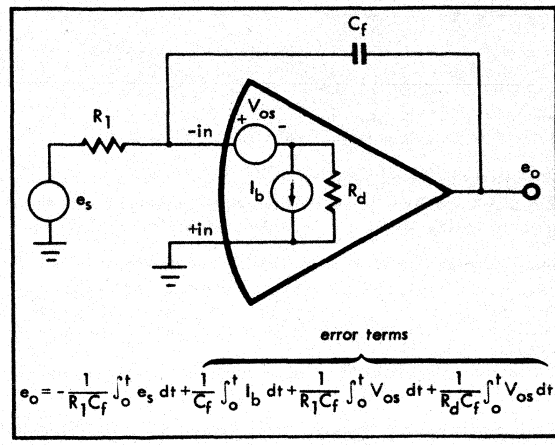


FIGURE 2. Long Term Integrator.

The circuits of Figures 3 and 4 are buffer amplifiers which provide high input impedance and, thus, low input current. In Figure 3, the amplifier is used to amplify the signal from a high impedance voltage source. Input impedance is $10^{14}\,\Omega$ for varactor models 3431J and 3431K.

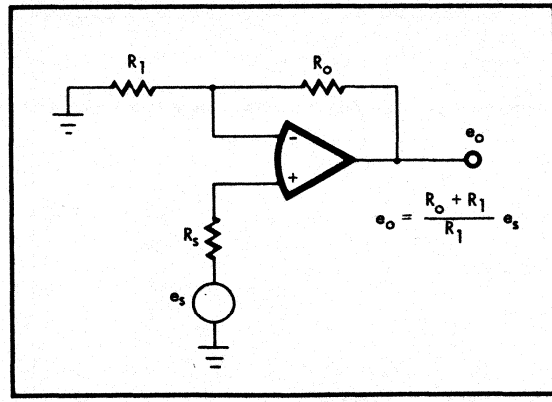


FIGURE 3. High Impedance Buffer Amplifier.

The unity gain voltage follower of Figure 4 is used to buffer the memory capacitor in a long-term sample/hold circuit. The $10^{14}\,\Omega$ input impedance and .01 pA bias current of varactor amplifiers allow the use of very low values of C_H and long hold times.

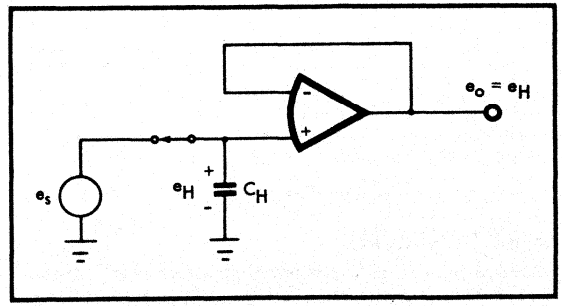


FIGURE 4. Unity Gain Buffer Used as Sample/Hold.

INPUT BIAS CURRENT

One of the primary characteristics of varactor amplifiers is the very low input bias current. This is defined as the current which flows into the amplifier for zero input potential and is measured in the test circuits of Figure 5. Note that bias current of varactor amplifiers is low only at the signal input.

Bias current at the inverting input flows through the feedback resistor and places a limit on resolution for current amplifiers such as that of Figure 1. For integrator circuits (Figure 2) the bias current flows into the feedback capacitor and causes integrator drift errors. For noninverting circuits (Figure 3) the bias current flows into the source resistance, generating an error voltage. If the source is capacitive, as in the case of a sample/hold amplifier (Figure 4), the bias current at the noninverting input causes decay of the voltage held on the capacitor and consequently limits the feasible hold time for a given size of capacitor.

Input current at the noninverting input consists of the bias current and an additional component of current due to the input voltage applied to the common mode input impedance.

The input bias current of varactor amplifiers is due to the leakage current of two matched varactor diodes. Because these varactors are zero biased and their individual leakage currents tend to cancel, the input bias current of the amplifier is extremely low (.01 pA).

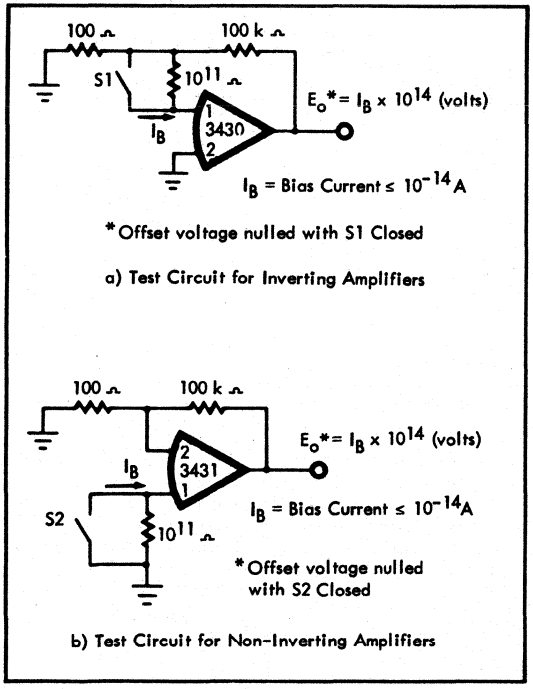


FIGURE 5. Bias Current Test Circuits for Varactor Amplifiers.

INPUT IMPEDANCE

Input impedance of varactor amplifiers requires further explanation. For inverting models 3430J and 3430K, the impedance from input to common is of interest. The diagram of Figure 6 defines the input impedance of these inverting models, including the input capacitance. Note that, although pin 2 is normally connected to common, it is possible to apply a voltage at this point. The resulting output voltage will depend on the feedback network. In any case, the external impedance from pin 2 to power supply common must be low.

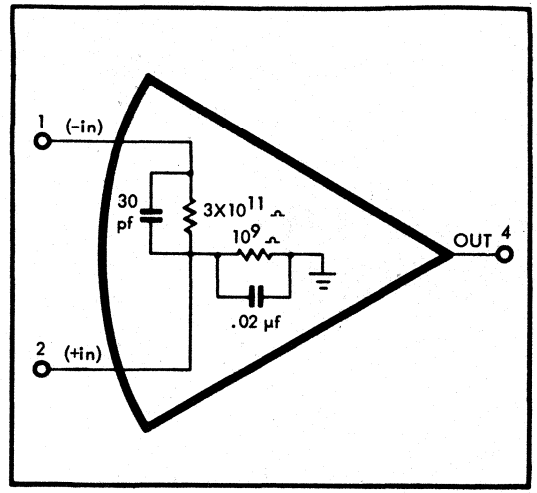


FIGURE 6. Equivalent Input Impedance Circuit of Varactor Models 3430J and 3430K.

The input impedance characteristics of the noninverting varactor models 3431J and 3431K are illustrated in Figure 7. Although the differential input impedance of these amplifiers is much lower than the common mode input impedance, the differential voltage remains very small (due to feedback). Thus the differential input impedance is bootstrapped to a value larger than the common mode input impedance, and may be considered negligible in comparison. Consequently, the effective input impedance of these noninverting amplifiers is 10^{14} Ω in parallel with 2 pf.

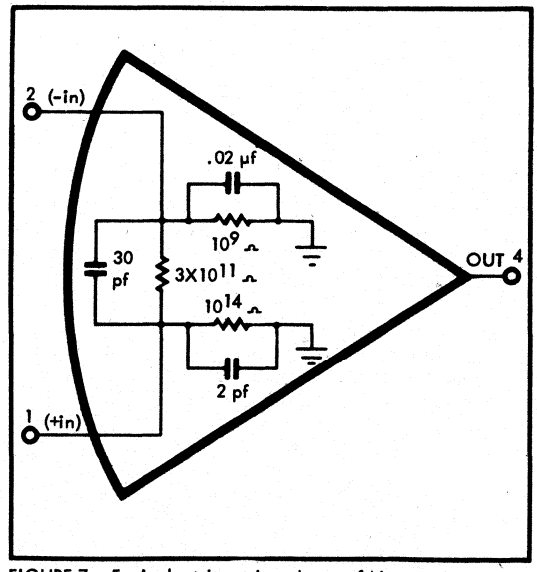


FIGURE 7. Equivalent Input Impedance of Varactor Models 3431J and 3431K.

COMMON MODE PERFORMANCE

Varactor amplifiers, because of the balanced, transformer coupled input stage offer a CMR of 100 dB (noninverting Models 3431J and 3431K). Common mode input voltage is limited only by transformer and capacitor breakdown voltages (±200V).

SLEW RATE, BANDWIDTH AND STABILITY

For applications where the ultimate in input current resolution is required, varactor amplifiers will represent the best choice, but will sacrifice speed of response. If slew rate becomes a limiting factor, the output voltage of the varactor amplifier should be scaled down and an additional amplifier should be used following the varactor to provide the additional gain of 10 or 100. Specifications of this second amplifier will not be critical - Model 3267/12C is a good choice.

Instability may be encountered in varactor amplifiers as a result of the relatively high differential input capacitance of the amplifier and large feedback resistors. If this is encountered, it can usually be cured by connecting a capacitor from output to inverting input. This capacitor will usually be less than 5 pf. Since it is in parallel with the large feedback resistor, it should have low leakage. Polystyrene or glass types are usually suitable. Note that this method improves stability at the expense of bandwidth.

AMPLIFIER NOISE

These varactor amplifiers are particularly low in current noise and, thus, are preferred in applications where high source impedances and low level current signals are encountered. Output voltage noise due to this current noise is proportional to the value of feedback resistance in inverting circuits. In non-inverting circuits the current noise flows in the source impedance, generating voltage noise which is then amplified by the closed loop gain factor of the amplifier.

RFI AND NOISE

Since the input circuit of a varactor amplifier operates from a high frequency ($\approx$ 130 kHz) carrier signal, beats between this carrier and other high frequency signals may appear at the amplifier input. If shielding does not eliminate the problem, filtering on the input or at the power supply leads may help. It is possible for an interfering signal to be generated by the carrier of another varactor amplifier operating from the same power supply.

LEAKAGE CURRENTS

In order to realize the current resolution capabilities of these amplifiers, the user must take certain precautions in the design and layout of external wiring and feedback elements. For varactor amplifiers, hard wiring is preferable to PC boards due to the difficulty of obtaining sufficiently low leakage currents on PC boards. If PC board mounting is necessary, teflon stand-offs and hard wiring of signal leads are recommended. Teflon insulated wire is best. The Burr-Brown 2800MC connector uses teflon insulators and is suitable for use with these amplifiers.

LARGE RESISTORS

In certain applications, such as current amplifiers and long-term integrators, it will be necessary to use very large resistors, 10^7 to 10^{12} ohms. Sources for such resistors are Victoreen*, Electra Mfg. Co. **, and Pyrofilm Resistor Co. ***. Metal film resistors have the best temperature stability (about 100 ppm/°C) and accuracies to 0.1% but are only available in values up to about 10^7 ohms. Special carbon resistors are available in values up to 10^{14} ohms but have relatively large temperature coefficients (about 1000 to 5000 ppm/°C), tolerances of 1% to 10%, and relatively poor long term stability.

*3151 Fiberglas Rd., Kansas City, Kansas 66115
**10101 Woodland Ave., Cleveland, Ohio 44114
***3 Saddle Rd., Cedar Knolls, N. J. 07927

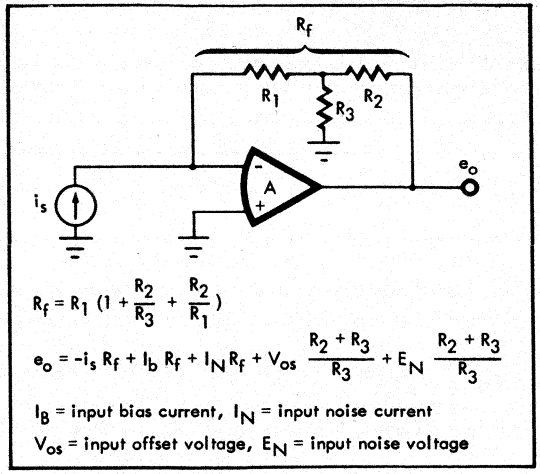


FIGURE 8. Current-to-Voltage Converter With Voltage Divider Feedback.

The current amplifier circuit of Figure 8 illustrates a means of obtaining an effectively very large resistor through the use of smaller more stable metal film types. Note, however, that voltage noise and offset are amplified by the ratio, $\frac{R_2 + R_3}{R_3}$.

Also the loop gain of the circuit is reduced by the factor, $\frac{R_3}{R_2 + R_3}$.

SHIELDING AND WIRING CONSIDERATIONS

Because of the high impedance levels at which these amplifiers may be operated, shielding is important to reduce noise pickup. It will usually be necessary to include feedback elements inside the shield. If the signal source is outside the shield, a shielded cable should be used. In order to eliminate microphonics, or self-generated cable noise (tribo-electric effect), caused by the shield of the coaxial cable rubbing against the insulation when the cable is flexed, a low noise cable having a graphite coating or conductive tape between insulation and cable should be used.*

The proper methods for grounding of varactor amplifiers are shown in Figures 9 and 10. Changes in capacitance between input wiring and other objects will cause extraneous voltages at the input. To minimize this effect, the wiring should be as rigid and as short as possible and should be spaced as far as possible from other objects.

Insulation of the components and wiring associated with the input signal terminal must be very good. Teflon standoffs and insulation are the best choice because of the insulation properties and the fact that dirt and moisture do not adhere to teflon. The Burr-Brown 2800MC connector has teflon insulated pin jacks and is recommended for use with these amplifiers.

The proper technique for zeroing of DC offset voltage is shown with the package configuration.

*For example, Amphenol Type 21-537

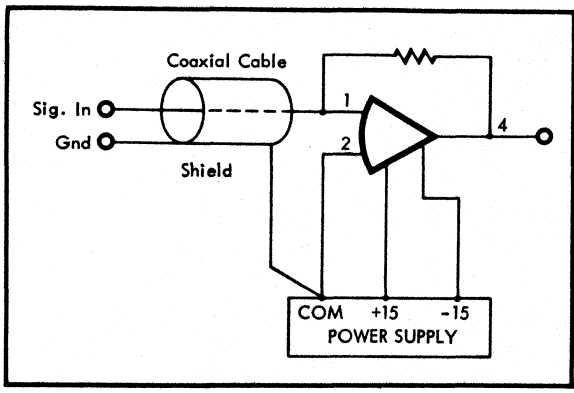


FIGURE 9. Proper Grounding of Inverting Varactor Amplifiers.

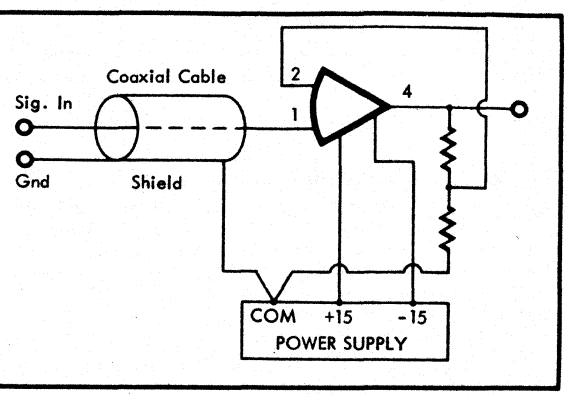
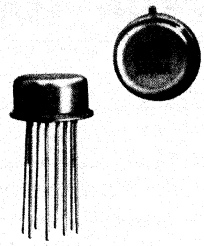


FIGURE 10. Proper Grounding of Noninverting Varactor Amplifiers.

BURR-BROWN



3500 SERIES

Low Bias Current OPERATIONAL AMPLIFIERS

FEATURES

- LOW BIAS CURRENT, ±15nA, max
- LOW DRIFT, ±3μV/°C, max
- LOW NOISE, 1.4μV, p-p
- WIDE SUPPLY RANGE, ±3VDC to ±20VDC
- INTERNAL COMPENSATION
- REPLACES 741 TYPE AMPLIFIERS

DESCRIPTION

The 3500 IC op amps are designed for low input current while maintaining slew rate and bandwidth adequate for most applications. The low input bias current is achieved by a unique bias current cancelling circuit. This method insures that the bias current remains low over the full temperature and common-mode voltage ranges. The same circuitry gives the amplifier high input impedance, both differential and common-mode. The amplifier maintains internal current levels essentially constant over the full range of power supply voltages. Thus the offset voltage and drift remain low for all combinations of supply voltage.

Both military and industrial temperature range versions are offered. Drift selected units are offered at ±3, ±5, ±10 and ±20μV/°C, max. The 3500 is also a very low noise IC op amp as illustrated by the curves included herein. Both current and voltage noise are low, including the low frequency "flicker" and "popcorn" noise which usually prevent the use of IC op amps for low-level signal processing.

The 3500 is internally compensated for unconditional stability for all feedback configurations, even with capacitive loads. The slew rate is independent of supply voltage level. The input stage of the 3500 series exhibits no latch-up when the common-mode voltage range is exceeded. The input impedance remains high with differential inputs as high as ±30V. Thus the amplifier can be used as a sensitive comparator. The output stage is internally current limited to provide protection against continuous short circuits. The 3500 is interchangeable with 741 type amplifiers but gives greatly improved performance.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-237J

Printed in U.S.A. July, 1978

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

MODELS 3500 A/B/C **
3500 R/S/T

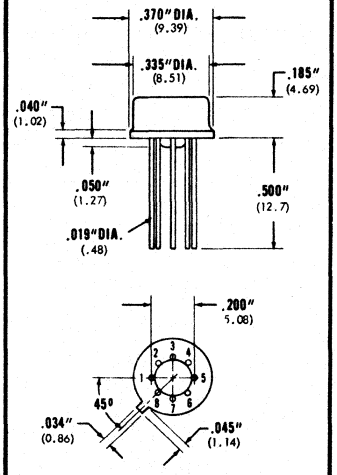
Specifications (Typical at 25°C and ±15 Vdc power supply unless otherwise noted.)

	3500A 3500R	3500B 3500S	3500C 3500T
OPEN LOOP GAIN, dc, no load	93 dB, min	*	*
RATED OUTPUT		*	*
Voltage	±10V, min		
Current	±10 mA, min		
Output Impedance	2 kΩ		
FREQUENCY RESPONSE		*	*
Unity Gain, Small Signal	1.5 MHz		
Full Power Sine Wave	10 kHz, min	12 kHz, min	15 kHz, min
Slew Rate	0.6 V/μsec, min	0.8 V/μsec, min	1.0 V/μsec, min
INPUT OFFSET VOLTAGE			
Initial Offset @ 25°C	±5 mV, max	±2 mV, max	±1 mV, max
Avg. vs. Temp (-25 to +85°C) max	±20 μV/°C(A)	±5 μV/°C(B)	±3 μV/°C (C)
(-55 to +125°C) max	±20 μV/°C(R)	±10 μV/°C(S)	±5 μV/°C(T)
vs. Supply Voltage	±40 μV/V	*	*
vs. Time	±2 μV/day	*	*
INPUT BIAS CURRENT			
@ 25°C (either input)	±30 nA, max	±20 nA, max	±15 nA, max
Avg. vs. Temp (-25°C to +85°C), max	±1.0 nA/°C(A)	±0.5 nA/°C(B)	±0.3 nA/°C(C)
(-55°C to +125°C), max	±1.5 nA/°C(R)	±1.0 nA/°C(S)	±0.5 nA/°C(T)
vs. Supply Voltage	±0.2 nA/V	*	*
INPUT DIFFERENCE CURRENT			
@ 25°C	±15 nA	±10 nA	±7 nA
Avg. vs. Temp (-25°C to +85°C)	±0.5 nA/°C(A)	±0.2 nA/°C(B)	±0.1 nA/°C(C)
(-55°C to +125°C)	±0.7 nA/°C(R)	±0.5 nA/°C(S)	±0.2 nA/°C(T)
vs. Supply Voltage	±0.1 nA/V	*	*
INPUT IMPEDANCE		*	*
Differential	10^7 Ω || 3 pf		
Common Mode	5×10^9 Ω || 3 pf		
INPUT NOISE		*	*
Voltage, .01 Hz to 10 Hz, p-p	2.0 μV		
10 Hz to 10 kHz, rms	1.4 μV		
Current, .01 Hz to 10 Hz, p-p	200 pA		
10 Hz to 10 kHz, rms	35 pA		
INPUT VOLTAGE RANGE		*	*
Common Mode Voltage	±11 V, min		
Common Mode Rejection @ ±10 V	100 dB		
Max. safe input voltage***	± supply		
POWER SUPPLY		*	*
Voltage, rated specification	±15 V		
Operating Range	±3 to ±20 V		
Current, quiescent	±3.5 mA, max		
TEMPERATURE RANGE, ambient			
Operating, Rated Specs A, B, C	-25 to +85°C	*	*
R, S, T	-55 to +125°C	*	*
Storage	-65 to +150°C	*	*

*Specifications same for all models. **The Mini-DIP package is available for Models 3500 A/B/C. This option is specified by adding an N suffix to the model number (e.g. 3500AN, 3500CN). If the N is omitted, the TO-99 package will be supplied. *** If signal voltage is applied to the input in the absence of power supply voltage, series resistance should be used to limit input current to 20 mA.

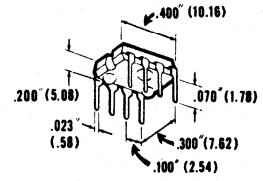
TO-99 PACKAGE

Specify 3500A, etc.



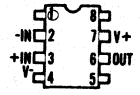
MINI-DIP PACKAGE

Specify 3500AN, etc.



TOP VIEW

Dimple appears over pin space #1



Note: Dimensions in millimeters are shown in parentheses.

PIN CONNECTIONS

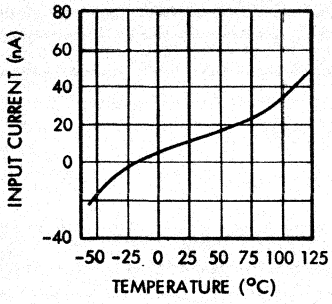
1) NULL	5) NULL
2) -IN	6) OUTPUT
3) +IN	7) V+
4) V-	8) N.C.

Pin 4 is connected to the case on the TO-99 package.
NC is no internal connection

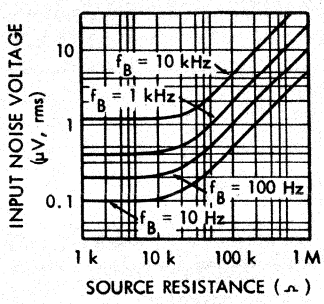
TYPICAL PERFORMANCE CURVES

(@ +25°C and ±15 Vdc unless otherwise specified)

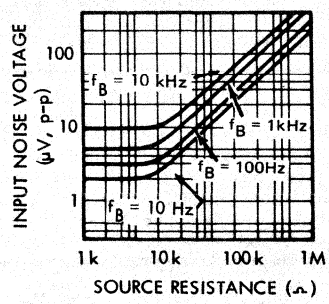
INPUT BIAS CURRENT vs. TEMPERATURE



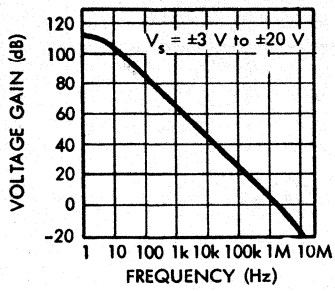
RMS INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



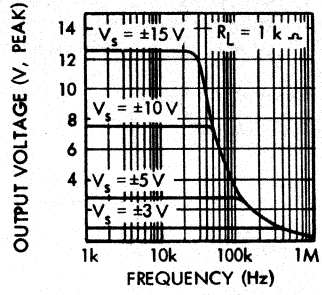
P-P INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



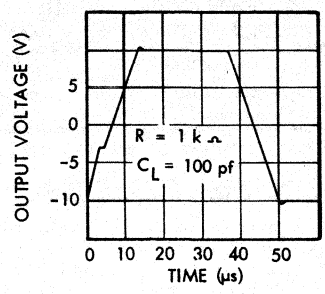
OPEN LOOP FREQUENCY RESPONSE



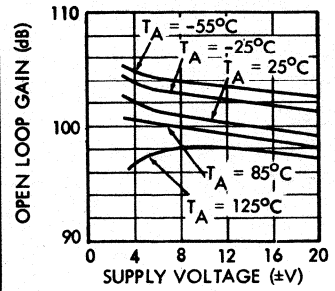
OUTPUT VOLTAGE vs. FREQUENCY



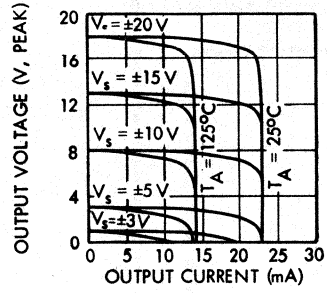
VOLTAGE FOLLOWER STEP RESPONSE



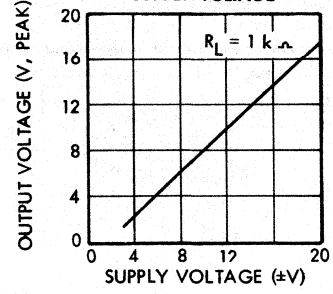
VOLTAGE GAIN vs. SUPPLY VOLTAGE



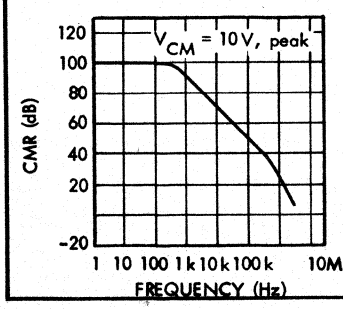
OUTPUT VOLTAGE vs. OUTPUT CURRENT



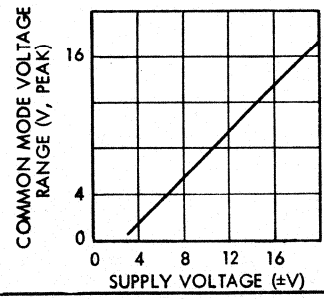
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



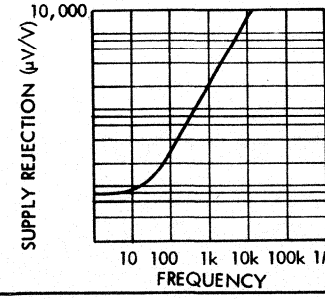
COMMON MODE REJECTION vs. FREQUENCY



COMMON MODE RANGE vs. SUPPLY VOLTAGE



POWER SUPPLY REJECTION vs. FREQUENCY



APPLICATIONS INFORMATION

OFFSET ADJUSTMENT

The input offset voltage of the Model 3500 may be adjusted to zero by connecting a 50 k Ω potentiometer between pins 1 and 5 with the wiper arm connected to negative supply (Figure 1a). This provides an adjustment range of approximately ±10 mV. This offset control is optional and may be omitted if the specified offset is considered sufficiently low.

Adjustment of the input offset voltage of the 3500 will affect the voltage drift to some extent. A rough "rule-of-thumb" is ±3 μV/°C change of drift for each 1.0 mV of offset adjustment. This is true of other IC op amps, such as the 741, 101, etc., but is usually masked by the greater drift of these units. However, in low drift amplifiers, such as the 3500C and 3500T, this effect must be considered. By use of a transistor as in Figure 1 the effect of offset adjustment on drift can be substantially reduced (by approximately a factor of six).

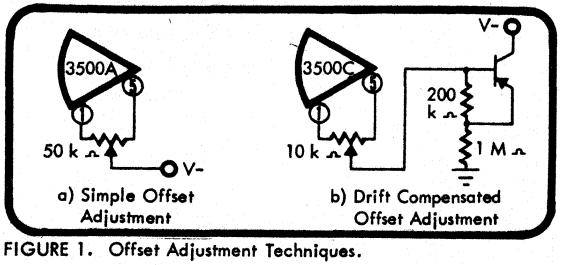


FIGURE 1. Offset Adjustment Techniques.

BIAS CURRENT EFFECTS

Input bias current of the amplifier creates additional offset voltages by flowing in the impedances of the signal source and the feedback network. Although the bias currents of the 3500 are quite small, their effects may be appreciable when these impedances are large. The bias currents at the two inputs tend to be equal and the difference current smaller than either. Thus equalizing the resistance from each input to common, as in Figure 2, is an effective means of reducing DC offset due to bias current.

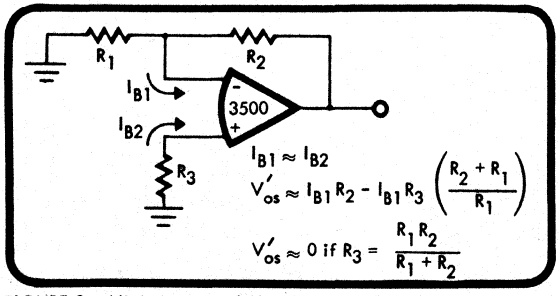


FIGURE 2. Minimization of Bias Current Effects.

OPERATION ON A SINGLE SUPPLY

Although virtually any op amp can be operated on a single supply if input and output voltage limitations are observed, the Model 3500 is particularly suitable for such use. It's wide supply range of ±3 to ±20 Vdc translates to a single supply operating range of 6 to 40 Vdc, plus or minus. Two possible modes of operation on a single supply are shown in Figure 3. The following conditions must be observed to keep the amplifier within its linear region of operation.

1) $+2 < e_o < (V_s - 2)$

2) $+3 < e_s < (V_s - 3)$, Figure 3b

When operating on a single supply ($+V_s$), shorting the output to common is equivalent to a short to supply and the internal power dissipation is approximately twice that which occurs for a short to common with balanced supplies of $\pm \frac{V_s}{2}$. This dissipation may exceed safe limits for single supply voltages greater than 20 volts and must be prevented by use of a series limiting resistor or other device, if short circuit protection is desired.

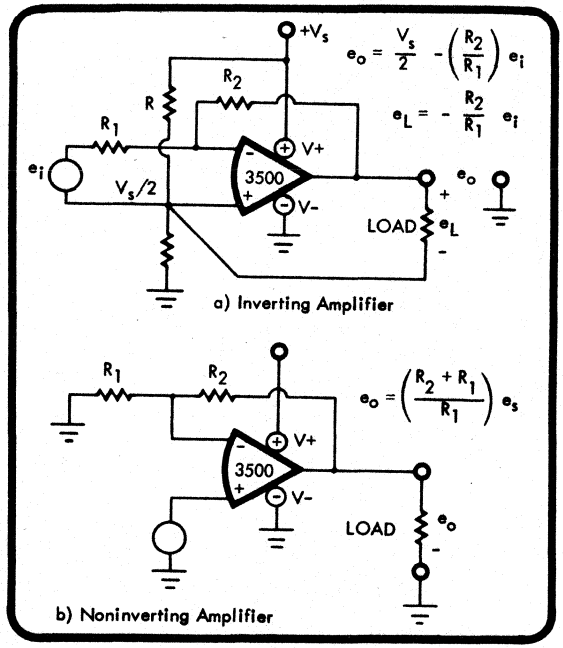
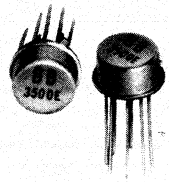


FIGURE 3. Operation on a Single Supply.

BURR-BROWN

3500E



Ultra-Low Drift Low Bias Current OPERATIONAL AMPLIFIERS

FEATURES

- ULTRA-LOW DRIFT, ±1μV/°C, max
- LOW BIAS CURRENT, ±50nA, max
- LOW NOISE, 1.4μV, p-p
- WIDE SUPPLY RANGE, ±3VDC to ±20VDC
- INTERNAL COMPENSATION
- REPLACES 741 TYPE AMPLIFIERS

DESCRIPTION

The 3500E is the most general purpose low drift (1μV/°C max) IC op amp presently available. The 3500E is internally fully compensated for unity gain operation; yet the full-power bandwidth is 12kHz min with a slew rate of 0.8V/μsec min. The small signal gain bandwidth is 1.5MHz. Complementing the low drift (1μV/°C) of the 3500E is its excellent low input noise characteristic of 1.4μV/p-p.

The 3500E retains the same chip geometry and all the other basic characteristics of Burr-Brown's 3500 series of IC op amps. Tight process control and careful selection by Burr-Brown make the new lower drift 3500E possible.

The 3500 IC op amps are designed for low input current while maintaining slew rate and bandwidth adequate for most applications. The low input bias current is achieved by a unique bias current cancelling circuit. This method insures that the bias current remains low over the full temperature and common-mode voltage ranges. The same circuitry gives the amplifier high input impedance, both differential and common-mode.

The amplifier maintains internal current levels essentially constant over the full range of power supply voltages. Thus the offset voltage and drift remain low for all combinations of supply voltage.

All units of the 3500 series are 100% tested to all min/max specifications - including voltage and current drift versus temperature. The 3500 is also the lowest noise IC op amp yet produced, as illustrated by the curves included herein. Both current and voltage noise are low, including the low frequency "flicker" and "popcorn" noise which usually prevent the use of IC op amps for low-level signal processing.

The 3500 is internally compensated and requires no external components for stability. The slew rate is independent of supply voltage level. The input stage of the 3500 series exhibits no latch-up when the common-mode voltage range is exceeded. The input impedance remains high with differential inputs as high as ±30V. Thus the amplifier can be used as a sensitive comparator. The output stage is internally current limited to provide protection against continuous short circuits. The 3500 is interchangeable with 741 type amplifiers but gives greatly improved performance.

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PDS-274C

Printed in U.S.A. July, 1978

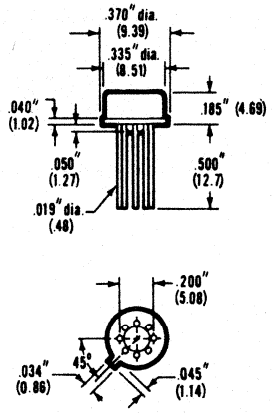
SPECIFICATIONS

Specifications (Typical at 25°C and ±15 Vdc power supply unless otherwise noted.)

MODEL 3500E	3500E
OPEN LOOP GAIN	100 dB
RATED OUTPUT	
Voltage	±10 V, min.
Current	±10 mA, min.
Output Impedance	1KΩ
FREQUENCY RESPONSE	
Unity Gain, Small Signal	1.5 MHz
Full Power Sine Wave	12 kHz, min.
Slew Rate	0.8 V/μsec, min.
INPUT OFFSET VOLTAGE	
Initial Offset @ 25°C	±500 μV, max.
Avg. vs. Temp (-25°C to +85°C), max	±1.0 μV/°C
vs. Supply Voltage	±40 μV/V
vs. Time	±5 μV/ month
INPUT BIAS CURRENT	
@ 25°C (either input)	±50 nA, max.
Avg. vs. Temp (-25°C to +85°C), max	±0.5 nA/°C
vs. Supply Voltage	±0.2 nA/V
INPUT DIFFERENCE CURRENT	
@ 25°C	±30 nA, max.
Avg. vs. Temp (-25°C to +85°C), max	±0.3 nA/°C
vs. Supply Voltage	±0.1 nA/V
INPUT IMPEDANCE	
Differential	10^7 Ω ‖ 3 pf
Common Mode	5×10^9 Ω ‖ 3 pf
INPUT NOISE	
Voltage, .01 Hz to 10 Hz, p-p	2.0 μV
10 Hz to 10 kHz, rms	1.4 μV
Current, .01 Hz to 10 Hz, p-p	200 pA
10 Hz to 10 kHz, rms	35 pA
INPUT VOLTAGE RANGE	
Common Mode Voltage	±11 V, min.
Common Mode Rejection @ ±10 V	100 dB
Max. safe input voltage*	± supply
POWER SUPPLY	
Voltage, rated specification	±15 V
Operating Range	±3 to ±20 V
Current, quiescent	±3.5 mA, max
TEMPERATURE RANGE, ambient	
Operating, Rated Specs	-25 to +85°C
Storage	-55 to +125°C

*If signal voltage is applied to the input in the absence of power supply voltage, series resistance should be used to limit input current to 20 mA.

TO-99 PACKAGE

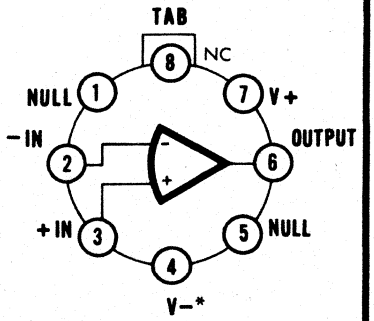


BOTTOM VIEW

Note: Dimensions in millimeters are shown in parentheses.

CONNECTION DIAGRAM

TOP VIEW

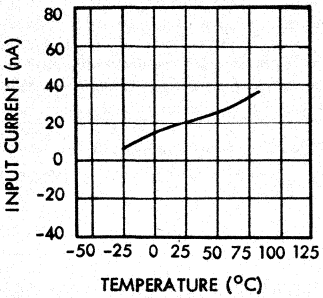


*Pin 4 is connected to case
NC is no internal connection

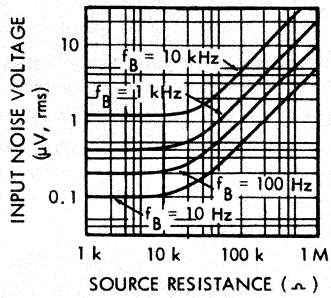
TYPICAL PERFORMANCE CURVES

(@ +25°C and ±15 Vdc unless otherwise specified)

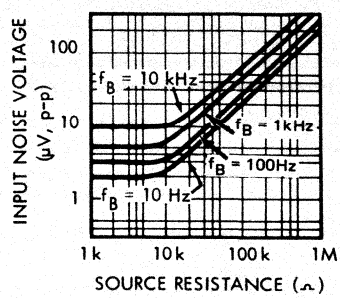
INPUT BIAS CURRENT vs. TEMPERATURE



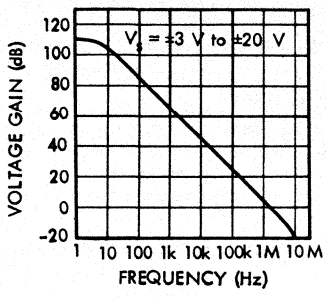
RMS INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



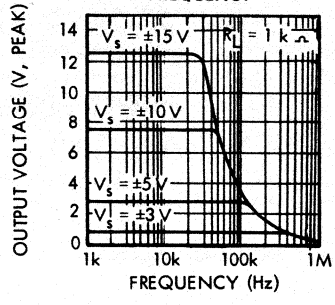
P-P INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



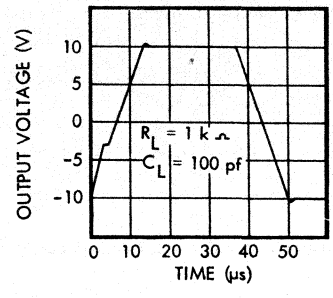
OPEN LOOP FREQUENCY RESPONSE



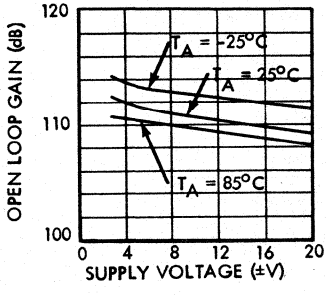
OUTPUT VOLTAGE vs. FREQUENCY



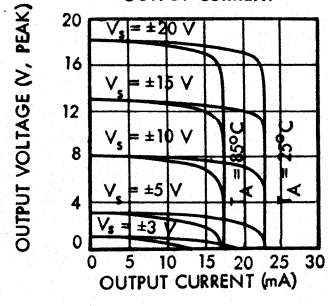
VOLTAGE FOLLOWER STEP RESPONSE



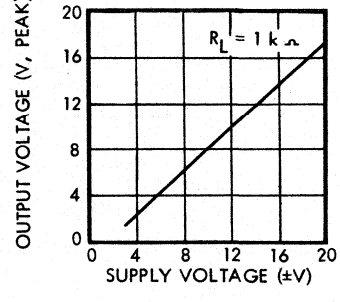
VOLTAGE GAIN vs. SUPPLY VOLTAGE



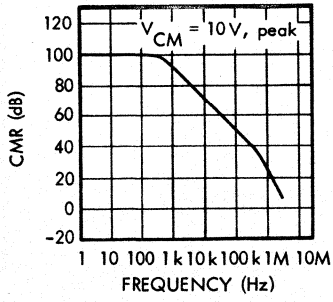
OUTPUT VOLTAGE vs. OUTPUT CURRENT



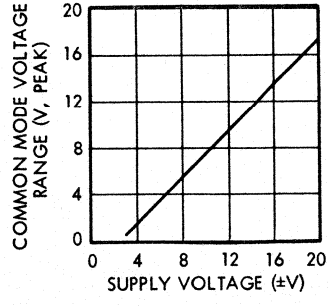
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



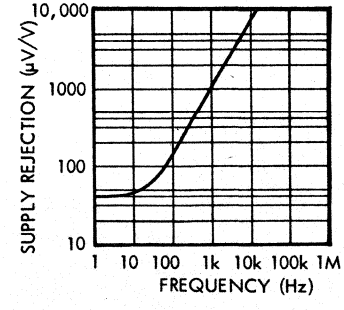
COMMON MODE REJECTION vs. FREQUENCY



COMMON MODE RANGE vs. SUPPLY VOLTAGE



POWER SUPPLY REJECTION vs. FREQUENCY



APPLICATIONS INFORMATION

BIAS CURRENT EFFECTS

Although the input bias currents of the 3500E are quite small for an IC op amp, the currents can generate significant equivalent offset voltages if the input resistors are large. Normally $I_{B1} \approx I_{B2} >> I_{B1} - I_{B2}$ (see Figure 1) and the effects of bias currents flowing in the input resistors may be minimized by making the source resistors equal ($R_s = R_1R_2 / R_1 + R_2$). However, in general the input offset current $I_{os} = I_{B1} - I_{B2}$ is not zero and has a temperature drift component. Hence, the bias currents still generate some offset voltage if the source resistance is non zero. Since I_{os} is random and unpredictable from unit to unit, the best advice is to keep the source resistances small. However, the 3500E does have max limits for I_{os} and I_{os} drift. The effect of R_s on V_{os} and V_{os} drift are shown in Figures 2 and 3. Generally speaking, source resistance up to 10 k Ω will not cause a problem in most applications.

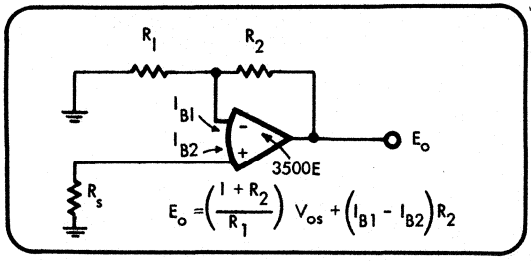


FIGURE 1. Bias Current Effects

WARM-UP DRIFT

Warm-up time is a significant parameter in a low drift op amp such as the 3500E. A low drift specification would be of little value if the unit took several hours to stabilize after turn on. Figure 4 shows that the input offset voltage of the 3500E has fully stabilized after only 2 minutes in free air. The warm-up drift is caused by the IC chip temperature being 10 to 15°C above ambient air due to quiescent internal power dissipation. The thermal time constant of the "chip" to free air is thus seen to be about 40 seconds. Note that the warm-up drift as shown in Figure 4 is monotonic. There is no "ringing" or other anomalies.

THERMAL SHOCK

Some low drift op amps exhibit peculiar behavior when subjected to thermal shock. Figure 5 shows that the thermal shock does not cause any unusual transient in the 3500E. The input offset voltage shifts by an amount representing the typical drift of 0.75 μV/°C. From this curve we may conclude that the thermal time constant of the chip to the case is about 6 seconds.

POWER SUPPLY DRIFT

In a very low drift amplifier like the 3500E, power supply instability can adversely affect drift. A 15 V power supply drift of .2%/°C will typically cause about 1 μV/°C offset voltage drift. Thus, the temperature coefficient of the power supplies should ideally be less than 0.02%/°C.

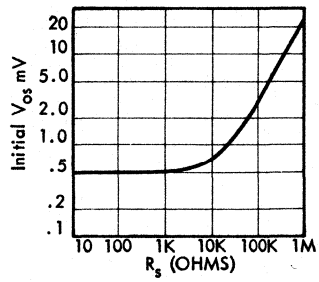


FIGURE 2. Equivalent Input Offset Voltage vs R_s.

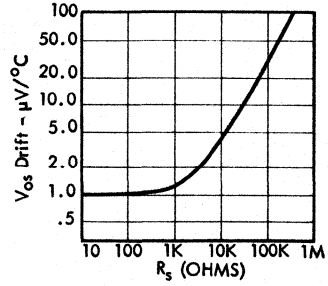


FIGURE 3. Equivalent Input Offset drift vs R_s.

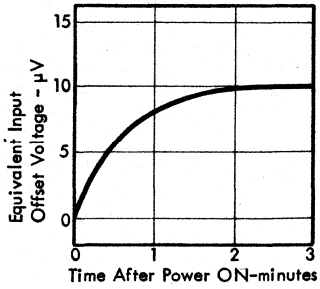


FIGURE 4. Warm-up Drift

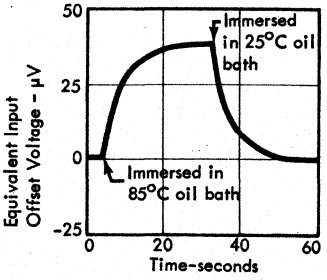


FIGURE 5. Effect of Thermal Shock on Offset Voltage

OFFSET VOLTAGE ADJUSTMENT

SINGLE POTENTIOMETER ADJUST

The 3500E has a low initial offset (500 μV) compatible with its low drift. However, some high accuracy applications may require external nulling of even this small initial offset voltage. Virtually any offset voltage adjustment method can increase offset voltage drift unless some care is used. For example, the initial offset voltage of most monolithic op amps (BB 3500, 741 types, 101, etc.) may be nulled using a single potentiometer, but offset voltage drift is typically increased by about 3 μV/°C for each mV of offset voltage adjust. The following circuits provide a collection of offset zeroing techniques suitable for use with the 3500E. Design tradeoffs are given where appropriate.

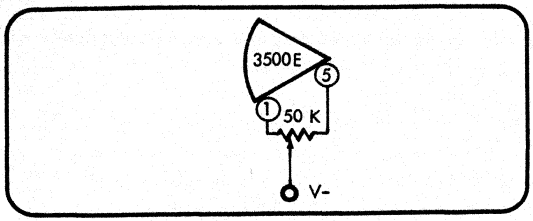


FIGURE 6. Single Potentiometer Adjust at Op Amp Trim Terminals.

Advantages of circuit in Figure 6

1. Simplest circuit
2. Compatible with most IC op amps

Disadvantages

1. Drift increased by circuit (Total drift for 3500E ≈ 3 μV/°C max)

EXTERNAL BIAS VOLTAGE OFFSET ADJUST

The circuit in Figure 7a has an equivalent circuit shown in Figure 7b. This equivalent bias voltage source may be connected in the op amp input circuitry and V_b adjusted (by adjusting R_a) to null the effect of the amplifier input offset voltage. Typical circuits using this offset zero technique are shown in Figures 8, 9, and 10.

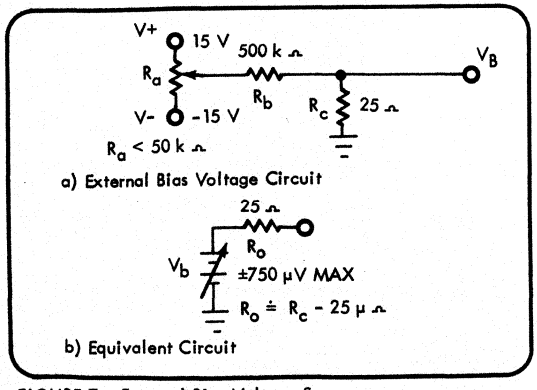


FIGURE 7. External Bias Voltage Source.

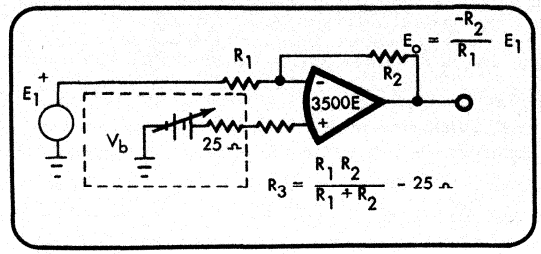


FIGURE 8. Inverting Amplifier Offset Voltage Adjust.

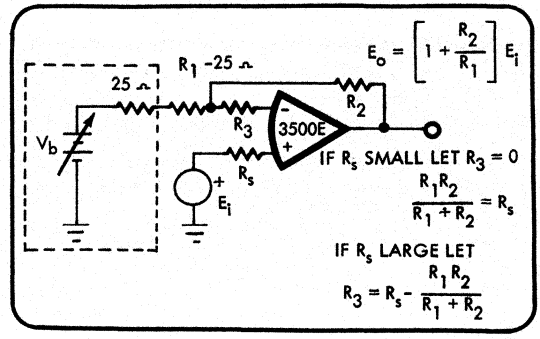


FIGURE 9. Non-Inverting Amplifier Offset Voltage Adjust.

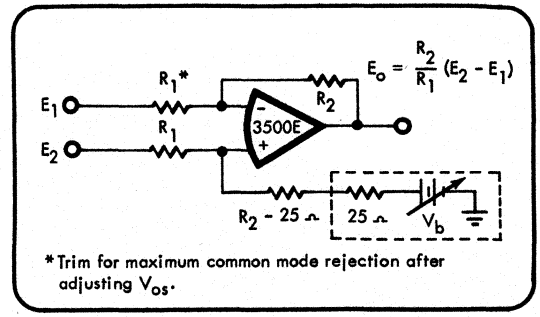


FIGURE 10. Differential Amplifier Offset Voltage Adjust.

Advantages of external bias voltage offset adjust

1. Simple circuit - only two fixed resistors more than simple single pot circuit.
2. Offset voltage drift is not affected if low drift resistors are used for R_b and R_c (Figure 7a). If metal film resistors (T.C. = 100 ppm/°C) are used for R_b and R_c, resistor drift will add at most 0.1 μV/°C to the offset voltage drift.
3. This offset null technique is compatible with any op amp provided R_b (Figure 7a) is chosen to provide sufficient adjustment range.

Disadvantages

1. This type offset adjust is not suitable for unity gain noninverting (buffer) circuits.

TEMPERATURE COMPENSATED POTENTIOMETER OFFSET VOLTAGE ADJUST

If the circuit in Figure 6 is replaced with a circuit which "drifts" with temperature, nulling the offset voltage will not increase the drift by so large an amount. The circuit shown in Figure 11 may be used to null initial offset voltage and drift will increase only about 0.5 μV/°C for each mV of offset adjust. In the case of the 3500E, this zeroing circuit will add at most 0.25 μV/°C of drift for a total offset voltage drift of 1.25 μV/°C.

Advantages

1. The op amp can be used in any configuration including unity gain noninverting.

Disadvantages

1. Circuit is more complex than other zeroing techniques.
2. Nulling offset voltage still increases drift by a small amount.

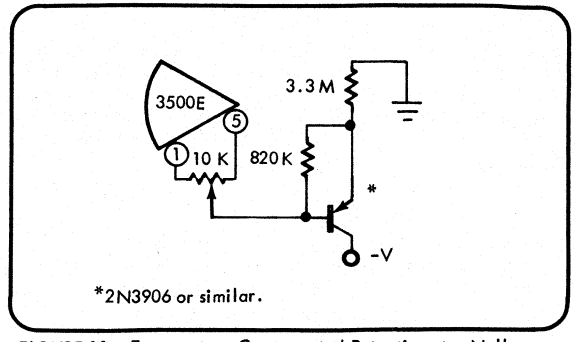
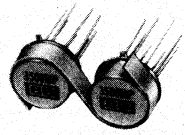


FIGURE 11. Temperature Compensated Potentiometer Null.

BURR-BROWN

3500MP



Matched Low Bias Current IC OPERATIONAL AMPLIFIERS

FEATURES

TWO MONOLITHIC OP AMPS WITH ...

- MATCHED OFFSET VOLTAGES - △ Vos = 200μV max
- MATCHED DRIFT, △Vos vs Temp. = 1μV/°C max
- LOW NOISE, 1.4μV p-p
- LOW BIAS CURRENT, 50nA max
- INTERNAL COMPENSATION
- WIDE POWER SUPPLY RANGE

APPLICATIONS

- INSTRUMENTATION AMPLIFIERS
- MULTISTAGE ACTIVE FILTERS WITH LOW OUTPUT OFFSET
- LOW DRIFT SINGLE-ENDED AMPLIFIERS WITH LOW NOISE
- DUAL CHANNEL AMPLIFIERS WITH MATCHED DRIFT

DESCRIPTION

Close process control and careful grading by Burr-Brown make possible a new dimension in IC op amps - drift matched pairs. Drifts as low as 1μV/°C may be obtained using the 3500MP op amps. The 3500MP IC's are selected from Burr-Brown's 3500 series of op amps, thus all the features of the 3500 series are automatically found in the 3500MP. This enables the 3500MP to provide very-low drift (1μV/°C) with very-low noise (1.4μV p-p) without sacrificing speed. (Slew rate 0.8V/μsec min.)

The 3500 IC op amps are designed for low input current while maintaining slew rate and bandwidth adequate for most applications. The low input bias current is achieved by a unique bias current cancelling circuit. This method insures that the bias current remains low over the full temperature and common-mode voltage ranges. The same circuitry gives the amplifier high input impedance, both differential and common-mode.

All units of the 3500E series are 100% temperature tested for voltage and current drift. The 3500 is also one of the lowest noise IC op amps yet produced, as illustrated by the curves on page 1-35. Both current and voltage noise are low, including the low frequency "flicker" and "popcorn" noise which usually prevent the use of IC op amps for low-level signal processing.

The 3500 is internally compensated for unconditional stability for all feedback configurations, even with capacitive loads. The slew rate is independent of supply voltage level. The input stage of the 3500 series exhibits no latch-up when the common-mode voltage range is exceeded. The input impedance remains high with differential inputs as high as ±30V. The output stage is internally current limited to provide protection against continuous short circuits. The 3500 is interchangeable with 741 type amplifiers but gives greatly improved performance.

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PDS-264E

Printed in U.S.A. July, 1978

SPECIFICATIONS

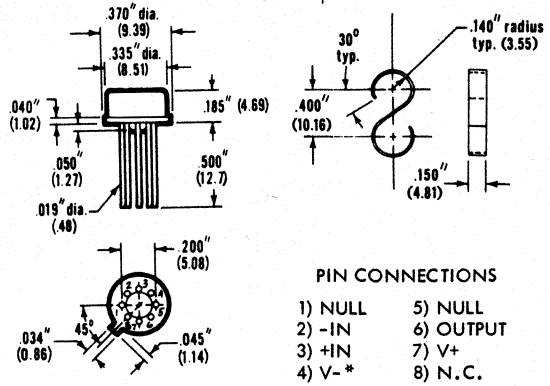
Specifications typical at 25°C and ±15 Vdc power supply unless otherwise noted.
(Two matched operational amplifiers Burr-Brown 3500 type)

MODEL	3500MP (Both Units)
OPEN LOOP GAIN	100 dB
RATED OUTPUT	
Voltage	±10 V, min.
Current	±10 mA, min.
Output Impedance	1 kΩ
FREQUENCY RESPONSE	
Unity Gain, Small Signal	1.5 MHz
Full Power Sine Wave	12 kHz, min.
Slew Rate	0.8 V/μsec, min.
INPUT OFFSET VOLTAGE V_{os1}, V_{os2}	
Initial Offset @ 25°C	±2 mV, max.
Avg. vs. Temp. (-25 to +85°C) max.	±5 μV/°C
vs. Supply Voltage	±40 μV/V
vs. Time	±5 μV/mo
DIFFERENTIAL INPUT OFFSET VOLTAGE $\Delta V_{os} = \lvert V_{os1} - V_{os2} \rvert$	
Initial Offset @ 25°C	±200 μV, max.
Avg. vs. Temp. (-25 to +85°C) max.	±1.0 μV/°C
INPUT BIAS CURRENT	
@ 25°C (either input)	±50 nA, max.
Avg. vs. Temp. (-25°C to +85°C) max.	±0.5 nA/°C
vs. Supply Voltage	±0.2 nA/V
INPUT DIFFERENCE CURRENT	
@ 25°C	±25 nA
Avg. vs. Temp. (-25°C to +85°C)	±0.25 nA/°C
vs. Supply Voltage	±0.1 nA/V
INPUT IMPEDANCE	
Differential	10^7 Ω || 3 pF
Common Mode	5×10^9 Ω || 3 pF
INPUT NOISE	
Voltage, 0.01 Hz to 10 Hz, p-p	2.0 μV
10 Hz to 10 kHz, rms	1.4 μV
Current, 0.01 Hz to 10 Hz, p-p	200 pA
10 Hz to 10 kHz, rms	35 pA
INPUT VOLTAGE RANGE	
Common Mode Voltage	±11 V, min.
Common Mode Rejection @ ±10 V	100 dB
Maximum Safe Input Voltage *	± supply
POWER SUPPLY	
Voltage, Rated Specification	±15 V
Operating Range	±3 to ±20 V
Current, Quiescent	±3.5 mA, max
TEMPERATURE RANGE	
Operating Ambient	-25 to +85°C
Storage	-65 to +125°C

* If signal voltage is applied to the input in the absence of power supply voltage, series resistance should be used to limit input current to 20 mA.

TO-99 PACKAGE

Dimensions in millimeters are shown in parentheses.



PIN CONNECTIONS

1) NULL	5) NULL
2) -IN	6) OUTPUT
3) +IN	7) V+
4) V- *	8) N.C.

*Pin 4 is connected to case. NC is no internal connection

OFFSET ADJUSTMENT

The input offset voltage of the Model 3500 may be adjusted to zero by connecting a 50 kΩ potentiometer between pins 1 and 5 with the wiper arm connected to negative supply (Figure 1a). This provides an adjustment range of approximately ±10 mV. This offset control is optional and may be omitted if the specified offset is considered sufficiently low.

Adjustment of the input offset voltage of the Model 3500 will affect the voltage drift to some extent. A rough "rule-of-thumb" is ±3 μV/°C change of drift for each 1.0 mV of offset adjustment. This is true of other IC op amps, such as the 741, 101, etc., but is usually masked by the greater drift of these units. However, in low drift amplifiers this effect must be considered. By use of a transistor as in Figure 1b the effect of offset adjustment on drift can be substantially reduced (by approximately a factor of six).

Whenever possible adjust V_{os1} to equal V_{os2} (zero differential offset). Do not adjust $V_{os1} = 0 = V_{os2}$ unless absolutely necessary. If both V_{os1} and V_{os2} are adjusted to zero, the drift compensated adjustment technique (Figure 1b) must be used or the ΔV_{os} drift of 1 μV/°C will be adversely affected.

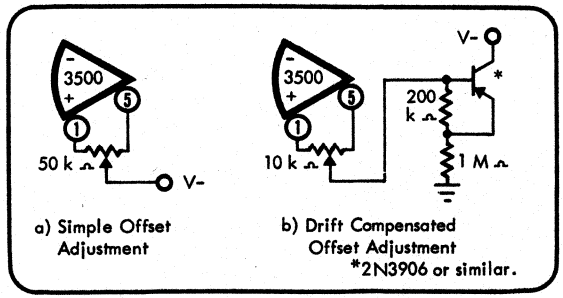
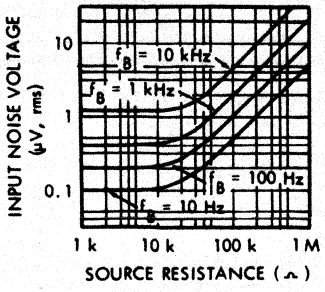


FIGURE 1. Offset Adjustment Techniques.

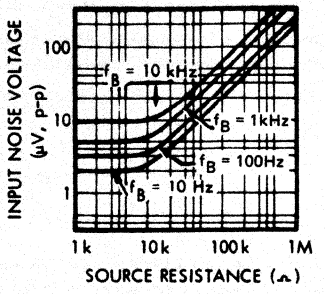
TYPICAL PERFORMANCE CURVES

(@ +25°C and ±15 Vdc unless otherwise specified)

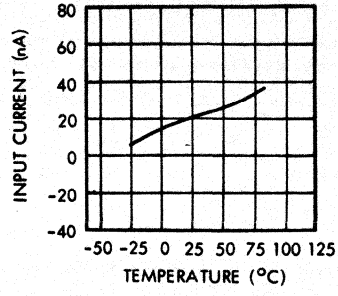
RMS INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



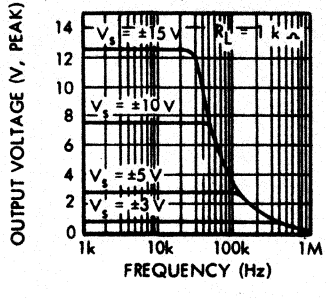
P-P INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



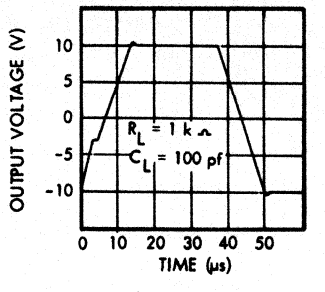
INPUT BIAS CURRENT vs. TEMPERATURE



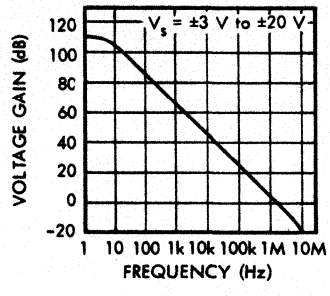
OUTPUT VOLTAGE vs. FREQUENCY



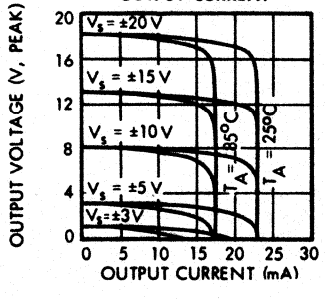
VOLTAGE FOLLOWER STEP RESPONSE



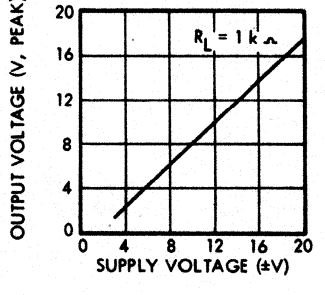
OPEN LOOP FREQUENCY RESPONSE



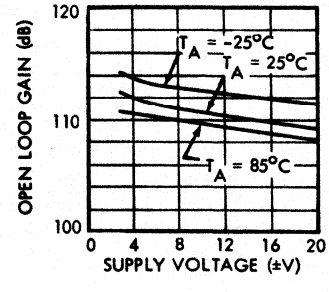
OUTPUT VOLTAGE vs. OUTPUT CURRENT



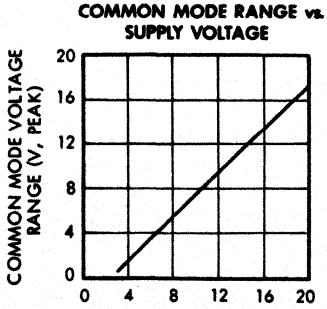
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



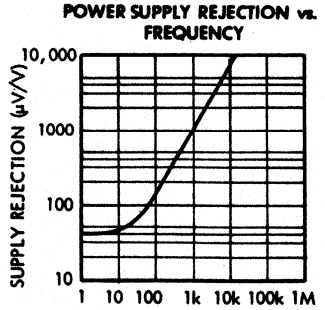
VOLTAGE GAIN vs. SUPPLY VOLTAGE



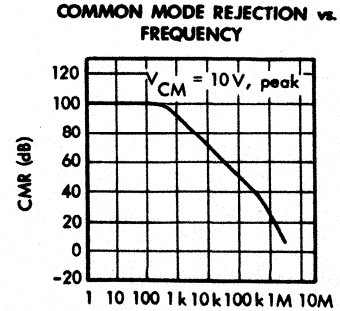
COMMON MODE RANGE vs. SUPPLY VOLTAGE



POWER SUPPLY REJECTION vs. FREQUENCY



COMMON MODE REJECTION vs. FREQUENCY



BIAS CURRENT EFFECTS

Input bias current of an amplifier can generate additional small offset voltages by flowing through the equivalent input source resistances. Although the bias currents for the 3500MP are quite small, the current-generated offset voltages may be significant for source resistances greater than 1 kΩ. When using the matched 3500MP amplifiers to obtain offset voltage drifts on the order of 1 μV/°C particular attention must be given to the input bias currents. Because of the great number of circuit configurations involving two operational amplifiers, it is only possible to give some general guidelines for minimizing bias current effects.

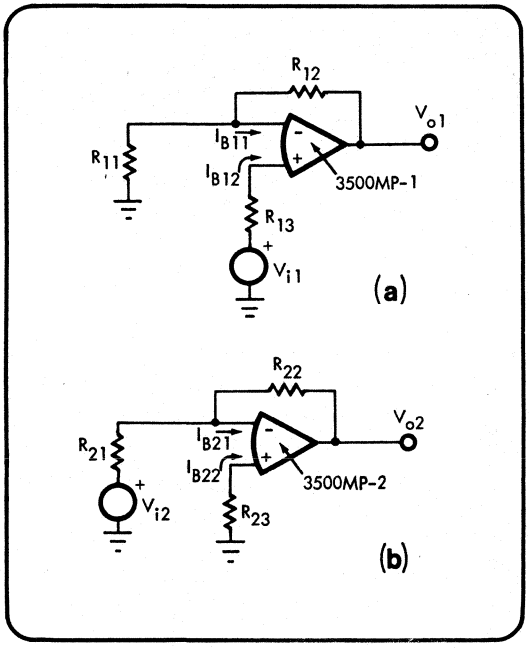


FIGURE 2. Bias Current Effects.

Bias currents generate offset voltages in two ways. If $I_{B11} = I_{B12}$ (see Figure 2a) no offset will be generated by I_{B11} and I_{B12}

$$\text{if } R_{13} = \frac{R_{11}R_{12}}{R_{11}+R_{12}}$$

However, in general, $I_{B11} = I_{B12} + I_{os1}$ where I_{os1} is the input offset current of op amp 1. I_{os} will vary from unit to unit and I_{os} is also subject to drift with time and temperature. Fortunately I_{os} is normally much less than I_{B11}. Therefore we may minimize effects of bias current by making the Thevenin equivalent input resistances equal (i.e. $R_{13} = \frac{R_{11}R_{12}}{R_{11}+R_{12}}$) and the effects of I_{os} may be minimized by making the equivalent source resistances small. Keep in mind that in some two amplifier circuits the "differential" bias current ($\Delta I_B = I_{B11} - I_{B12}$) will generate the predominate source of bias current errors.

Similarly for the circuit configuration of Figure 2b bias current effects are minimized by setting

$$R_{23} = \frac{R_{21}R_{22}}{R_{21}+R_{22}}$$

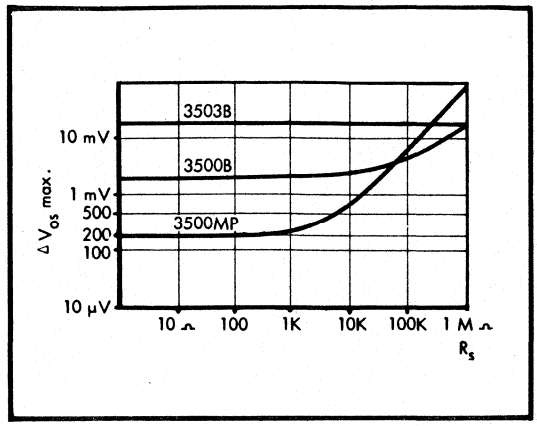


FIGURE 3. ΔV_{os} vs. Source Resistance.

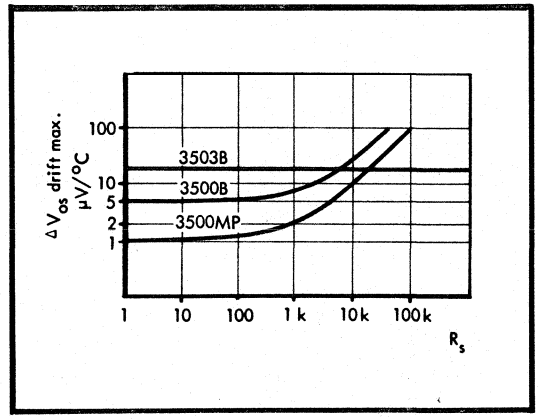


FIGURE 4. ΔV_{os} Drift vs. Source Resistance.

The effect of offset currents are summarized in Figures 3 and 4 which plot offset voltage (ΔV_{os}) between the two amplifiers and ΔV_{os} drift as a function of source resistance (R_s). Curves for a single 3500B type amplifier and an FET input 3503B) amplifier are included for comparison. Note that a 3500MP provides superior performance for low source resistance.

THERMAL CONSIDERATIONS

The very low ΔV_{os} drift specification for the 3500MP assumes both integrated circuits have the same "chip" temperature. A metal clip is furnished with the 3500MP to provide close thermal matching between the two device cases. However, care should be taken to see that each op amp drives approximately the same load or thermal offsets will result due to internal self heating. In any case thermal offsets are much less critical with the 3500MP than with matched transistors. A 1°C temperature offset will cause a voltage offset in a matched pair of transistors of about 2.5 mV but the ΔV_{os} of a 3500MP will be only 5 μV for 1°C temperature offset.

APPLICATIONS

COMPOSITE LOW DRIFT OP AMP

The two matched op amps in the 3500MP may be connected to simulate a single op amp with very low initial offset voltage and drift. The circuit shown in Figure 5a may be used in any conventional op amp circuit to obtain low drift. A typical feedback circuit with an inverting gain of 100 is shown in Figure 5c. Note the addition of R_3, R_4, and R_5 to minimize bias current effects on the offset voltage.

The composite op amp will be stable in circuits with voltage gains greater than about three. For lower voltage gains the compensation shown in Figure 5b may be used if required. For unity gain non-inverting operation, the compensation technique of Figure 5b will not decrease the composite amplifier bandwidth below the bandwidth of the individual op amps.

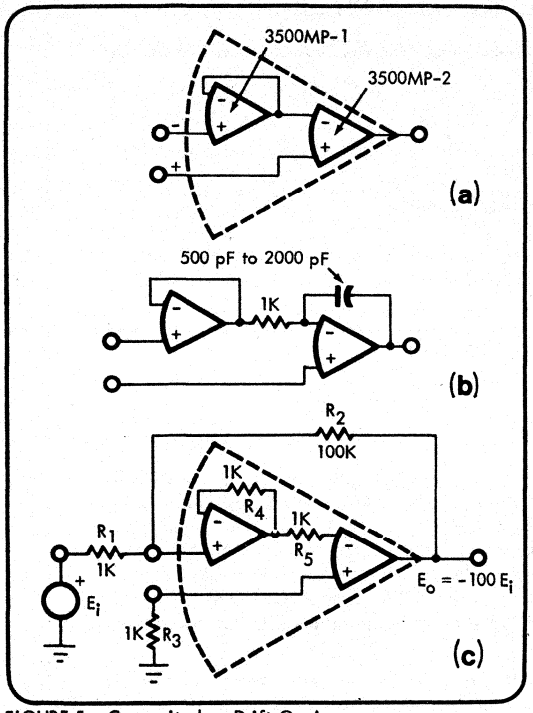


FIGURE 5. Composite low Drift Op Amp.

HIGH INPUT IMPEDANCE DIFFERENTIAL AMPLIFIER

The circuit in Figure 7 acts as a high input impedance differential amplifier provided $R_1 / R_2 = R_4 / R_3$. A mismatch of resistance ratios results in a common mode gain A_C as shown below. In addition to finite common mode gain, a resistance mismatch causes a differential gain error equal to A_C / A_D. Notice that the output offset error is proportional to ΔV_{os} which is made very small by the matching of the two op amps. (In most practical cases $A_D \Delta V_{os} >> A_C (V_{os1} + V_{os2}) / 2$.)

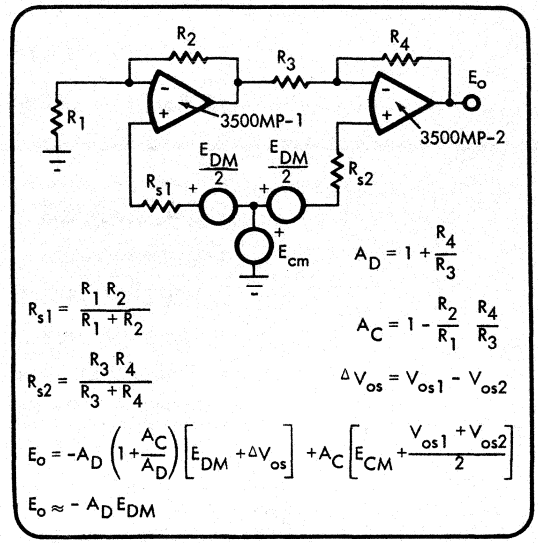


FIGURE 7. Differential Amplifier.

LOW PASS FILTER WITH LOW DC ERROR

Multistage low pass active filters often have large amounts of d.c. offset and drift because the offsets of the op amps used tend to add. The inverting synthesis technique shown in Figure 6 to realize each pole pair causes the amplifier offset voltages to cancel if they are matched. The net offset error without trimming will be less than 400 μV and the total drift of the filter is less than 2 μV/°C. The output d.c. error is made essentially independent of bias current effects by choosing small resistor values. However the small resistance values limit the maximum output voltage to about 1.0 V p-p and $R_L > 125\ \Omega$.

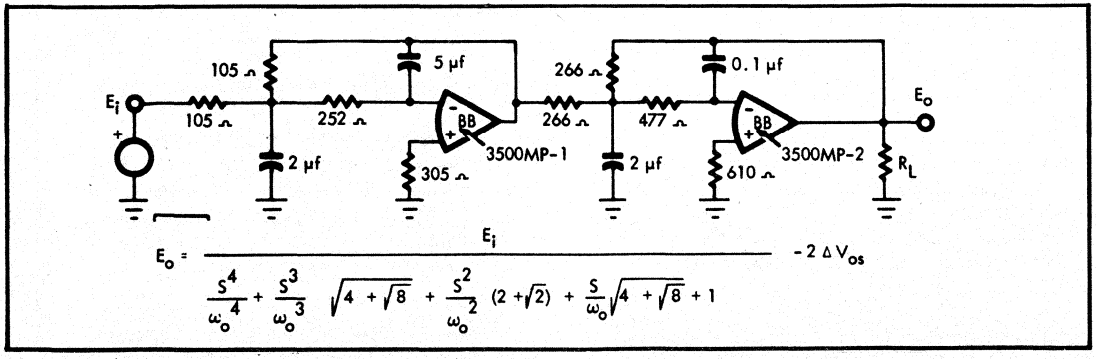
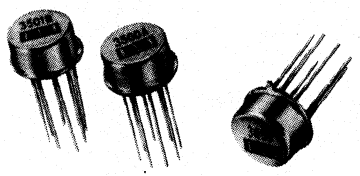


FIGURE 6. 4 Pole Low Pass Butterworth Filter; f_o = 1 kHz.

BURR-BROWN

3501



Low Bias Current OPERATIONAL AMPLIFIERS

FEATURES

- LOW BIAS CURRENT, ±3nA, max
- LOW DRIFT, ±5μV/°C, max ±30pA/°C, max
- LOW NOISE, 0.8μV, p-p 30pA, p-p
- WIDE SUPPLY RANGE, ±3VDC to ±20VDC
- INTERNAL COMPENSATION
- REPLACES 108 AND 741 TYPE AMPLIFIERS

DESCRIPTION

The 3501 series is designed to minimize input voltage drift and input bias current, without resorting to exotic processing. The low input bias current is achieved by a current cancellation technique developed by Burr-Brown's IC Engineering Group. The same input circuitry gives the 3501 very-high input impedance, both differential and common-mode. Internal current levels of the amplifier are maintained essentially constant over the full range of supply voltages by relying on basic semiconductor properties and device matching. The result is that major performance parameters - open-loop gain, bias current, voltage drift, slew rate and output current - are affected only slightly by wide variations of supply voltage. Quiescent power drain is quite low over the supply voltage range.

The 3501 is internally compensated for unconditional stability in all feedback configurations, even with capacitive loads. Thus it is interchangeable with both 741 and 108 type amplifiers (eliminating the external frequency compensation required of 108 type amplifiers).

Because of the unique input stage design of the 3501, its common-mode rejection is very-high (100dB). The result is excellent linearity (.01% or better) as a noninverting buffer. Also the input stage exhibits no latch-up when the common-mode voltage range is exceeded. The input impedance remains high for input voltages up to the value of the supply voltages.

The output stage is internally current limited to provide protection against continuous circuits.

All units of the 3501 series are 100% tested to all min/max specifications - including voltage and current drift versus temperature. Units are drift selected with maximum specifications at ±5μV/°C, ±10μV/°C and ±20μV/°C. Both military and industrial temperature range versions are offered.

The 3501 is also a very-low noise amplifier. Both current and voltage noise are low, including the low frequency "flicker" and "popcorn" noise which usually dictate against the use of utility op amps, such as the 741, for low-level signal processing.

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PDS-249E

Printed in U.S.A. July, 1978

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

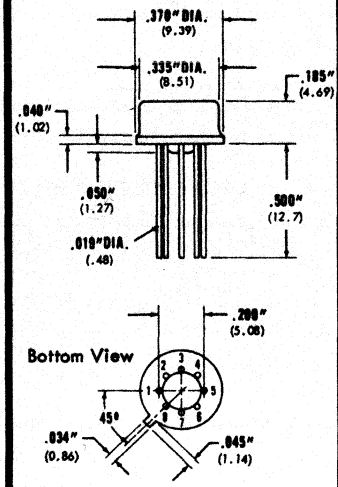
Typical at 25°C and ±15 Vdc unless otherwise noted.

MODEL	3501A 3501R	3501B 3501S	3501C
OPEN LOOP GAIN, dc, no load	93 dB, min	*	*
RATED OUTPUT		*	*
Voltage	±10V, min		
Current	±5 mA, min		
Capacitive Load Range	0 to 1000 pF		
Output Impedance	2 kΩ		
FREQUENCY RESPONSE		*	*
Unity Gain, Open Loop	0.5 MHz		
Full Power Sine Wave	1.6 kHz, min		
Slew Rate	0.1 V/μsec, min		
INPUT OFFSET VOLTAGE			
Initial Offset @ 25°C	±5 mV, max	±2 mV, max	±2 mV, max
Avg. vs. Temp. (-25° to +85°C) max	±20 μV/°C (A)	±10μV/°C (B)	±5 μV/°C (C)
(-55° to +125°C) max	±20 μV/°C (R)	±10 μV/°C (S)	
vs. Supply Voltage	±40 μV/V	*	*
vs. Time	±2 μV/day	*	*
INPUT BIAS CURRENT			
@ 25°C	±15 nA, max	±7 nA, max	±3 nA, max
Avg. vs. Temp. (-25° to +85°C) max	±0.2 nA/°C (A)	±0.15 nA/°C(B)	±0.1 nA/°C(C)
(-55° to +125°C) max	±0.2 nA/°C (R)	±0.15 nA/°C(S)	
vs. Supply Voltage	±30 pA/V	*	*
INPUT DIFFERENCE CURRENT			
@ 25°C	±5 nA	±3 nA	±2 nA
Avg. vs. Temp. (-25° to +85°C)	±0.1 nA/°C (A)	±0.05 nA/°C(B)	±0.03nA/°C(C)
(-55° to +125°C	±0.1 nA/°C (R)	±0.05 nA/°C(S)	
vs. Supply Voltage	±10 pA/V	*	*
INPUT IMPEDANCE		*	*
Differential	5×10^7 Ω ‖ 3 pF		
Common Mode	10^{10} Ω ‖ 3 pF		
INPUT NOISE		*	*
Voltage, .01 Hz to 10 Hz, p-p	2 μV		
10 Hz to 10 kHz, rms	1.4 μV		
Current, .01 Hz to 10 Hz, p-p	66 pA		
10 Hz to 10 kHz, rms	12 pA		
INPUT VOLTAGE RANGE		*	*
Common Mode Voltage	±11 V, min		
Common Mode Rejection @ ±10V	100 dB		
Max. Safe Input Voltage	±supply**		
POWER SUPPLY		*	*
Voltage, rated specification	±15 Vdc		
Operating Range	±3V to ±20V		
Absolute Max	±22 Vdc		
Current, quiescent	±1.5 mA, max.		
TEMPERATURE RANGE			
Operating, Rated Specs A, B, C	-25° to +85°C	*	*
R, S	-55° to +125°C	*	*
Storage	-65° to +150°C	*	*

* Specifications same for all models. ** If input voltage is applied in the absence of power supply voltage, series resistance should be added to limit current flow to ±20 mA.

TO-99 PACKAGE

Specify 3501A, etc.



Note: Dimensions in millimeters are shown in parentheses.

PIN CONNECTIONS

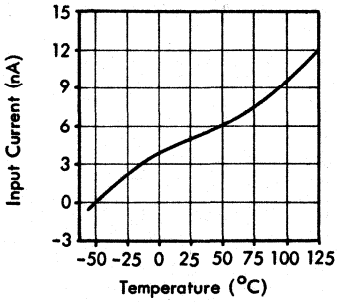
1) NULL	5) NULL
2) -IN	6) OUTPUT
3) +IN	7) V+
4) V-*	8) N.C.

*Pin 4 connected to case

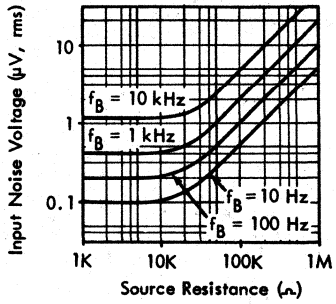
TYPICAL PERFORMANCE CURVES

(@ +25°C and ±15 Vdc unless otherwise specified)

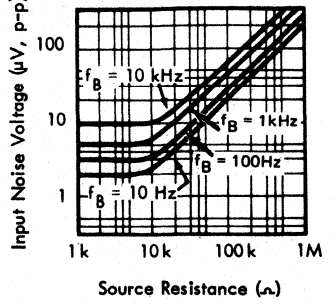
INPUT BIAS CURRENT vs. TEMPERATURE



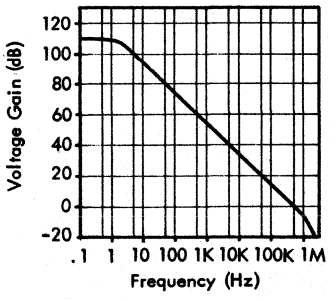
RMS INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



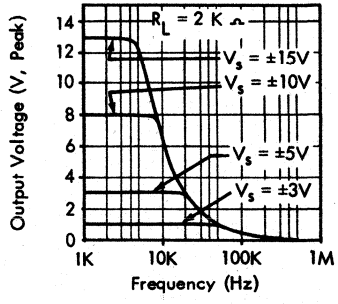
P-P INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



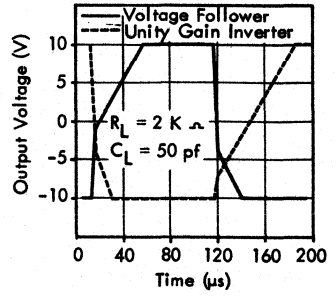
OPEN LOOP FREQUENCY RESPONSE



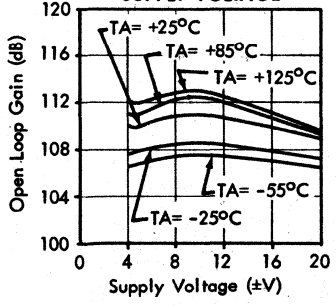
OUTPUT VOLTAGE vs. FREQUENCY



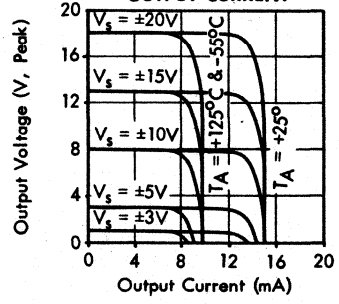
LARGE SIGNAL STEP RESPONSE



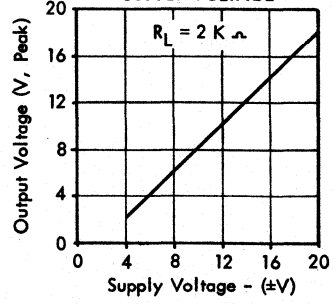
VOLTAGE GAIN vs. SUPPLY VOLTAGE



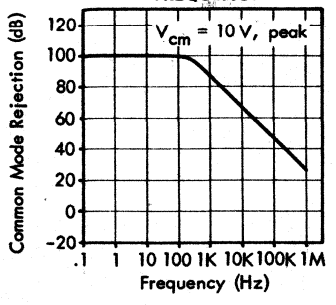
OUTPUT VOLTAGE vs. OUTPUT CURRENT



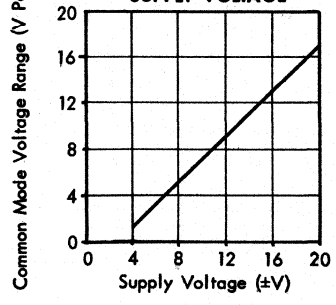
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



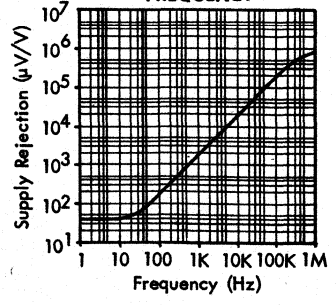
COMMON MODE REJECTION vs. FREQUENCY



COMMON MODE RANGE vs. SUPPLY VOLTAGE



POWER SUPPLY REJECTION vs. FREQUENCY



APPLICATIONS INFORMATION

OFFSET ADJUSTMENT

The input offset voltage of the Model 3501 may be adjusted to zero by connecting a 50 k Ω potentiometer between pins 1 and 5 with the wiper arm connected to negative supply (Figure 1a). This provides an adjustment range of approximately ±10 mV. This offset control is optional and may be omitted if the specified offset is considered sufficiently low.

Adjustment of the input offset voltage of the 3501 will affect the voltage drift to some extent. A rough "rule-of-thumb" is ±3 μV/°C change of drift for each 1.0 mV of offset adjustment. This is true of other IC op amps, such as the 741, 101, etc., but is usually masked by the greater drift of these units. However, in low drift amplifiers, such as the 3501C, this effect must be considered. By use of a transistor as in Figure 1 the effect of offset adjustment on drift can be substantially reduced (by approximately a factor of six).

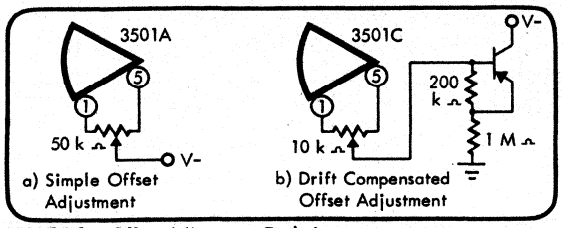


FIGURE 1. Offset Adjustment Techniques.

BIAS CURRENT EFFECTS

Input bias current of the amplifier creates additional offset voltages by flowing in the impedances of the signal source and the feedback network. Although the bias currents of the 3501 are quite small, their effects may be appreciable when these impedances are large. The bias currents at the two inputs tend to be equal and the difference current smaller than either. Thus equalizing the resistance from each input to common, as in Figure 2, is an effective means of reducing DC offset due to bias current.

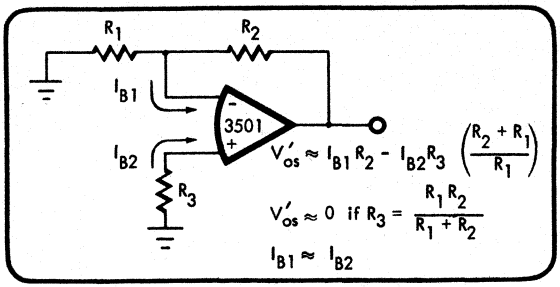


FIGURE 2. Minimization of Bias Current Effects.

OPERATION ON A SINGLE SUPPLY

Although virtually any op amp can be operated on a single supply if input and output voltage limitations are observed, the Model 3501 is particularly suitable for such use. It's wide supply range of ±3 to ±20 Vdc translates to a single supply operating range of 6 to 40 Vdc, plus or minus. Two possible modes of operation on a single supply are shown in Figure 3. The following conditions must be observed to keep the amplifier within its linear region of operation.

1) $+2 < e_o < (V_s - 2)$

2) $+3 < e_s < (V_s - 3)$, Figure 3b

When operating on a single supply (V_s), shorting the output to common is equivalent to a short to supply and the internal power dissipation is approximately twice that which occurs for a short to common with balanced supplies of $\pm \frac{V_s}{2}$. This dissipation may exceed safe limits for single supply voltages greater than 20 volts and must be prevented by use of a series limiting resistor or other device, if short circuit protection is desired.

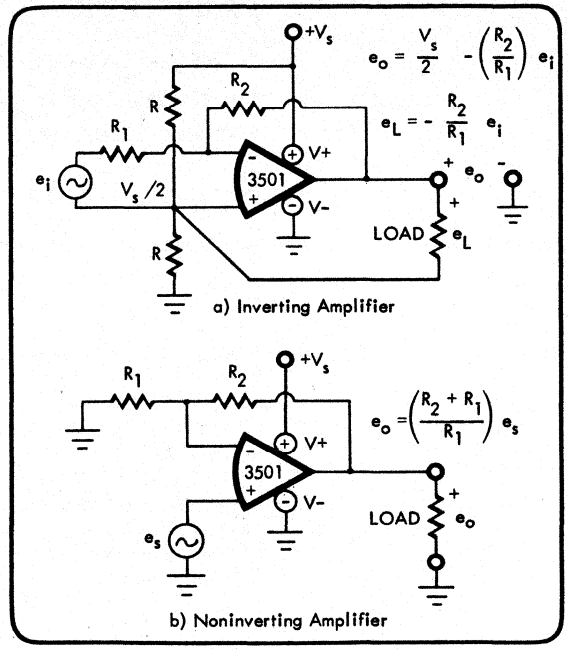
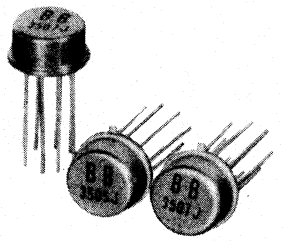


FIGURE 3. Operation on a Single Supply.

BURR-BROWN



3505J
3507J

Fast-Slewing OPERATIONAL AMPLIFIERS

FEATURES

- 120V/μsec SLEW RATE
- 20MHz GAIN-BANDWIDTH PRODUCT
- INTERCHANGEABLE WITH 741 TYPES

DESCRIPTION

Burr-Brown models 3505J and 3507J are intended for use in circuits requiring fast transient response - pulse amplifiers, D/A converters, comparators, fast followers, etc. Key parameters such as slew rate, settling time and bandwidth are orders of magnitude better than for most other IC op amps.

The DC and low frequency performance of the two models (3505J and 3507J) is identical. They differ substantially, however, in transient and AC performance. The 3505J, for instance, has a stable 6dB/octave gain rolloff at high frequency and is therefore stable at all gains, including unity, without external compensation. The 3507J on the other hand, is compensated to allow faster slewing and greater bandwidth for gains of 3 or more. For gains greater than 3, the gain rolloff of the 3507J is 6dB/octave. By use of a single external 20pF compensation capacitor the 3507J can be stabilized at unity gain, and will then have performance much like that of the 3505J. In addition, by use of an alternate compensation technique, it is possible to stabilize the 3507J at unity gain without sacrificing its faster slew rate.

Both models are pin-compatible with other standard IC op amps while offering greater speed and higher output current. Both also are input-and output-protected to prevent damage if the output is shorted to common, or the input is shorted to supply voltage.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-297A

Printed in U.S.A. July, 1978

SPECIFICATIONS

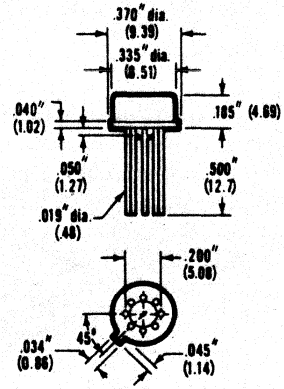
Specifications typical at ±15 Vdc and +25°C unless otherwise noted.

ELECTRICAL

MODELS	3505J		3507J	
	Typical	Guaranteed	Typical	Guaranteed
OPEN LOOP GAIN, dc				
No load	94 dB		90 dB	
2 kΩ load	88 dB	84 dB	83 dB	77 dB
RATED OUTPUT				
Voltage (1 kΩ load)	±12 V	±10 V	±12 V	±10 V
Current	±20 mA	±10 mA	±20 mA	±10 mA
DYNAMIC RESPONSE				
Small Signal Bandwidth (0 dB)	6 MHz		--	
Gain-Bandwidth Product (A_{CL}=10)	12 MHz		20 MHz	
Full Power Bandwidth	500 kHz	300 kHz	1.6 MHz	1.2 MHz
Slew Rate	30V/μsec	20V/μsec	120V/μsec	80V/μsec
Settling Time (0.1%)	300 nsec		200 nsec	
Rise Time (10-90%, small signal)	25 nsec	50 nsec	25 nsec	50 nsec
Overshoot	25%	50%	--	--
INPUT OFFSET VOLTAGE				
Initial (without adjust) @ +25°C	±4 mV	±8 mV	±5 mV	±10 mV
over temperature		±10 mV		±14 mV
(Avg. 0°C to +70°C)	±20μV/°C		±30μV/°C	
vs. supply voltage	±30μV/V	200 μV/V	±30μV/V	200 μV/V
vs. Time	±50μV/mo		±50μV/mo	
INPUT BIAS CURRENT				
Initial @ +25°C	+50 nA	+250 nA	+50 nA	+250 nA
over temperature		+500 nA		+500 nA
(Avg. 0°C to +70°C)	±0.5 nA/°C		±0.5 nA/°C	
INPUT DIFFERENCE CURRENT				
Inital @ +25°C	±20 nA	±50 nA	±20 nA	±50 nA
over temperature		±100 nA		±100 nA
(Avg. 0°C to +70°C)	±0.1 nA/°C		±0.1 nA/°C	
INPUT IMPEDANCE				
Differential	50MΩ‖3 pF	20 MΩ	100MΩ‖3 pF	40 MΩ
Common Mode	500MΩ‖5 pF		1000MΩ‖5 pF	
INPUT VOLTAGE RANGE				
Common Mode (linear operation)	±12 V	±10 V	±12 V	±10 V
Differential (between inputs)		±15 V		±15 V
Absolute Max. (either input)		± Supply		± Supply
Common Mode Rejection	90 dB	74 dB	90 dB	74 dB
POWER SUPPLY				
Rated Voltage		±15 Vdc		±15 Vdc
Voltage Range, derated	±8V to ±20V		±8V to ±20V	
Current, quiescent	±4 mA	±6 mA	±4 mA	±6 mA
TEMPERATURE RANGE				
Specifications		0° to +70°C		0° to +70°C
Operating		-25°C to +85°C		-25°C to +85°C
Storage		-65°C to +150°C		-65°C to +150°C

MECHANICAL

TO-99 PACKAGE

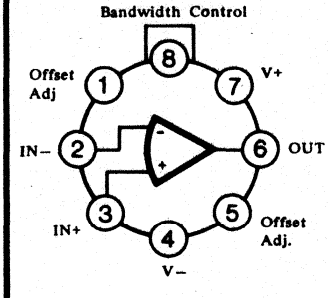


(BOTTOM VIEW)

Dimensions in millimeters are shown in parentheses.

Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).

CONNECTION DIAGRAM

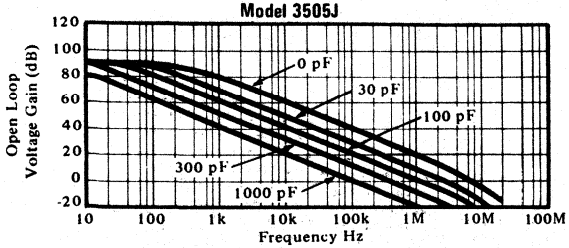


(TOP VIEW)

TYPICAL PERFORMANCE CURVES

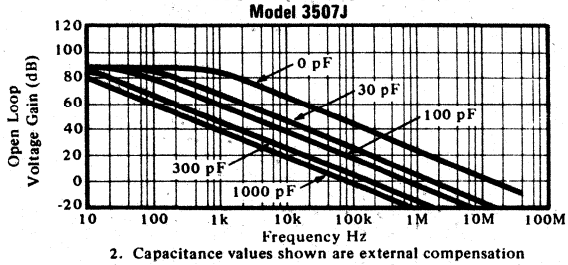
(@ +25°C and ±15 Vdc unless otherwise specified)

OPEN LOOP FREQUENCY RESPONSE[1]
Model 3505J



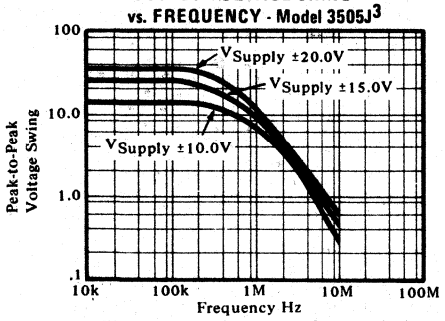
1. Capacitance values shown are external compensation from pin 8 to COMMON. Not required for stability on 3505J.

OPEN LOOP FREQUENCY RESPONSE[2]
Model 3507J



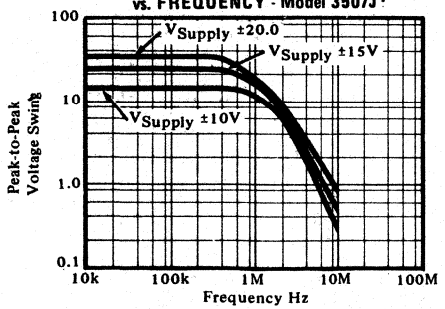
2. Capacitance values shown are external compensation from pin 8 to COMMON.

OUTPUT VOLTAGE SWING vs. FREQUENCY - Model 3505J[3]



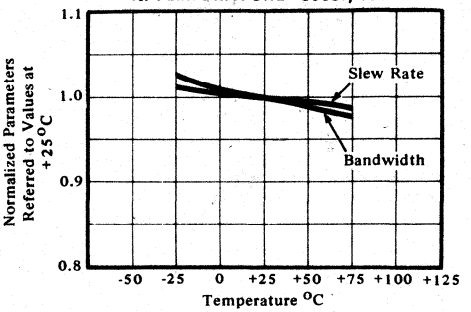
3. With no external compensation capacitance.

OUTPUT VOLTAGE SWING vs. FREQUENCY - Model 3507J[4]

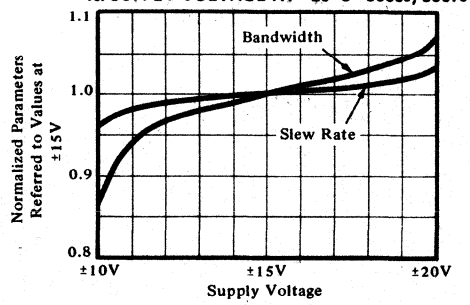


4. With no external compensation capacitance.

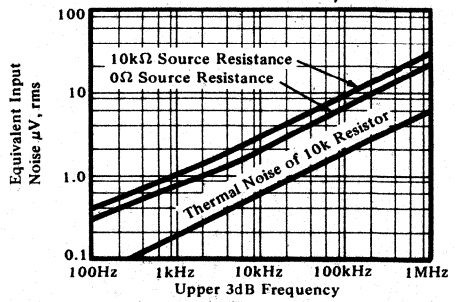
NORMALIZED AC PARAMETERS vs. TEMPERATURE - 3505J, 3507J



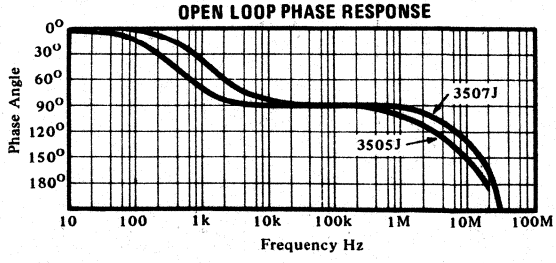
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE AT +25°C - 3505J, 3507J



EQUIVALENT INPUT NOISE vs. BANDWIDTH - 3505J, 3507J



OPEN LOOP PHASE RESPONSE



APPLICATIONS

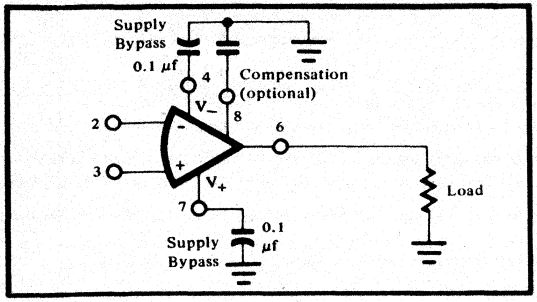


FIGURE 1. Compensated Amplifier with Supply and Load Bypassing.

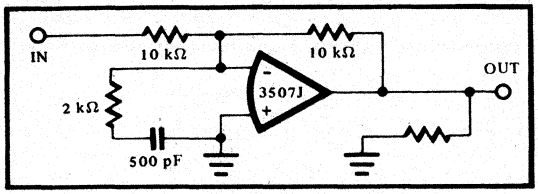


FIGURE 2. Alternate Method for Unity - Gain Compensation of 3507J.

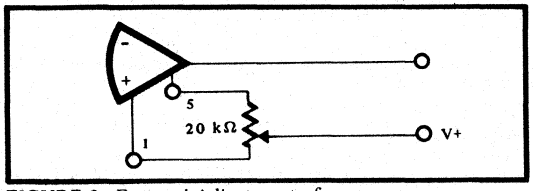


FIGURE 3. External Adjustment of Offset Voltage

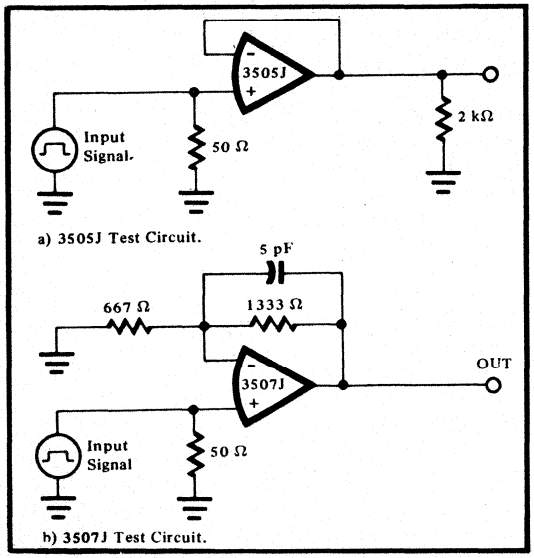


FIGURE 4. Dynamic Response Test Circuits.

BANDWIDTH COMPENSATION

The frequency response of both the 3505J and the 3507J can be adjusted by use of an external compensation capacitor from pin 8 to common, as shown in Figure 1. The open loop frequency response curves of page 3 illustrate the effect of various values of capacitance. The 3505J is stable at any gain level without the use of compensation, provided that stray wiring capacitance and/or load capacitance are not excessive, and that moderate values of feedback resistance are used ($R_{FB} \leq$ 10 k Ω). A load capacitance of ≈ 50 pF is desirable in all feedback configurations. The 3507J is stable for gains of 3 or greater without external compensation (subject to the same limits on stray and load capacitance and resistance levels). A 20 pF compensation capacitor will stabilize the 3507J for all values of gain, at the sacrifice of bandwidth and slew rate.

The circuit of Figure 2 illustrates another approach to compensation of the 3507J. This method yields unity gain stability without sacrificing slew rate.

STABILITY

Because the 3505J and 3507J are extremely fast amplifiers with high gain, stray wiring capacitance and inductance in power supply leads can cause circuit oscillation. This can be prevented by proper circuit layout (all leads or patterns as short as possible) and by properly by-passing the power supply lines to common at points close to the amplifier. In addition, it is recommended that the load be bypassed by a 50 pF capacitor see Figure 1.

OFFSET VOLTAGE ADJUSTMENT

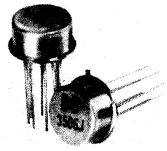
Although the offset voltage of these amplifiers is only a few millivolts, it may be desirable in some cases to null this offset. This is done by use of a 20 k Ω potentiometer as shown in Figure 3.

TEST CIRCUIT – DYNAMIC RESPONSE

The test circuits of Figure 4 are used for measurement of slew rate, settling time, rise time and overshoot. Both rise time and overshoot are measured under small signal conditions (V_{OUT} = ±200 mV). Slew rate and settling time are measured for a 10 V p-p square wave.

BURR-BROWN

3506J
3508J



Wideband OPERATIONAL AMPLIFIERS

FEATURES

- 100MHz GAIN BANDWIDTH PRODUCT
- 5nA INPUT BIAS CURRENT
- 103dB OPEN-LOOP GAIN
- INTERCHANGEABLE WITH 741 TYPES

DESCRIPTION

Burr-Brown models 3506J and 3508J are wideband operational amplifiers intended for use in circuits requiring extended bandwidth and high gain. Typical examples of applications are: RF signal amplifiers, fast recovery voltage references, high speed integrators, high frequency active filters, and photodiode amplifiers.

Model 3506J is internally compensated for stability at all gains, including the unity gain voltage follower configuration. It's bandwidth can be decreased, if desired, by addition of an external capacitor.

Model 3508J is internally compensated for stability at gains greater than five and thus has a higher gain-bandwidth product and faster slew rate than the 3506J. Like the 3506J, the 3508J can be externally compensated by use of a single capacitor, and can thus be stabilized at any value of gain. By use of an alternate compensation scheme the 3508J can be stabilized at unity gain without sacrificing slew rate.

In addition to its wide bandwidth and high gain the amplifier has a number of other significant advantages over other IC op amps: low bias current, high output current, and high common-mode rejection. Inputs are protected against voltages up to the value of the power supplies. The output is current-limited to provide short-circuit protection.

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PDS-298A Printed in U.S.A. July, 1978

SPECIFICATIONS

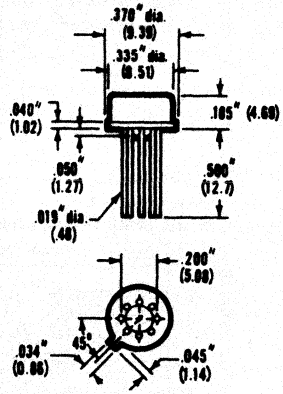
Specifications typical at ±15 Vdc and +25°C unless otherwise noted.

ELECTRICAL

MODELS	3506J		3508J	
	Typical	Guaranteed	Typical	Guaranteed
OPEN LOOP GAIN, dc				
No Load	106 dB		106 dB	
2 KΩ Load	103 dB	98 dB	103 dB	98 dB
RATED OUTPUT				
Voltage	±12 V	±10 V	±12 V	±10 V
Current	±18 mA	±10 mA	±18 mA	±10 mA
DYNAMIC RESPONSE				
Small Signal Bandwidth (0 dB)	12 MHz			
Gain-Bandwidth Product (A_{CL}=100)			100 MHz	
Full Power Bandwidth	75 kHz	50 kHz	600 kHz	320 kHz
Slew Rate	7 V/μsec	4 V/μsec	35 V/μsec	20 V/μsec
Settling Time (0.1%)	1.5 μsec		—	—
Rise Time (10-90%, small signal)	30 nsec	60 nsec	17 nsec	45 nsec
Overshoot	25%	40%	—	—
INPUT OFFSET VOLTAGE				
Initial (without adj.) @ +25°C	±3 mV	±5 mV	±3 mV	±5 mV
over temperature		±7 mV		±7 mV
(Avg. 0°C to +70°C)	±20 μV/°C		±30 μV/°C	
vs. supply voltage	±30 μV/V	±200 μV/V	±30 μV/V	±200 μV/V
vs. time	±50 μV/mo		±50 μV/mo	
INPUT BIAS CURRENT				
Initial @ +25°C	±15 nA	±25 nA	±15 nA	±25 nA
over temperature		±40 nA		±40 nA
(Avg. 0°C to +70°C)	±0.5 nA/°C		±0.5 nA/°C	
INPUT DIFFERENCE CURRENT				
Initial @ +25°C	±5 nA	±25 nA	±5 nA	±25 nA
over temperature		±40 nA		±40 nA
(Avg. 0°C to +70°C)	±0.2 nA/°C		±0.2 nA/°C	
INPUT IMPEDANCE				
Differential	300MΩ‖3 pF	40 MΩ	300MΩ‖3 pF	40 MΩ
Common Mode	1000MΩ‖3 pF		1000MΩ‖3 pF	
INPUT VOLTAGE RANGE				
Common Mode (linear operation)	±13 V	±11 V	±13 V	±11 V
Differential Mode (between inputs)		±12 V		±12 V
Abs. Max. (either input)		± Supply		± Supply
Common Mode Rejection	100 dB	74 dB	100 dB	74 dB
POWER SUPPLY				
Rated Voltage		±15 Vdc		±15 Vdc
Voltage Range, derated	±8V to ±22V		±8V to ±22V	
Current, quiescent	±3 mA	±4 mA	±3 mA	±4 mA
TEMPERATURE RANGE				
Specification		0° to +70°C		0° to +70°C
Operating		−25°C to +85°C		-25°C to +85°C
Storage		−65°C to +150°C		−65°C to +150°C

MECHANICAL

TO-99 PACKAGE

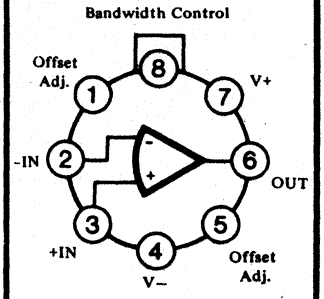


(BOTTOM VIEW)

Dimensions in millimeters are shown in parentheses.

Pin material and plating composition conform to method 208 (solderability) of Mil-Std-202.

CONNECTION DIAGRAM

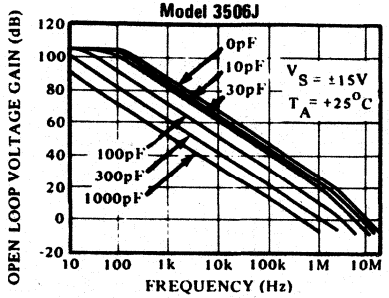


(TOP VIEW)

TYPICAL PERFORMANCE CURVES

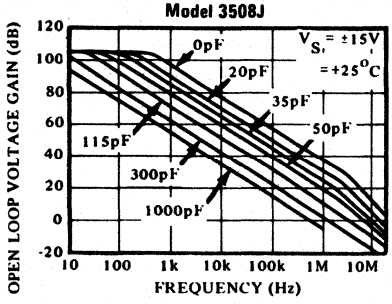
(@ +25°C and ±15 Vdc unless otherwise specified)

OPEN LOOP FREQUENCY RESPONSE*
Model 3506J



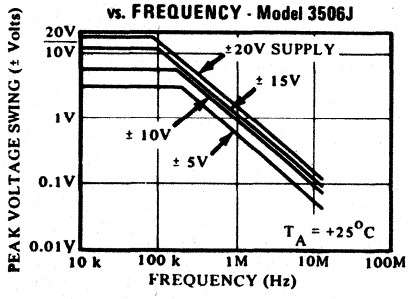
*Capacitance values shown are compensation from pin 8 to common. Not required for stability

OPEN LOOP FREQUENCY RESPONSE**
Model 3508J

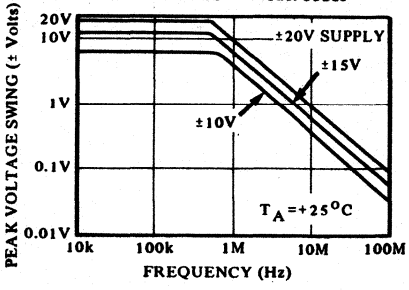


**Capacitance values shown are bandwidth compensation from pin 8 to common.

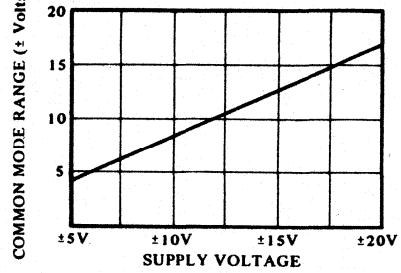
OUTPUT VOLTAGE SWING
vs. FREQUENCY - Model 3506J



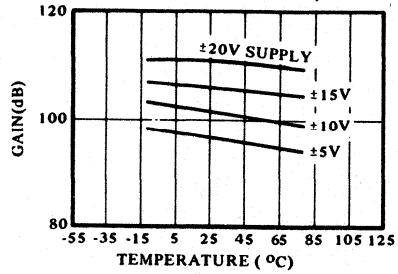
OUTPUT VOLTAGE SWING
vs. FREQUENCY - Model 3508J



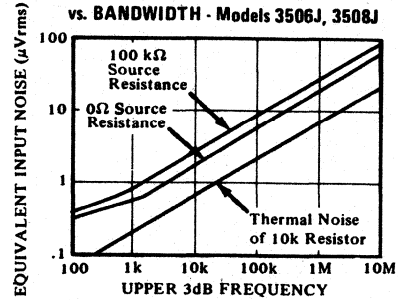
COMMON MODE VOLTAGE RANGE
vs. SUPPLY VOLTAGE - Models 3506J, 3508J



OPEN LOOP VOLTAGE GAIN
vs. TEMPERATURE - Models 3506J, 3508J

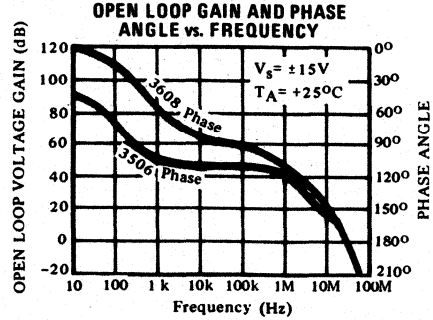


EQUIVALENT INPUT NOISE
vs. BANDWIDTH - Models 3506J, 3508J



(LOWER 3dB FREQUENCY -10Hz)

OPEN LOOP GAIN AND PHASE ANGLE vs. FREQUENCY



APPLICATIONS

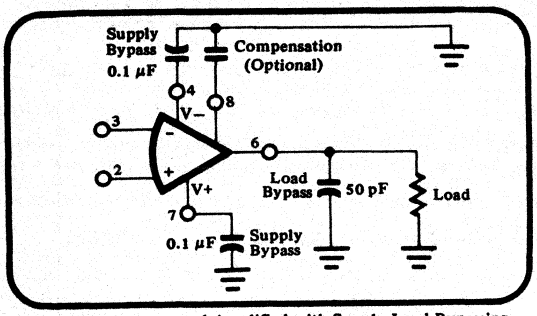


FIGURE 1. Compensated Amplified with Supply Load Bypassing.

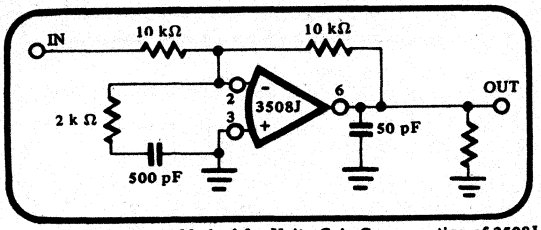


FIGURE 2. Alternate Method for Unity Gain Compensation of 3508J.

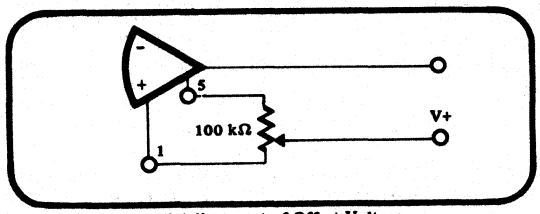


FIGURE 3. External Adjustment of Offset Voltage

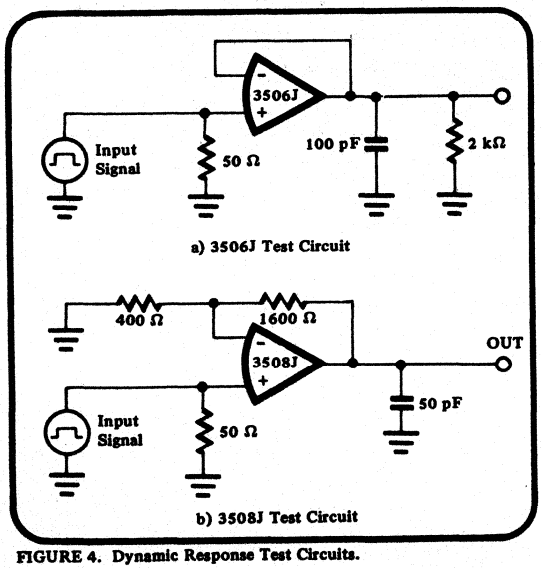


FIGURE 4. Dynamic Response Test Circuits.

BANDWIDTH COMPENSATION

The frequency response of both the 3506J and the 3508J can be adjusted by use of an external compensation capacitor from pin 8 to common as shown in Figure 1. The open loop frequency response curves of page 1-48 illustrate the effect of various values of capacitance. The 3506J is stable at any gain level without the use of compensation, provided that stray wiring capacitance and/or load capacitance are not excessive, and that moderate values of feedback resistance are used ($R_{FB} \leq$ 10 k Ω). A load capacitance of ≈ 50 pF is desirable in all feedback configurations. The 3508J is stable for gains of 5 or greater without external compensation (subject to the same limits on stray and load capacitance and resistance levels). A 20 pF compensation capacitor will stabilize the 3508J for all values of gain, at the sacrifice of bandwidth and slew rate.

The circuit of Figure 2 illustrates another approach to compensation of the 3508J. This method yields unity gain stability without sacrificing slew rate.

STABILITY

Because the 3506J and 3508J are extremely fast amplifiers with high gain, stray wiring capacitance and inductance in power supply leads can cause circuit oscillation. This can be prevented by proper circuit layout (all leads or patterns as short as possible) and by properly by-passing the power supply lines to common at points close to the amplifier. In addition, it is recommended that the load be bypassed by a 50 pF capacitor see Figure 1.

OFFSET VOLTAGE ADJUSTMENT

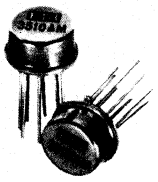
Although the offset voltage of these amplifiers is only a few millivolts, it may in some cases be desirable to null this offset. This is done by use of a 100 k Ω potentiometer as shown in Figure 3.

TEST CIRCUITS – DYNAMIC RESPONSE

The test circuits of Figure 4 are used for measurement of slew rate, settling time, rise time and overshoot. Both rise time and overshoot are measured for a small output signal (V_{OUT} = ±100 mV). Slew rate and settling time are measured for a 10 V p-p square wave.

BURR-BROWN

3510



Very Low Drift - Precision OPERATIONAL AMPLIFIER

FEATURES

- VERY-LOW DRIFT - ±0.5µV/°C max
- VERY-LOW OFFSET - ±60µV max
- LOW BIAS CURRENT - ±15nA max
- HIGH OPEN LOOP GAIN - 120dB min
- HIGH CMR - 110dB min
- VERY-LOW THERMAL FEEDBACK - ±0.1µV/V

DESCRIPTION

High overall accuracy is offered by Burr-Brown's 3510 Operational Amplifier. It's designed expressly for use in high gain analog circuits where very low drift and high accuracy are essential requirements.

This precision, instrumentation grade op amp provides an economical method to maintain high circuit accuracy and reliability over temperature ranges from -25°C to +85°C, surpassing competitive units rated for only 0°C to +70°C.

Additional performance features of the 3510 include high open loop gain, extremely low initial offset voltage, high CMR, very low thermal feedback, low input bias current and very low voltage drift vs temperature.

Burr-Brown's rigid control of monolithic processing and its rigid quality control standards result in very low voltage and current noise in the 3510. It's specifically designed for use in low level analog signal processing. Performance specifications are met exactly by precision trimming at the wafer level with complete testing before shipment. Performance of the 3510 significantly exceeds that of Burr-Brown's popular 3500 op amp.

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PDS-374A

Printed in U.S.A. July, 1978

ELECTRICAL SPECIFICATIONS

Specifications at T_A = 25°C and ±15VDC, unless otherwise noted. Standard specifications after warm-up.

MODELS	3510AM			3510BM/3510SM			3510CM			UNITS
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN, DC										
2kΩ Load	120			*			*			dB
RATED OUTPUT										
Voltage	±10			*			*			V
Current	±10			*			*			mA
Output Resistance		300			*			*		Ω
Load Capacitance		1000			*			*		pF
FREQUENCY RESPONSE										
Unity Gain, Open Loop, Small Signal C_c = 4700pF		0.4			*			*		MHz
Closed Loop Gain, C_c = 0, Stable Operation		≥10			*			*		V/V
Full Power Response, C_c = 0, A_{CL} = 10	7	12		*	*		*	*		kHz
Slew Rate, C_c = 0, A_{CL} = 10	0.5	0.8		*	*		*	*		V/μs
INPUT OFFSET VOLTAGE										
Initial Offset, 25°C			150			120			60	μV
vs Temp[1] - unnulled V_{os}			2.0			1.0			0.5	μV/°C
vs Temp[1] - nulled V_{os}			2.5			1.4			0.7	μV/°C
vs Time		0.2			*			*		μV/mo
Power Supply Rejection	110	130		*	*		*	*		dB
Thermal Feedback, R_L = 2kΩ, f = 1Hz		±0.1			*			*		μV/V
INPUT BIAS CURRENT										
Initial Bias, 25°C			±35			±25			±15	nA
vs Temp[1]			±0.6			±0.4			±0.25	nA/°C
vs Supply Voltage		±0.1			*			*		nA/V
INPUT DIFFERENCE CURRENT										
Initial Difference, 25°C			±20			±15			±10	nA
vs Temp[1]			±0.4			±0.25			±0.15	nA/°C
vs Supply Voltage		±10			*			*		pA/V
INPUT IMPEDANCE										
Differential		1 ‖ 3			*			*		MΩ ‖ pF
Common-mode		10 ‖ 3			*			*		GΩ ‖ pF
INPUT NOISE										
Voltage, 0.1Hz to 10Hz		0.8			*			*		μV, p-p
f_o = 10 Hz		14			*			*		nV/√Hz
f_o = 100 Hz		12			*			*		nV/√Hz
f_o = 1 kHz		12			*			*		nV/√Hz
Current, 0.1 Hz to 10 Hz		50			*			*		pA, p-p
f_o = 10 Hz		0.8			*			*		pA/√Hz
f_o = 100 Hz		0.46			*			*		pA/√Hz
f_o = 1 kHz		0.35			*			*		pA/√Hz
INPUT VOLTAGE RANGE										
Common-mode Voltage Range, linear operation		±(|V_{cc}|-3)		*			*			V
Common-mode Rejection at ±10V	110			*			*			dB
Maximum Safe Input Voltage		±V_{cc}			*			*		V
POWER SUPPLY										
Rated Voltage		±15			*			*		V
Voltage Range, derated performance	±3		±20	*		*	*		*	V
Quiescent Current		±2.5	±3.5		*	*		*	*	mA
TEMPERATURE RANGE										
Specification, (A, B, C)	-25		+85	*		*	*		*	°C
, (S)				-55		+125				°C
Operating, derated performance	-55		+125	*		*	*		*	
Storage	-65		+150	*		*	*		*	°C
θ junction-case		40			*			*		°C/W
θ junction-ambient		150			*			*		°C/W

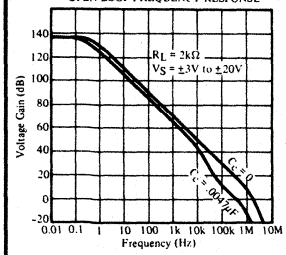
*Specification limits same as 3510AM.

(1) Temperature coefficient specifications: -25°C to +85°C for AM, BM, CM
-55°C to +125°C for SM

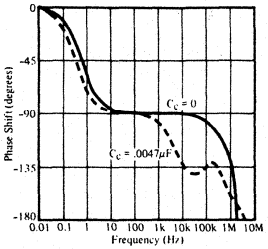
TYPICAL PERFORMANCE CURVES

Typical at T_A = 25°C and ±15VDC, unless otherwise noted.

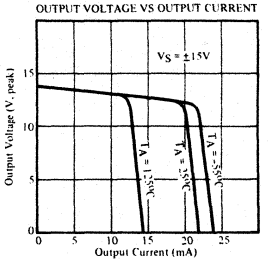
OPEN LOOP FREQUENCY RESPONSE



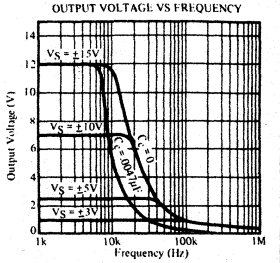
OPEN LOOP PHASE RESPONSE



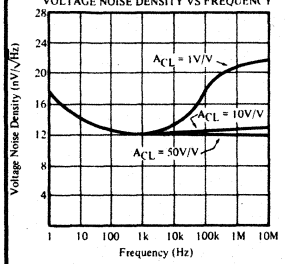
OUTPUT VOLTAGE VS OUTPUT CURRENT



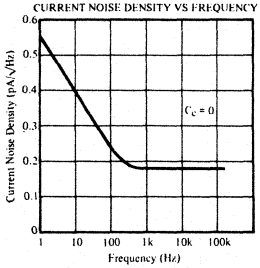
OUTPUT VOLTAGE VS FREQUENCY



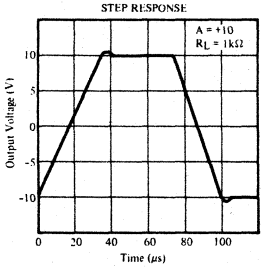
VOLTAGE NOISE DENSITY VS FREQUENCY



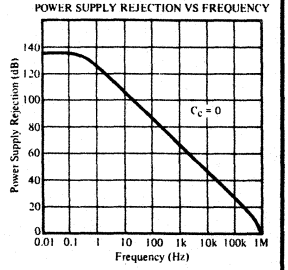
CURRENT NOISE DENSITY VS FREQUENCY



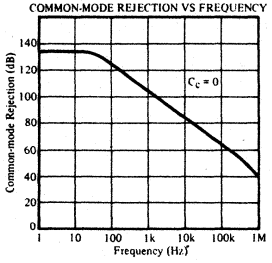
STEP RESPONSE



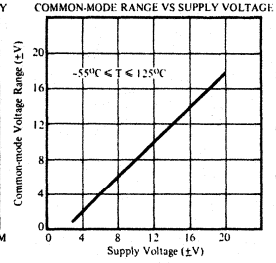
POWER SUPPLY REJECTION VS FREQUENCY



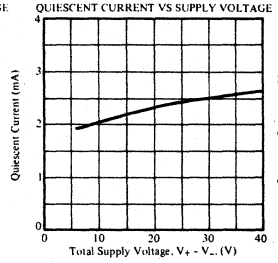
COMMON-MODE REJECTION VS FREQUENCY



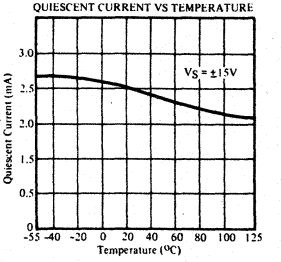
COMMON-MODE RANGE VS SUPPLY VOLTAGE



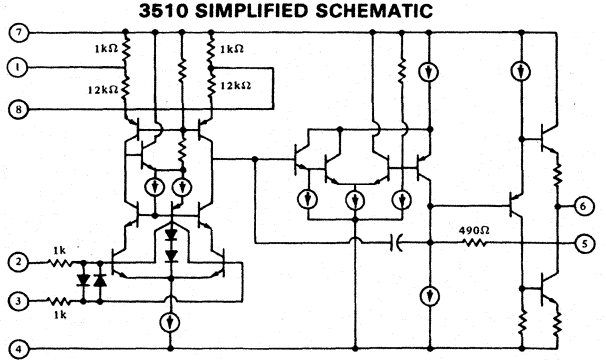
QUIESCENT CURRENT VS SUPPLY VOLTAGE



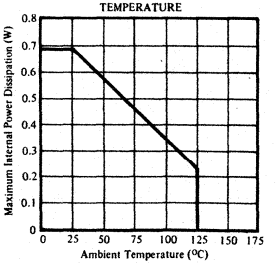
QUIESCENT CURRENT VS TEMPERATURE



3510 SIMPLIFIED SCHEMATIC

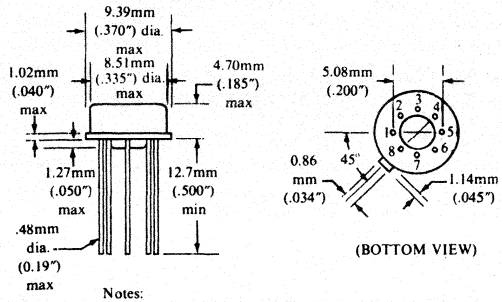


MAXIMUM POWER DISSIPATION VS. TEMPERATURE



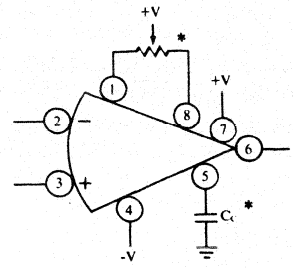
MECHANICAL SPECIFICATIONS

TO-99



Notes:
1. There is no case connection
2. The case is metalic and is conductive
3. The case and leads are bright acid tin plated

Amplifier Connections



*Optional
See applications information

APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT, NULLING AND DRIFT

Unlike some competitive models it is not necessary to null the offset voltage of the 3510 to achieve minimum voltage drift versus temperature. Drift of the 3510 is specified both nulled and unnulled.

In this op amp, the input offset voltage and the input offset voltage drift versus temperature are trimmed, at the wafer level, during manufacture. This feature, combined with the op amp's electrical design and high quality, closely controlled processing produce the low offset voltages and drifts indicated in the specifications. These figures are 100% guaranteed.

Should it be necessary to null the offset voltage to the lowest possible value this can be accomplished by inserting a potentiometer between pins 1 and 8. See "Alternate Nulling Techniques" for other methods. Nulling ultra low offset amplifiers may, however, be undesirable when these factors are considered:

Cost of potentiometer and labor to install and null.

Decreased reliability through introduction of additional components.

Possible degradation of overall performance due to temperature coefficients of external nulling resistors (not true with 3510).

Nulling the offset voltage of most modern op amps will minimize offset voltage drift. In the 3510, an ultra low offset amplifier, a major portion of the offset voltage is trimmed during manufacture. Additional trimming by the user may increase the voltage drift slightly. Drift changes 0.33μV/°C for each 100μV of offset voltage nulled. Due to second order effects, the point of minimum voltage drift does not occur at the point of zero offset voltage in approximately 25% of the cases. In these instances, nulling the offset voltage may cause a slight increase in voltage drift, but not beyond the guaranteed nulled voltage drift specified. Nulling the offset voltage will decrease the voltage drift in approximately 75% of cases.

ALTERNATE NULLING TECHNIQUES

When it is essential to null offset voltage and achieve the lowest guaranteed voltage drift specifications, the following methods can be used:

Burr-Brown recommends nulling in a following stage as shown in Figure 1.

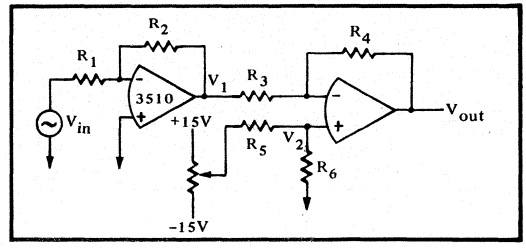


Figure 1. Multi-stage Nulling Circuit

In this circuit, with $V_{in} = 0$, V_1 will be due to E_{os} and I_{bias} of 3510. The component of V_{out} due to V_1 is $\frac{V_1 R4}{R3}$. Resistors R_5 and R_6 are selected so that the component of V_{out} due to V_2 will cancel the component of V_{out} due to V_1. The specific values of R_5 and R_6 are selected to provide the desired range and resolution and will depend upon the model of the 3510 involved and the gain in each stage.

When only a single stage of amplification is used the following circuits could be employed.

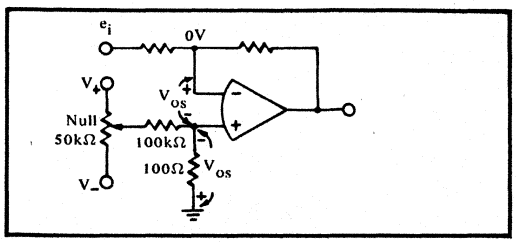


FIGURE 2. Inverting Amplifier

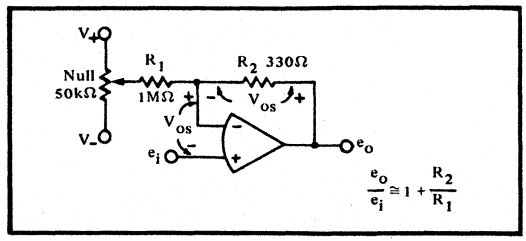


FIGURE 3. Non-Inverting Amplifier

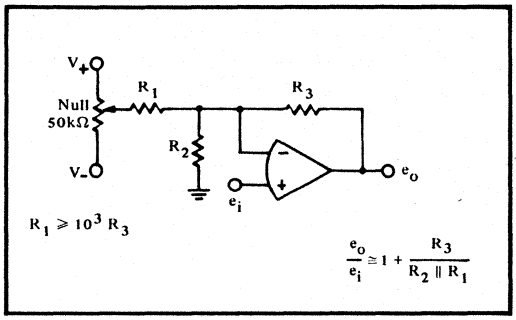


FIGURE 4. Follower Amplifier

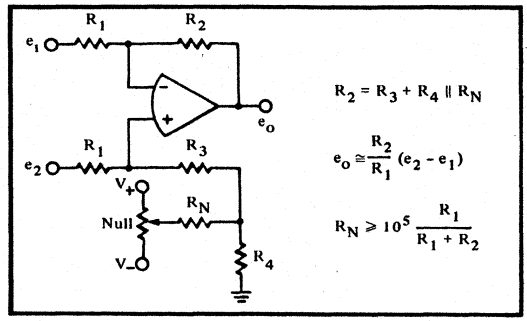


FIGURE 5. Difference Amplifier

RESOLUTION OF NULLING POTENTIOMETER

One of the advantages of the 3510 is the ease of nulling the offset voltage, even with a low cost, single turn potentiometer. A single turn linear potentiometer can be used with good resolution. Unlike some competitive, low offset op amps, the 3510 does not require multiturn pots or fixed resistors padded with a pot to produce a high level of trim resolution.

Resolution and range of the offset trim potentiometer at various resistance values are shown in Table I.

Potentiometer Value	Offset Adjustment Range		Resolution at Pot Center	Sensitivity of $\Delta V_{os}/\Delta T$ to Potentiometer (1) T.C.R. (2)
	10% - 90% Rotation	0% - 100% Rotation		
*100kΩ	±170μV	±2mV	1μV/% rotation	10^{-4}μV/ppm/°C
20kΩ	±600μV	±2mV	3.5μV/% rotation	10^{-4}μV/ppm/°C
10kΩ	±800μV	±2mV	6μV/% rotation	10^{-4}μV/ppm/°C

* Recommended offset adjustment potentiometer.

(1) T.C.R. = temperature coefficient of resistance

(2) Sensitivity after nulling ±120μV of V_{os}; typically the sensitivity is one-half the value shown.

TABLE I. Offset Potentiometer Effects

POTENTIOMETER

Because the external offset 100kΩ potentiometer parallels two internal 1kΩ resistors, the temperature coefficient of the potentiometer will affect the offset voltage temperature drift of the 3510 to a very small degree. In addition, the potentiometer halves have the same temperature coefficient, therefore the percent rotation does not drift. Sensitivity of the offset voltage to the external potentiometer is very low, only 10^{-4}μV/ppm/°C and must be added to the amplifier's drift. However, even when using a 100ppm industrial pot, this figure is ±0.01μV/°C and can be ignored.

THERMAL FEEDBACK

When an amplifier achieves the high performance levels of the 3510 some effects previously masked by larger error terms (and now reduced by the 3510's high accuracy, high performance and low error terms) may become observable. This situation exists with a condition referred to as thermal feedback.

Thermal feedback is an error generating condition which can be caused by the power dissipation and resultant temperature rise of the amplifier's output stage. This error is fed back to a previous stage of the amplifier and alters its usual operation. Normally the input stage is affected. This error is described as a change in input offset voltage per volt of output voltage change. When the 3510 has a 2kΩ load the specification is ±0.1μV/V.

This phenomena is most noticeable at frequencies below a few hertz and most easily observed on an oscilloscope. Thermal feedback can add a small error term to the "average" temperature effects normally described as input offset voltage drift versus temperature and input bias current versus temperature.

To minimize the effect of thermal feedback, the 3510 circuits are carefully laid out and thermally balanced to minimize thermal feedback.

THERMAL RESPONSE TIME

In low drift operational amplifiers like the 3510, thermal response time is an important performance parameter. In precision applications the response of the amplifier to warm-up or environmental change should be considered.

Figure 5 and 7 show typical thermal response of the 3510. Note that the offset voltage does not overshoot and that the response time is very short - less than three minutes. Some competitive low drift operational amplifiers require 15 minutes to warm up.

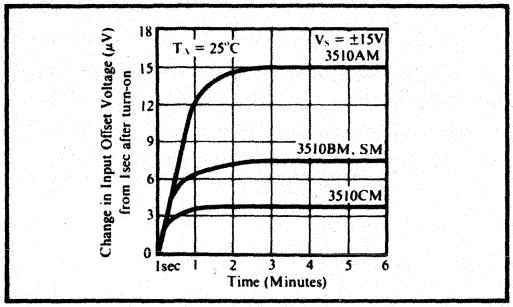


FIGURE 6. Warm-up Drift.

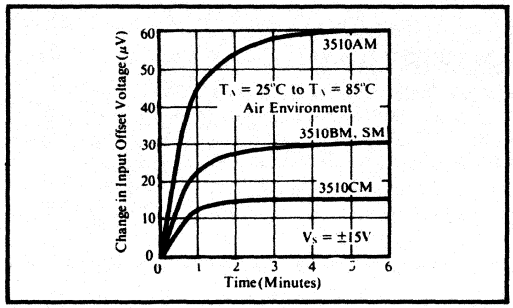


FIGURE 7. Offset Response to an Environmental Change.

NOISE

In a high performance amplifier such as the 3510, noise may well be the final and limiting criteria for system accuracy. See specifications and performance curves.

While the 3510 noise is very acceptable in low and mid-frequencies, it is fairly large above 100kHz. Whether or not this unique characteristic will cause user problems depends on the application of the 3510 and steps taken to reduce high frequency noise effects.

If circuitry following the 3510 does not respond to noise above 100kHz, no corrective steps need to be taken. This situation is common in applications where a 0.5V/μs amplifier is satisfactory. When high frequency noise must be reduced, a low pass filter should be installed in a stage following the 3510 (filtering at the 3510 itself has little effect).

Two high frequency filtering approaches are shown in Figures 8 and 9.

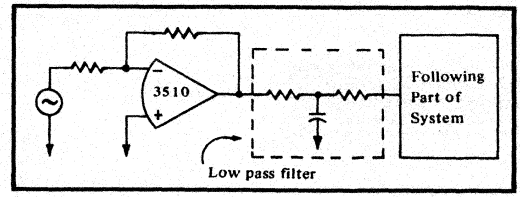


FIGURE 8. High Frequency Filter For Single Stage Amplifier.

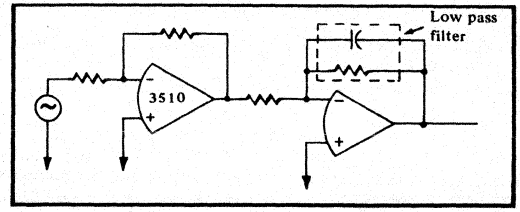


FIGURE 9. High Frequency Filter For Multi-stage Amplifier

COMPENSATION

At closed loop gains above 10V/V, the 3510 op amp is stable without additional frequency compensation. The amplifier is compensated as shown in Figure 10 for gains below 10V/V.

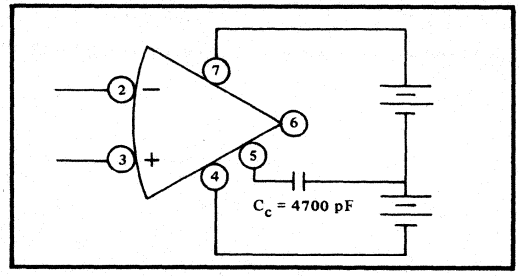


FIGURE 10. Amplifier Compensation Circuit

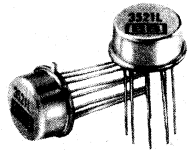
Alternately, the capacitor may be connected between pin 5 and $+V_{cc}$ (pin 7) if the supply is well bypassed to ground.

SHORT CIRCUIT PROTECTION

The 3510 may be short circuited to ground continuously without damage. Output shorts other than to ground may be tolerated if the "Maximum Power Dissipation vs Temperature" ratings given in the performance curves are not exceeded. Power dissipation can be determined as the product of $(V_{cc} - V_{out}) \times I_{out}$. I_{out} under current limit conditions is specified in the "Output Voltage vs Output Current" performance curve.

BURR-BROWN

3521 SERIES



Ultra-Low Drift - FET Input OPERATIONAL AMPLIFIERS

FEATURES

- ULTRA-LOW DRIFT, 1μV/°C max
- LOW INITIAL OFFSET VOLTAGE, 250μV, max
- LOW BIAS CURRENT, 10pA, max
- LOW NOISE
- HIGH COMMON-MODE REJECTION, 90dB, typ
- WIDE POWER SUPPLY RANGE, ±5VDC to ±20VDC

DESCRIPTION

With input offset voltage drifts as low as 1μV/°C, the Burr-Brown 3521 IC Operational Amplifier provides FET input performance combined with drift equal to the best bipolar IC's (e.g. BB 3500E). The spectacular performance is achieved through truly state-of-the-art hybrid design and manufacturing, including monolithic FET pairs and active laser trimming.

The 3521 has an exceptionally fast thermal response. This fast warm-up is achieved without any heat sinking.

While low drift and FET input impedance are the outstanding features of the 3521, other specifications have not been compromised. The 3521 is internally compensated for unity-gain configuration and the initial voltage offset is guaranteed less than 250μV so for most applications the 3521 is ready to "plug in and go." Like other low drift IC's from Burr-Brown the 3521 has ample speed and bandwidth for most any application. (Slew rate = 0.8V/μsec). The high common-mode rejection ratio (90dB, typ.) enables the 3521 to be used as a .01% accurate buffer with low drift and extremely high input impedance. The 3521 also has very-low input noise to complement the low drift. The output is current limited to provide protection for continuous output shorts to common.

The 3521 is pin compatible with 741 type amplifiers, but provides FET input performance with ultra-low drift while exceeding all other specifications for general purpose operational amplifiers of the 741 type. Burr-Brown tests and guarantees all units to meet all max/min specifications.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

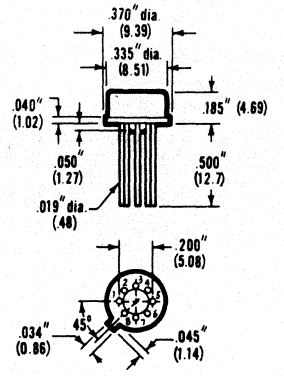
PDS-2731 Printed in U.S.A. July, 1978

SPECIFICATIONS

Specifications typical at 25°C and ±15 Vdc Power Supply unless otherwise noted.

MODELS	3521H	3521J	3521K	3521L	3521R
OPEN LOOP GAIN, dc					
Rated load, min		*	94 dB	94 dB	*
RATED OUTPUT					
Voltage, min.			±10 V		
Current, min.	*	*	±10 mA	*	*
Output Impedance			100 Ω		
FREQUENCY RESPONSE					
Unity Gain, Open Loop			1.5 MHz		
Full Power Response, min	*	*	10 kHz	*	*
Slew Rate, min			0.6 V/μsec		
INPUT OFFSET VOLTAGE					
Initial Offset, 25°C, max.	±500μV	250μV	250μV	250μV	250μV
vs. Temp(0° to 70°C),** max.	±10μV/°C	±5μV/°C	±2μV/°C	±1μV/°C	±5μV/°C**
(-25° to +85°C)	±15μV/°C	±8μV/°C	±4μV/°C	±2μV/°C	±2μV/°C
vs. Supply Voltage	*	*	±25 μV/V	*	*
vs. Time	*	*	5 μV/mo	*	*
INPUT BIAS CURRENT					
Initial bias, 25°C, max.	-20 pA	-20 pA	- 15 pA	- 10 pA	- 20 pA
(doubles every +10°C)					
vs. Supply Voltage	*	*	1 pA/V	*	*
INPUT DIFFERENCE CURRENT					
Initial difference, 25°C	±2 pA	±2 pA	±2 pA	±2 pA	±2 pA
INPUT IMPEDANCE					
Differential	*	*	10^{11} Ω	*	*
Common Mode			10^{12} Ω		
INPUT NOISE					
Voltage, .01 Hz - 10 Hz, p-p			4 μV		
10 Hz - 1 kHz, rms	*	*	2 μV	*	*
Current, .01 Hz - 10Hz, p-p			0.3 pA		
10 Hz - 1 kHz, rms			0.6 pA		
NPUT VOLTAGE RANGE					
Common Mode Voltage			±10 V		
Common Mode Rejection	*	*	90 dB	*	*
Max. Safe Input Voltage			± Supply		
POWER SUPPLY					
Rated Voltage			±15 Vdc		
Voltage Range, derated	*	*	±5 to ±20 Vdc	*	*
Current, quiescent			±4 mA		
TEMPERATURE RANGE					
Specification	0° to +70°C				-55° to +125°C
Operating	-25° to +85°C				-55° to +125°C
Storage	*	*	-65° to +150°C		*

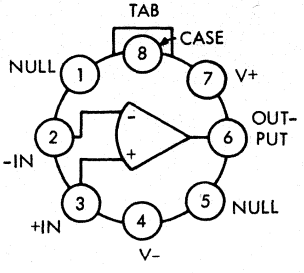
TO-99 PACKAGE



(BOTTOM VIEW)

CONNECTION DIAGRAM

(TOP VIEW)



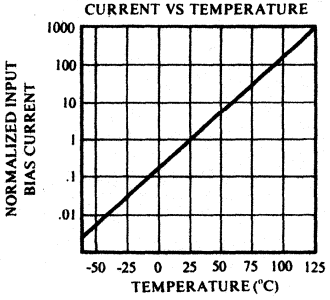
* Specification same for all models

** -55° to +125°C for 3521R

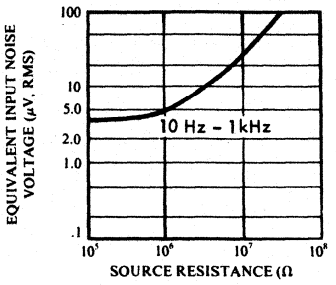
TYPICAL PERFORMANCE CURVES

(at +25°C and ±15VDC unless otherwise specified)

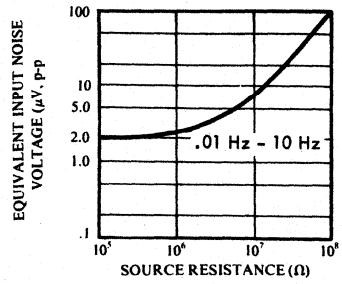
NORMALIZED INPUT BIAS CURRENT VS TEMPERATURE



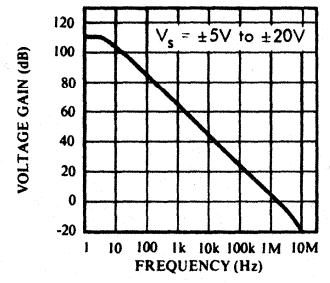
RMS INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



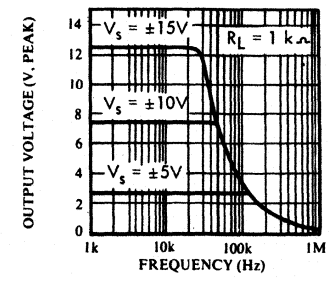
P-P INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



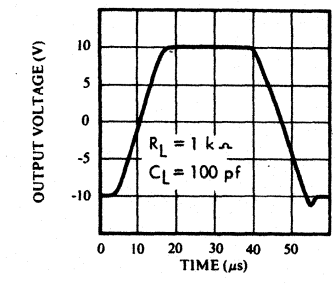
OPEN LOOP FREQUENCY RESPONSE



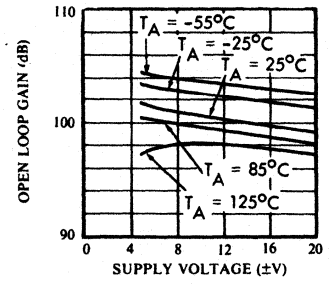
OUTPUT VOLTAGE VS FREQUENCY



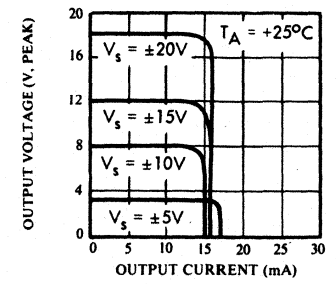
VOLTAGE FOLLOWER STEP RESPONSE



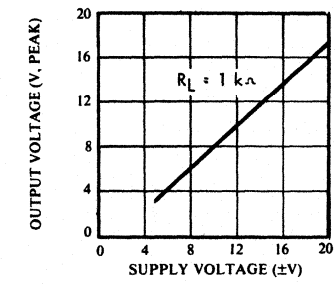
VOLTAGE GAIN VS SUPPLY VOLTAGE



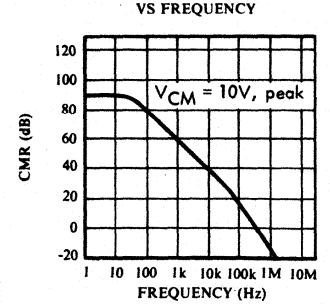
OUTPUT VOLTAGE VS OUTPUT CURRENT



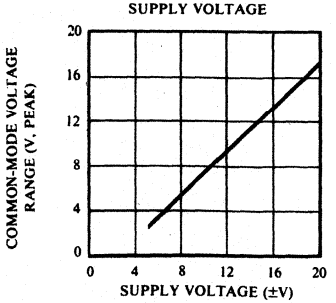
OUTPUT VOLTAGE VS SUPPLY VOLTAGE



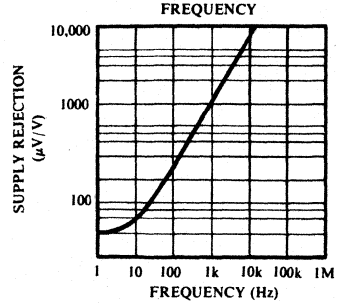
COMMON MODE REJECTION VS FREQUENCY



COMMON-MODE RANGE VS SUPPLY VOLTAGE



POWER SUPPLY REJECTION VS FREQUENCY



APPLICATIONS INFORMATION

THERMAL RESPONSE TIME

Thermal response time is an important parameter in low drift operational amplifiers like the 3521. A low drift specification would be of little value if the amplifier took several hours to stabilize after turn-on or ambient temperature change. The TO-99 packaging is particularly well suited for devices requiring fast thermal response. Figure 1 shows the typical warm-up drift of the 3521. Note that the offset voltage has stabilized in less than 4 minutes. Similar warm-up times for some discrete low drift operational amplifiers range from 7 to 15 minutes.

Offset voltage response to thermal shock can provide some real surprises, particularly for amplifiers packaged in discrete modules. Again the 3521 TO-99 package proves superior. Figure 2 shows that the response to thermal shock settles very quickly. The 3521 quickly and smoothly assumes a new value of offset voltage as dictated by the drift specification.

BIAS CURRENT EFFECTS

The low bias currents and offset currents of FET input stages overcome most of the source resistance limitations of bipolar operational amplifiers. However for very large source resistances or large unbalances in source resistance (5 MΩ and up) the input offset voltage and drift will be affected as shown in Figures 3 and 4.

COMMON MODE PROPERTIES

The input stage of the 3521 is a monolithic FET pair, which affords very good matching between the two input transistors. This close matching makes the 90 dB common mode rejection ratio (CMRR) possible. Because of its excellent common mode properties the 3521 may be used as a 0.01% accurate buffer amplifier for inputs between ±10 V. Figure 5 below illustrates typical common mode performance of the 3521.

POWER SUPPLIES AND DRIFTS

Note that a power supply change of 40 mV will typically introduce an input offset voltage change of 1 µV. Since power supply drift will have the same effect as offset voltage drift, the power supply temperature coefficients of ±15 V supplies should be about 0.1%/°C for optimum drift performance of the 3521L.

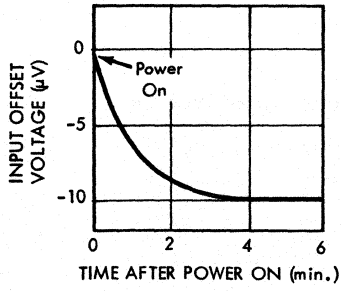


FIGURE 1. Typical Warmup Drift.

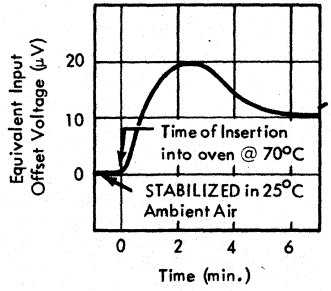
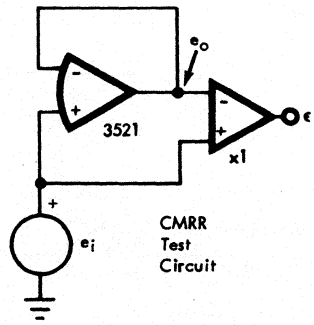


FIGURE 2. Effect of Thermal Shock on Offset Voltage.



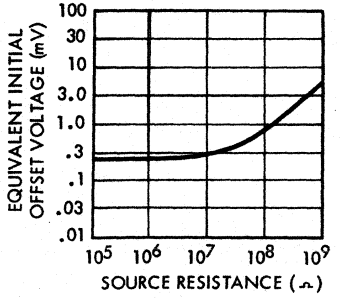


FIGURE 3. Typical Effects of Source Resistance on Initial Offset Voltage.

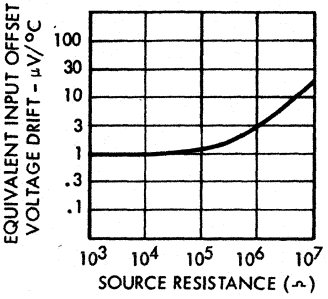


FIGURE 4. Typical Effects of Source Resistance on Equivalent Input Offset Voltage Drift.

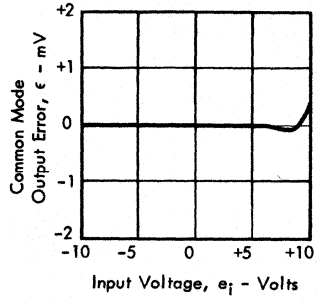


FIGURE 5. Common Mode Performance.

WIRING CONSIDERATIONS (SHIELDING and GUARDING)

The ultra low drift, very low bias current and high input impedance make the 3521 well suited to a number of unique applications. However, careless signal wiring can degrade "system" performance several orders of magnitude below the 3521 capability.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large value feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the 3521. Perhaps more important, unbalanced leakage paths (When is leakage ever balanced?) can generate significant input offset voltages when large source impedances (100 k Ω and up) are involved. To avoid leakage problems, it is recommended that the inputs of the 3521 be wired to teflon standoffs. If the 3521 must be soldered directly into a printed circuit board, utmost care should be used in designing the board layout. A "guard" pattern should completely surround the two input leads and be connected to a low impedance point at the common mode input voltage. Figure 6 shows suggested guard connections for various amplifier feedback configurations. The amplifier case should be connected to any input shield or guard via pin 8.

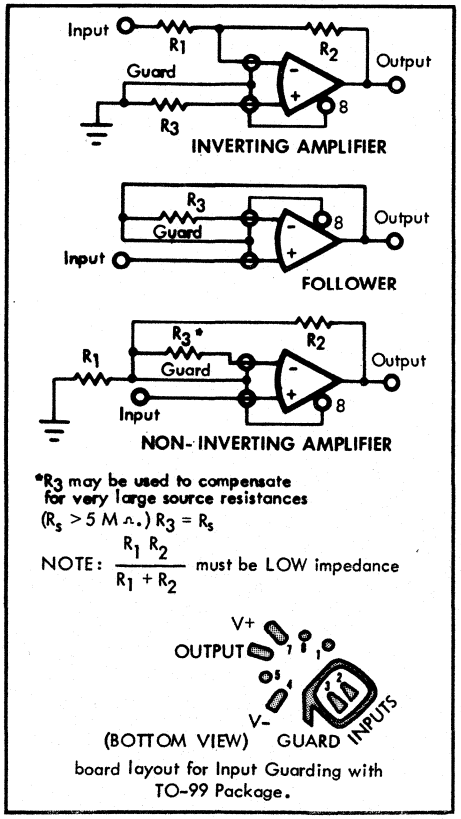


FIGURE 6. Connection of Input Guard.

OFFSET VOLTAGE ADJUSTMENT

The 3521 has a low initial offset (250 μV) compatible with its low drift. However, some high accuracy applications may require external nulling of even this small initial offset voltage. Virtually any offset voltage adjustment method can increase offset voltage drift unless some care is used. For example, the initial offset voltage of most monolithic op amps (BB 3500, 741 types, 101, etc.) may be nulled using a single potentiometer, but offset voltage drift is typically increased by about 3 μV/°C for each mV of offset voltage adjust. This same relationship will also hold for the 3521.

SINGLE POTENTIOMETER ADJUST

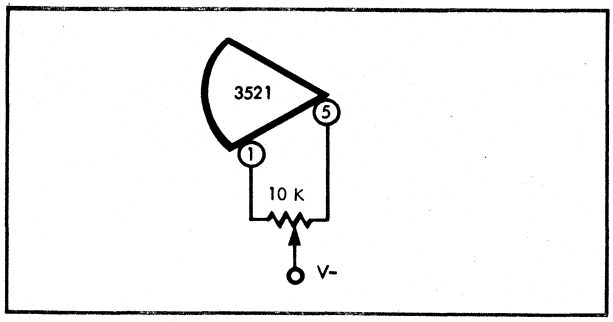


FIGURE 7. Single Potentiometer Adjust at Op Amp Trim Terminals.

Advantages

1. Simplest circuit
2. Compatible with most IC op amps

Disadvantages

1. Drift increased by circuit about 0.75 μV/°C for 3521.

TEMPERATURE COMPENSATED POTENTIOMETER OFFSET VOLTAGE ADJUST

If the circuit in Figure 7 is replaced with a circuit which "drifts" with temperature, nulling the offset voltage will not increase the drift by so large an amount. The circuit shown in Figure 8 may be used to null initial offset voltage and drift will increase only about 0.5 μV/°C for each mV of offset adjust. In the case of the 3521, this zeroing circuit will typically add at most .14 μV/°C.

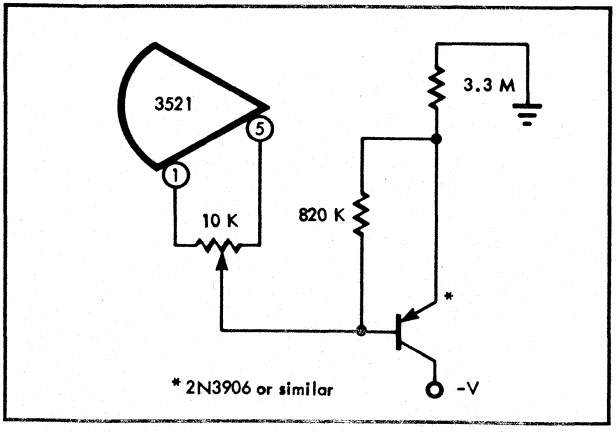


FIGURE 8. Temperature Compensated Potentiometer Null.

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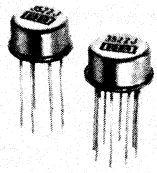
3522 SERIES



FET Input
OPERATIONAL AMPLIFIERS

FEATURES

- LOW BIAS CURRENT, 1pA, max
- LOW OFFSET VOLTAGE, 500μV, max
- LOW NOISE, 2μV, rms
- HIGH CMR, 90dB
- WIDE SUPPLY RANGE, ±5VDC to ±18VDC

DESCRIPTION

These FET amplifiers offer excellent input characteristics at moderate cost through the use of monolithic chips, thin-film technology, and laser trimming. Unlike other FET op amps of comparable cost, they have low input noise, low offset voltage, and moderate voltage drift. Thus they are suitable for a number of applications where previous monolithic or hybrid FET op amps were, at best, marginal. The low value of input offset voltage usually means that no external nulling will be required. This in turn makes for significantly lower installed cost, high system reliability, and decreased packaging volume (or PC board area).

In addition, the 3522 series are extremely stable amplifiers having internal frequency compensation. Other built-in features are output short-circuit protection, input protection to supply voltage, and operation over a wide range of supply voltages.

The pin configuration of the 3522 is conventional (same as 741 type amplifiers) except for pin 8 which is connected to the case. In the usual IC operational amplifier, the case is connected to the negative supply voltage. However, in FET amplifiers it is often desirable to connect the case to a low impedance "guard" potential. This aids in eliminating noise "pickup" in high impedance circuits and preserves the low input currents of the amplifier.

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PDS-289F

Printed in U.S.A. July, 1978

SPECIFICATIONS

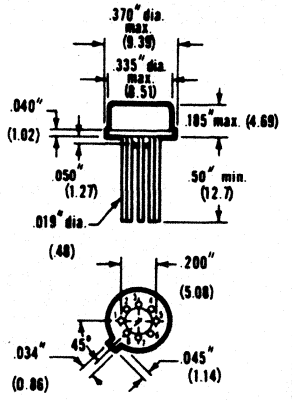
Prices and specifications subject to change without notice.

ELECTRICAL

Specifications typical at 25°C and ±15 Vdc Power Supply unless otherwise noted.

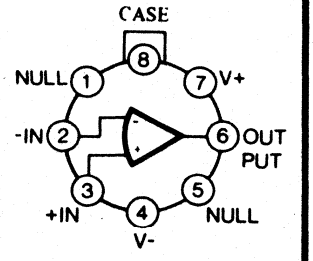
MODELS	3522J	3522K	3522L	3522S
OPEN LOOP GAIN, dc Rated load, min	94 dB	94 dB	94 dB	94 dB
RATED OUTPUT Voltage, min. Current, min. Output Impedance	±10V ±10 mA 100 Ω	*	*	*
FREQUENCY RESPONSE Unity Gain, Open Loop Full Power Response, min. Slew Rate, min.	1 MHz 10 kHz 0.6 V/μsec	* 10 kHz 0.6 V/μsec	* 10 kHz 0.6V/μsec	* 10 kHz 0.6V/μsec
INPUT OFFSET VOLTAGE Initial Offset, 25°C, max. vs. Temp (0° to +70°C), max. (-55° to +125°C), max. vs. Supply Voltage vs. Time	±1 mV ±50 μV/°C ±25 μV/V ±10 μV/mo	±500 μV ±10 μV/°C * *	±500 μV ±10 μV/°C * *	±500 μV ±25 μV/°C * *
INPUT BIAS CURRENT *** Initial bias, 25°C, max. (doubles every +10°C) vs. Supply Voltage	-10 pA ±0.1 pA/V	-5 pA *	-1 pA *	-5 pA *
INPUT DIFFERENCE CURRENT Initial difference, 25°C	±2 pA	±1 pA	±0.5 pA	±1 pA
INPUT IMPEDANCE Differential Common Mode	10^{11} Ω 10^{12} Ω	*	*	*
INPUT NOISE Voltage, .01 Hz - 10 Hz, p-p 10 Hz - 1 kHz, rms Current, .01 Hz - 10 Hz, p-p 10 Hz - 1 kHz, rms	 4 μV 2 μV .3 pA .6 pA	*	*	*
INPUT VOLTAGE RANGE Common Mode Voltage Common Mode Rejection Max. Safe Input Voltage	±10 V 90 dB ±supply	*	*	*
POWER SUPPLY Rated Voltage Voltage Range, derated Current, quiescent	±15 Vdc ±5 to ±20 Vdc ±4 mA	*	*	*
TEMPERATURE RANGE Specification Operating Storage	 0° to +70°C -25° to +85°C -65° to +150°C	*	*	 -55° to +125°C -55° to +125°C *
PRICE 1 - 24 Contact factory for 25 - 99 latest prices.	 13.45 10.75	 16.35 13.20	 22.65 18.00	 30.60 25.30
*Specification same as for 3522J. ***After Warm-Up				

TO-99 PACKAGE



(BOTTOM VIEW)

CONNECTION DIAGRAM

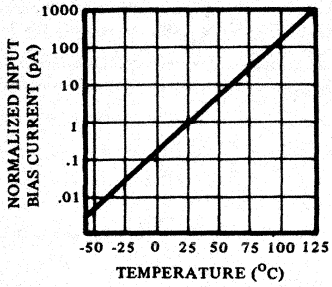


(TOP VIEW)

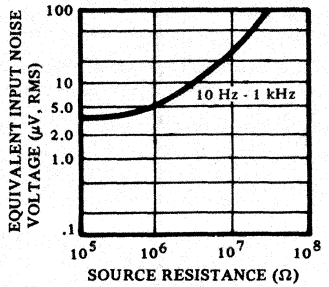
TYPICAL PERFORMANCE CURVES

(@ +25°C and ±15 Vdc unless otherwise specified)

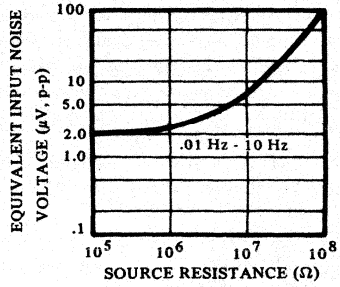
NORMALIZED INPUT BIAS CURRENT vs. TEMPERATURE



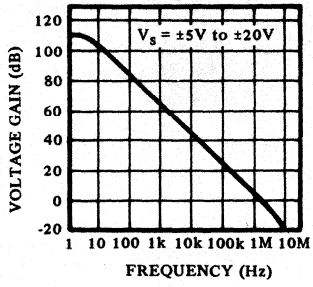
RMS INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



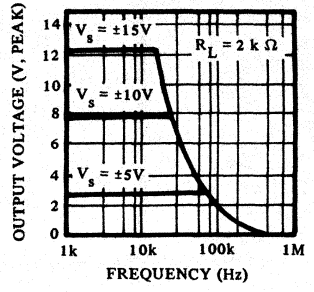
P-P INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



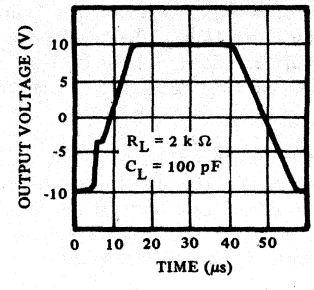
OPEN LOOP FREQUENCY RESPONSE



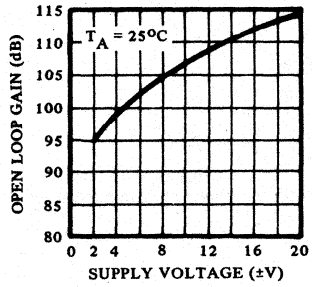
OUTPUT VOLTAGE vs. FREQUENCY



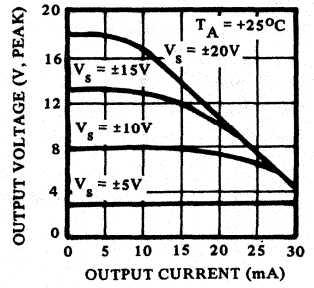
VOLTAGE FOLLOWER STEP RESPONSE



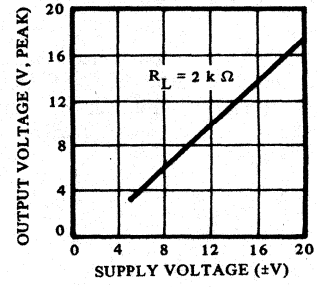
VOLTAGE GAIN vs. SUPPLY VOLTAGE



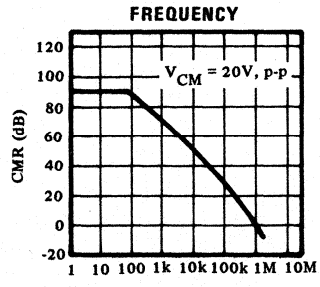
OUTPUT VOLTAGE vs. OUTPUT CURRENT



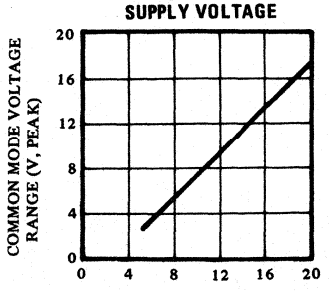
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



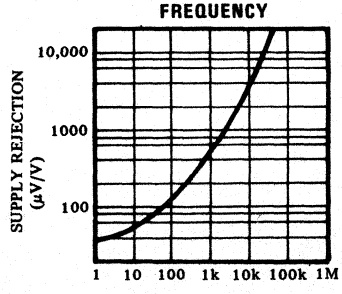
COMMON MODE REJECTION vs. FREQUENCY



COMMON MODE RANGE vs. SUPPLY VOLTAGE



POWER SUPPLY REJECTION vs. FREQUENCY



WIRING CONSIDERATIONS

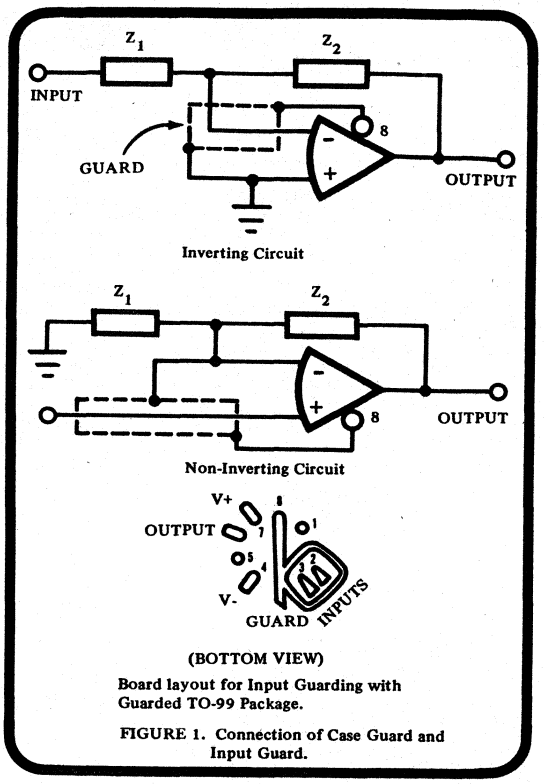
Shielding and Guarding

The ultra-low bias current and high input impedance of the 3522 are well-suited to a number of stringent applications. However, careless signal wiring or printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the 3522.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the 3522. To avoid leakage problems, it is recommended that the signal input lead of the 3522 be wired to a Teflon standoff. If the 3522 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 1 illustrates the use of the guard for both inverting and non-inverting circuits.



Board layout for Input Guarding with Guarded TO-99 Package.

FIGURE 1. Connection of Case Guard and Input Guard.

OFFSET VOLTAGE ADJUSTMENT

Although the 3522 has a low initial offset voltage (500μV), compatible with it's moderate voltage drift, some applications may require external nulling of this small offset, Figure 2 shows the recommended circuit for adjustment of the offset voltage.

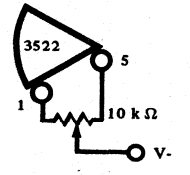
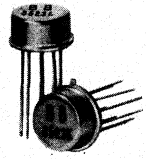


FIGURE 2. External nulling of Offset Voltage.

BURR-BROWN

3523 SERIES



Ultra-Low Bias Current FET OPERATIONAL AMPLIFIERS

FEATURES

- BIAS CURRENT, 0.1pA, max
- OFFSET VOLTAGE, 500μV, max
- VOLTAGE DRIFT, 25μV/°C, max
- INPUT IMPEDANCE, $10^{13}\Omega$
- Noise (10Hz), 0.003pA, p-p

DESCRIPTION

The Burr-Brown 3523 Series amplifiers are the first IC operational amplifiers to achieve sub-picoampere input currents without exhibiting excessive offset voltage, voltage drift and voltage noise. The high common-mode rejection, ultra-low bias current, and $10^{13}\Omega$ input impedance of the 3523 make it the best choice for a variety of buffer and electrometer applications. These include pH measurement, photocurrent amplification, long term integration, and low droop sample/hold or track/hold applications. Because its input offset voltage is laser-trimmed to less than 500μV, the 3523 can usually be used without offset nulling. This is a distinct advantage in applications where it is desired to locate the 3523 near the signal source (e.g., in a signal probe).

The package of the 3523 is designed to preserve its ability to measure ultra-low currents and to avoid noise pickup. The case guard (pin no. 8) may be connected to a point which is at signal potential. This minimizes leakage current input from pins to case. Also, it shields the amplifier's sensitive input circuitry from power line frequency "hum", switching transients, and other sources of electrical noise.

Bias current specifications of the 3523 are guaranteed after warm-up in ambient air with no heat sink. Thus, the ultra-low bias current specifications become even more significant since internal power dissipation can easily raise case temperature by 20°C in many applications.

The bias current on many FET amplifiers is a strong function of applied common-mode voltage. This is not the case with the 3523. The input stage design of the 3523 make the input bias current virtually independent of the common-mode voltage over its full range.

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PDS-309C

Printed in U.S.A. July, 1978

SPECIFICATIONS

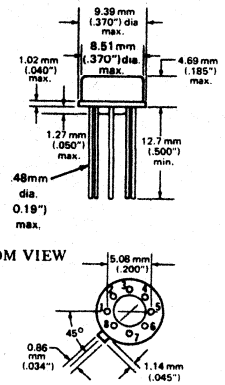
Specifications typical at 25°C and ±15 Vdc Power Supply unless otherwise noted.

ELECTRICAL

MODELS	3523J	3523K	3523L
OPEN LOOP GAIN, dc no load		100 dB	
1 kΩ, load, min		94 dB	
RATED OUTPUT			
Voltage, min		±10 V	
Current min		±10 mA	
Output Impedance		100 Ω	
FREQUENCY RESPONSE			
Unity Gain, Open Loop		1 MHz	
Full Power Response, min		10 kHz	
Slew Rate, min		0.6 V/μsec	
INPUT OFFSET VOLTAGE			
Initial Offset, 25°C, max	±1 mV	±500 μV	±500 μV
vs. Temp (0° to 70°C), max	±50 μV/°C	±25 μV/°C	±25 μV/°C
vs. Supply Voltage		±25 μV/V	
vs. Time		±5 μV/mo	
INPUT BIAS CURRENT			
Initial bias, 25°C, max	-0.5 pA	-0.25 pA	-0.1 pA
(doubles every +10°C)			
vs. Supply Voltage		±0.01 pA/V	
INPUT DIFFERENCE CURRENT			
Initial difference, 25°C	±0.2 pA	±0.1 pA	±0.05 pA
INPUT IMPEDANCE			
Differential		10^{12} Ω	
Common Mode		10^{13} Ω	
INPUT NOISE			
Voltage, .01 Hz - 10 Hz, p-p		4 μV	
10 Hz - 10 kHz, rms		2 μV	
Current, .01 Hz - 10 Hz, p-p		.003 pA	
10 Hz - 10 kHz, rms		0.01 pA	
INPUT VOLTAGE RANGE			
Common Mode Voltage		±($\|V_S\|$-2) V	
Common Mode Rejection @ 10V		80 dB	
Max. Safe Input Voltage		± Supply	
POWER SUPPLY			
Rated Voltage		±15 Vdc	
Voltage Range, derated		±5 to ±20 Vdc	
Current, quiescent		±4 mA	
TEMPERATURE RANGE			
Specification		0° to +70°C	
Operating		-55° to +125°	
Storage		-65° to +150°C	

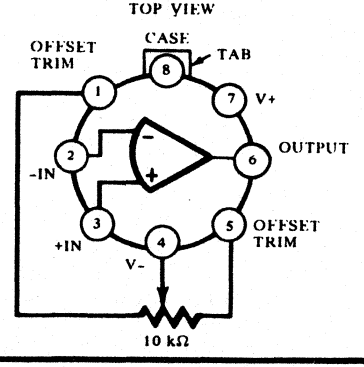
MECHANICAL

TO-99

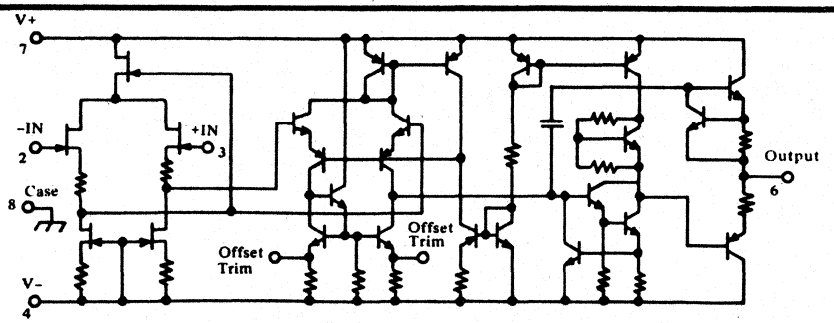


Dimensions in inches are in parentheses. Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

CONNECTION DIAGRAM



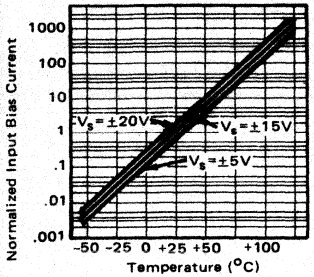
SIMPLIFIED SCHEMATIC



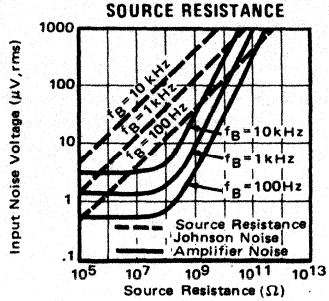
TYPICAL PERFORMANCE CURVES

(@ +25°C and ±15 Vdc unless otherwise specified)

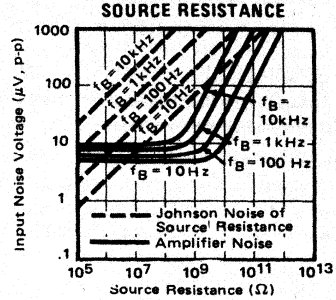
NORMALIZED INPUT BIAS CURRENT vs. TEMPERATURE



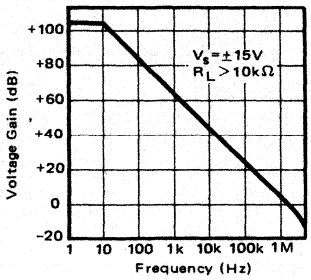
RMS INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



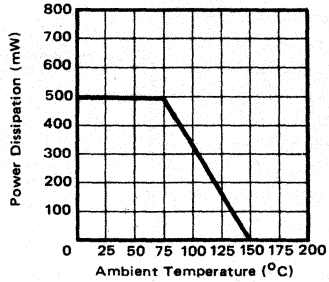
P-P INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



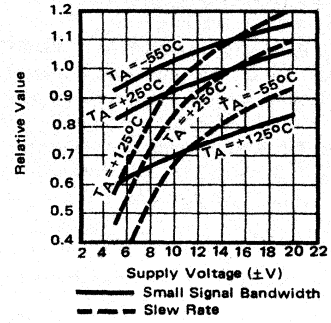
OPEN LOOP FREQUENCY REPONSE



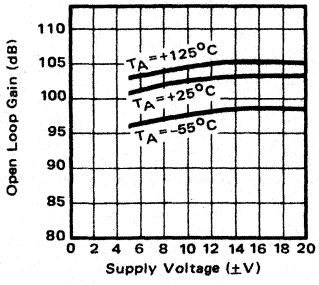
MAXIMUM POWER DISSIPATION



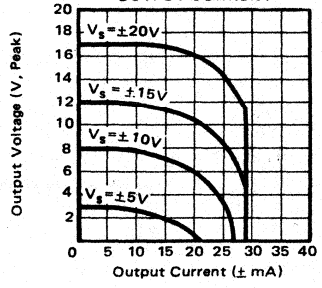
FREQUENCY CHARACTERISTICS vs. SUPPLY VOLTAGE



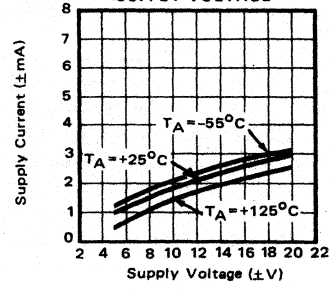
OPEN LOOP GAIN vs. SUPPLY VOLTAGE



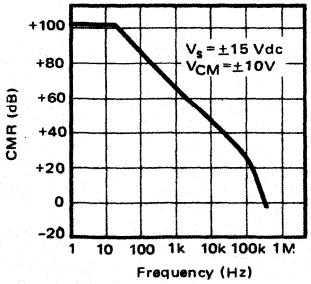
OUTPUT VOLTAGE vs. OUTPUT CURRENT



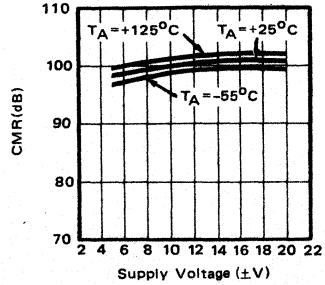
SUPPLY CURRENT vs. SUPPLY VOLTAGE



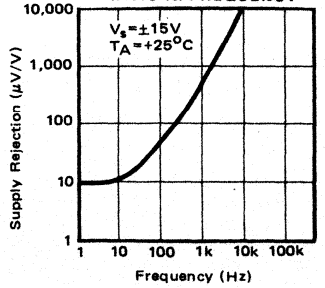
COMMON MODE REJECTION vs. FREQUENCY



COMMON MODE REJECTION vs. SUPPLY VOLTAGE



POWER SUPPLY REJECTION RATIO vs. FREQUENCY



APPLICATION CONSIDERATIONS

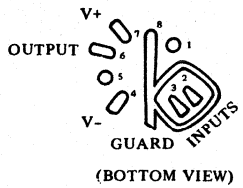
The ultra-low bias current and high input impedance of the 3523 are well suited to a number of challenging applications. In order to fully benefit from the outstanding specifications of this unit careful layout, shielding and guarding is required. Careless signal wiring or printed circuit board layout can easily degrade circuit performance several orders of magnitude below the capability of the 3523.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. The metal case of the 3523 is connected to pin 8 and is not connected to any internal amplifier circuitry. Thus it is possible to use the case as a shield to reduce noise pick-up.

Leakage currents across printed circuit boards can easily exceed the bias current of the 3523. To avoid leakage problems, it is recommended that a Teflon IC socket be used or that at least the signal input lead of the 3523 be wired to a Telfon standoff. If this is not done and instead the 3523 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential. (See Figure 1) The amplifier case, pin 8, should also be connected to the guard. This insures that the entire amplifier circuitry is fully surrounded by the guard potential. This minimizes the voltage placed across any leakage paths and thus reduces leakage currents.

Figures 2, 3, and 4 show typical applications using the guard and case shielding.

Cleanliness is also a prime concern in ultra low bias current circuits. It is recommended that after installation is complete the assembly be washed with a low residue solvent such as TMC Freon followed by rinsing with deionized water. The use of some form of high dielectric conformal coating such as a good two part urathane should be considered if the assembly will be used in air environment which could deposit contaminants on the low current circuitry.



Board layout for Input Guarding with Guarded TO-99 Package.

FIGURE 1. Connection of Case Guard and Input Guard.

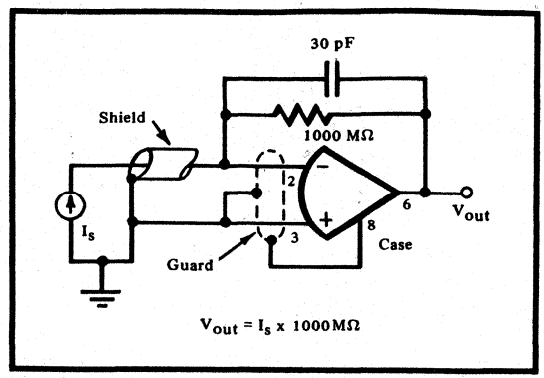


FIGURE 2. Ultra Low Current to Voltage Converter.

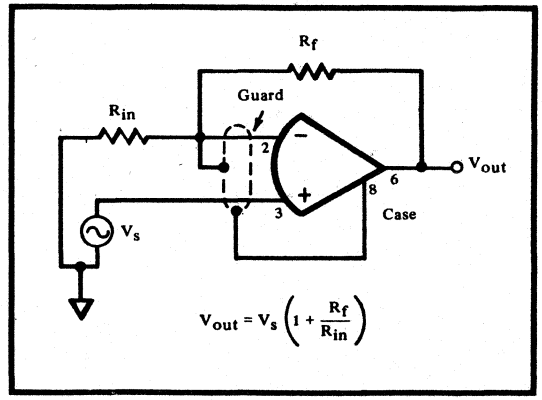


FIGURE 3. Ultra High Input Impedance Noninverting Circuit.

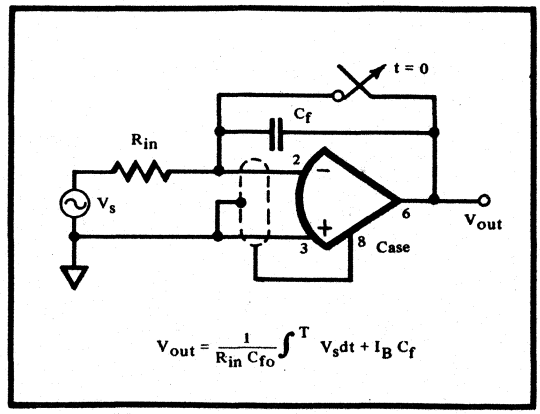
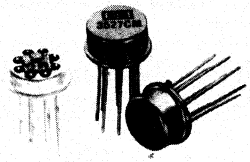


FIGURE 4. Ultra Low Drift Integrator.

BURR-BROWN

3527



Low Drift - Low Bias Current FET Input OPERATIONAL AMPLIFIER

FEATURES

- LOWER PRICED
- ULTRA-LOW DRIFT, 2μV/°C, max
- LOW INITIAL OFFSET VOLTAGE, 250μV, max
- LOW BIAS CURRENT, 2pA, max
- LOW NOISE

DESCRIPTION

The Burr-Brown 3527 is a precision operational amplifier. It offers spectacular performance at moderate cost through the use of hybrid construction, monolithic ICs, matched FETs, thin-film resistors, and active laser trimming.

The 3527 low, initial offset voltage (250μV, max) allows higher design accuracy at lower installed cost. Costly pots and external nulling of the offset voltage is not required for most applications. Also, higher system reliability is achieved by using fewer parts.

The offset voltage temperature drift of the 3527 is exceptionally low (2μV/°C, max) and is compatible with the best bipolar amplifiers (BB3500E). It is achieved by laser-adjusting the offset during manufacture and means that high system accuracy is maintained over the temperature range.

The low bias current (guaranteed 2pA, max) allows the use of larger feedback resistor values, and smaller bias current errors are realizable.

Of course, all the other desirable features of high quality op amps are engineered into the 3527. It has low input noise, is free from latch-up, is short-circuit-protected for continuous output shorts to common, is internally compensated for unity-gain stability, and is pin-compatible with 741 amplifiers. Guarding is achieved by the pin 8 case connection.

For increased reliability screening, consult Burr-Brown.

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PDS-370

Printed in U.S.A. July, 1978

SPECIFICATIONS

Specifications typical at T_A = 25°C and ±15VDC, unless otherwise noted.

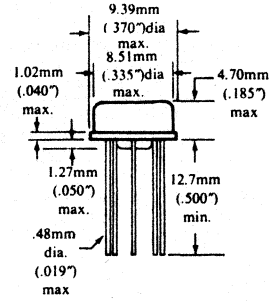
ELECTRICAL

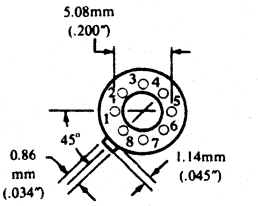
MODELS	3527AM			3527BM			3527CM		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
OPEN LOOP GAIN, dc									
No Load		112dB		*	*		*	*	
Rated Load	100dB	108dB							
RATED OUTPUT									
Voltage	±10V	±12V		*	*		*	*	
Current	±10mA	±20mA							
Output Impedance		600Ω							
Load Capacitance		1000 pF							
FREQUENCY RESPONSE									
Unity Gain, Open Loop		1 MHz		*	*		*	*	
Full Power Response	10kHz	14 kHz							
Slew Rate	.6 V/μs	.9 V/μs							
Settling time (.01%)		45 μs							
INPUT OFFSET VOLTAGE									
Initial Offset, 25°C		±200 μV	±500 μV		±100	±250		±100	±250
vs. Temp (-25°C to +85°C)		±5 μV/°C	±10μV/°C		±2	±5		±1	±2
vs. Supply Voltage		±75 μV/V			*			*	
vs. Time		±20 μV/mo			*			*	
INPUT BIAS CURRENT									
Initial bias, 25°C		-2 pA	-5 pA		-.7	-2		-2	-5
vs. Temp		**			**			**	
vs. Supply Voltage		±5 pA/V			*			*	
INPUT DIFFERENCE CURRENT									
Initial difference, 25°C		±.3 pA			*			*	
INPUT IMPEDANCE									
Differential		10^{12}			*			*	
Common-mode		10^{15}							
INPUT NOISE									
Voltage, f_o = 10 Hz		75nV/$\sqrt{Hz}$			*			*	
f_o = 100 Hz		35nV/$\sqrt{Hz}$							
f_o = 1 kHz		30nV/$\sqrt{Hz}$							
f_o = 10 kHz		25nV/$\sqrt{Hz}$							
.3 Hz-10 Hz, p-p		2.6μV							
10 Hz-10 kHz, rms		3μV							
Current, .3 Hz -10 Hz, p-p		15 fA							
10 Hz -10 kHz, rms		60 fA							
INPUT VOLTAGE RANGE									
Common-mode Voltage Range		±(|V_s|-3)V			*			*	
Common-mode Rejection at ±10V		76 dB							
Max. Safe Input Voltage		±V_s							
POWER SUPPLY				*	*	*	*	*	*
Rated Voltage		±15V							
Voltage Range, derated performance	±5V		±20V						
Current, quiescent		2.6 mA	4 mA						
TEMPERATURE RANGE (ambient)				*		*	*		*
Specification	-25°C		+85°C						
Operating	-55°C		+125°C						
Storage	-65°C		+150°C						
θ junction-ambient		150°C/W							

* Specifications same as for 3527AM
** Doubles every +10°C

MECHANICAL

TO-99 PACKAGE



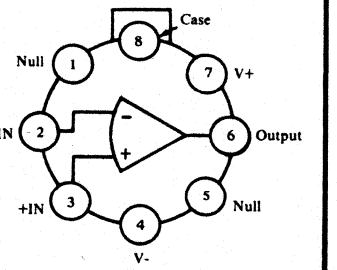


(BOTTOM VIEW)

The TO-99 can and leads are bright acid tin plated.

Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).

CONNECTION DIAGRAM

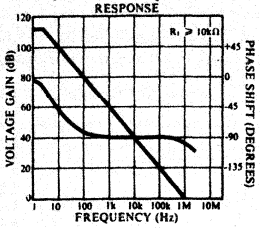


(TOP VIEW)

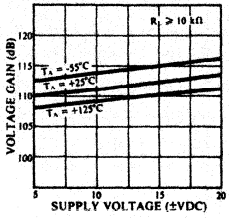
TYPICAL PERFORMANCE CURVES

at T_A = +25°C and ±15VDC unless otherwise noted.

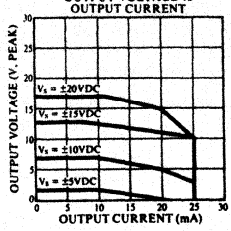
OPEN LOOP FREQUENCY RESPONSE



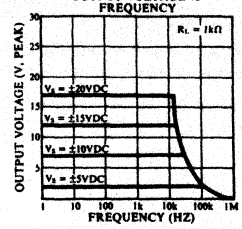
VOLTAGE GAIN



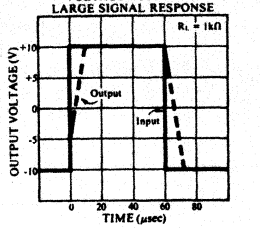
OUTPUT VOLTAGE vs OUTPUT CURRENT



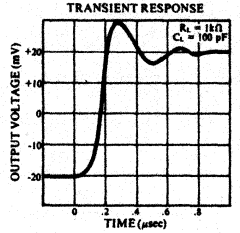
OUTPUT VOLTAGE vs FREQUENCY



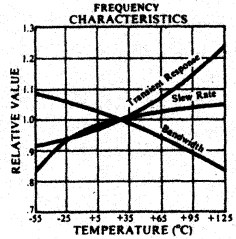
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



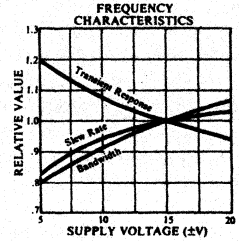
TRANSIENT RESPONSE



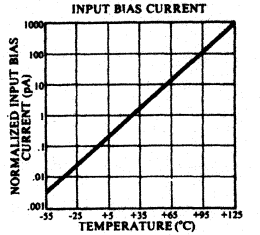
FREQUENCY CHARACTERISTICS



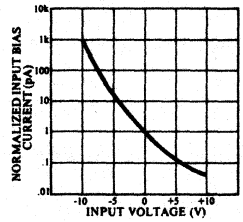
FREQUENCY CHARACTERISTICS



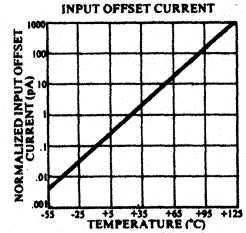
INPUT BIAS CURRENT



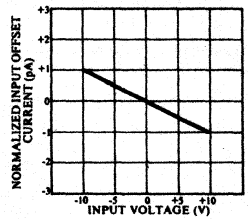
INPUT BIAS CURRENT



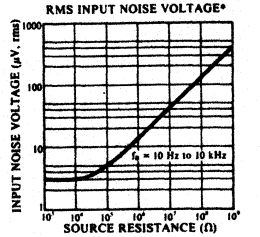
INPUT OFFSET CURRENT



INPUT OFFSET CURRENT

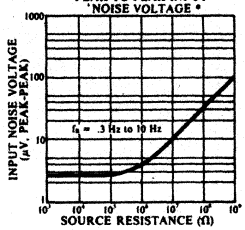


RMS INPUT NOISE VOLTAGE*

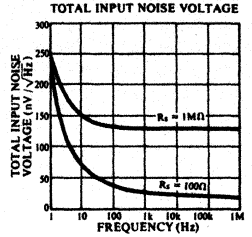


* Includes contribution from source resistance.

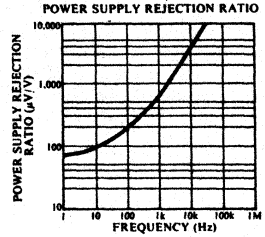
PEAK-TO-PEAK INPUT NOISE VOLTAGE *



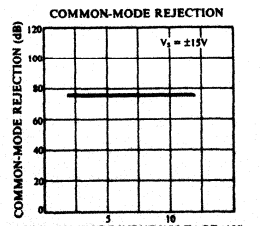
TOTAL INPUT NOISE VOLTAGE



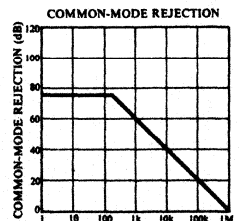
POWER SUPPLY REJECTION RATIO



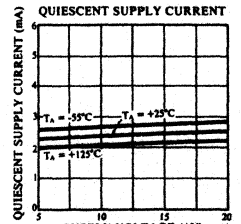
COMMON-MODE REJECTION



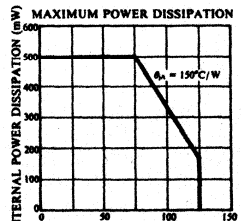
COMMON-MODE REJECTION



QUIESCENT SUPPLY CURRENT



MAXIMUM POWER DISSIPATION



APPLICATIONS INFORMATION

THERMAL RESPONSE TIME

Thermal response time is an important parameter in low drift operational amplifiers like the 3527. A low drift specification would be of little value if the amplifier took several hours to stabilize after turn-on or ambient temperature change. The TO-99 packaging is particularly well suited for devices requiring fast thermal response. Figure 1 shows the typical warm-up drift of the 3527. Note that the offset voltage has stabilized in less than 1 minute. Similar warm-up times for some low drift operational amplifiers range from 2 to 15 minutes.

Offset voltage response to thermal shock can provide some real surprises, particularly for amplifiers packaged in discrete modules. Again the 3527 TO-99 package proves superior. Figure 2 shows that the response to thermal shock settles very quickly. The 3527 quickly and smoothly assumes a new value of offset voltage as dictated by the drift specification.

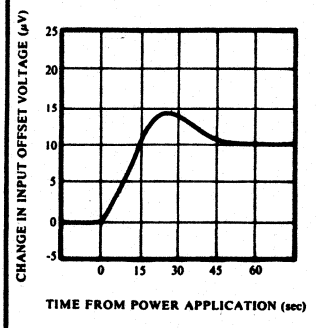


FIGURE 1. Typical Warmup Drift.

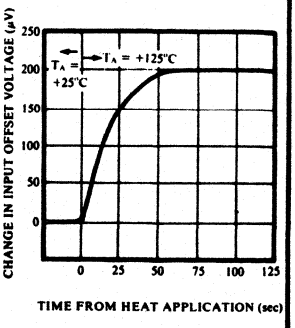


FIGURE 2. Effect of Thermal Shock on Offset Voltage.

GUARDING AND SHIELDING

The ultra-low bias current and high input impedance of the 3527 are well-suited to a number of stringent applications. However, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the 3527.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the 3527. To avoid leakage problems, it is recommended that the signal input lead of the 3527 be wired to a Teflon standoff. If the 3527 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 3 illustrates the use of the guard.

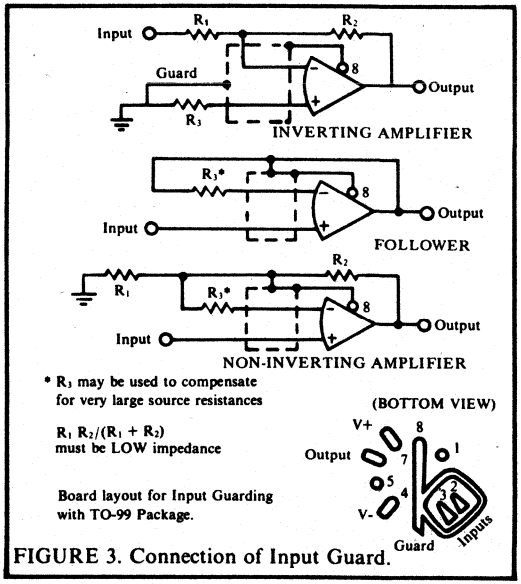


FIGURE 3. Connection of Input Guard.

OFFSET VOLTAGE ADJUSTMENT

Although the 3527 has a low initial offset voltage (250μV), some applications may require external nulling of this small offset. Figure 4 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser adjusted offset voltage temperature drift slightly. For each microvolt of offset adjusted, an additional drift of $\pm$0.002 μV/°C is induced.

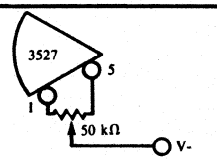
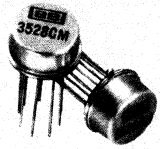


FIGURE 4. External Nulling of Offset Voltage.

BURR-BROWN

3528



Ultra Low Bias Current FET OPERATIONAL AMPLIFIER

FEATURES

- 75fA MAX INPUT BIAS CURRENT
- 250μV MAX OFFSET VOLTAGE
- 5μV/°C MAX OFFSET VOLTAGE DRIFT

APPLICATIONS

- PHOTODIODE AMPLIFIER
- PHOTOMULTIPLIER TUBE AMPLIFIER
- LOW DRIFT INTEGRATOR
- CURRENT-TO-VOLTAGE CONVERTER

DESCRIPTION

An excellent combination of specifications for applications requiring ultra low input bias currents are provided by the 3528 amplifier family. These applications include photometers, selective ion detectors, long term integrators and low-droop sample hold circuits.

The 3528 is unique in that in addition to providing bias currents as low as 75fA (3528CM) it also provides very low offset voltage drift (5μV/°C max, 3528BM) and offset voltage (250μV, 3528BM). Thus, user trimming offset voltage with an external potentiometer is usually avoided.

The output is protected from damage due to short circuits to ground or either supply and the unit is specified over the full -25°C to +85°C temperature range rather than the more limited 0°C to 70°C range.

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PDS-389

Printed in U.S.A. July, 1978

ELECTRICAL SPECIFICATIONS

At T_A = 25°C and $\pm V_{cc}$ = ±15VDC unless otherwise noted.

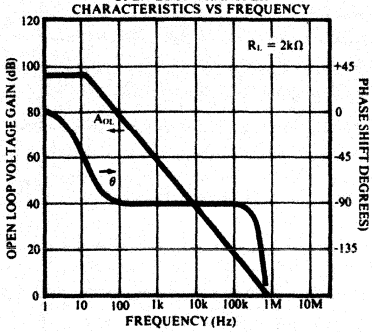
PARAMETER	CONDITIONS	3528AM MIN	3528AM TYP	3528AM MAX	3528BM MIN	3528BM TYP	3528BM MAX	3528CM MIN	3528CM TYP	3528CM MAX	UNITS
OPEN LOOP GAIN, DC											
$R_L \geq 2k$	V_o = 20V p-p	88	93		92	95		90	93		dB
$R_L \geq 10k$	V_o = 20V p-p	94	114		100	*		98	*		
RATED OUTPUT											
Voltage	R_L = 2kΩ	±10	±12		*	*		*	*		V
	R_L = 10k	±12	±13		*	*		*	*		V
Current	V_o = ±10V	±5	±10		*	*		*	*		mA
Output Resistance Open Loop	f = DC		1.5	3		*	*		*	*	kΩ
Short Circuit Current	R_L = 0Ω		19			*			*		mA
DYNAMIC RESPONSE											
Bandwidth, Unity Gain	Small Signal		0.7			*			*		MHz
Full Power Bandwidth	R_L = 2kΩ	5	11		*	*		*	*		kHz
Slew Rate	R_L = 2kΩ	0.3	0.7		*	*		*	*		V/μsec
Settling time	to 1%		30			*			*		μs
	to 0.1%		150			*			*		μs
	to 0.01%		1			*			*		ms
INPUT OFFSET VOLTAGE											
Initial Offset	T_A = 25°C		±200	±500		±100	±250		±200	±500	μV
vs Temperature	-25°C ≤ T_A ≤ +85°C		±5	±15		±2	±5		±5	±10	μV/°C
vs Supply Voltage	$\pm V_{cc}$ = 15V to 20V, to 5V		±25	±100		*	*		*	*	μV/V
vs Time			20			*			*		μV/mo
INPUT BIAS CURRENT											
Initial	T_A = 25°C			-300			-150			±75	fA
at Temperature	at T_A = 85°C		-40	-60		-20	-30		-10	-15	pA
vs Supply Voltage			1			*			*		fA/V
INPUT DIFFERENCE CURRENT											
Initial	T_A = 25°C		±80			±40			±20		fA
at Temperature	at T_A = 85°C		±8			±4			±2		pA
INPUT IMPEDANCE											
Differential			10^{13} || 0.8			*			*		Ω || pF
Common-mode			10^{15} || 1			*			*		Ω || pF
INPUT NOISE											
Voltage Noise Density	f_o = 1Hz		475			*			*		nV/√Hz
	f_o = 10Hz		120			*			*		nV/√Hz
	f_o = 100Hz		55			*			*		nV/√Hz
	f_o = 1kHz		40			*			*		nV/√Hz
	f_o = 10kHz		40			*			*		nV/√Hz
Voltage Noise	f_B = 0.3Hz to 10Hz		6			*			*		μV, p-p
	f_B = 10Hz to 10kHz		4			*			*		μV, rms
Current Noise Density	f_o = 1Hz		0.25			0.2			0.15		fA/√Hz
	f_o = 10Hz		0.25			0.2			0.15		fA/√Hz
	f_o = 100Hz		0.25			0.2			0.15		fA/√Hz
	f_o = 1kHz		0.25			0.2			0.15		fA/√Hz
Current Noise	f_B = 0.3Hz to 10Hz		7			5			4		fA, p-p
	f_B = 10Hz to 10kHz		26			20			15		fA, rms
INPUT VOLTAGE RANGE											
Common-mode Voltage Range	Linear Operation		$\pm(\lvert V_{cc}\rvert-3)$			*			*		V
Common-mode Rejection	f = DC, V_{CM} = ±10V	66	74		80	86		70	86		dB
Max. Safe Input Voltage			$\pm V_{cc}$			*			*		V
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range, derated performance		±5		±20	*		*	*		*	V
Current, quiescent			1	1.5		*	*		*	*	mA
TEMPERATURE RANGE (ambient)											
Specification		-25		+85	*		*	*		*	°C
Operating, derated performance		-55		+125	*		*	*		*	°C
Storage		-65		+150	*		*	*		*	°C

TABLE I. Electrical Specifications

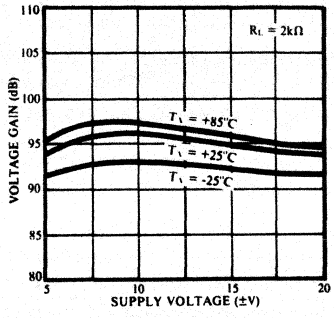
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted)

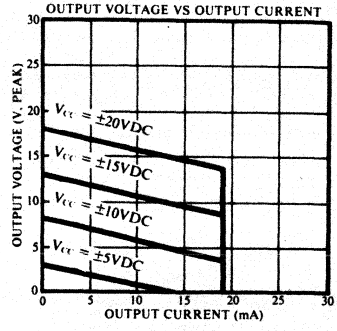
OPEN LOOP TRANSFER CHARACTERISTICS VS FREQUENCY



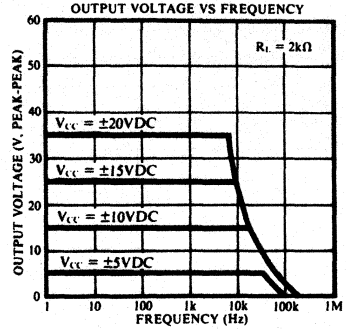
VOLTAGE GAIN VS SUPPLY VOLTAGE



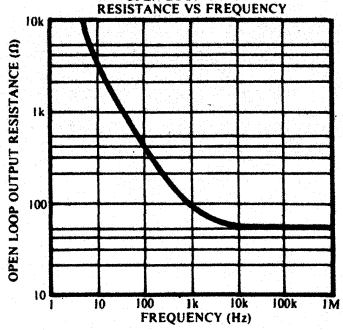
OUTPUT VOLTAGE VS OUTPUT CURRENT



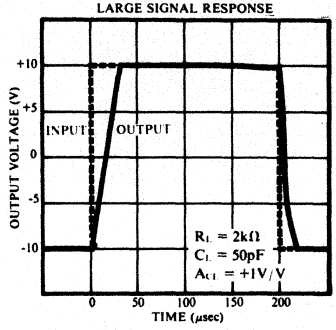
OUTPUT VOLTAGE VS FREQUENCY



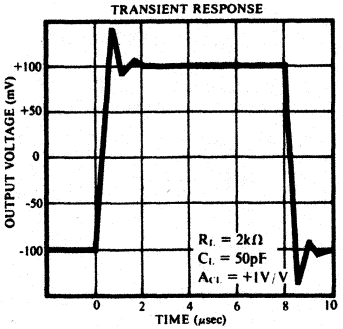
OPEN LOOP OUTPUT RESISTANCE VS FREQUENCY



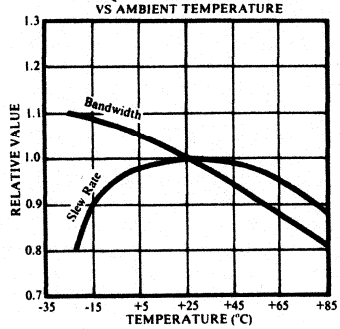
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



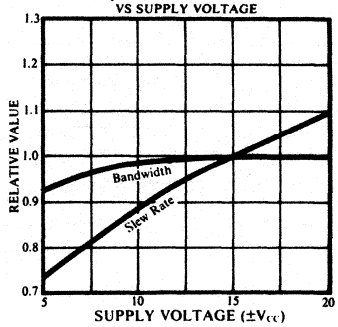
TRANSIENT RESPONSE



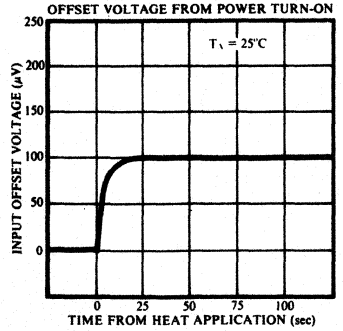
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



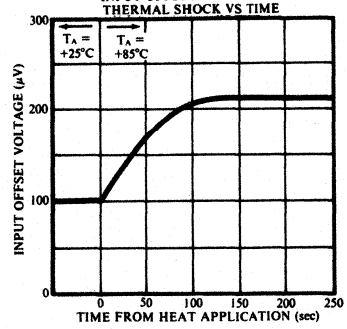
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



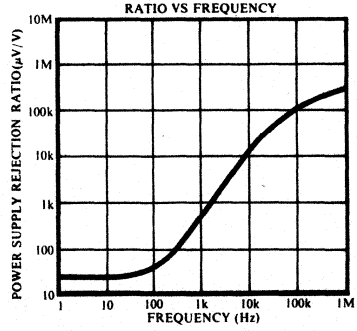
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



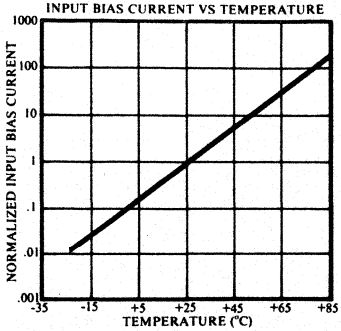
INPUT OFFSET VOLTAGE VS THERMAL SHOCK VS TIME



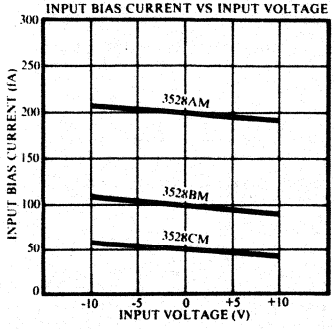
POWER SUPPLY REJECTION RATIO VS FREQUENCY



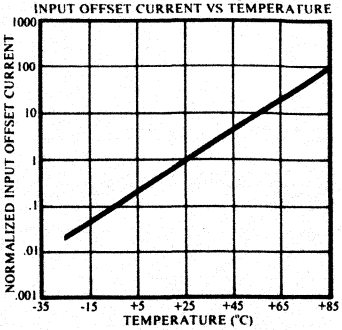
INPUT BIAS CURRENT VS TEMPERATURE



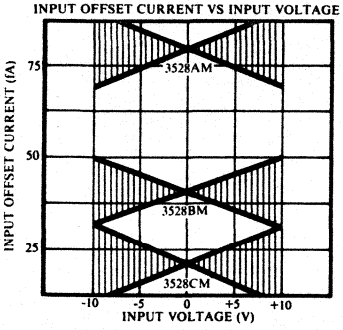
INPUT BIAS CURRENT VS INPUT VOLTAGE



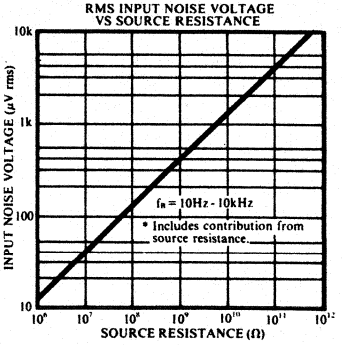
INPUT OFFSET CURRENT VS TEMPERATURE



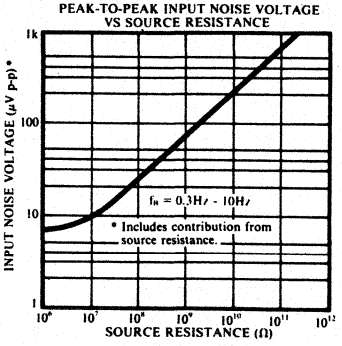
INPUT OFFSET CURRENT VS INPUT VOLTAGE



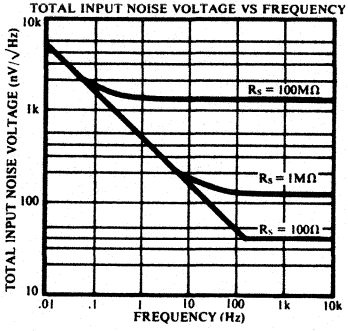
RMS INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



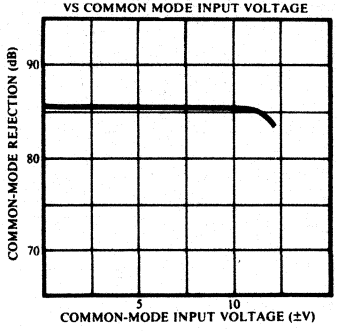
PEAK-TO-PEAK INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



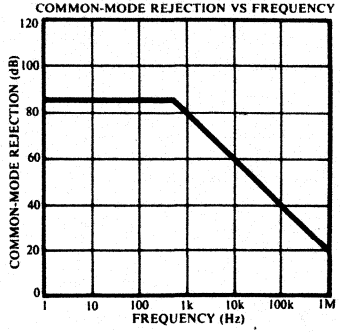
TOTAL INPUT NOISE VOLTAGE VS FREQUENCY



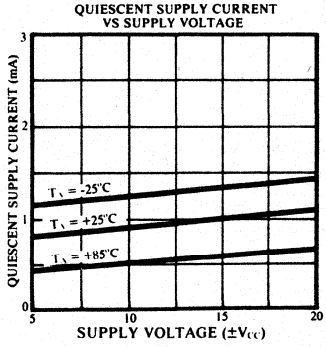
COMMON-MODE REJECTION VS COMMON MODE INPUT VOLTAGE



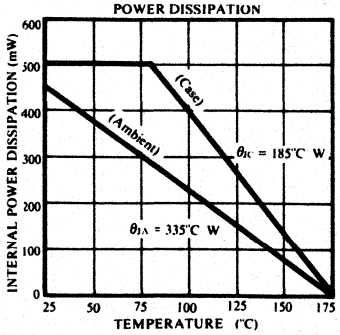
COMMON-MODE REJECTION VS FREQUENCY



QUIESCENT SUPPLY CURRENT VS SUPPLY VOLTAGE



POWER DISSIPATION



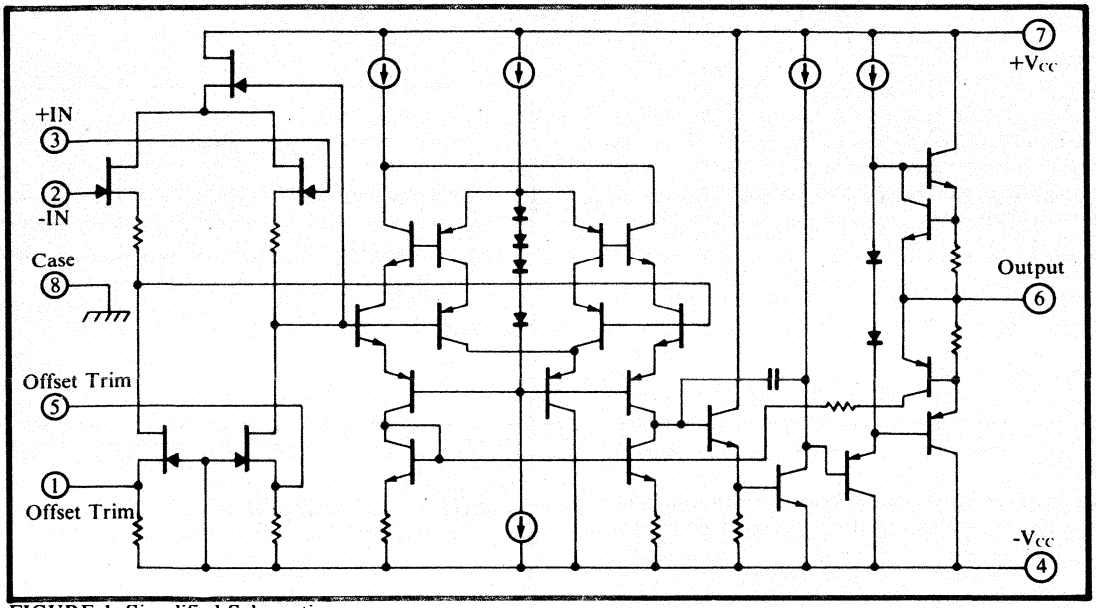


FIGURE 1. Simplified Schematic

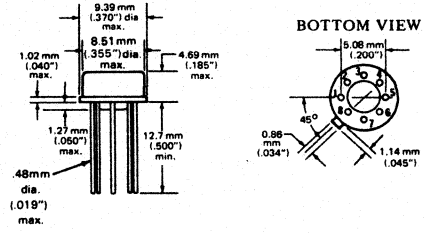
ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation (note 1)	500mW
Differential Input Voltage (note 2)	±40VDC
Input Voltage Range (note 2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	300°C
Output Short - Circuit Duration (note 3)	Continuous
Junction Temperature	T_j = +175°C

NOTES:

1. Package must be derated based on a junction to ambient thermal resistance of 335°C/W.
2. For supply voltages less than ±20VDC, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +115°C case temperature or +75°C. ambient temperature.

TO-99 PACKAGE



Dimensions in inches are in parentheses. Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883

FIGURE 2. Mechanical Specifications

CONNECTION DIAGRAM

TOP VIEW

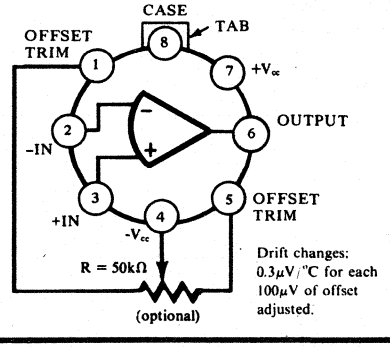


FIGURE 3. Pin Connections

APPLICATION CONSIDERATIONS

The ultra-low bias current and high input impedance of the 3528 are well suited to a number of challenging applications. In order to fully benefit from the outstanding specifications of this unit careful layout, shielding and guarding is required. Careless signal wiring or printed circuit board layout can easily degrade circuit performance several orders of magnitude below the capability of the 3528.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. The metal case of the 3528 is connected to pin 8 and is not connected to any internal amplifier circuitry. Thus it is possible to use the case as a shield to reduce noise pick-up.

Leakage currents across printed circuit boards can easily exceed the bias current of the 3528. To avoid leakage problems, it is recommended that a Teflon IC socket be used or that at least the signal input lead of the 3528 be wired to a Teflon standoff. If this is not done and instead the 3528 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 4). The amplifier case, pin 8, should also be connected to the guard. This insures that the entire amplifier circuitry is fully surrounded by the guard potential. This minimizes the voltage placed across any leakage paths and thus reduces leakage currents.

Figures 5, 6, and 7 show typical applications using the guard and case shielding.

Cleanliness is also a prime concern in ultra-low bias current circuits. It is recommended that after installation is complete the assembly be washed with a low residue solvent such as TMC Freon followed by rinsing with deionized water. The use of some form of high dielectric conformal coating such as a good two part urathane should be considered if the assembly will be used in air environment which could deposit contaminants on the low current circuitry.

Board layout for Input Guarding with Guarded TO-99 Package.

FIGURE 4. Connection of Case Guard and Input Guard.

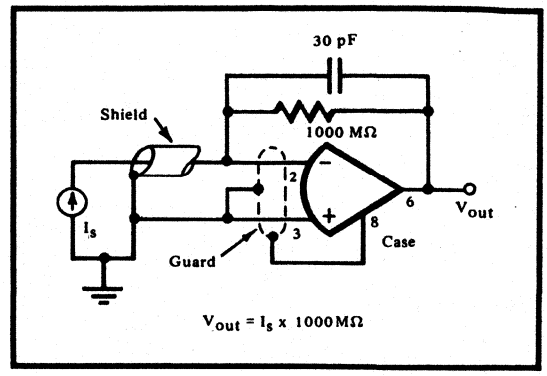


FIGURE 5.Ultra Low Current to Voltage Converter.

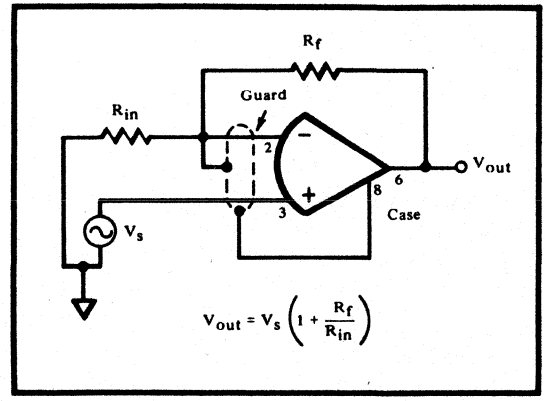


FIGURE 6. Ultra High Input Impedance Noninverting Circuit.

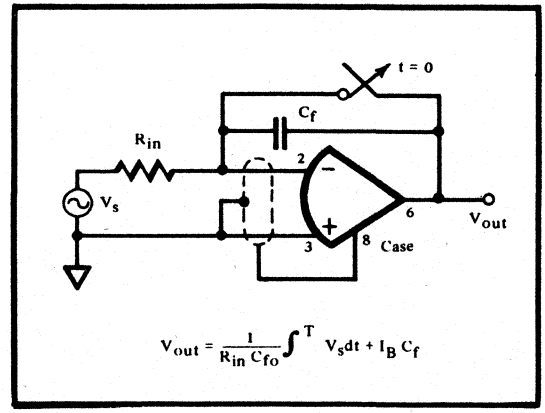
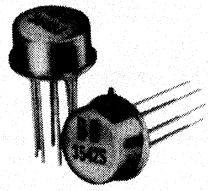


FIGURE 7. Ultra Low Drift Integrator.

BURR-BROWN



3542 SERIES

FET Input OPERATIONAL AMPLIFIERS

FEATURES

- HIGH INPUT IMPEDANCE, $10^{11}\ \Omega$
- LOW NOISE, 2μV, p-p
- HIGH CMR, 80dB
- WIDE SUPPLY RANGE, ±5VDC to ±20VDC
- INTERNAL FREQUENCY COMPENSATION
- INDUSTRIAL AND MILITARY VERSIONS

DESCRIPTION

These FET amplifiers offer excellent input characteristics at low cost through the use of monolithic chips and thin film hybrid technology. Unlike other FET op amps of comparable cost, they have low input noise and moderate voltage drift. Thus they are suitable for a number of applications where previous hybrid or monolithic FET op amps were, at best marginal.

In addition, the 3542 series are extremely stable amplifiers having internal frequency compensation. Other built-in features are output short-circuit protection, input protection to supply voltage, and operation over a wide range of supply voltages.

The pin configuration of the 3542 is conventional (same as 741 type amplifiers) except for pin 8, which is connected to the case. In the usual IC operational amplifier, the case is connected to the negative supply voltage. However, in FET amplifiers it is often desirable to connect the case to a low impedance "guard" potential. This aids in eliminating noise "pickup" in high impedance circuits and preserves the low input currents of the amplifier.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-293D

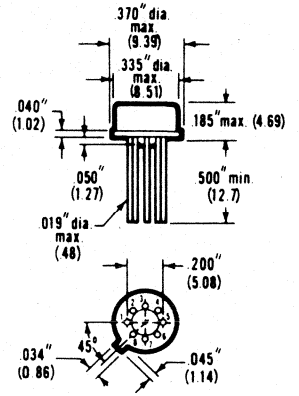
Printed in U.S.A. July, 1978

SPECIFICATIONS

Specifications typical at 25°C and ±15 Vdc Power Supply unless otherwise noted.

MODEL	3542J	3542S
OPEN LOOP GAIN, dc rated load, min.	88 dB	
RATED OUTPUT Voltage, min. Current, min. Output Impedance	±10V ±10 mA 75 Ω	
FREQUENCY RESPONSE Unity Gain, Open Loop Full Power Response Slew Rate	1 MHz 8 kHz 0.5 V/μsec	
INPUT OFFSET VOLTAGE Initial Offset, 25°C, max. vs. Temp (0° to 70°C) vs. Supply Voltage vs. Time	±20 mV ±10μV/°C, typ; ±50μV/°C, max ±50μV/V typ; ±150μV/V max ±100 μV/mo	
INPUT BIAS CURRENT Initial bias, 25°C (doubles every +10°C) vs. Supply Voltage	-10 typ, -25 max. pA 1 pA/V	
INPUT DIFFERENCE CURRENT Initial difference, 25°C	±2 pA	
INPUT IMPEDANCE Differential Common Mode	10^{11} Ω 10^{11} Ω	
INPUT NOISE Voltage, .01 Hz - 10 Hz, p-p 10 Hz - 1 kHz, rms Current, .01 Hz - 10 Hz, p-p 10 Hz - 1 kHz, rms	2 μV 3 μV 0.3 pA 0.6 pA	
INPUT VOLTAGE RANGE Common Mode Voltage Common Mode Rejection Max. Safe Input Voltage	±($\|V_S\|$ -5 V) 74dB min, 80dB typ $\pm V_S$	
POWER SUPPLY Rated Voltage Voltage Range, derated Current, quiescent	±15 VDC ±5 to ±20 VDC ±4 mA	
TEMPERATURE RANGE Specification Operating Storage	0° to +70°C -25° to +85°C -65° to +150°C	-55° to +125°C -55° to +125°C

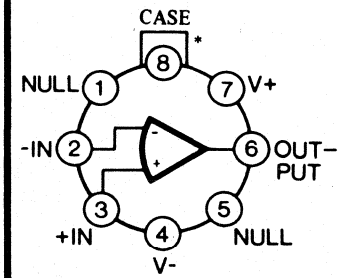
TO-99 PACKAGE



(BOTTOM VIEW)

CONNECTION DIAGRAM

(TOP VIEW)

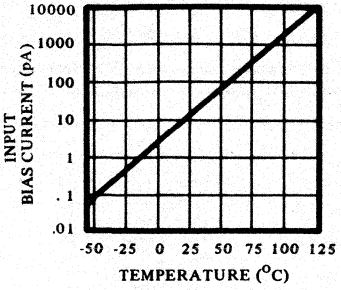


*Pin 8 is connected to case

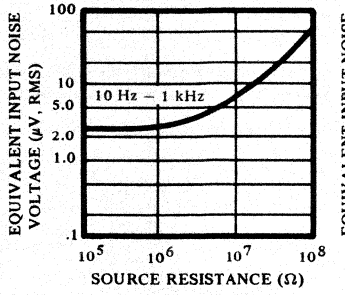
TYPICAL PERFORMANCE CURVES

(@ +25°C and ±15 Vdc unless otherwise specified)

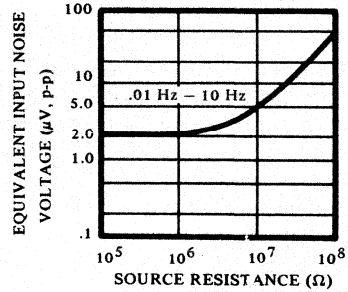
NORMALIZED INPUT BIAS CURRENT vs. TEMPERATURE



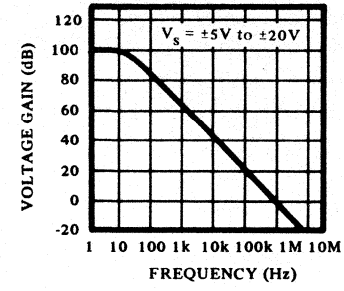
RMS INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



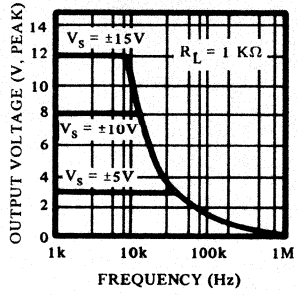
P-P INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



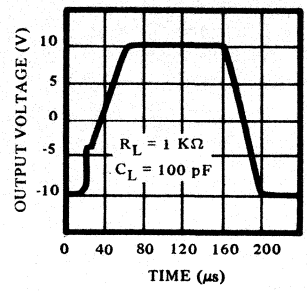
OPEN LOOP FREQUENCY RESPONSE



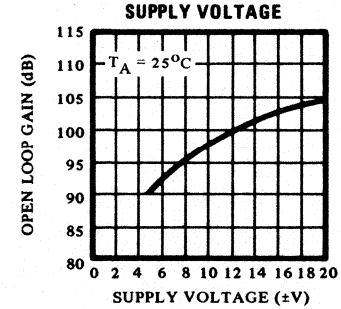
OUTPUT VOLTAGE vs. FREQUENCY



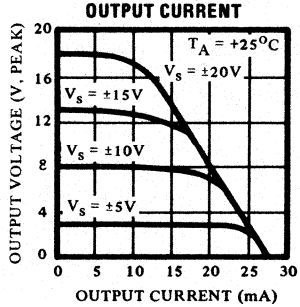
VOLTAGE FOLLOWER STEP RESPONSE



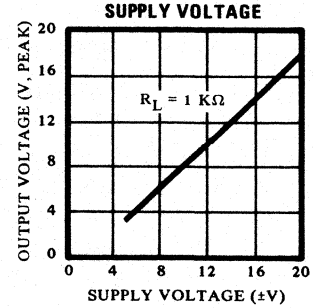
VOLTAGE GAIN vs. SUPPLY VOLTAGE



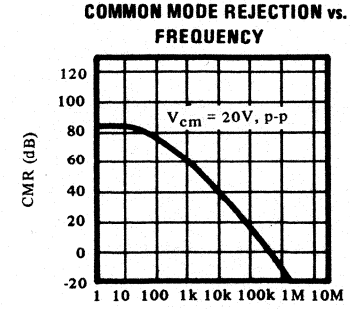
OUTPUT VOLTAGE vs. OUTPUT CURRENT



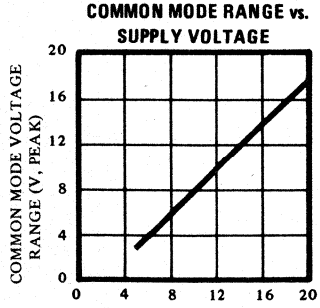
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



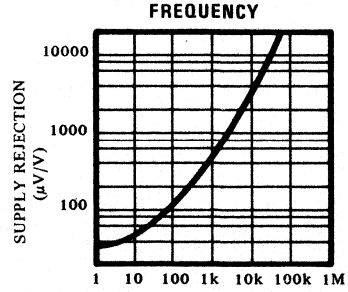
COMMON MODE REJECTION vs. FREQUENCY



COMMON MODE RANGE vs. SUPPLY VOLTAGE



POWER SUPPLY REJECTION vs. FREQUENCY



WIRING CONSIDERATIONS

SHIELDING AND GUARDING

The low bias current and high input impedance of the 3542 are well-suited to a number of stringent applications. However, careless signal wiring or printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the 3542.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the 3542. To avoid leakage problems, it is recommended that the signal input lead of the 3542 be wired to a Teflon standoff. If the 3542 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 1 illustrates the use of the guard for both inverting and non-inverting circuits.

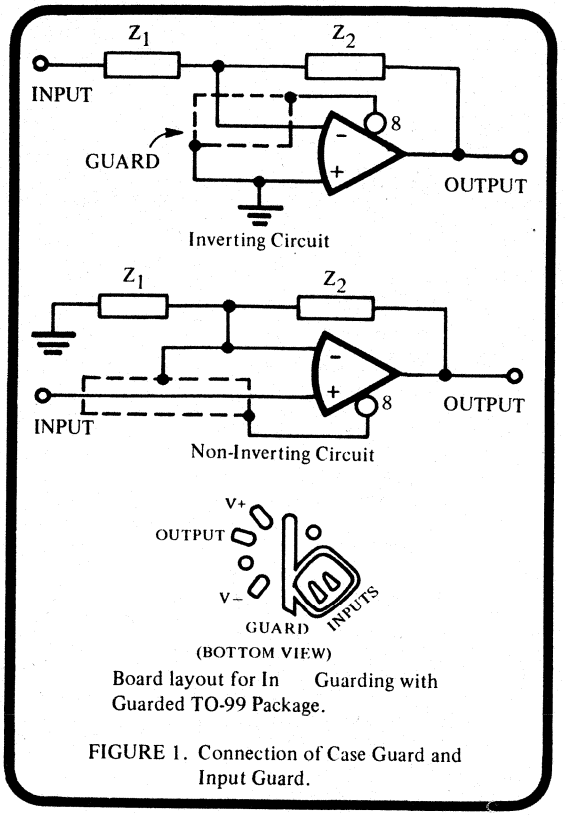


FIGURE 1. Connection of Case Guard and Input Guard.

OFFSET VOLTAGE ADJUSTMENT

Although the 3542 has a moderately low initial offset voltage (5 mV, typ) compatible with it's moderate voltage drift, some applications may require external nulling of this small offset. Figure 2 shows the recommended circuit for adjustment of the offset voltage.

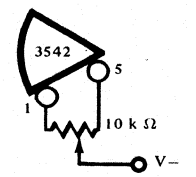
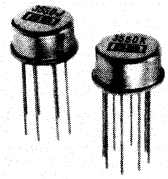


FIGURE 2. External Nulling of Offset Voltage.

BURR-BROWN



3550 SERIES

Fast-Settling FET OPERATIONAL AMPLIFIERS

FEATURES

- SETTLING TIME (0.01%), 600ns, max
- TRUE DIFFERENTIAL INPUT
- SLEW RATE, 100V/μs, min
- FULL POWER, 1.5MHz, min
- INPUT IMPEDANCE, $10^{11}\Omega$
- INTERNALLY COMPENSATED
- STABLE OPERATION, 1000pF, typ

DESCRIPTION

The 3550 is specifically designed for fast transient applications such as D/A and A/D conversion, sample/hold, multiplexer buffering and pulse amplification where the primary amplifier requirements are fast settling, good accuracy, and high input impedance.

Because the 3550 is internally compensated, elaborate compensation schemes requiring external components are not necessary. The smooth 6dB/octave rolloff of open-loop gain and the low output impedance provides the excellent step response and smooth settling without sacrificing frequency stability (no oscillations even with 1000pF of capacitive load)! A 10 to 1 improvement in settling time with large capacitive loads can be obtained with the addition of a single capacitor.

Unlike many wideband and fast settling amplifiers the 3550 has a true differential input. This means it can provide its excellent transient performance in the inverting, non-inverting, current to voltage, and difference configurations.

The 3550J and S have identical specifications except for temperature range: The 3550J is specified for 0°C to +70°C and the 3550S is specified for -55°C to +125°C. The 3550K has improved dynamic specifications and is specified over the 0°C to +70°C temperature range.

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PDS-302

Printed in U.S.A. July, 1978

SPECIFICATIONS

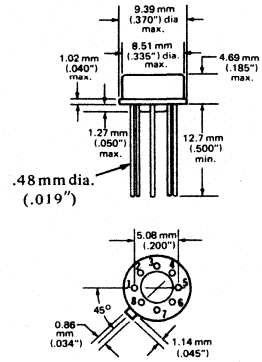
ELECTRICAL

Specifications typical at 25°C and ±15 Vdc Power Supply unless otherwise noted.

MODELS	3550J	3550K	3550S
OPEN LOOP GAIN, dc			
no load		100 dB	
1 kΩ, load min		88 dB	
RATED OUTPUT			
Voltage, min		±10 V	
Current, min		±10 mA	
Open loop Output Resistance		100 Ω @ 1 MHz	
DYNAMIC RESPONSE			
Bandwidth (0 dB, small signal)	10 MHz	20 MHz	10 MHz
Full Power Response, min	1.0 MHz	1.5 MHz	1.0 MHz
Slew Rate, min	65 V/μs	100 V/μsec	65 V/μs
Settling Time (0.01%), max	1 μs	0.6 μs	1 μs
INPUT OFFSET VOLTAGE			
Initial Offset, 25°C, max		±1 mV	
vs. Temp		±50 μV/°C	
vs. Supply Voltage		±500 μV/V	
vs. Time		±100 μV/mo	
INPUT BIAS CURRENT			
Initial Bias, 25°C, max		-100 pA (after full warm-up)	
vs. Temperature		doubles every 10°C	
vs. Supply Voltage		±1 pA/V	
INPUT DIFFERENCE CURRENT			
Initial Difference, 25°C		±10 pA	
INPUT IMPEDANCE			
Differential		10^{11} Ω ‖ 3 pF	
Common Mode		10^{11} Ω ‖ 3 pF	
INPUT NOISE			
Voltage, .01 Hz - 10 Hz, p-p		20 μV	
10 Hz - 10 kHz, rms		4 μV	
Current, .01 Hz - 10 Hz, p-p		0.2 pA	
10 Hz - 10 kHz, rms		1.5 pA	
INPUT VOLTAGE RANGE			
Common Mode Voltage		±(|V_S| -5) V	
Common Mode Rejection		70 dB @ +5 V, -10V	
Max. Safe Input Voltage		±Supply	
POWER SUPPLY			
Rated Voltage		±15 Vdc	
Voltage Range, derated		±5 to ±20 Vdc	
Current, quiescent	(1)	11 mA	
TEMPERATURE RANGE			
Specification		0° to +70°C	-55° to +125°C
Operating		-55°C to +125°C	-55° to +125°C
Storage		-65° to +150°C	

(1) The use of a finned heatsink is recommended.

MECHANICAL TO-99

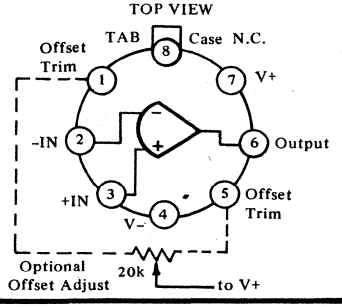


BOTTOM VIEW

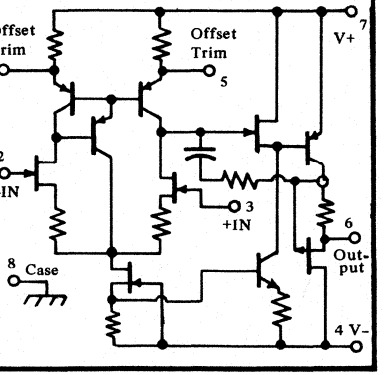
Dimensions in inches are in parentheses.

Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]

CONNECTION DIAGRAM



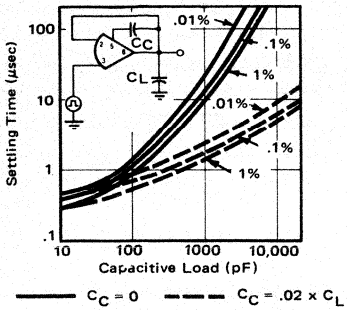
Simplified Schematic



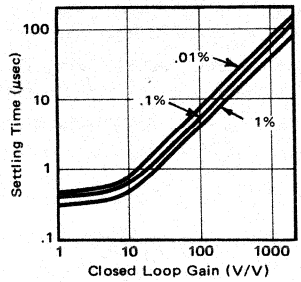
TYPICAL PERFORMANCE CURVES

$T_A = 25^oC$ $V_S = \pm 15$ Vdc unless otherwise indicated.

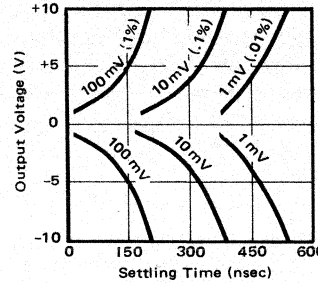
SETTLING TIME vs. CAPACITIVE LOAD



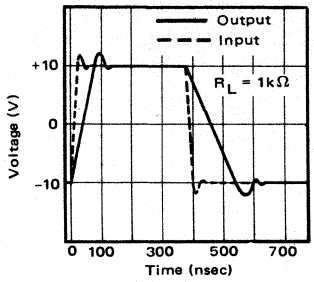
SETTLING TIME vs. CLOSED LOOP GAIN



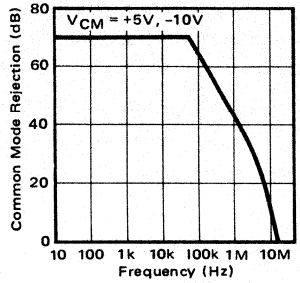
SETTLING TIME vs. OUTPUT VOLTAGE CHANGE



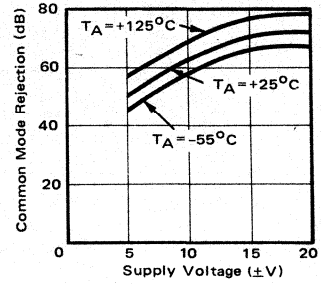
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



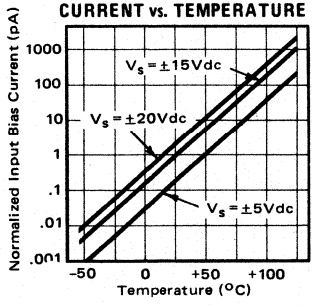
COMMON MODE REJECTION vs. FREQUENCY



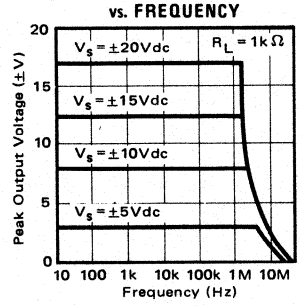
COMMON MODE REJECTION vs. SUPPLY VOLTAGE



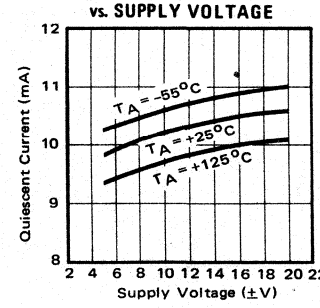
NORMALIZED INPUT BIAS CURRENT vs. TEMPERATURE



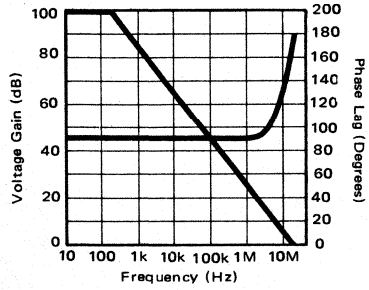
OUTPUT VOLTAGE vs. FREQUENCY



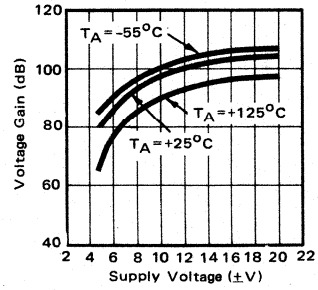
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



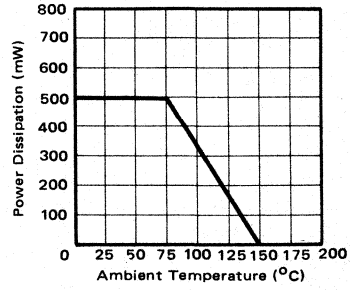
OPEN LOOP RESPONSE



OPEN LOOP GAIN vs. SUPPLY VOLTAGE



MAXIMUM POWER DISSIPATION



APPLICATIONS

SETTLING TIME

Settling time of an amplifier is defined (see Figure 1) as the total time required, after an input step signal, for the output to "settle" within a specified error band around the final value. This error band is expressed as a percentage of the magnitude of the step transition. A recommended test circuit for settling time is shown in Figure 2. The output error signal appears, attenuated by a factor of two, at point A and may be observed at this point with the aid of an oscilloscope. The diodes act as limiters to prevent overloading the oscilloscope during the fast leading edge of the input signal. All resistors should be 2 kΩ or less to eliminate degradation of performance due to stray capacitance. A typical measurement desired is the settling time to .01% for a 10 volt step input. This is the time required for the signal at point A to decrease to 0.5 mV or less and remain below this level.

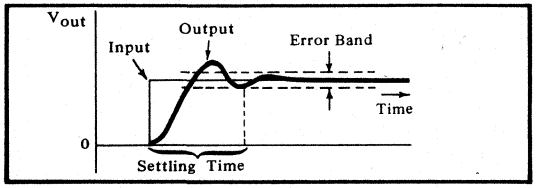


FIGURE 1. Concept of Settling Time.

Settling time for noninverting circuits can also be measured but requires the use of ultra-fast differential amplifier test fixtures. For the 3550 settling time is equal for inverting or noninverting circuits of equal gain.

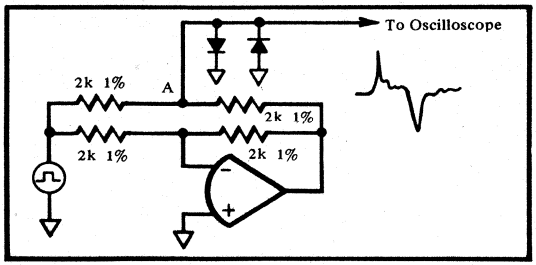


FIGURE 2. Settling Time Test Circuit.

Because settling time is affected by bandwidth which in turn is dependent upon closed-loop gain, the settling time of any operational amplifier will be a function of closed loop gain. Settling time vs. gain curves on page 1-85 illustrate this effect for the 3550 at several levels of settling accuracy.

The 3550 is remarkably tolerant of load capacitance because of its stable, 6 dB/octave gain rolloff and low output impedance. Settling time vs. load capacitance curves show this characteristic for the unity-gain configuration. For larger values of load capacitance the compensation technique of Figure 3 may be used to optimize the response. The slight negative feedback provided by C_C tends to reduce any ringing at the top of the output voltage waveform without significantly affecting the slew rate. See the settling time vs. load capacitance curves for typical improvements in settling time.

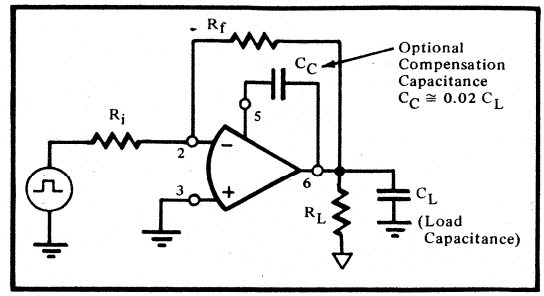


FIGURE 3. Compensation for Load Capacitance.

WIRING RECOMMENDATIONS

In order to fully realize the high frequency performance capabilities of the 3550, proper attention must be given to layout, component selection and grounding. All leads associated with the input and feedback elements should be as short as possible and all connections should be made as close to the amplifier terminals as possible. Input and feedback resistors should be made as small as possible consistent with other circuit constraints. Capacitance from the output to noninverting input can cause high frequency oscillations, particularly in high gain circuits operating from large source impedances. Careful layout of wiring or PC board patterns is the only satisfactory way of preventing such problems.

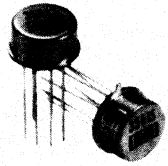
In order to prevent high frequency oscillations due to lead inductance the power supply leads should be bypassed. This should be done by connecting a 10 μf tantalum capacitor in parallel with a 0.001 μf ceramic capacitor from pins 7 and 4 to the power supply common.

INPUT AND OUTPUT VOLTAGE RANGE

Although the 3550 is specified for best operation on power supply voltage of ±15 Vdc, it will operate with minor performance changes over a power supply voltage range of ±5VDC to ±20VDC. Many of the curves on page 1-85 show performance of the 3550 when operated from supplies other than ±15 Vdc.

BURR-BROWN

3551 SERIES



Wideband and Fast-Settling FET OPERATIONAL AMPLIFIERS

FEATURES

- **REDUCES WIDEBAND ERRORS**
  - **50MHz Gain-bandwidth product (ACL ≥10)**
  - **250V/μs slew rate (Cf = 0)**
- **VERSATILE**
  - **Single compensation capacitor allows optimum response**
  - **True differential input**
- **PRESERVES DC ACCURACY**
  - **Bias current, 100pA, max**
  - **Laser-trimmed offset voltage**

DESCRIPTION

The 3551 is designed to offer the user versatility in wideband steady state and fast transient applications. The use of a single external compensation capacitor allows the user to optimize frequency response for maximum bandwidth for a variety of closed loop-gains and capacitive loads. The amplifier is stable at closed-loop gains of greater than 10V/V. with no external compensation and may be stablized at all gains with the single 10pF compensation capacitor.

In addition to the excellent dynamic response characteristics, the 3551 also has good DC properties. The use of a monolithic FET input stage gives the 3551 very low input bias and offset currents. This is in contrast to the high input currents usually associated with fast amplifiers having bipolar input stages. Also, the input offset voltage and offset voltage drift are low as a result of Burr-Brown's laser-trimming techniques.

Unlike many wideband and fast settling amplifiers, the 3551 has a true differential input. This means it can provide its excellent wideband response in the inverting, noninverting, current-to-voltage and difference configurations.

The 3551 is an excellent choice for applications such as fast D/A and A/D converters, high speed comparators and fast sampling circuits, to name just a few.

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PDS-301A

Printed in U.S.A. July, 1978

SPECIFICATIONS

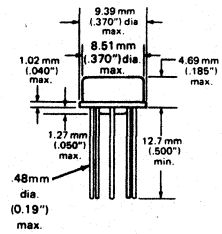
ELECTRICAL

Specifications typical at 25°C and ±15 VDC Power Supply unless otherwise noted.

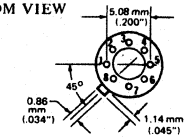
MODELS	3551J	3551S
OPEN LOOP GAIN, DC		
No load	100 dB	
1 kΩ, load min	88 dB	
RATED OUTPUT		
Voltage, min	±10 V	
Current, min	±10 mA	
Open loop Output Resistance	100 Ω @ 1 MHz	
DYNAMIC RESPONSE		
Gain-Bandwidth Product		
Gain = 1000	50 MHz	
Gain = 10	50 MHz	
Slew Rate (C_f = 0)	250 V/μs	
INPUT OFFSET VOLTAGE		
Initial Offset, 25°C, max	±1 mV	
vs. Temp	±50 μV/°C	
vs. Supply Voltage	±500 μV/V	
vs. Time	±100 μV/mo	
INPUT BIAS CURRENT		
Initial Bias, 25°C, max	-100 pA (after full warm-up)	
vs. Temperature	doubles every 10°C	
vs. Supply Voltage	±1 pA/V	
INPUT DIFFERENCE CURRENT		
Initial Difference, 25°C	±10 pA	
INPUT IMPEDANCE		
Differential	10^{11} Ω ‖ 3 pF	
Common Mode	10^{11} Ω ‖ 3 pF	
INPUT NOISE		
Voltage, .01 Hz - 10 Hz, p-p	20 μV	
10 Hz - 10 kHz, rms	4 μV	
Current, .01 Hz - 10 Hz, p-p	0.2 pA	
10 Hz - 10 kHz, rms	1.5 pA	
INPUT VOLTAGE RANGE		
Common-Mode Voltage	± ($\|V_{CC}\|$-5) V	
Common-Mode Rejection	70 dB @ +5 V, -10 V	
Max. Safe Input Voltage	± Supply	
POWER SUPPLY		
Rated Voltage	± 15 VDC	
Voltage Range, derated	±5 to ±20 VDC	
Current, quiescent (1)	11 mA	
TEMPERATURE RANGE		
Specification	0°C to +70°C	-55°C to +125°C
Operating	-55°C to +125°C	-55°C to +125°C
Storage	-65°C to +150°C	

(1) The use of a finned heatsink is recommended.

MECHANICAL TO-99

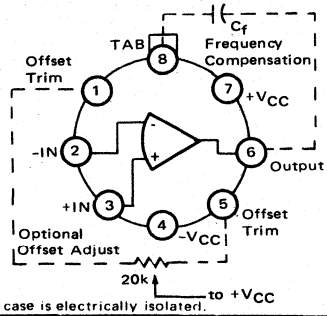


BOTTOM VIEW



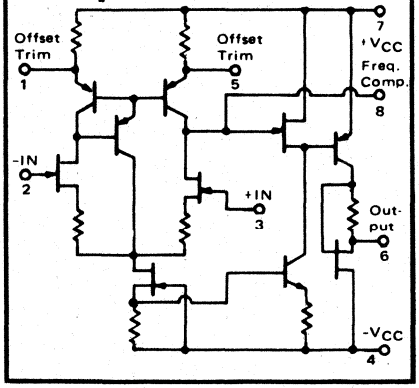
Dimensions in inches are in parentheses. Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

CONNECTION DIAGRAM



The case is electrically isolated.

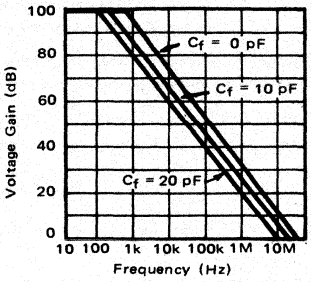
Simplified Schematic



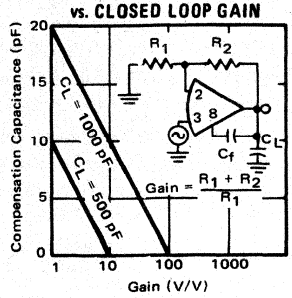
TYPICAL PERFORMANCE CURVES

T_A = 25°C V_s = ±15 VDC unless otherwise indicated.

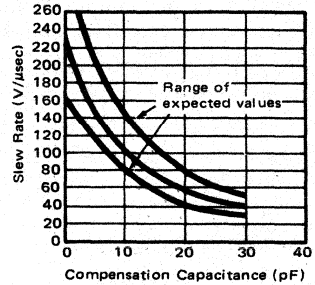
OPEN LOOP RESPONSE



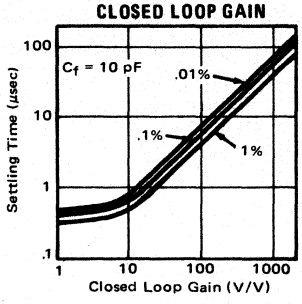
RECOMMENDED VALUES OF FREQUENCY COMPENSATION CAPACITANCE vs. CLOSED LOOP GAIN



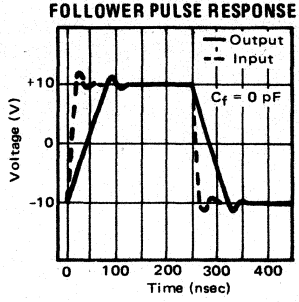
SLEW RATE vs. COMPENSATION CAPACITANCE



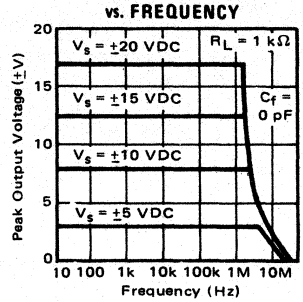
SETTLING TIME vs. CLOSED LOOP GAIN



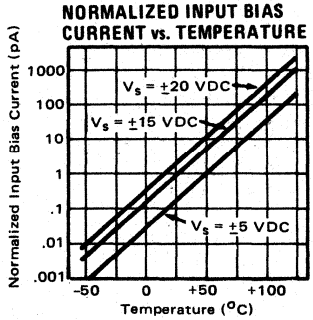
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



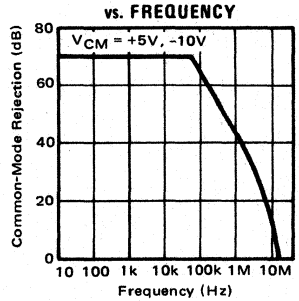
OUTPUT VOLTAGE vs. FREQUENCY



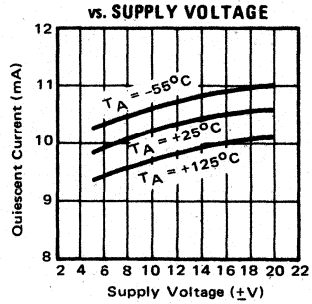
NORMALIZED INPUT BIAS CURRENT vs. TEMPERATURE



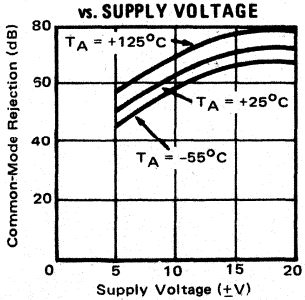
COMMON-MODE REJECTION vs. FREQUENCY



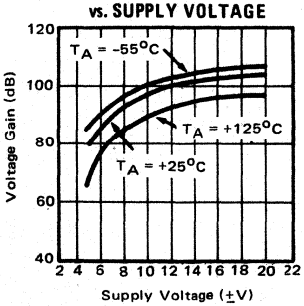
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



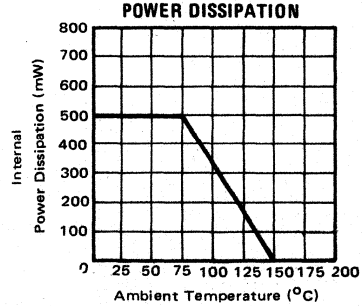
COMMON-MODE REJECTION vs. SUPPLY VOLTAGE



OPEN LOOP GAIN vs. SUPPLY VOLTAGE



MAXIMUM POWER DISSIPATION



APPLICATIONS

WIRING RECOMMENDATIONS

In order to fully realize the high frequency performance capabilities of the 3551, proper attention must be given to layout, component selection and grounding. All leads associated with the input and feedback elements should be as short as possible and all connections should be made as close to the amplifier terminals as possible. Input and feedback resistors should be made as small as possible consistent with other circuit constraints. Capacitance from the output to non-inverting input can cause high frequency oscillations, particularly in high gain circuits operating from large source impedances. Careful layout of wiring or PC board patterns is the only satisfactory way of preventing such problems.

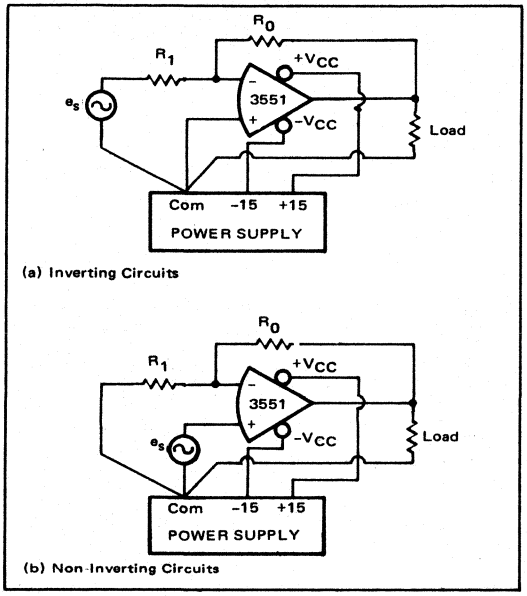


FIGURE 1. Proper Grounding Methods

In order to prevent high frequency oscillations due to lead inductance the power supply leads should be bypassed. This should be done by connecting a 10 μf tantalum capacitor in parallel with a 0.001 μf ceramic capacitor from pins 7 and 4 to the power supply common.

INPUT AND OUTPUT VOLTAGE RANGE

Although the 3551 is specified for best operation on power supply voltage of ±15 VDC, it will operate with minor performance changes over a power supply voltage range of ±5 VDC to ±20 VDC. Many of the performance curves show performance of the 3551 when operated from supplies other than ±15 VDC.

INPUT/OUTPUT PROTECTION

All of the amplifiers listed in the specification table are designed to withstand input voltages as high as the supply voltage, without damage to the amplifier. Thus, inputs may be subjected to either supply voltage, in any combination, without damage.

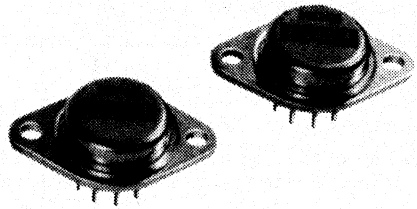
Output stages are internally current limited and will withstand short-circuit-to-ground conditions. However, application of nonzero potential to the output pin may cause permanent damage and should be prevented by the proper precautions.

SETTLING TIME

Settling time of an amplifier is defined as the total time required, after an input step signal, for the output to "settle" within a specified error band around the final value. This error band is expressed as a percentage of the magnitude of the step transition.

Because settling time is affected by bandwidth which in turn is dependent upon closed loop gain, the settling time of any operational amplifier will be a function of closed loop gain. Settling time vs. gain curves illustrate this effect for the 3551 at several levels of settling accuracy.

BURR-BROWN



3553

Wideband - Fast-Slewing BUFFER AMPLIFIER

FEATURES

- GAIN = .99V/V
- OUTPUT CURRENT, ±200mA
- BANDWIDTH, 300MHz
- SLEW RATE, 2000V/μsec
- ELECTRICALLY ISOLATED CASE
- EXTENDS OP AMP DRIVING CAPABILITY WHILE PRESERVING BANDWIDTH & SETTLING TIME

DESCRIPTION

The 3553 is a unity-gain amplifier designed to be used either as a signal buffer, or as the power output stage for an operational amplifier. Because of its wideband response (300MHz, -3dB bandwidth) and fast slewing capability (2000V/μsec) the 3553 is capable of following very fast signals. When used inside the feedback loop of an operational amplifier, these high speed characteristics are essential in order to preserve the performance and stability of the feedback amplifier circuit.

With its ±200mA of output current capability, the 3553 is capable of driving a signal of ±10V into a 50Ω load. This power capability, coupled with its extremely high speed and wide bandwidth, makes the 3553 ideally suited for line driving applications where fast pulses or wideband signals are involved.

In addition to its fast/wideband characteristics and high output current, the 3553 has low input offset voltage and drift. This adds to its versatility, particularly in stand-alone buffer amplifier applications.

The 3553 is packaged in a reliable hermetically sealed TO-3 package for environmental ruggedness. The metal case is completely electrically isolated. This simplifies mounting and reduces cost since the need for insulating spacers and bushings is eliminated.

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SPECIFICATIONS

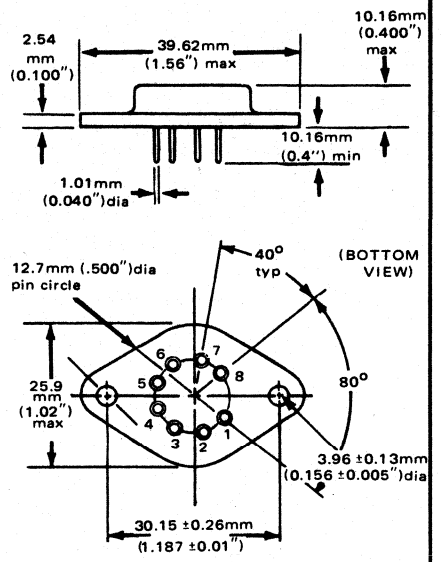
Specifications are typical at +25°C Case Temperature and ± 15 VDC power supply unless otherwise noted.

ELECTRICAL

MODEL	3553AM
GAIN, DC	
No Load	0.98 V/V
50 Ω Load, min	0.92 V/V
RATED OUTPUT	
Voltage, min	±10 V
Current, min	±200 mA
Output Resistance	1 Ω
DYNAMIC RESPONSE	
Slew Rate, min	2000 V/μsec
Full Power Bandwidth, min	32 MHz
Small Signal -3dB Bandwidth	300 MHz
Settling Time to 1%	7.2 nsec
to .01%	14.5 nsec
INPUT PARAMETERS	
Input Voltage, linear range	±10 V
Input Voltage, absolute, max	±Supply Voltage
Input Impedance	10^{11} Ω
Input Bias Current @ +25°C (doubles/+10°C)	-200 pA
OUTPUT OFFSET VOLTAGE	
Initial Offset @ +25°C, max	±50 mV
vs. Temperature (average) -25°C to +85°C	±300 μV/°C
POWER SUPPLY	
Rated Voltage	±15 VDC
Voltage Range, derated	±5 VDC to ±20 VDC
Current, Quiescent, max	±80 mA
typ	±50 mA
TEMPERATURE RANGE (Case)	
Specification	-25°C to +85°C
Operation (derate above +120°C Case)	-55°C to +125°C
Storage	-65°C to +150°C
θ_{JC} Thermal Resistance, junction to case	6°C/W
θ_{JA} Thermal Resistance, junction to ambient	33°C/W

MECHANICAL

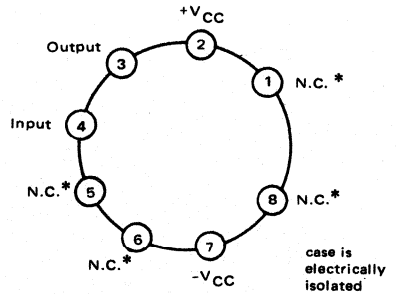
M PACKAGE (TO-3)



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]

CONNECTION DIAGRAM

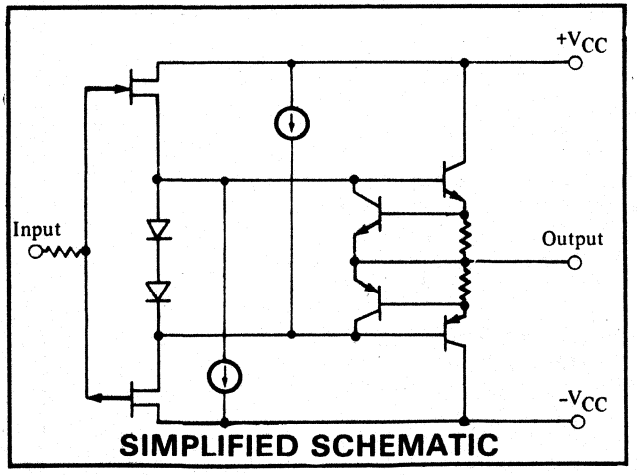
(TOP VIEW)



*No internal connection

CONNECTOR: 0803MC

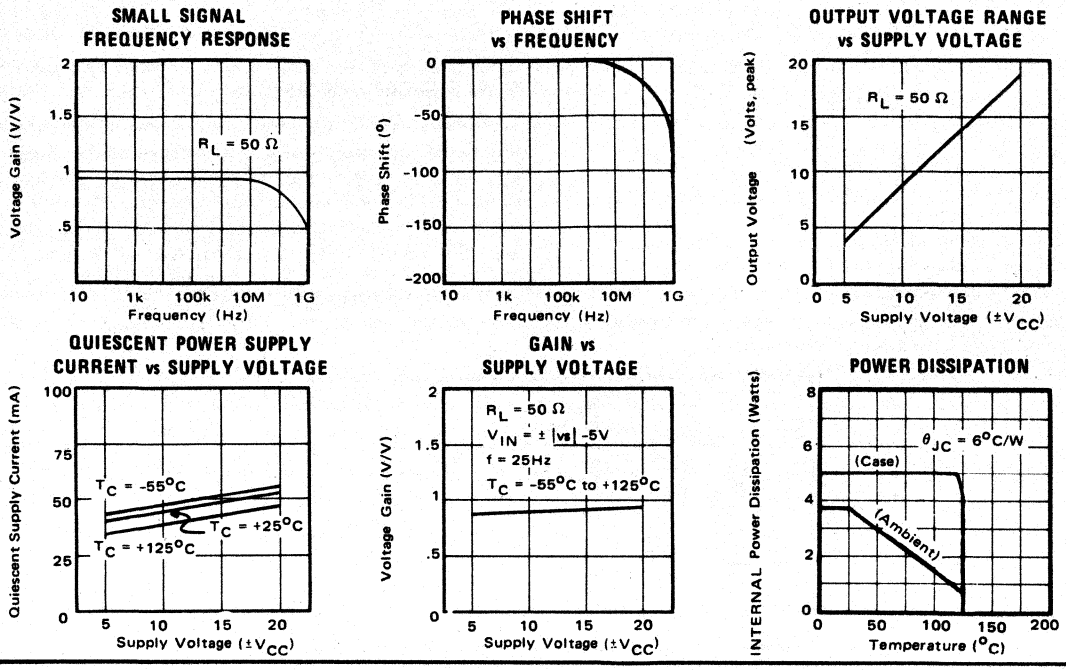
HEATSINKS: 0803HS 12°C/W
0804HS 4.2°C/W
0805HS 3°C/W



SIMPLIFIED SCHEMATIC

TYPICAL PERFORMANCE CURVES

Typical at 25°C and rated supply voltage unless otherwise noted.



APPLICATION INFORMATION

BOOSTER AMPLIFIER

One of the primary applications for the 3553 is that of a current booster for an operational amplifier. The circuit of Figure 1 is typical of such applications. Note that the 3553 is used inside the feedback loop and becomes, effectively, the output stage of the composite amplifier. Because the 3553 has unity voltage gain, wideband response, fast slewing rate, and very little phase delay, the dynamic response of the operational amplifier is virtually unaffected by the addition of the booster.

The already low offset voltage of the 3553 is effectively reduced by a factor equal to the open loop gain of the operational amplifier and becomes a negligible factor in total offset error of the circuit.

Input impedance of the 3553 is extremely high, thus requiring almost no drive current from the operational amplifier. On the other hand, the presence of the 3553 in the circuit increases the output current capability to ±200 mA, drastically lowers the output impedance of the loop, and permits the driving of low impedance loads such as a terminated 50Ω coaxial line.

Capacitive loads, often a source of instability and oscillations in operational amplifier circuits, are buffered by the presence of the 3553. In driving heavily capacitive loads the slew rate of the 3553 will be seen to decrease. This is due simply to the large currents required by fast voltage slewing in a capacitive load,

$$I_c = C_{load} \frac{dV}{dt}.$$

The internal current limit of the 3553 (approximately 600 mA) places a limit on the slewing rate under such conditions.

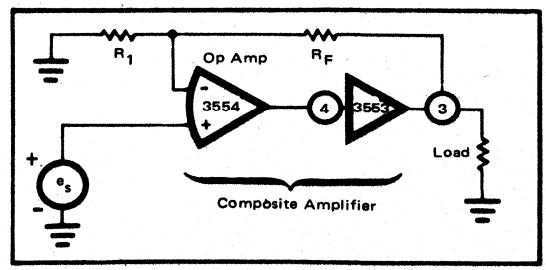


FIGURE 1. Model 3553 as a power booster.

BUFFER AMPLIFIER

The 3553 may also be used, as shown in Figure 2, as a unity gain buffer amplifier. No operational amplifier is required in this mode of operation. Since the 3553 is then operated without feedback, it's offset voltage and drift are translated to the output. While the gain is not precisely unity in this mode, the accuracy is adequate for many applications.

INPUT/OUTPUT PROTECTION

The output stage of the 3553 is current limited at approximately 600 mA. This will provide a measure of output short circuit protection for the amplifier for a period of time as determined by the heatsinking used, the amplifier's thermal resistance, the ambient temperature, etc. The amplifier's output stage transistors should not be allowed to exceed $^{1}50^{o}C$ ($175^{o}C$ absolute max).

The input stage is designed to allow the application of either supply voltage without damage to the amplifier.

POWER DISSIPATION

The power dissipation capability of the 3553 varies with ambient temperature and with the type of heat sink used. A heat sink may be used to increase the dissipation capability or to achieve a given dissipation capability at higher temperature. The power derating curve is given in the typical performance curves on page 1-93.

WIRING RECOMMENDATIONS

No special wiring techniques are necessary with the 3553. However, it is recommended, as a good engineering practice, that the power supply lines be bypassed to common at a point near the amplifier. (A 1.0 μF electrolytic in parallel with a 1000 pF ceramic is recommended.) If the 3553 is used with a wideband operational amplifier, all leads must be kept as short as possible to minimize stray capacitance and unwanted feedback paths.

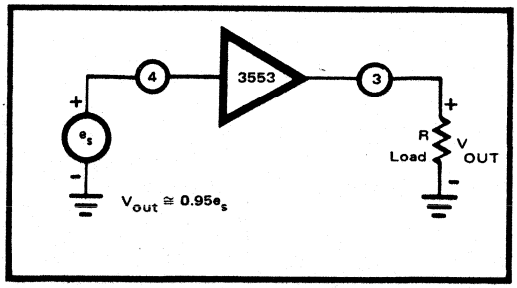
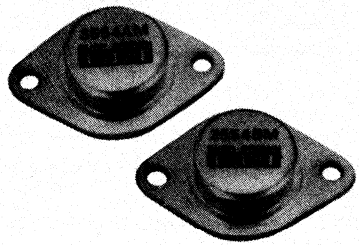


FIGURE 2. Model 3553 as a unity gain buffer.

BURR-BROWN



3554

Wideband - Fast-Settling OPERATIONAL AMPLIFIER

FEATURES

- SLEW RATE, 1000V/μsec
- FAST SETTLING, 150nsec, max (to ±.05%)
- GAIN-BANDWIDTH PRODUCT, 1.7GHz
- FULL DIFFERENTIAL INPUT

APPLICATIONS

- PULSE AMPLIFIERS
- TEST EQUIPMENT
- WAVEFORM GENERATORS
- FAST D/A CONVERTERS

DESCRIPTION

The 3554 is a full differential input, wideband operational amplifier. It is designed specifically for the amplification or conditioning of wideband data signals and fast pulses. It features an unbeatable combination of gain-bandwidth product, settling time and slew rate. It uses hybrid construction. On the beryllia substrate are matched input FETs, thin-film resistors and high speed silicon dice. Active laser trimming and complete testing provide superior performance at a very moderate price.

The 3554 has a slew rate of 1000V/μsec and will output ±10V and ±100mA. When used as a fast settling amplifier, the 3554 will settle to ±0.05% of the final value within 150nsec. A single external compensation capacitor allows the user to optimize the bandwidth, slew rate or settling time in the particular application.

The 3554 is reliable and rugged and addresses almost any application when speed and bandwidth are serious considerations. It is particularly a good choice for use in fast settling circuits, fast D/A converters, multiplexer buffers, comparators, waveform generators, integrators, and fast current amplifiers. It is available in several grades to allow selection of just the performance required.

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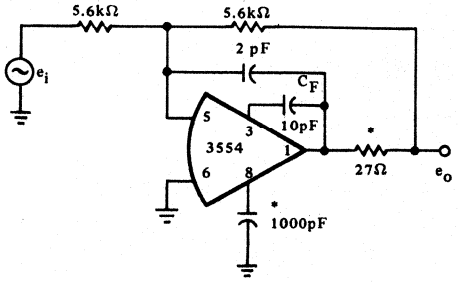
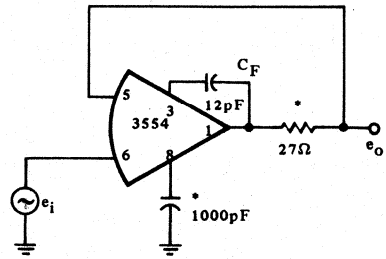
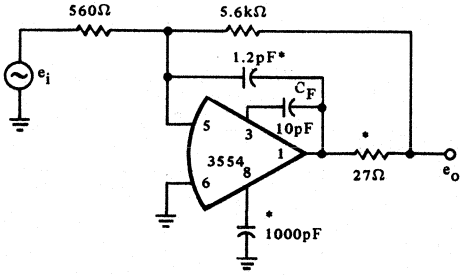
TYPICAL CIRCUITS



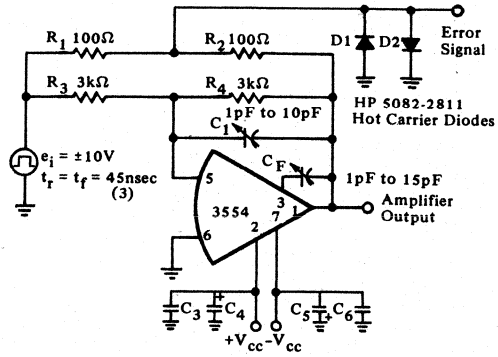
X1 Inverters



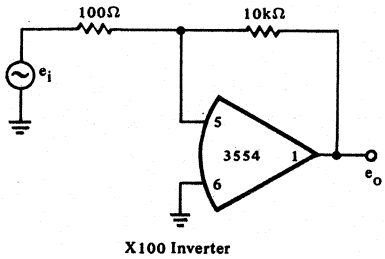
X1 Non-Inverter



X10 Inverter

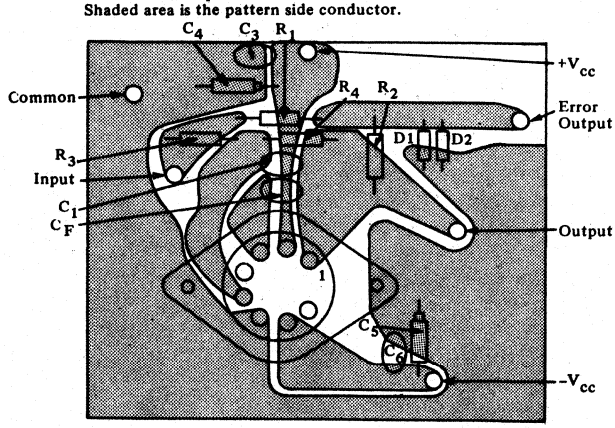


Settling Time Test Circuit Schematic



X100 Inverter

View from Component Side.
Shaded area is the pattern side conductor.



Settling Time Test Circuit Layout

NOTES:

1. These circuits are optimized for driving large capacitive loads (to 470pF).
2. The 3554 is stable at gains of greater than 55 ($C_L \leq$ 100pF) without any frequency compensation.
3. 45nsec is optimum. Very fast rise times (10-20nsec) may saturate the input stage causing less than optimum settling time performance.

*Indicates component that may be eliminated when large capacitive loads are not being driven by the device.

ELECTRICAL SPECIFICATIONS

At T_{CASE} = 25°C and ±15VDC, unless otherwise noted.

PARAMETERS	CONDITIONS	3554AM			3554BM			3554SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OPEN LOOP GAIN, DC					*	*	*	*	*	*	
No Load		100	106								dB
Rated Load	R_L = 100Ω	90	96								dB
RATED OUTPUT					*	*	*	*	*	*	
Voltage	I_O = ±100mA	±10	±11								V
Current	V_O = ±10V	±100	±125								mA
Output Resistance, open loop	f = 10MHz		20								Ω
DYNAMIC RESPONSE					*	*	*	*	*	*	
Bandwidth (0dB, small signal)	C_F = 0	70†	90								MHz
Gain-bandwidth Product	C_F = 0, G = 10 V/V	150	225								MHz
	C_F = 0, G = 100 V/V	425	725								MHz
	C_F = 0, G = 1000 V/V	1000	1700								MHz
Full Power Bandwidth	C_F = 0, V_o = 20Vp-p, R_L = 100Ω	16	19								MHz
Slew Rate	C_F = 0, V_o = 20Vp-p, R_L = 100Ω	1000	1200								V/μsec
Settling Time to ±1%	A = -1		60								nsec
to ±.1%	A = -1		120								nsec
to ±.05%	A = -1		140	150							nsec
to ±.01%	A = -1		200	250							nsec
INPUT OFFSET VOLTAGE											
Initial offset, T_A = 25°C			±0.5	±2		±0.2	±1		±0.2	±1	mV
vs. Temp (T_A = -25°C to +85°C)			±20	±50		±8	±15				μV/°C
vs. Temp (T_A = -55°C to +125°C)									±12	±25	μV/°C
vs. Supply Voltage			±80	±300		*	*		*	*	μV/V
INPUT BIAS CURRENT					*	*	*	*	*	*	
Initial bias, 25°C		0	-10	-50							pA
vs. Temp			**								
vs. Supply Voltage			±1								pA/V
INPUT DIFFERENCE CURRENT					*	*	*	*	*	*	
Initial difference, 25°C			±2	±10							pA
INPUT IMPEDANCE						*			*		
Differential			10^{11} ‖ 2								Ω ‖ pF
Common-mode			10^{11} ‖ 2								Ω ‖ pF
INPUT NOISE					*	*	*	*	*	*	
Voltage, f_o = 1Hz	R_S = 100Ω		125	450†							nV/√Hz
f_o = 10 Hz	R_S = 100Ω		50	160†							nV/√Hz
f_o = 100 Hz	R_S = 100Ω		25	90†							nV/√Hz
f_o = 1 kHz	R_S = 100Ω		15	50†							nV/√Hz
f_o = 10 kHz	R_S = 100Ω		10	35†							nV/√Hz
f_o = 100 kHz	R_S = 100Ω		8	25†							nV/√Hz
f_o = 1 MHz	R_S = 100Ω		7	25†							nV/√Hz
f_B = .3 Hz to 10 Hz	R_S = 100Ω		2	7†							μV, p-p
f_B = 10 Hz to 1 MHz	R_S = 100Ω		8	25							μV, rms
Current, f_B = .3 Hz to 10 Hz	R_S = 100Ω		45								fA, p-p
f_B = 10 Hz to 1 MHz	R_S = 100Ω		2								pA, rms
INPUT VOLTAGE RANGE					*	*	*	*	*	*	
Common-mode Voltage Range	Linear Operation		$\pm(\lvert V_{CC}\rvert - 4)$								V
Common-mode Rejection	f = DC, V_{CM} = +7V, -10V	44	78								dB
Max. Safe Input Voltage			±Supply								V
POWER SUPPLY					*	*	*	*	*	*	
Rated Voltage			±15								VDC
Voltage Range, derated performance		±5		±18							VDC
Current, quiescent		±17	±35	±45							mA
TEMPERATURE RANGE (ambient)											
Specification		-25		+85	-25		+85	-55		+125	°C
Operating, derated performance		-55		+125	-55		+125	-55		+125	°C
Storage		-65		+150	-65		+150	-65		+150	°C
θ junction-case			15			15			15		°C/W
θ junction-ambient			45			45			45		°C/W

* Specifications same as for 3554AM

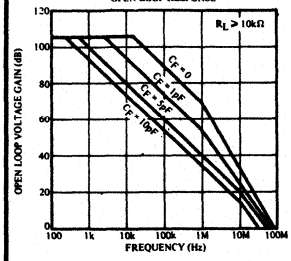
** Doubles every +10°C

† This parameter is untested and is not guaranteed. This specification is established to a 90% confidence level.

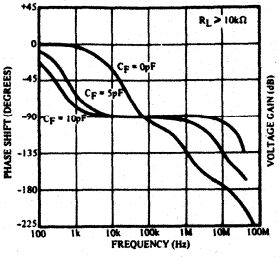
TYPICAL PERFORMANCE CURVES

at T_C = +25°C and ±15VDC unless otherwise noted.

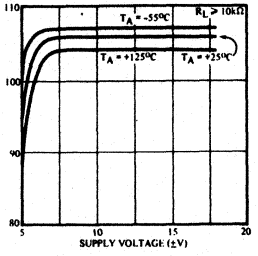
OPEN LOOP RESPONSE



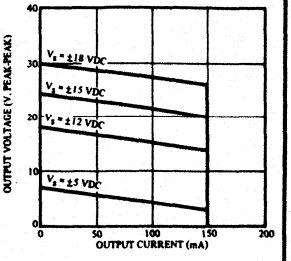
OPEN LOOP RESPONSE



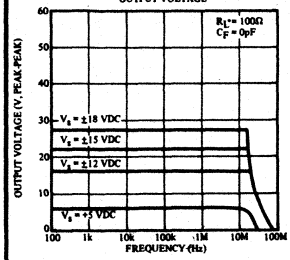
VOLTAGE GAIN



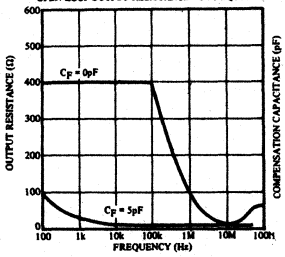
OUTPUT VOLTAGE VS OUTPUT CURRENT



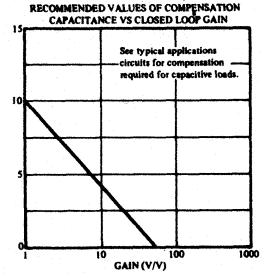
OUTPUT VOLTAGE



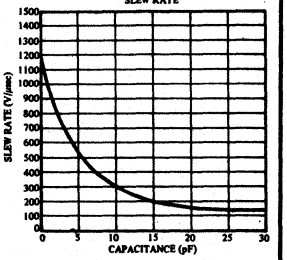
OPEN LOOP OUTPUT RESISTANCE VS FREQUENCY



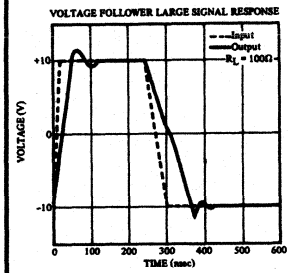
RECOMMENDED VALUES OF COMPENSATION CAPACITANCE VS CLOSED LOOP GAIN



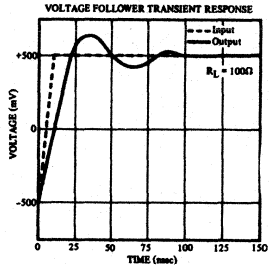
SLEW RATE



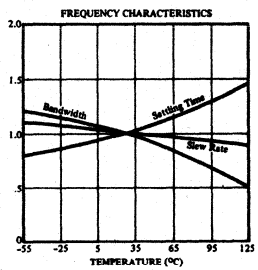
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



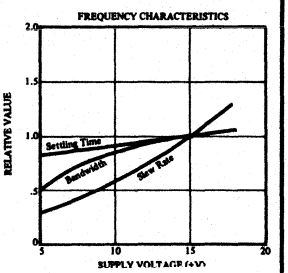
VOLTAGE FOLLOWER TRANSIENT RESPONSE



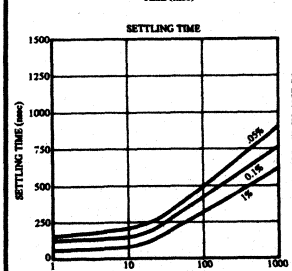
FREQUENCY CHARACTERISTICS



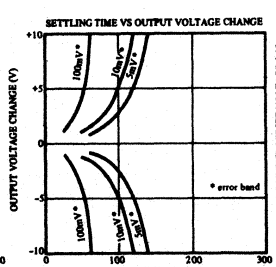
FREQUENCY CHARACTERISTICS



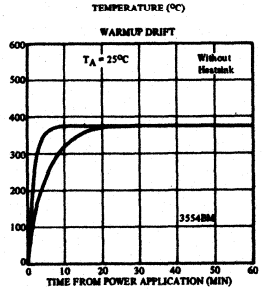
SETTLING TIME



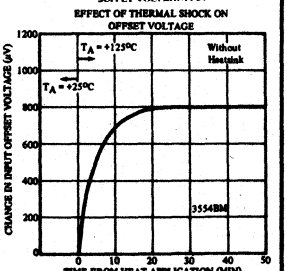
SETTLING TIME VS OUTPUT VOLTAGE CHANGE



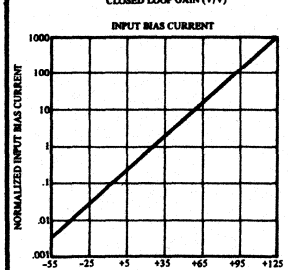
WARMUP DRIFT



EFFECT OF THERMAL SHOCK ON OFFSET VOLTAGE



INPUT BIAS CURRENT



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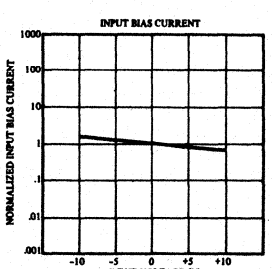
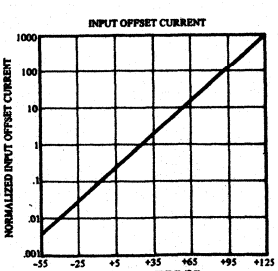
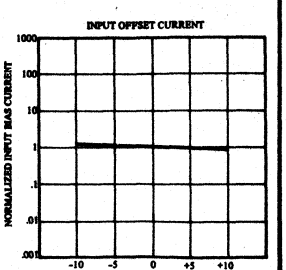
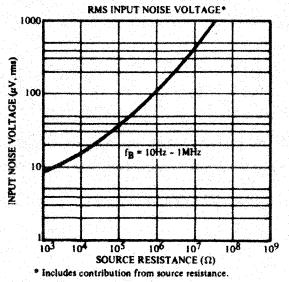


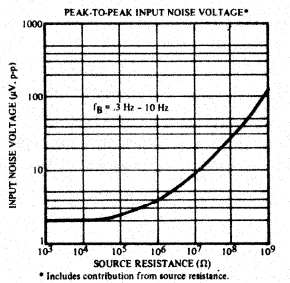
INPUT OFFSET CURRENT

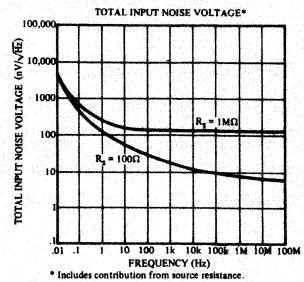


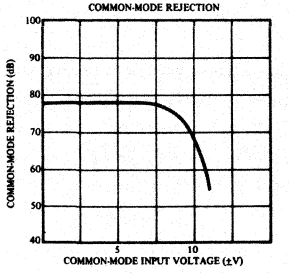
INPUT OFFSET CURRENT

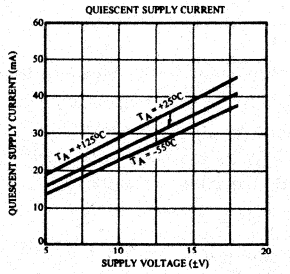


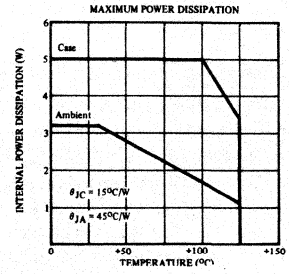






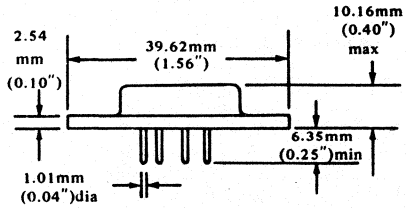


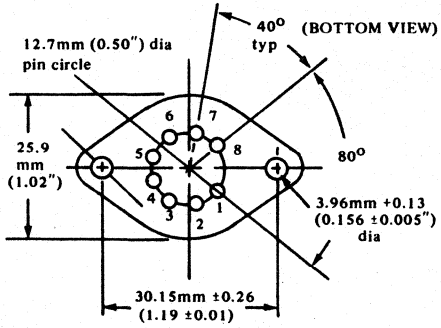




MECHANICAL

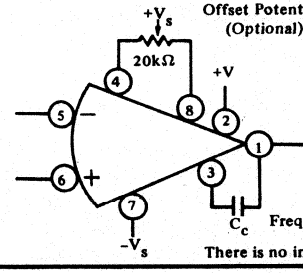
TO-3



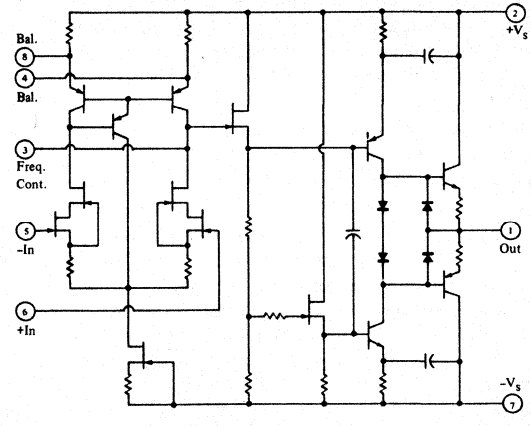


Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

AMPLIFIER CONNECTIONS



There is no internal case connection.



APPLICATIONS INFORMATION

WIRING PRECAUTIONS

The 3554 is a wideband, high frequency operational amplifier that has a gain-bandwidth product exceeding 1 Gigahertz. The full performance capability of this amplifier will be realized by observing a few wiring precautions and high frequency techniques.

Of all the wiring precautions, grounding is the most important and is described in an individual section. The mechanical circuit layout also is very important. All circuit element leads should be as short as possible. All printed circuit board conductors should be wide to provide low resistance, low inductance connections and should be as short as possible. In general, the entire physical circuit should be as small as practical. Stray capacitances should be minimized especially at high impedance nodes such as the input terminals of the amplifier. Pin 5, the inverting input, is especially sensitive and all associated connections must be short. Stray signal coupling from the output to the input or to pin 8 should be minimized. A recommended printed circuit board layout is shown with the TYPICAL CIRCUITS. It also may be used for test purposes as described below.

When designing high frequency circuits low resistor values should be used; resistor values less than 5.6kΩ are recommended. This practice will give the best circuit performance as the time constants formed with the circuit capacitances will not limit the performance of the amplifier.

GROUNDING

As with all high frequency circuits a ground plane and good grounding techniques should be used. The ground plane should connect all areas of the pattern side of the printed circuit board that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns. The ground plane also reduces stray signal pick up. An example of an adequate ground plane and good high frequency techniques is the Settling Time Test Circuit Layout shown with the TYPICAL CIRCUITS.

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins. A combination of a 1μF tantalum capacitor in parallel with a 470pF ceramic capacitor is a suitable bypass.

In inverting applications it is recommended that pin 6, the non-inverting input, be grounded rather than being connected to a bias current compensating resistor. This assures a good signal ground at the non-inverting input. A slight offset error will result; however, because the resistor values normally used in high frequency circuits are small and the bias current is small, the offset error will be minimal.

If point to point wiring is used or a ground plane is not, single point grounding should be used. The input signal return and the load signal return and the power supply common should all be connected at the same physical point. This will eliminate any common current paths or ground loops which could cause signal modulation or unwanted feedback.

It is recommended that the case of the 3554 not be grounded during use (it may, if desired). A grounded case will add a slight capacitance to each pin. To an already functional circuit grounding the case will probably require slight compensation readjustment and the compensation capacitor values will be slightly different from those recommended in the typical performance curves. There is no internal connection to the case.

Proper grounding is the single most important aspect of high frequency circuitry.

GUARDING

The input terminals of the 3554 may be surrounded by a guard ring to divert leakage currents from the input terminals. This technique is particularly important in low bias current and high input impedance applications. The guard, a conductive path that completely surrounds the two amplifier inputs, should be connected to a low impedance point which is at the input signal potential. It blocks unwanted printed circuit board leakage currents from reaching the input terminals. The guard also will reduce stray signal coupling to the input.

In high frequency applications guarding may not be desirable as it increases the input capacitance and can degrade performance. The effects of input capacitance, however, can be compensated by a small capacitor placed across the feedback resistor. This is described further in the COMPENSATION section.

COMPENSATION

The 3554 uses external frequency compensation so that the user may optimize the bandwidth or slew rate or settling time for his particular application. Several typical performance curves are provided to aid in the selection of the correct compensation capacitance value. In addition several typical circuits show recommended compensation in different applications.

The primary compensation capacitor, C_F, is connected between pins 1 and 3. As the performance curves show, larger closed loop gain configurations require less capacitance and an improved gain-bandwidth product will be realized. Note that no compensation capacitor is required for closed loop gains above 55 V/V and when the load capacitance is less than 100 pF.

When driving large capacitive loads, 470 pF and greater,

an additional capacitor, C_8, is connected between pin 8 and ground. This capacitor is typically 1000 pF. It is particularly necessary in low closed loop voltage gain configurations. The value may be varied to optimize performance and will depend upon the load capacitance value. In addition, the performance may be optimized by connecting a small resistance in series with the output and a small capacitor from pin 1 to 5. See the TYPICAL CIRCUITS for the X10 Inverter.

The flat high frequency response of the 3554 may be preserved and any high frequency peaking avoided by connecting a small capacitor in parallel with the feedback resistor. This capacitor will compensate for the closed loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2 pF, and the input and feedback resistors. Using small resistor values will keep the break frequency of this zero sufficiently high, avoiding peaking and preserving the phase margin. Resistor values less than 5.6kΩ are recommended. The selected compensation capacitor may be a trimmer, a fixed capacitor or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed loop gain. It will typically be 2 pF for a clean layout using low resistances (1kΩ) and up to 10 pF for circuits using larger resistances.

SETTLING TIME

Settling time is truly a complete dynamic measure of the 3554's total performance. It includes the slew rate time, a large signal dynamic parameter, and the time to accurately reach the final value, a small signal parameter that is a function of bandwidth and open loop gain. The settling time may be optimized for the particular application by selection of the closed loop gain and the compensation capacitance. The best settling time is observed in low closed loop gain circuits. A performance curve shows the settling time to three different error bands.

Settling time is defined as the total time required, from the signal input step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the magnitude of the output transition.

SLEW RATE

Slew rate is primarily an output, large signal parameter. It has virtually no dependence upon the closed loop gain or the bandwidth, per se. It is dependent upon compensation. Decreasing the compensation capacitor value will increase the available slew rate as shown in the performance curve. Stray capacitances may appear to the amplifier as compensation. To avoid limiting the slew rate performance, stray capacitances should be minimized.

CAPACITIVE LOADS

The 3554 will drive large capacitive loads (up to 1000 pF) when properly compensated. See the APPLICATIONS INFORMATION section on COMPENSATION. The effect of a capacitive load is to decrease the phase margin of the amplifier. With compensation the amplifier will provide stable operation even with large capacitive loads.

The 3554 is particularly well suited for driving 50Ω loads connected via coaxial cables due to its ±100mA output drive capability.The capacitance of the coaxial cable, 29 pF/foot of length for RG-58, does not load the amplifier when the coaxial cable or transmission line is terminated in the characteristic impedance of the transmission line.

OFFSET VOLTAGE ADJUSTMENT

The offset voltage of the 3554 may be adjusted to zero by connecting a 20kΩ linear potentiometer between pins 4 and 8 with the wiper connected to the positive supply. A small, non-inductive potentiometer is recommended. The leads connecting the potentiometer to pins 4 and 8 should be no longer than 6 inches to avoid stray capacitance and stray signal pickup. Stray coupling from the output, pin 1, to pin 4 (negative feedback) or to pin 8 (positive feedback) should be avoided.

The potentiometer is optional and may be omitted when the guaranteed offset voltage is considered sufficiently low for the particular application.

For each microvolt of offset voltage adjusted, the offset voltage temperature drift will change by ±0.004 μV/°C.

HEATSINKING

The 3554 does not require a heatsink for operation in most environments. The use of a heatsink, however, will reduce the internal thermal rise and will result in cooler operating temperatures. At extreme temperature and under full load conditions a heatsink will be necessary as indicated in the MAXIMUM POWER DISSIPATION curve. A heatsink with 8 holes for the 8 amplifier pins should be used. Burr-Brown has heatsinks available in three sizes – 3°C/W, 4.2°C/W and 12°C/W. A separate product data sheet is available upon request.

When heatsinking the 3554, it is recommended that the heatsink be connected to the amplifier case and the combination not connected to the ground plane. For a single sided printed circuit board, the heatsink may be mounted between the 3554 and the non-conductive side of the PC board, and insulating washers, etc., will not be required. The addition of a heatsink to an already functional circuit will probably require slight compensation readjustment for optimum performance due to the change in stray capacitances. The added stray capacitance from the heatsink to each pin will depend on the thickness and type of heatsink used.

SHORT CIRCUIT PROTECTION

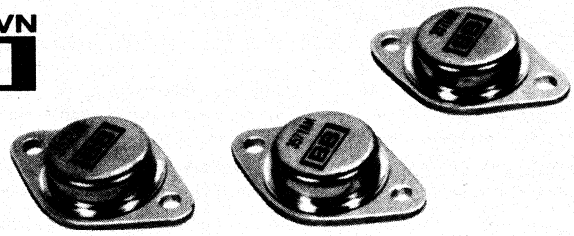
The 3554 is short circuit protected for continuous output shorts to common. Output shorts to either supply will destroy the device, even for momentary connections. Output shorts to other potential sources are not recommended as they may cause permanent damage.

TESTING

The 3554 may be tested in conventional operational amplifier test circuits; however, to realize the full performance capabilities of the 3554, the test fixture must not limit the full dynamic performance capability of the amplifier. High frequency techniques must be employed. The most critical dynamic test is for settling time. The 3554 Settling Time Test Circuit Schematic and a test circuit layout is shown with the TYPICAL CIRCUITS on page 1-00. The input pulse generator must have a flat topped, fast settling pulse to measure the true settling time of the amplifier. The layout exemplifies the high frequency considerations that must be observed. The layout also may be used as a guide for other test circuits. Good grounding, truly square drive signals, minimum stray coupling and small physical size are important.

Every 3554 is thoroughly tested prior to shipment assuring the user that all parameters equal or exceed their specifications.

BURR-BROWN



3571
3572

OPERATIONAL AMPLIFIERS

FEATURES

- **HIGH CURRENT**
  Up to 5A peak, 2A continuous
- **EASY TO USE**
  Adjustable current limits
  Electrically isolated case
  Small size - 8-pin TO-3 package
- **HIGH VOLTAGE**
  Up to 70V p-p output
- **SELF-PROTECTED**
  Self-contained automatic thermal sensing and shutdown
- **HIGH POWER**
  Delivers up to 70W to load

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PDS-334C

Printed in U.S.A. July, 1978

DESCRIPTION

The 3571AM and 3572AM are high output current integrated circuit operational amplifiers. Their performance, ease of use and compact size make them ideal to use in a variety of high current applications. They are especially well suited for driving permanent magnet DC servo and torque motors.

The equivalent circuit for the 3571AM and 3572AM is shown in Figure 1. The design uses a monolithic FET input stage for high input impedance, low bias current, and low voltage drift versus temperature. The high input impedance provides negligible source impedance loading errors when the noninverting circuit configuration is used. The low bias currents minimize offset errors when large values of source and feedback resistors are used.

The input offset voltage at 25°C and the input offset voltage drift versus temperature are compensated by state-of-the-art laser trimming techniques. The offset voltage is low enough so that trimming will not be required in most applications. The excellent input characteristics and the high gain available mean that the use of a preamplifier, sometimes required with other servo type amplifiers, will not be necessary with the 3571AM and 3572AM.

The output stage is a class AB design which provides low distortion and minimizes quiescent current drain. The output circuitry provides for external current limiting resistors for both positive and negative output currents. This allows the user to select the current limit value suited to his particular application. This is especially desirable for driving permanent magnet motors where the high current seen during direction reversal (plugging) can demagnetize the motor.

The 3571AM and 3572AM have been designed to operate over a relatively wide supply range (±15VDC to ±40VDC) while still maintaining the high output current capability. This allows the user a wide range for the selection of the proper output voltage and current and makes the amplifiers useful for many different types of loads.

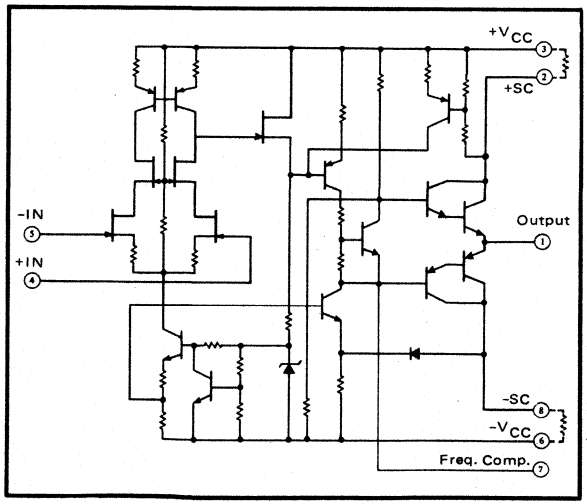


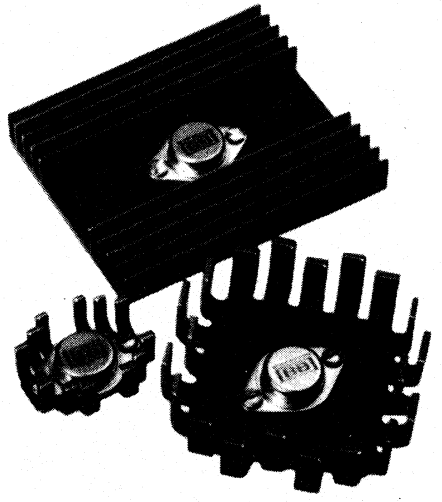
FIGURE 1. Equivalent Circuit.

The output circuit has a unique protection feature which is only practical in integrated circuit amplifiers - self-contained automatic thermal sensing and shut off circuitry which automatically turns the amplifier off when the internal temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating the amplifiers biasing network when the temperature reaches 150°C. As this happens, the output load current limits at a safe value and the amplifier's quiescent current decreases. The output current may remain at a low value or oscillate between two values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal load condition is removed.

Internal thermal protection removes some of the constraints of power derating for abnormal operating conditions. The amplifier will protect itself for many conditions of excess power dissipation (see POWER DERATING CURVE, page 1-106). This allows the use of a smaller heat sink to protect against abnormal output conditions since the amplifier has its own internal protection for many conditions of excess power dissipation. The output constraints of the SAFE OPERATING AREA curves (see page 1-106) must still be observed.

The 3571AM and 3572AM have several other features that improve their utility. For instance, the metal case of the units is completely electrically isolated. (This can be contrasted to most power semiconductors where the case is connected to the collector of the device.) This simplifies mounting and reduces cost since the need for insulating spacers and bushings is eliminated. The hermetically sealed package improves reliability and will withstand severe environments better than discrete component amplifiers. The small package size makes mounting more convenient.

Burr-Brown offers three heat sinks as accessories; 0803HS with a thermal resistance of 12°C/watt, 0804HS at 5.2°C/watt, and 0805HS at 3°C/watt. A convenient mating connector, 0803MC is also available.



SPECIFICATIONS

Typical @ T_{case} = 25°C and $\pm V_{CC}$ = ±35 VDC max unless otherwise noted.

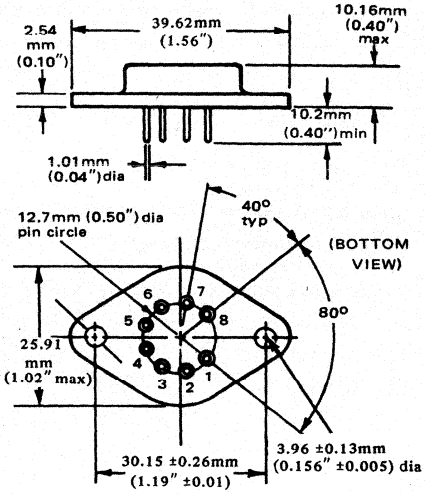
ELECTRICAL

MODELS	3571AM	3572AM
RATED OUTPUT (to load)		
Power to Load		
Continuous, min(1)	30 Watts	60 Watts
Peak, min(1)	60 Watts	150 Watts
Output Voltage, ±(|V_{CC}|-5)V		
Continuous, min(1)	±30V @ ±1A	±30V @ ±2A
Peak, min(1)	±30V @ 2A	±30V @ 5A
Load Capacitance	3300 pF	
DISSIPATION RATING		
at 25°C Case Temperature	33 Watts	50 Watts
Derating Above 25°C	See typical performance curves	
Thermal Resistance, Case to Free Air	30°C/Watt	
Thermal Time Constant (No heat sink)	2 minutes	
Thermal Resistance, Junction to Case	2.5°C/W	
POWER SUPPLY		
Voltage, $\pm V_{CC}$	±15 to ±40 VDC	
Quiescent Current, max	±35 mA	
OPEN LOOP		
Gain min, at R_{load} = 30Ω (3572AM) R_{load} = 60Ω (3571AM)	94 dB	
Output Impedance	2.5 Ω	
FREQUENCY RESPONSE		
Unity Gain Bandwidth, Small Signal	500 kHz	
Full Power Bandwidth	16 kHz @ Vpk = 30 V	
Slew Rate, C_C = 1000 pF	3V/μs	
INPUT OFFSET VOLTAGE		
Initial @ 25°C, max	±2mV	
Drift vs. Temp., max	±40 μV/°C	
Drift vs. Supply Voltage	±100 μV/V	
Drift vs. Time	50 μV/mo	
Drift vs. Power Dissipation (T_C constant)	20 μV/Watt	
INPUT BIAS CURRENT		
Initial @ 25°C, max	-100 pA	
Drift vs. Temp.	doubles every 10°C	
Drift vs. Supply Voltage	0.5 pA/V	
INPUT OFFSET CURRENT		
Initial @ 25°C	±50 pA	
Drift vs. Temp.	doubles every 10°C	
Drift vs. Supply Voltage	0.5 pA/V	
INPUT IMPEDANCE		
Differential	10^{11} Ω‖10 pF	
Common-Mode	10^{11}Ω	
INPUT NOISE		
Voltage 0.01 Hz to 10 Hz, p-p	4 μV	
10 Hz to 1 kHz, RMS	3 μV	
Current 0.01 Hz to 10 Hz, p-p	1 pA	
10 Hz to 1 kHz, RMS	0.1 pA	
INPUT VOLTAGE RANGE		
Max Safe Differential Voltage	($+V_{CC}$ + | $-V_{CC}$|)	
Max Safe Common-Mode Voltage	$+V_{CC}$ to $-V_{CC}$	
Common-Mode Voltage, Linear Operation	±(|V_{CC}|-10)V	
Common-Mode Rejection	80 dB min., 90 dB, typ.	
TEMPERATURE RANGE (Case)		
Specification	-25°C to +85°C	
Operating	-55°C to +125°C	
Storage	-55°C to +125°C	
ACCESSORIES		
Heat Sink	0803HS (12°C/W)	
	0804HS (5.2°C/W)	
	0805HS (3°C/W)	
Connector	0803MC	

(1) SAFE OPERATING AREA and POWER DERATING limitations must be observed.

MECHANICAL

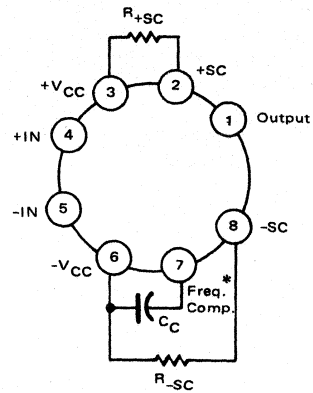
"M" PACKAGE (TO-3)



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std 883 [except paragraph 3.2.].

Connection Diagram

(TOP VIEW)



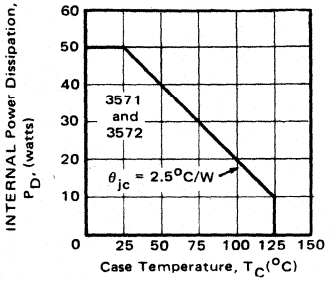
The case is electrically isolated. It is recommended that the case be grounded during use.

* A 1000 pF ±20% ceramic capacitor is recommended for all circuit configurations and at all amplifier gains. The capacitor's lead lengths should be short. For gains above 10 V/V, C_c is not absolutely required.

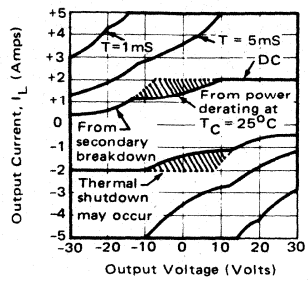
TYPICAL PERFORMANCE CURVES

(Typical T_{case} = 25°C and $\pm V_{CC}$ = ±35 VDC unless otherwise noted.)

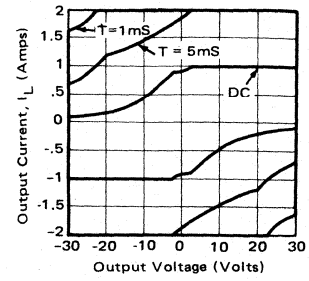
POWER DERATING



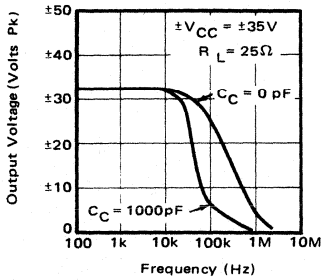
3572 SAFE OPERATING AREA



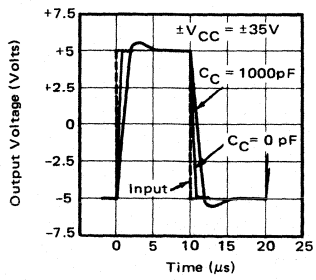
3571 SAFE OPERATING AREA



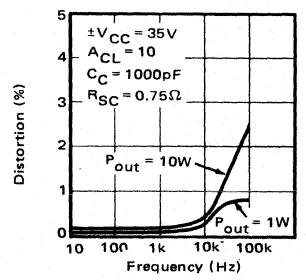
OUTPUT VOLTAGE VS. FREQUENCY



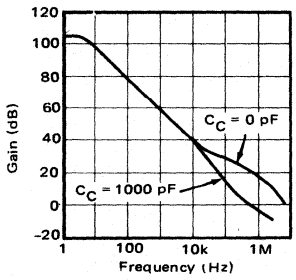
VOLTAGE FOLLOWER PULSE RESPONSE



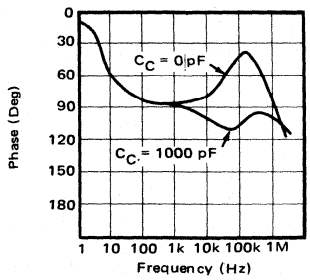
DISTORTION VS. FREQUENCY



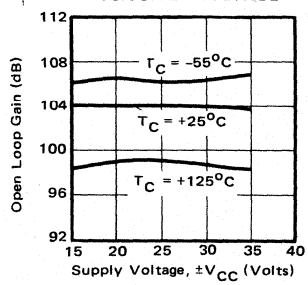
OPEN LOOP GAIN VS. FREQUENCY



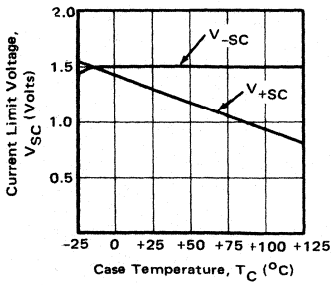
OPEN LOOP PHASE



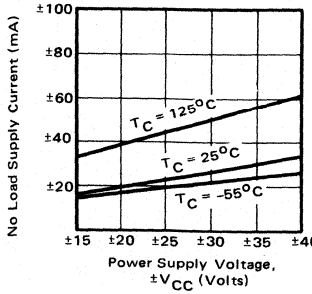
OPEN LOOP GAIN VS. SUPPLY VOLTAGE



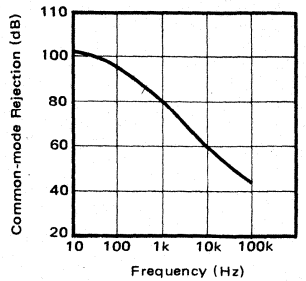
CURRENT LIMIT VOLTAGE VS. TEMPERATURE



QUIESCENT CURRENT VS. SUPPLY VOLTAGE



COMMON-MODE REJECTION VS. FREQUENCY



INSTALLATION and OPERATING INSTRUCTIONS

General Precautions

CURRENT LIMITING

It is recommended that during initial amplifier setup, particularly in breadboarding and when a lack of familiarity with the amplifier exists, that the current limit be set at about 250 mA ($R_{SC} \cong 5.6\Omega$). This will allow verification of the circuit and will minimize the possibility of damaging the amplifier. Later, when the circuit configuration and connections have been proven, the current limits can be raised to the desired value.

MINIMUM HEAT SINK

The 3571AM and 3572AM require a minimum heat sink of 16°C/watt or lower in order to insure thermal stability (mounting on a 3" x 3" x 0.06" piece of 80% copper-clad printed circuit board material will be sufficient). Normally this will not be a consideration since a larger heat sink will be used to provide the proper power dissipation as described in the THERMAL CONSIDERATIONS section which follows.

PROPER GROUNDING & POWER SUPPLY BYPASSING

Particular attention should be given to proper grounding practices because the large output currents can cause significant ground loop errors. Figure 2 illustrates proper connections.

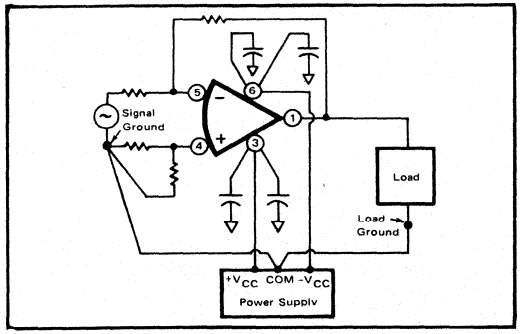


FIGURE 2. Proper power supply connections.

Note that the connections are such that the load current does not flow through the wire connecting the signal ground point to the power supply common. Also, power supply and load leads should be run physically separated from the amplifier input and signal leads.

The amplifier should be power supply bypassed with 50 μF tantalum capacitors connected in parallel with 0.01 μF ceramic capacitors connected as close to pins 3 and 6 as possible. The capacitors should be connected to the load ground rather than the signal ground.

Current Limits

The amplifiers are designed so that both the positive and negative load current limits can be adjusted with external resistors, R_{+SC} and R_{-SC} respectively. The value of the resistors are given by the following equations:

$$R_{+SC} = \frac{1.3\ (\text{volts})}{I_{+\text{limit}}(\text{amps})}, \quad R_{-SC} = \frac{1.5\ (\text{volts})}{I_{-\text{limit}}(\text{amps})}$$

I_{limit} is the desired maximum current. The maximum power dissipation of the resistors is $P_{max} = R_{SC}(I_{limit})^2$. The current limits determined by the equations above are accurate to about ±10%. The variation of I_{limit} vs. temperature is shown in the Typical Performance Curves. Both $+V_{CC}$ and $-V_{CC}$ must be on for the current limits to function.

To avoid introducing unwanted inductance into the current limit circuitry, which may introduce oscillations and permanent damage, both current limit resistors must be non-inductive. Do not use wire wound resistors. Carbon composition resistors are preferred and paralleling them can provide a wide current limit range at the wattage needed.

The maximum value of the negative current limit resistor is 15 ohms (100 mA, minimum). Exceeding this value, or an open circuit, could permanently damage the internal 75Ω, thin-film resistor which parallels R_{-SC}.

The amplifier should be used with as low a current limit as possible for the particular application. This will minimize the chance of damaging the amplifier under abnormal load conditions and increase reliability by limiting the internal power dissipation of the amplifier.

Thermal Considerations

The 3571AM and 3572AM are rated for 150°C maximum junction temperature. The thermal resistance from junction to case (θ_{jc}) is 2.5°C per watt. The corresponding Power Derating Curve is given in the Typical Performance Curves section.

The internal power dissipation of the amplifier is given by the equation $P_D = P_{DQ} + P_{DL}$ where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipated in the output stage due to the load. (For $\pm V_{CC} = \pm 40V$, $P_{DQ} = 80 \times 0.035 = 2.8$ watts max) For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{out}$) the maximum value of P_{DL} occurs at $\pm V_{out} = \frac{\pm V_{CC}}{2}$ and is equal to $P_{DL_{max}} = \frac{(\pm V_{CC})^2}{4R_L}$. Figure 3 shows P_D as function of the output voltage with the load resistance as a running parameter.

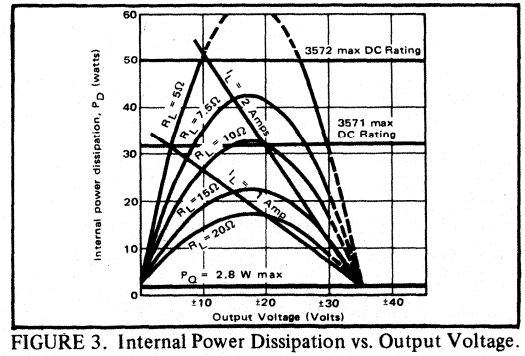


FIGURE 3. Internal Power Dissipation vs. Output Voltage.

P_{DL} for any other value of V_{out} can be computed from

$$P_{DL} = (\pm V_{CC} - \pm V_{out}) \cdot I_L = (\pm V_{CC} - \pm V_{out})\left(\frac{\pm V_{out}}{R_L}\right)$$

The use of an adequate heat sink is mandatory and thermal resistance of the heat sink (θ_{hs}) can be determined from the equation:

$$\theta_{hs} = \frac{T_J - T_A}{P_D} - \theta_{jc}$$

where T_J is the desired amplifier junction temperature (+150°C max), T_A is the ambient temperature, P_D is the amplifiers dissipation, $P_D = P_{DO} + P_{DL}$, and θ_{jc} is the junction to case thermal resistance of the amplifier. Burr-Brown Application Note AN-83 entitled, "How to Determine What Heatsink to Use", is available for additional information.

The electrically isolated case of the 3571AM and 3572AM simplifies mounting the amplifiers to the heat sink (and the heat sink to any other assemblies) since there is no need for electrical insulation. Thermal joint compound and lock washers should be used to prevent mechanical relaxation due to thermal stresses.

SAFE OPERATING AREA

There are additional constraints on the output voltage and current other than those just due to the maximum internal power dissipation of the amplifiers. These are related to the prevention of secondary breakdown in the output stage transistors. These restrictions are shown in the SAFE OPERATING AREA CURVES in the Typical Performance Curves.

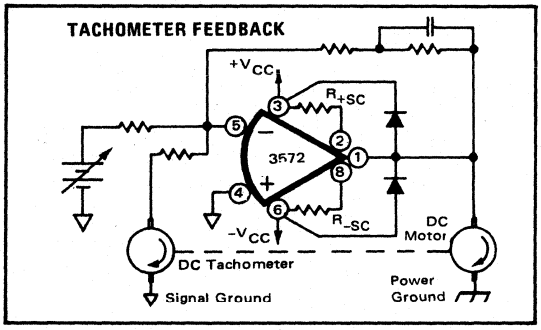
APPLICATION CONSTRAINT

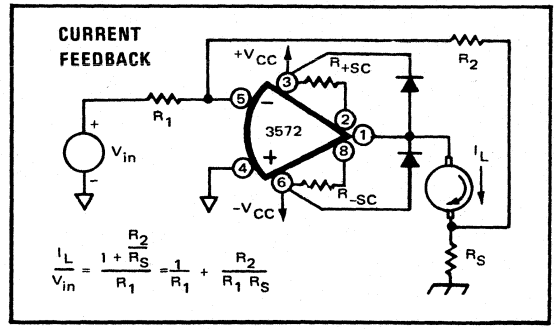
Because of the possibility of damaging the output stage if frequency instability (oscillations) occurs, applications with an inductive load which will activate the current limit of the amplifier, are constrained to have a load impedance phase angle of less than 60° leading, over the frequency band of 10kHz to 100kHz. Increasing the load's series resistance will decrease the phase angle, if necessary. Larger inductive loads may be applied if current limit is not activated.

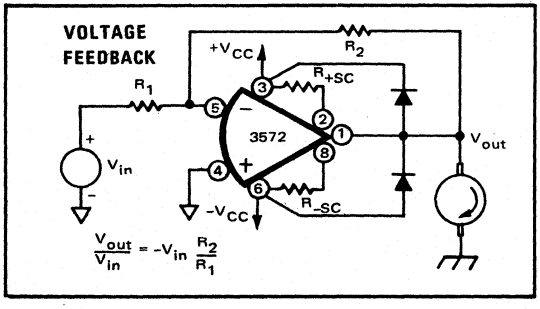
FREQUENCY COMPENSATION

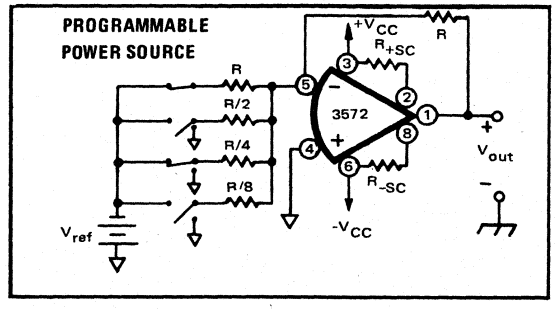
The optimum value of the compensation capacitor is 1000 pF. A ±20% tolerance ceramic capacitor is recommended. The compensation capacitor should be used with all circuit configurations and at all amplifier gains.

TYPICAL APPLICATIONS



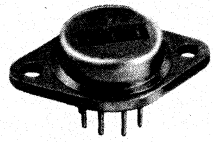






BURR-BROWN

3573



High Current - High Power OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT POWER
  - 100 Watts Peak
  - 40 Watts Continuous
- WIDE SUPPLY RANGE
  - ±10 to ±34 Volts
- HIGH OUTPUT CURRENT
  - ±5 Amps Peak
  - ±2 Amps Continuous
- SMALL SIZE: TO-3 PACKAGE
- LOW COST

APPLICATIONS

- DC MOTORS
- AC MOTORS
- ACTUATORS
- ELECTRONIC VALVES
- SYNCROS

DESCRIPTION

If you need to supply 100 watts peak or 40 watts continuous, yet must choose a small, easy to use op amp, you'll find the 3573 a logical solution. This hybrid IC delivers ±5A peak minimum at ±20V minimum to the load when operated from ±28V power supplies. The design of this op amp has been optimized for low cost while preserving moderately good input and distortion characteristics.

Output circuitry provides for external current limiting resistors for both positive and negative currents. This allows current limits to be set to values dictated by the op amp's application. 3573 is internally frequency compensated and is unconditionally stable with capacitive loads to 3300pF.

Housed in a small, rugged, hermetically sealed 8-lead TO-3 package, 3573 will withstand severe environments far better than discrete component amplifiers. The metal case is completely electrically isolated from the amplifier circuitry. Thus, mounting is easier (no isolation washers or spacers) and the hazards of a case connected to the output or supply voltage is eliminated.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-393

Printed in U.S.A. July, 1978

ELECTRICAL SPECIFICATIONS

At T_{case} = 25°C and $\pm V_{CC}$ = ±28VDC unless otherwise noted.

PARAMETER	CONDITIONS	3573AM MIN	3573AM TYP	3573AM MAX	UNITS
OPEN LOOP GAIN, DC	$R_L \geq 30\Omega$	94	115		dB
RATED OUTPUT					
Power to Load[1]					
Continuous		40			W
Peak		100			W
Output Current					
Continuous		±2			A
Peak		±5			A
Output Voltage	$I_{out} = \pm 5A$[4]	±20	±23		V
DYNAMIC RESPONSE					
Bandwidth, Unity Gain	Small Signal		1		MHz
Full Power Bandwidth		15	23		kHz
Slew Rate		1.5	2.6		V/µs
INPUT OFFSET VOLTAGE					
Initial Offset			±5	±10	mV
vs Temperature	-25°C ≤ T_{case} ≤ 85°C		±10	±65	µV/°C
vs Supply Voltage			±35		µV/V
INPUT BIAS CURRENT					
Initial	T_{case} = 25°C		15	40	nA
vs Temperature	-25°C ≤ T_{case} ≤ 85°C		±0.05		nA/°C
vs Supply Voltage			±0.02		nA/V
INPUT DIFFERENCE CURRENT					
Initial	T_{case} = 25°C		±5	±10	nA
vs Temperature	-25°C ≤ T_{case} ≤ 85°C		±0.01		nA/°C
INPUT IMPEDANCE					
Differential			10		MΩ
Common-mode			250		MΩ
INPUT NOISE					
Voltage Noise	f_n = 0.3Hz to 10Hz		3		µV p-p
	f_n = 10Hz to 10kHz		5		µVrms
Current Noise	f_n = 0.3Hz to 10Hz		20		pA p-p
	f_n = 10Hz to 10kHz		4.5		pA rms
INPUT VOLTAGE RANGE					
Common-mode Voltage	Linear Operation	±(V_{CC}-6)	±(V_{CC}-3)		V
Common-mode Rejection	f = DC, V_{CM} = ±22	70	110		dB
POWER SUPPLY					
Rated Voltage			±28		V
Voltage Range, derated		±10		±34	V
Current, quiescent			±2.6	±5	mA
TEMPERATURE RANGE					
Operating	T_{case}	-25		+85	°C
Storage		-65		+150	°C

TABLE I. Electrical Specifications

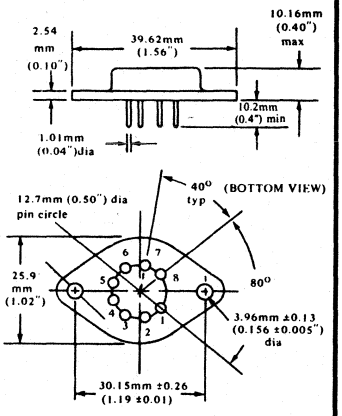
ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range	±34VDC
Internal Power Dissipation[1]	45W
Differential Input Voltage[2]	±62VDC
Input Voltage Range[2]	±31VDC
Storage Temperature Range	-65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C
Output Short-Circuit Duration[3]	Continuous
Junction Temperature	150°C

1. Package must be derated based on a junction to case thermal resistance of 2.8°C/W, or a junction to ambient thermal resistance of 30°C/W.
2. For supply voltages less than ±34VDC, the absolute maximum voltage is three volts less than supply voltage.
3. Safe Operating Area and Power Derating Curves must be observed.
4. With R±SC = 0.

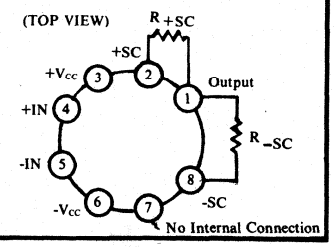
MECHANICAL

TO-3



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

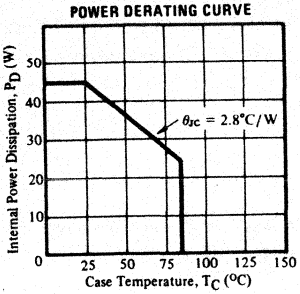
CONNECTION DIAGRAM



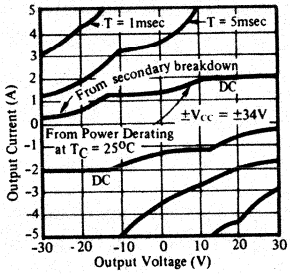
TYPICAL PERFORMANCE CURVES

(Typical at 25°Case and $\pm V_{cc} = \pm 28$ VDC unless otherwise noted.)

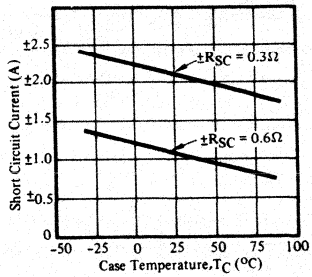
POWER DERATING CURVE



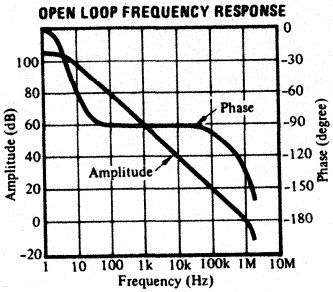
SAFE OPERATING AREA



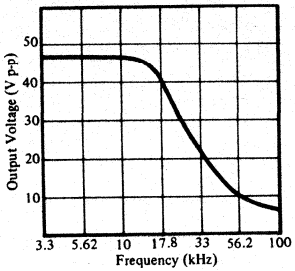
CURRENT LIMITING



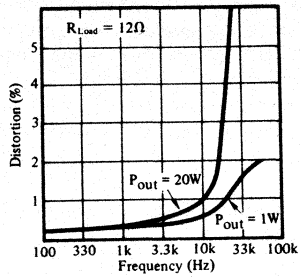
OPEN LOOP FREQUENCY RESPONSE



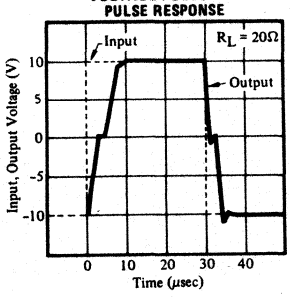
OUTPUT VOLTAGE VS FREQUENCY



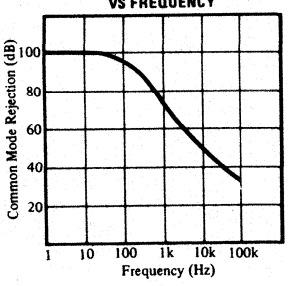
HARMONIC DISTORTION



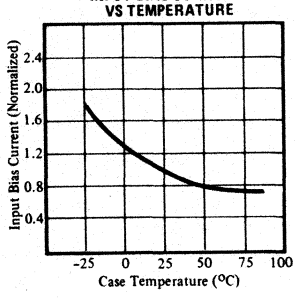
VOLTAGE FOLLOWER PULSE RESPONSE



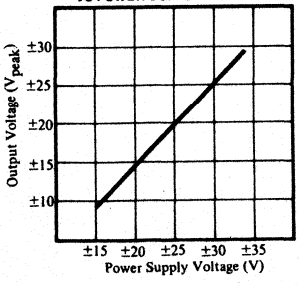
COMMON MODE REJECTION VS FREQUENCY



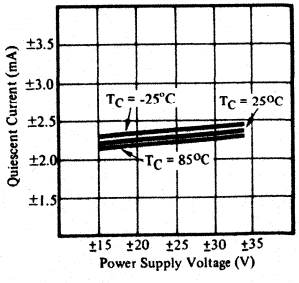
INPUT BIAS CURRENT VS TEMPERATURE



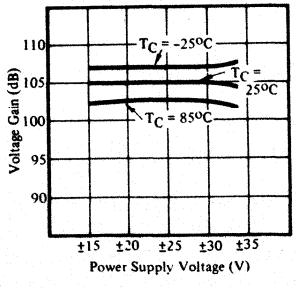
OUTPUT VOLTAGE SWING VS POWER SUPPLY VOLTAGE



QUIESCENT CURRENT VS POWER SUPPLY VOLTAGE



OPEN LOOP GAIN VS POWER SUPPLY VOLTAGE



INSTALLATION AND OPERATING INSTRUCTIONS

GENERAL PRECAUTIONS

CURRENT LIMITING

It is recommended that during initial amplifier setup, particularly in breadboarding and when a lack of familiarity with the amplifier exists, that the current limit be set at about 250mA ($R_{SC} \cong 2.6\Omega$). This will allow verification of the circuit and will minimize the possibility of damaging the amplifier. Later, when the circuit configuration and connections have been proven, the current limits can be raised to the desired value.

PROPER GROUNDING & POWER SUPPLY BYPASSING

Particular attention should be given to proper grounding practices because the large output currents can cause significant ground loop errors. Figure 1 illustrates proper connections.

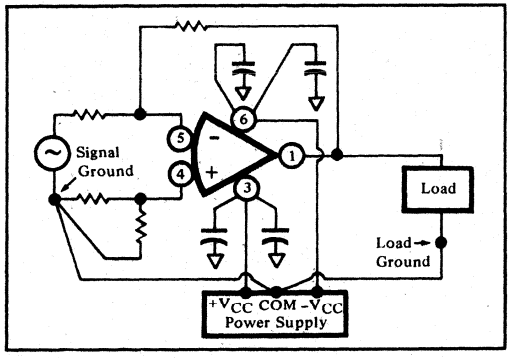


FIGURE 1. Proper Power Supply Connections.

Note that the connections are such that the load current does not flow through the wire connecting the signal ground point to the power supply common. Also, power supply and load leads should be run physically separated from the amplifier input and signal leads.

The amplifier should be power supply bypassed with 50μF tantalum capacitors connected in parallel with 0.01 μF ceramic capacitors connected as close to pins 3 and 6 as possible. The capacitors should be connected to the load ground rather than the signal ground.

CURRENT LIMITS

The amplifier is designed so that both the positive and negtive load current limits can be adjusted with external resistors, R_{+SC} and R_{-SC} respectively. The value of the resistors are given by the following equation:

$$R_{SC} = \frac{0.65 \text{ (volts)}}{I_{limit} \text{ (amps)}}$$

I_{limit} is the desired maximum current. The maximum power dissipation of the resistors is $P_{max} = R_{SC} (I_{limit})^2$. The current limits determined by the equations above are accurate to about ±10%. The variation of I_{limit} vs temperature is shown in the Typical Performance Curves.

The amplifier should be used with as low a current limit as possible for the particular application. This will minimize the chance of damaging the amplifier under abnormal load conditions and increase reliability by limiting the internal power dissipation of the amplifier.

THERMAL CONSIDERATIONS

The 3573AM is rated for 150°C maximum junction temperature. The thermal resistance from junction to case (θ_{jc}) is 2.8°C/W per watt. The corresponding Power Derating Curve is given in the Typical Performance Curves section.

The internal power dissipation of the amplifier is given by the equation $P_D = P_{DQ} + P_{DL}$ where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipated in the output stage due to the load.

The thermal resistance of the required heat sink (θ_{hs}) can be determined from the equation:

$$\theta_{hs} = \frac{T_J - T_A}{P_D} - \theta_{jc}$$

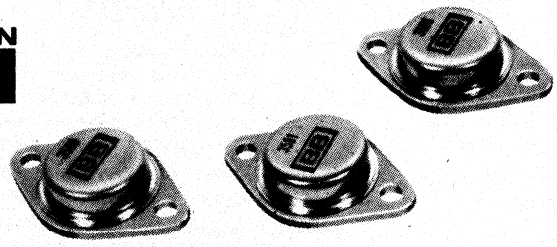
where T_J is the desired amplifier junction temperature (+150°C max), T_A is the ambient temperature, P_D is the amplifier's dissipation, $P_D = P_{DQ} + P_{DL}$, and θ_{jc} is the junction to case thermal resistance of the amplifier.

The electrically isolated case of the 3573AM simplifies mounting the amplifiers to the heat sink (and the heat sink to any other assemblies) since there is no need for electrical insulation. Thermal joint compound and lock washers should be used to prevent mechanical relaxation due to thermal stresses.

SAFE OPERATING AREA

There are additional constraints on the output voltage and current other than those just due to the maximum internal power dissipation of the amplifiers. These are related to the prevention of secondary breakdown in the output stage transistors. These restrictions are shown in the SAFE OPERATING AREA CURVES in the Typical Performance Curves.

BURR-BROWN



3580
3581
3582

High Voltage OPERATIONAL AMPLIFIERS

FEATURES

- HIGH OUTPUT SWINGS, up to ±145V (3582)
- LARGE LOAD CURRENTS, up to ±60mA (3580)
- DIFFICULT TO DAMAGE, automatic thermal shutoff
- REDUCES SOURCE LOADING, 10^{11} Ω Input Z
- PRESERVES SYSTEM ACCURACY, 110dB CMR 20pA bias current

DESCRIPTION

The 3580 series is the first family of Integrated Circuit operational amplifiers which will provide output voltage swings of up to ±145V.

The monolithic FET input stage has low bias currents (20pA) which minimized the offset voltages caused by the bias current and the large resistance normally associated with high voltage circuits.

The 3580 series is packaged in a TO-3 package which will dissipate over 3W of power without a heat sink and 4.5W with a suitable heat sink.

The input stage is protected against overvoltages and the output stage is protected against short-circuits-to-ground. A special thermal sensing circuit prevents damage to the amplifier by automatically shutting the amplifier down when too much power is being dissipated.

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PDS-313A

Printed in U.S.A. July, 1978

THEORY OF OPERATION

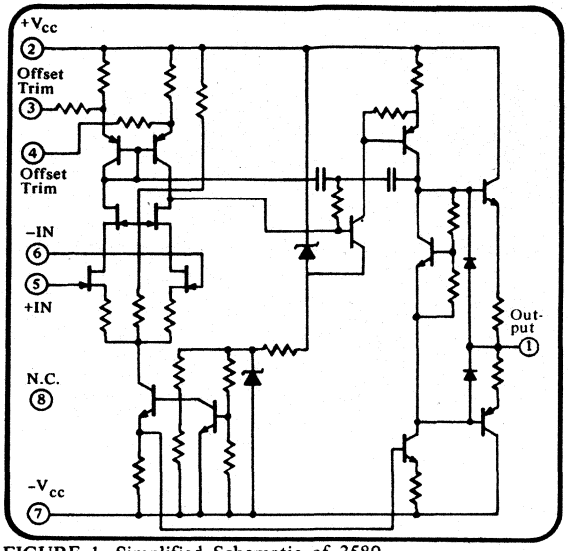


FIGURE 1. Simplified Schematic of 3580.

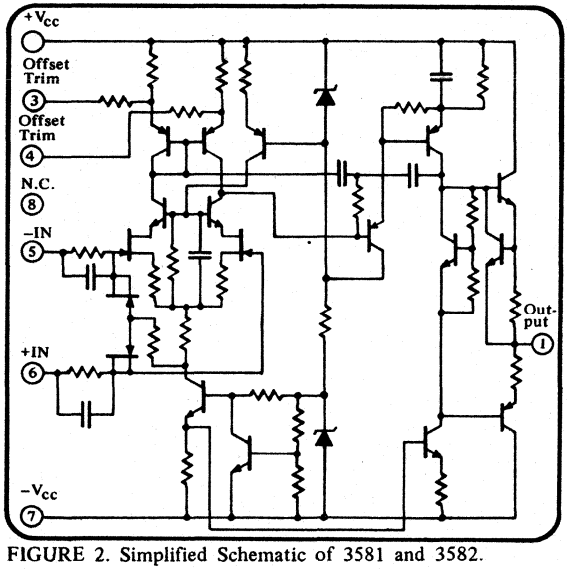


FIGURE 2. Simplified Schematic of 3581 and 3582.

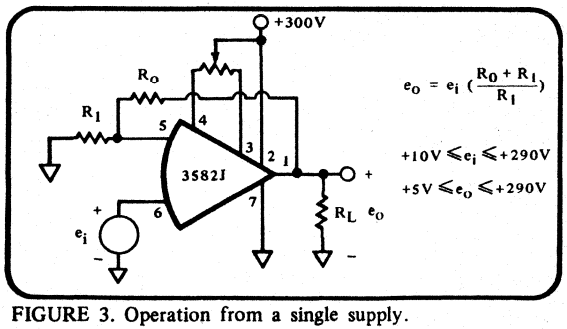


FIGURE 3. Operation from a single supply.

The 3580 family of integrated circuit high voltage amplifiers provides performance which previously was only available in bulky modular packages. In addition to the smaller size and inherent reliability, the integrated circuit construction offers other advantages not normally available in modular or discrete component units. The amplifiers have thermal sensing and shut-off circuitry which automatically turns the amplifier off when the internal temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating the input stage current source when the temperature reaches a critical level. As this happens, the output load current limits at a safe value and the amplifier's quiescent current decreases.

If the cause of the abnormal power dissipation is continuous (such as a short circuit across the load) the output current may remain at a low value or oscillate between 2 values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal condition is removed.

The incorporation of thermal sensing and shut-off in the amplifier will allow the use of a smaller heat sink than would otherwise be required. This is due to the fact that the amplifier will protect itself and does not require a massive heat sink for protection under abnormal conditions.

Another unique feature of the 3580 family is the thorough testing the unit receives. In addition to the normal tests, all amplifiers are 100% tested for input protection at its full rated differential voltage ($+V_{CC}$-V_{CC}). Each unit is also 100% tested for output short circuit to common at maximum supply voltage.

The 3581 and 3582 have an unique feature that is important in many high voltage applications. In these two models the input bias current is virtually independent of the applied common mode voltage. This is accomplished by the true cascode input stage which keeps the drain to source voltage of the input transistors constant as the common mode voltage changes.

OPERATION FROM A SINGLE SUPPLY

It may be desirable in some applications to operate the amplifiers from a single supply. The circuit in Figure 3 illustrates a typical application.

Note that there are restrictions on the input and output voltages (e_i and e_o) which are necessary in order to keep the amplifier circuits operating in a linear manner.

It should be noted that when the 3581 and 3582 amplifiers are operated from a single supply, the output stage, which is still short circuit current limited and thermally protected, is not protected against short circuits to ground (the 3580 will still be short circuit protected under these conditions). When the amplifiers are operated from a single supply, the voltage across one of the output transistors is high enough that secondary breakdown is a consideration. The output current must be limited in order to prevent damage. This can be done by keeping the load resistor larger than 5k ohms for the 3582 and greater than 1k ohm for the 3581.

SPECIFICATIONS

Typical at 25°C and $\pm V_{cc}$ max unless otherwise noted.

ELECTRICAL

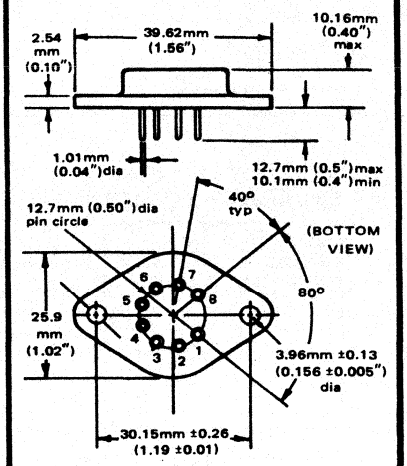
MODELS	3580J	3581J	3582J
POWER SUPPLY			
Voltage, $\pm V_{cc}$	±15 to ±35 Vdc	±32 to ±75 Vdc	±70 to ±150 Vdc
Quiescent Current, max	±10 mA	±8 mA	±6.5 mA
RATED OUTPUT			
Voltage, $\pm(\lvert V_{cc}\rvert -5)$Vdc, min	±10 to ±30 Vdc	±27 to ±70 Vdc	±65 to ±145 Vdc
Current, min	±60 mA	±30 mA	±15 mA
Current, Short Circuit	±100 mA	±50 mA	±25 mA
Load Capacitance, max	*	10 nF	*
OPEN LOOP GAIN			
No Load, dc	106 dB	112 dB	118 dB
Rated Load, dc, min	86 dB	94 dB	100 dB
FREQUENCY RESPONSE			
Unity Gain Bandwidth, Small Signal	*	5 MHz, min	*
Full Power Bandwidth	100 kHz	60 kHz	30 kHz
Slew Rate	15 V/μs	20V/μs	20 V/μs
Settling Time, 0.1%	*	12 μs	*
INPUT OFFSET VOLTAGE			
Initial @ 25°C, max	±10 mV	±3 mV	±3 mV
Drift vs Temp, max	±30 μV/°C	±25 μV/°C	±25 μV/°C
Drift vs Supply Voltage	100 μV/V	20 μV/V	20 μV/V
Drift vs Time	100 μV/mo	50 μV/mo	50 μV/mo
INPUT BIAS CURRENT			
Initial @ 25°C, max	-50 pA	-20 pA	-20 pA
Drift vs Temp		doubles every 10°C	
Drift vs Supply Voltage	0.5 pA/V	0.2 pA/V	0.2 pA/V
INPUT OFFSET CURRENT			
Initial @ 25°C	*	±20 pA	*
Drift vs Temp	*	doubles every 10°C	*
Drift vs Supply Voltage	0.5 pA/V	0.2 pA/V	0.2 pA/V
INPUT IMPEDANCE			
Differential	*	$10^{11}\ \Omega \parallel 10$ pF	*
Common Mode	*	$10^{11}\ \Omega$	*
INPUT NOISE			
Voltage 0.01 Hz to 10 Hz p-p	*	5μV	*
10 Hz to 1 kHz rms	1 μV	1.7μV	1.7μV
Current 0.01 Hz to 10 Hz p-p	1 pA	0.3 pA	0.3 pA
INPUT VOLTAGE RANGE			
Max Safe Differential Voltage (1)	*	$(+V_{cc} + \lvert -V_{cc}\rvert)$	*
Max Safe Common Mode Voltage	*	$+V_{cc}$ to $-V_{cc}$	*
Common Mode Voltage, Linear Operation	$\pm(\lvert V_{cc}\rvert -8)$V	$\pm(\lvert V_{cc}\rvert -10)$V	$\pm(\lvert V_{cc}\rvert -10)$V
Common Mode Rejection	86 dB	110 dB	110 dB
TEMPERATURE RANGE (Case)			
Specification	*	0°C to 70°C	*
Operating	*	-55°C to +125°C	*
Storage	*	-55°C to +150°C	*

*Specifications same for all models.

(1) On Models 3581 and 3582 the inputs may be damaged by pulses at pins 5 or 6 with dV/dt > 1V/ns. Any possible damage can be eliminated by limiting the input current to 150 mA with external resistors in series with those pins. No external protection is needed for slower voltage.

MECHANICAL

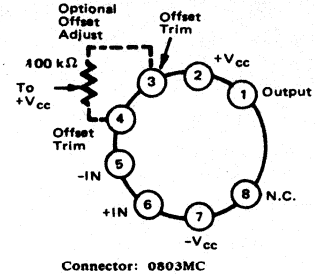
TO-3



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

CONNECTION DIAGRAM

(TOP VIEW) *



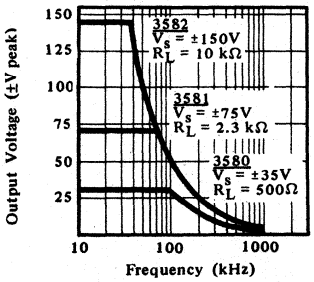
Connector: 0803MC
Heat sink: 0803HS
0804HS
0805HS

* The case is electrically isolated. It is recommended that the case be grounded during use.

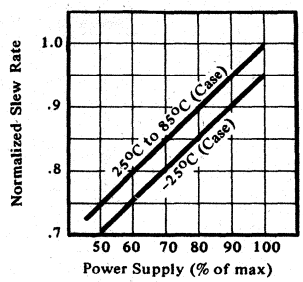
TYPICAL PERFORMANCE CURVES

Typical at 25°C and $\pm V_{cc}$ max unless otherwise noted.

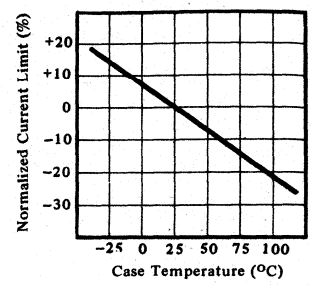
OUTPUT VOLTAGE vs FREQUENCY



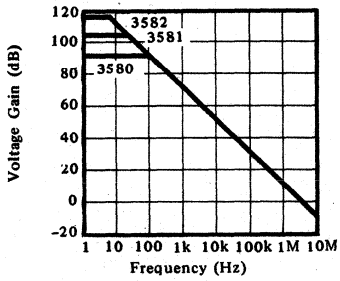
SLEW RATE vs SUPPLY VOLTAGE @ FULL LOAD



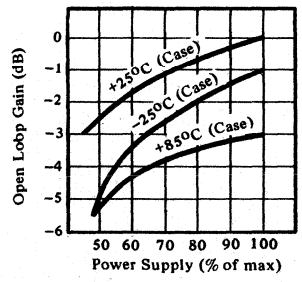
CURRENT LIMIT vs TEMPERATURE



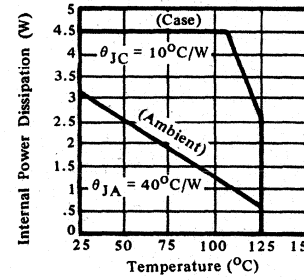
OPEN LOOP FREQUENCY RESPONSE–FULL LOAD



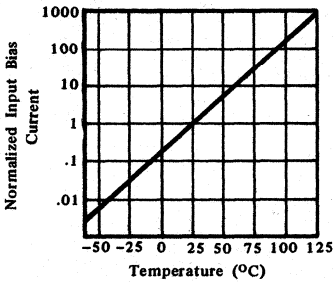
OPEN LOOP GAIN vs SUPPLY VOLTAGE @ MAX LOAD



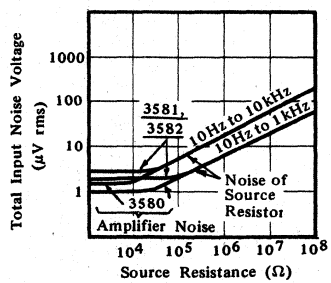
MAXIMUM POWER DISSIPATION



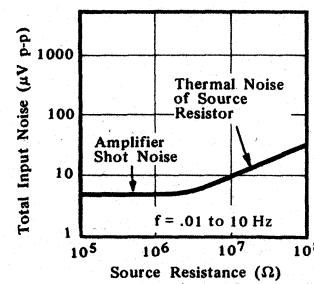
NORMALIZED INPUT BIAS CURRENT vs TEMPERATURE



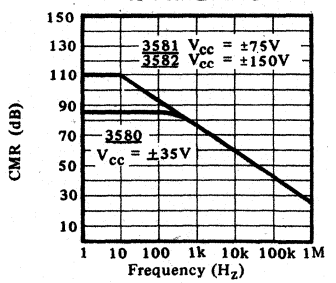
TOTAL INPUT NOISE VOLTAGE vs SOURCE RESISTANCE



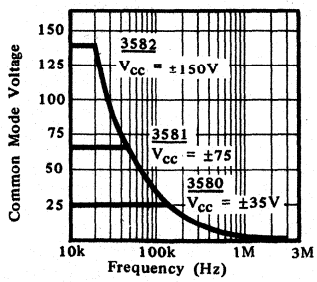
TOTAL LOW FREQUENCY INPUT NOISE vs SOURCE RESISTANCE



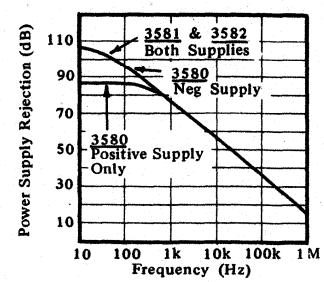
COMMON MODE REJECTION vs FREQUENCY



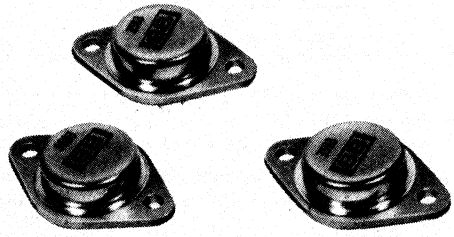
MAXIMUM COMMON MODE VOLTAGE vs. FREQUENCY



POWER SUPPLY REJECTION vs FREQUENCY



BURR-BROWN



3583

High Voltage - High Current OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT SWINGS, up to ±140V
- LARGE LOAD CURRENTS, ±75mA
- PROTECTED OUTPUT STAGE, automatic thermal shutoff
- REDUCES SOURCE LOADING, $10^{11}\Omega$ Input Z
- PRESERVES SYSTEM ACCURACY, 110dB CMR 20pA bias current

DESCRIPTION

The 3583 is the first integrated circuit operational amplifier to provide output voltage swings of ±140V with currents as high as ±75mA.

The amplifier operates over a wide supply range (±50VDC to ±150VDC) and has excellent input characteristics (110dB CMR, 3mV E_{os}, 25μV/°C $\Delta E_{os}/\Delta T$).

The monolithic FET input stage has low bias current (20pA) which minimizes the offset voltages caused by the bias current and the large resistances normally associated with high voltage circuits.

The input stage is protected against overvoltages and the output stage is protected against short circuits to ground for supply voltages below ±100VDC. A special thermal sensing circuit prevents damage to the amplifier by automatically shutting the amplifier down when too much power is being dissipated.

Two temperature ranges are available: 0°C to +70°C (3583JM) and -25°C to +85°C (3583AM).

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PDS-343A

Printed in U.S.A. July, 1978

DESCRIPTION

The 3583 is a high, voltage high output current integrated circuit operational amplifier. Its ease of use, compact size, and excellent input and output specifications makes it well suited for a wide variety of high voltage applications.

The equivalent circuit for the 3583 is shown in Figure 1. The design uses a monolithic FET input stage for high input impedance, low bias current, and low voltage drift versus temperature. The offset voltage at 25°C and the drift versus temperature are compensated by state-of-the-art laser trimming techniques. They are low enough so that user trimming will not be required in most applications. The high input impedance provides negligible source impedance loading errors when the noninverting circuit configuration is used. The low bias currents minimize offset errors when large values of source and feedback resistors are used.

A true cascode input stage is used together with considerable protection circuitry. There are voltage limiting transistors to prevent damage due to reverse bias breakdown of the input pair and current limiting resistors to limit the input current to 1mA with the inputs at ±150 volts. The units are conservatively rated (and 100% tested) at full rated differential voltage (+150 and -150V) but typically will withstand a 50% overvoltage without damage.

The unit operates over a wide supply range (±50V to ±150V) with outstanding common-mode rejection (110dB). It also has another feature which is important in many high voltage applications. The input bias current is virtually independent of applied common-mode voltage. The output circuit has a unique protection feature which is only practical in integrated circuit amplifiers - self contained automatic thermal sensing and shut off circuitry which automatically turns the amplifier off when the internal temperature reaches approximately 150°C.

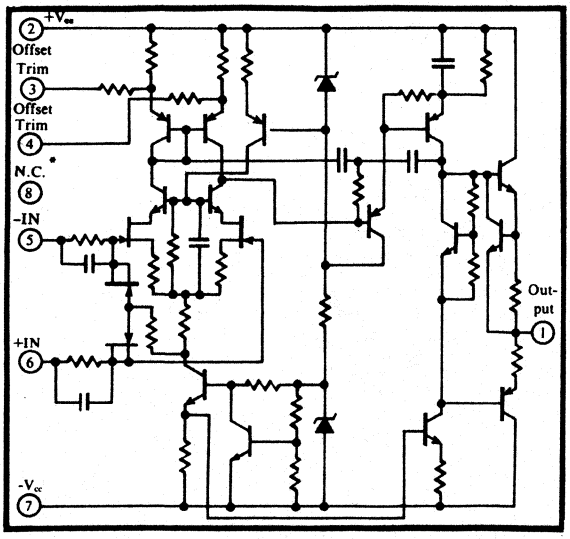


FIGURE 1. 3583 Equivalent Circuit.
(* N.C. = No internal connection.)

This is accomplished by sensing the subtrate temperature and deactivating the amplifiers biasing network when the temperature reaches 150°C. As this happens, the output load current limits at a safe value and the amplifier's quiescent current decreases. The output current will remain at a low value or oscillate between two values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal load condition is removed.

Internal thermal protection removes some of the constraints of power derating for abnormal operating conditions. The amplifier will protect itself for many conditions of excess power dissipation (see POWER DERATING CURVE, page 1-120). This allows the use of a smaller heat sink to protect against abnormal output conditions since the amplifier has its own internal protection for many conditions of excess power dissipation. The output constraints of the SAFE OPERATING AREA CURVES (page 1-120) must still be observed.

The 3583 has several other features that improve its utility. For instance, the metal case of the unit is completely electrically isolated. (This can be contrasted to most power semiconductors where the case is connected to the collector of the device.) This simplifies mounting and reduces cost since the need for insulating spacers and bushings is eliminated. The hermetically sealed package improves reliability and will withstand severe environments better than discrete component amplifiers. The small package size reduces weight and makes mounting more convenient.

SPECIFICATIONS

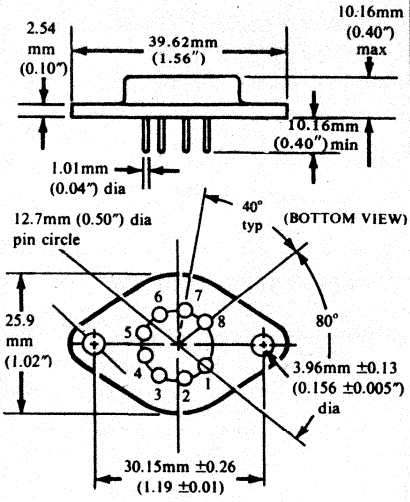
ELECTRICAL

Typical at 25°C and $\pm V_{cc}$ max unless otherwise noted.

MODELS	3583AM	3583JM
POWER SUPPLY		
Voltage, $\pm V_{cc}$	±50 to ±150 VDC	
Quiescent Current, max	8.5mA	
RATED OUTPUT		
Voltage, ± (| V_{cc} | -10)VDC, min	±40 to ±140 VDC	
Current, min	±75mA	
Current, Short Circuit	±100mA	
Load Capacitance, max	10 nF	
OPEN LOOP GAIN		
No Load, DC	118dB	
Rated Load, DC	94dB min, 105dB, typ	
FREQUENCY RESPONSE		
Unity Gain Bandwidth, Small Signal	5 MHz	
Full Power Bandwidth R_L = 10kΩ	60 kHz	
Slew Rate	30 V/μs	
Settling Time, 0.1%	12 μs	
INPUT OFFSET VOLTAGE		
Initial @ 25°C, max	±3 mV	
Drift vs Temp, max	±25 μV/°C	
Drift vs Supply Voltage	20 μV/V	
Drift vs Time	50 μV/mo	
INPUT BIAS CURRENT		
Initial @ 25°C, max	-20 pA	
Drift vs Temp	doubles every 10°C	
Drift vs Supply Voltage	0.2 pA/V	
INPUT OFFSET CURRENT		
Initial @ 25°C	±20 pA	
Drift vs Temp	doubles every 10°C	
Drift vs Supply Voltage	0.2 pA/V	
INPUT IMPEDANCE		
Differential	10^{11} Ω || 10 pF	
Common Mode	10^{11} Ω	
INPUT NOISE		
Voltage 0.01 Hz to 10 Hz p-p	5 μV	
10 Hz to 1 kHz rms	1.7 μV	
Current 0.01 Hz to 10 Hz p-p	0.3 pA	
INPUT VOLTAGE RANGE		
Max Safe Differential Voltage(1)	(+V_{cc} + | -V_{cc} |)	
Max Safe Common Mode Voltage	+V_{cc} to -V_{cc}	
Common Mode Voltage, Linear Operation	±(| V_{cc} | -10)V	
Common Mode Rejection	110dB	
TEMPERATURE RANGE (Case)		
Specification:	-25°C to +85°C	0°C to 70°C
Operating	-55°C to +125°C	
Storage	-55°C to +125°C	

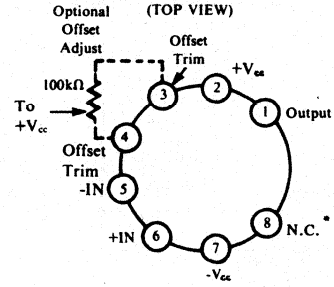
MECHANICAL

TO-3



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]

Connection Diagram



Connector: 0803MC

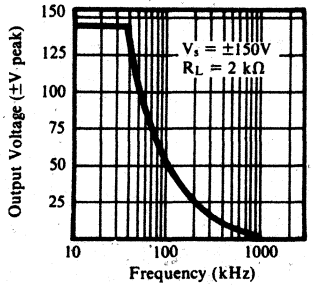
* No internal connection.
The metal case is electrically isolated. It is recommended that the case be grounded during use.

(1) The inputs may be damaged by pulses at pins 5 or 6 with $dV/dt \geq 1$ V/ns. Any possible damage can be eliminated by limiting the input current to 150 mA with external resistors in series with those pins. No external protection is needed for slower voltage changes.

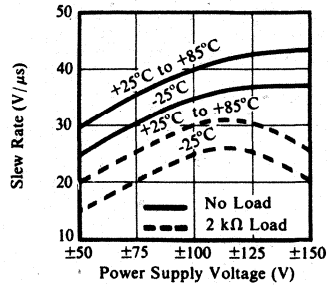
TYPICAL PERFORMANCE CURVES

Typical at 25°C case and $\pm V_{cc}$ max unless otherwise noted.

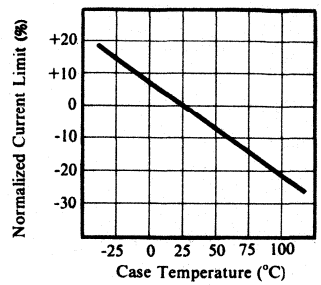
OUTPUT VOLTAGE vs. FREQUENCY



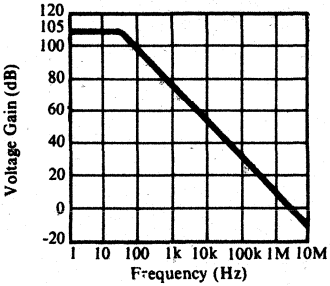
SLEW RATE vs. SUPPLY VOLTAGE



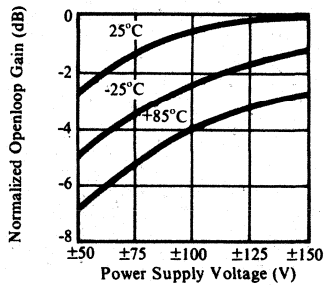
CURRENT LIMIT vs. TEMPERATURE



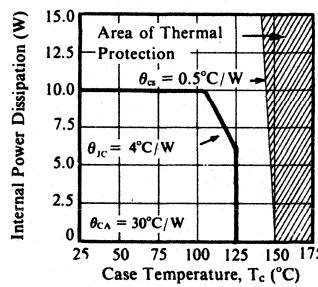
OPEN LOOP FREQUENCY RESPONSE—FULL LOAD



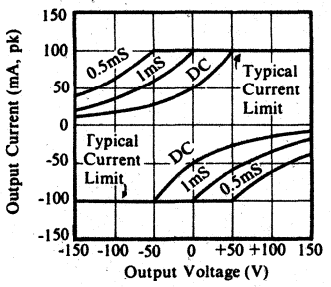
OPEN LOOP GAIN vs. SUPPLY VOLTAGE @ FULL LOAD



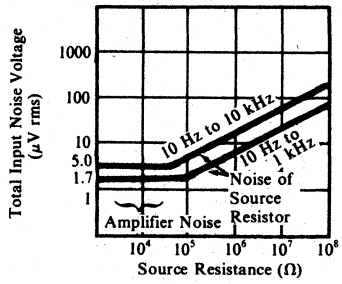
RECOMMENDED POWER DERATING



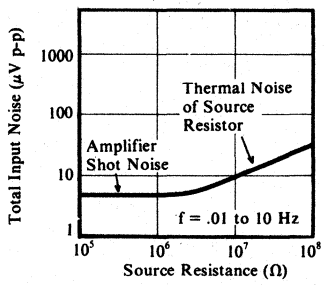
RECOMMENDED SAFE OPERATING AREA (Secondary Breakdown)



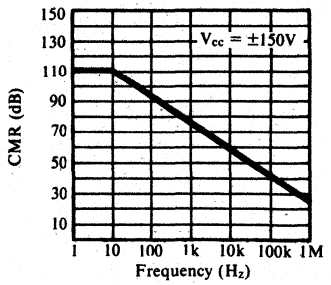
TOTAL INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



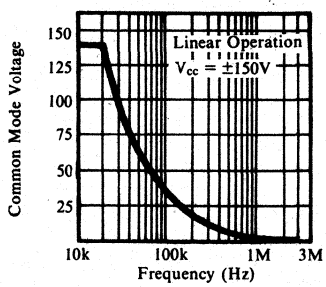
TOTAL LOW FREQUENCY INPUT NOISE vs. SOURCE RESISTANCE



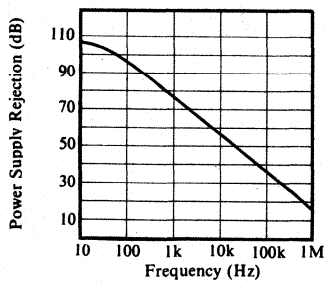
COMMON-MODE REJECTION vs. FREQUENCY



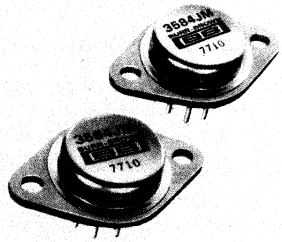
COMMON-MODE VOLTAGE vs. FREQUENCY



POWER SUPPLY REJECTION vs. FREQUENCY



BURR-BROWN



3584

High Voltage OPERATIONAL AMPLIFIER

FEATURES

- TYPICAL GAIN-BANDWIDTH, 50MHz
- OUTPUT, +145V
- PROTECTED OUTPUT, automatic thermal shutoff
- BIAS CURRENT, -20pA
- CMR, 110dB
- SLEW RATE, 150V/usec

APPLICATIONS

- ANALOG SIMULATORS
- DIGITALLY-CONTROLLED POWER SUPPLIES
- CRT DEFLECTION
- ELECTROSTATIC TRANSDUCERS

DESCRIPTION

The 3584 is a high voltage, integrated circuit operational amplifier that will provide up to ±145V output.

The amplifier will provide a gain-bandwidth product of 20MHz minimum, 50MHz typical. The amplifier uses external frequency compensation (one R and one C) so that the user may optimize the bandwidth and slew rate for his particular application.

The amplifier operates over a wide supply range (±70VDC to ±150VDC) and has excellent input characteristics (110dB CMR, 3mV E_{os}, and 25μV/°C E_{os} Drift). The input stage is a FET. The low -20pA bias current minimizes the offset errors caused by the large value resistors normally used in high voltage circuits.

The input stage is protected against overvoltages and the output stage is protected against short circuits to ground. A special thermal sensing circuit helps to prevent damage to the amplifier by automatically shutting the amplifier down when too much power is being dissipated.

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PDS-376A

Printed in U.S.A. July, 1978

DISCUSSION

The 3584 is a high voltage, integrated circuit operational amplifier. Its ease of use, compact size, and excellent input and output specifications makes it well suited for a wide variety of high voltage and high speed applications.

The design uses a monolithic FET input stage for high input impedance, low bias current, and low voltage drift versus temperature. The offset voltage and the drift are laser trimmed. They are low enough so that user trimming will not be required in most applications.

To achieve the high common-mode voltage capability and rejection a true cascode input stage is used together with considerable protection circuitry. There are voltage limiting diodes to prevent damage due to reverse bias breakdown of the input pair and current limiting resistors to limit the steady state input current to 1mA with the inputs at ±150 volts. The units are conservatively rated (and 100% tested) at full rated differential voltage (+150 and -150V) but typically will withstand a 50% overvoltage without damage.

It also has another feature which is important in many high voltage applications. The input bias current is virtually independent of applied common-mode voltage. This is a benefit of the true cascode input stage which keeps the drain to source voltage of the input transistors constant as the common-mode voltage changes.

The amplifier contains automatic thermal sensing and shut-off circuitry which automatically turns the amplifier off when the internal (substrate) temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating all current sources when the temperature reaches a critical level. As this happens, the output current gradually decreases to zero. The output current may remain at a low value or oscillate between 2 values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal condition is removed.

The incorporation of thermal sensing and shut-off in the amplifier will require a smaller heat sink than normal. This is due to the fact that the amplifier will protect itself and does not require a massive heat sink for protection under abnormally high power dissipation.

The 3584 has several other features that improve its utility. The metal case of the unit is completely electrically isolated. This simplifies mounting and reduces cost since the need for insulating spacers is eliminated. The hermetically sealed package improves reliability and will withstand severe environments better. And the small package size reduces weight and makes mounting more convenient.

OPERATION FROM A SINGLE SUPPLY

It may be desirable in some applications to operate the amplifiers from a single supply. The circuit in Figure 1 illustrates a typical application. Note that there are restrictions on the input and output voltages (e_i and e_o) which are necessary in order to keep the amplifier circuits operating in a linear manner.

It should be noted that when the amplifier is operated from a single supply, the output stage, which is still short circuit current limited and thermally protected, is not protected for short circuits to ground under all operating conditions. Consult the safe operating area curve.

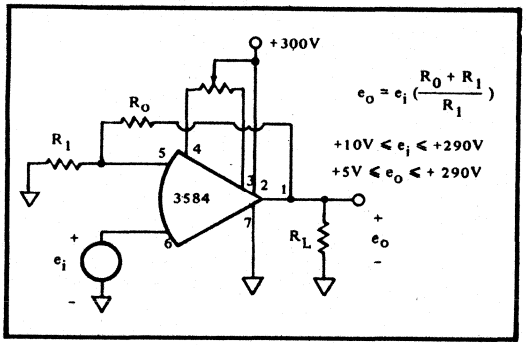


FIGURE 1. Operation from a single supply.

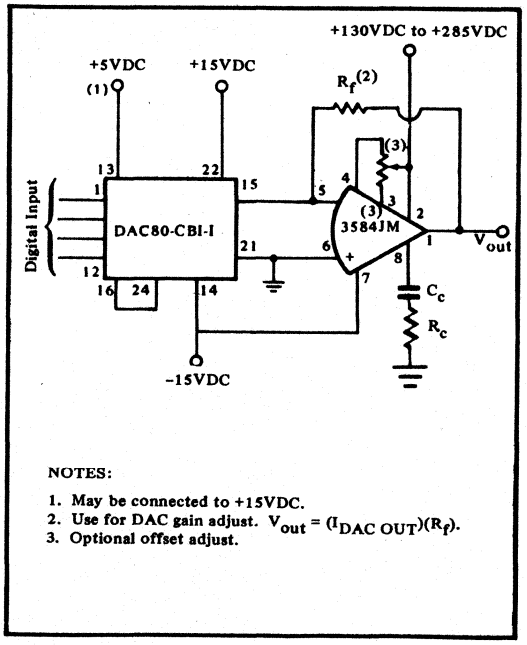


FIGURE 2. High Speed, High Voltage DAC.

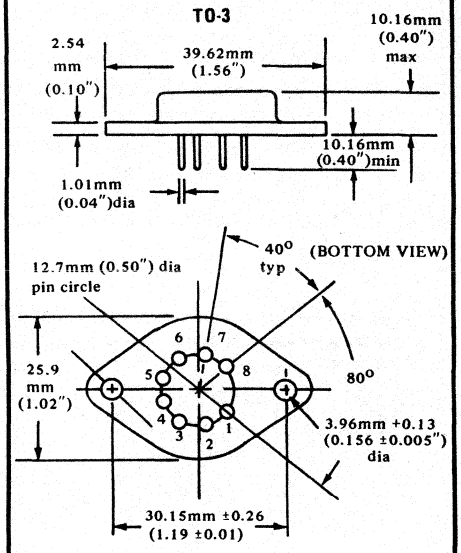
SPECIFICATIONS

ELECTRICAL

Typical at 25°C and $\pm V_{cc}$ max unless otherwise noted.

MODELS	3584JM
POWER SUPPLY	
Voltage, $\pm V_{cc}$	±70 to ±150 VDC
Quiescent Current, max	±6.5mA
RATED OUTPUT	
Voltage, ± (| V_{cc} | -5)VDC, min	±65 to ±145 VDC
Current, min	±15mA
Current, Short Circuit	±25mA
Load Capacitance, max	10 nF
OPEN LOOP GAIN	
No Load, DC	120 dB
Rated Load, DC, min	100dB
FREQUENCY RESPONSE	
Unity Gain Bandwidth, Small Signal	7 MHz
Gain-bandwidth Product, f = 1 kHz, G = 100	20 MHz, min
Full Power Bandwidth, G = 100	135 kHz
Slew Rate, G = 100,	150 V/μs
Settling Time, 0.1%, G = 100	12 μs
INPUT OFFSET VOLTAGE	
Initial @ 25°C, max	3 mV
Drift vs Temp, max	25 μV/°C
Drift vs Supply Voltage	20 μV/V
Drift vs Time	50 μV/mo
INPUT BIAS CURRENT	
Initial @ 25°C, max	-20 pA
Drift vs Temp	doubles every 10°C
Drift vs Supply Voltage	0.2 pA/V
INPUT OFFSET CURRENT	
Initial @ 25°C	±20 pA
Drift vs Temp	doubles every 10°C
Drift vs Supply Voltage	0.2 pA/V
INPUT IMPEDANCE	
Differential	10^{11} Ω || 10 pF
Common Mode	10^{11} Ω
INPUT NOISE	
Voltage 0.01 Hz to 10 Hz p-p	5 μV
10 Hz to 1 kHz rms	1.7 μV
Current 0.01 Hz to 10 Hz p-p	0.3 pA
INPUT VOLTAGE RANGE	
Max Safe Differential Voltage(1)	(+V_{cc} + | -V_{cc} |)
Max Safe Common Mode Voltage	+V_{cc} to -V_{cc}
Common Mode Voltage, Linear Operation	±(| V_{cc} | -10)V
Common Mode Rejection	110dB
TEMPERATURE RANGE (Case)	
Specification:	0°C to 70°C
Operating	-55°C to +125°C
Storage	-55°C to +150°C

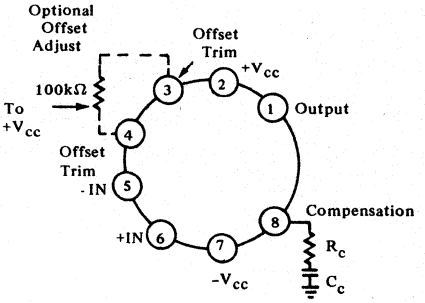
MECHANICAL



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]

CONNECTION DIAGRAM

(TOP VIEW)



Connector: 0803MC
Heatsinks: 0803HS, 0804HS, or 0805HS

Compensation		
Gain	C_c	R_c
1	10 nF	200Ω
10	500 pF	2kΩ
100	50 pF	20kΩ
1000	not required	

For intermediate values of gain, R and C values may be interpolated.

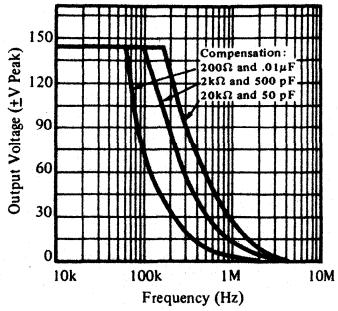
The case is electrically isolated. It is recommended that the case be grounded during use.

(1) The inputs may be damaged by pulses at pins 5 or 6 with $dV/dt \geq 1$ V/ns. Any possible damage can be eliminated by limiting the input current to 150mA with external resistors in series with those pins. No external protection is needed for slower voltage changes.

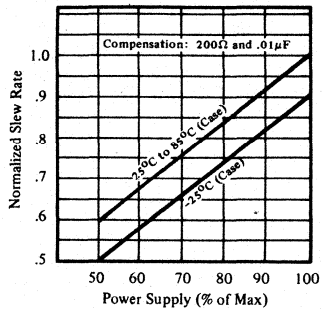
TYPICAL PERFORMANCE CURVES

Typical at 25°C and $\pm V_{CC}$ max unless otherwise noted.

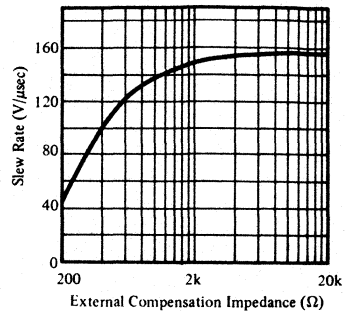
OUTPUT VOLTAGE vs FREQUENCY



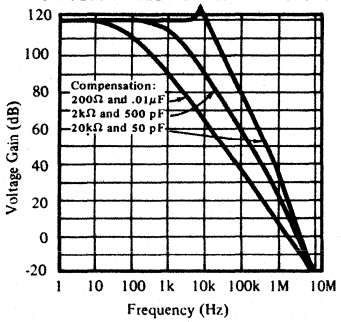
SLEW RATE vs SUPPLY VOLTAGE @ FULL LOAD



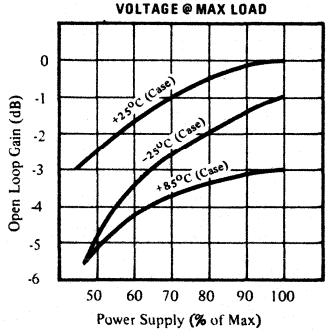
SLEW RATE vs COMPENSATION



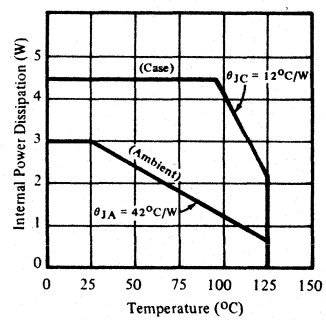
OPEN LOOP FREQUENCY RESPONSE FULL LOAD



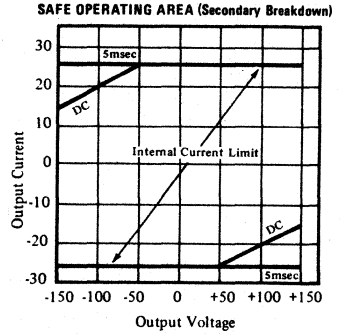
OPEN LOOP GAIN vs SUPPLY VOLTAGE @ MAX LOAD



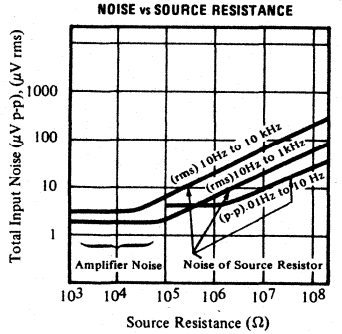
POWER DISSIPATION



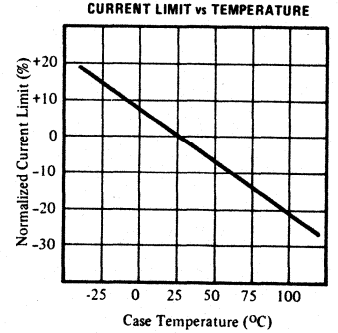
SAFE OPERATING AREA (Secondary Breakdown)



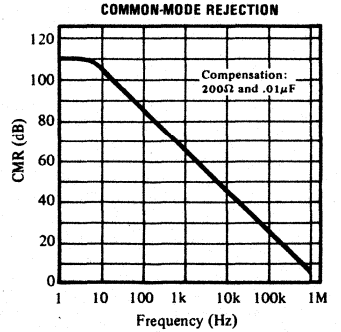
NOISE vs SOURCE RESISTANCE



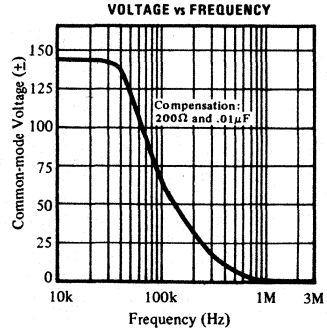
CURRENT LIMIT vs TEMPERATURE



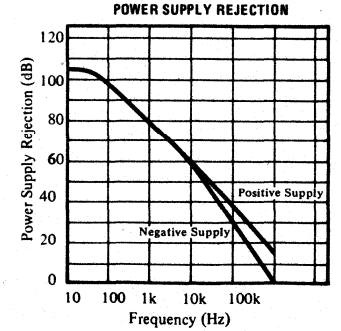
COMMON-MODE REJECTION



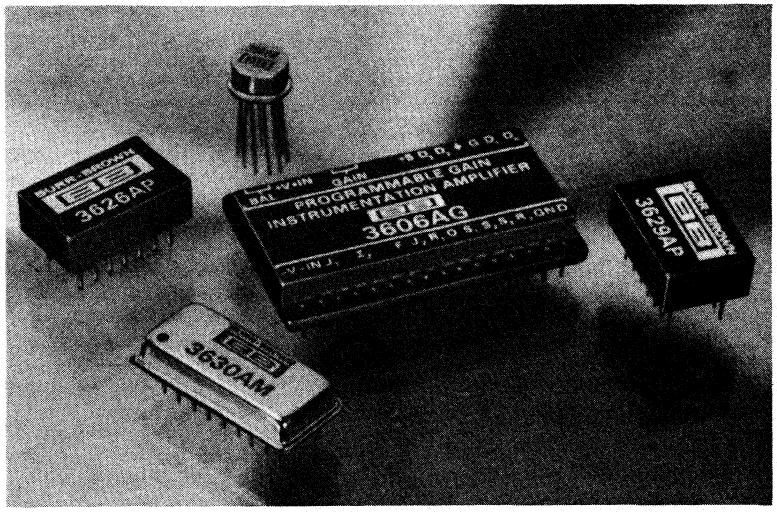
MAXIMUM COMMON-MODE VOLTAGE vs FREQUENCY



POWER SUPPLY REJECTION



2. INSTRUMENTATION AMPLIFIERS



WHAT IS AN INSTRUMENTATION AMPLIFIER?

An instrumentation amplifier is a closed-loop, differential input gain block. It is a committed circuit with the primary function of accurately amplifying the voltage applied to its inputs.

Ideally, the instrumentation amplifier responds only to the difference between the two input signals and exhibits extremely-high impedances between the two input terminals, and from each terminal to ground. The output voltage is developed single-ended with respect to ground and is equal to the product of amplifier gain and the difference of the two input voltages (see Figure 1).

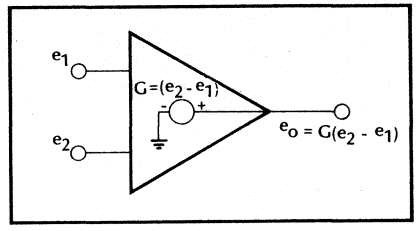


FIGURE 1. Idealized Model of an Instrumentation Amplifier.

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Product Data Sheets 2-7

The amplifier gain G is normally set by the user with a single external resistor. The properties of this model may be summarized as infinite input impedance, zero output impedance, the output voltage proportional to only the difference voltage ($e_2 - e_1$), a precisely known gain constant (implying no nonlinearity), and unlimited bandwidth. This amplifier would completely reject signal components common to both inputs (common-mode rejection) and would exhibit no DC offset voltage or drift.

CHARACTERISTICS OF INSTRUMENTATION AMPLIFIERS

It is desirable to achieve, as close as possible, the characteristics of the ideal instrumentation amplifier. The following paragraphs are a discussion of the, other-than-ideal, characteristics of the instrumentation amplifiers.

Input Impedance - A simple model of a realistic instrumentation amplifier is shown in Figure 2. The impedance Z_{id} represents the differential input impedance. The common-mode input impedance Z_{icm} is represented as two

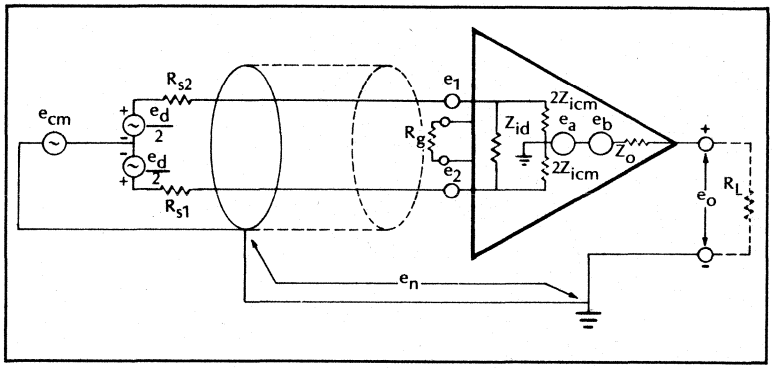


FIGURE 2. Simple Model of an Instrumentation Amplifier Shown in a Typical Application Configuration.

equal components, $2Z_{icm}$, from each input to ground. These finite resistances contribute an effective gain error due to loading of the source resistance. The instrumentation amplifier provides a load on the source of $Z_i = Z_{id} \| Z_{icm}$. If source impedance is $R_S = R_{S1} + R_{S2}$, the gain error caused by this loading is:

$$\text{Gain Error} = 1 - \frac{Z_i}{Z_i + R_s} = \frac{R_s}{Z_i + R_s} \cong \frac{R_s}{Z_i} \text{ if } Z_i \gg R_s$$

If R_S is 10kΩ and Z_i is 10MΩ,

$$\text{Gain Error} \cong \frac{10 \times 10^3}{10 \times 10^6} = 0.1\%$$

The DC common-mode input impedance Z_{icm} will be independent of gain. The DC differential input impedance Z_{id} may vary as a function of gain. Specifications give the worst case value. The nonzero output impedance of the amplifier will also create a gain error, the value of which depends on the load resistance.

Nonlinearity - The linearity of gain is possibly of more importance than the gain accuracy, since the value of the gain can be adjusted to compensate for simple gain errors. The nonlinearity is specified to be the peak deviation from a "best fit" straightline, expressed as a percent of peak-to-peak full scale output.

Common-mode Rejection - As illustrated in Figure 2, the output voltage has two components. One component is proportional to the differential input voltage $e_d = (e_2 - e_1)$. The second component is proportional to the common-mode

input voltage. The common-mode voltage which appears at the amplifier's input terminals is defined as $E_{CM} = e_2 + e_1/2$. This may consist of some common-mode voltage in the source itself, e_{cm}, (such as bridge excitation) plus any noise voltage, e_n, between the source common and the amplifier common. As shown in Figure 2, the constant G represents the differential amplifier gain factor (fixed by the external gain-setting resistor). The constant (G/CMRR) represents the common-mode signal gain of the amplifier. The CMRR (common-mode rejection ratio) is the ratio of differential gain to common-mode gain. Thus CMRR is proportional to the differential gain and CMRR increases as the differential (gain G) increases. Hence, CMRR is usually specified for the maximum and the minimum values of gain of the amplifier. The common-mode rejection may be expressed in dB as - CMRR (dB) = 20 $\log_{10}$ CMRR.

For an ideal instrumentation amplifier the output voltage component due to common-mode voltage should be zero. For a realistic instrumentation amplifier, the CMRR though very high, is still not infinite and so will cause an error voltage of E_{CM}/CMRR x G to appear at the output.

Source Impedance Unbalance - If the source impedances are unbalanced the source voltages ($e_{cm} + e_n$) are divided unequally upon the common-mode impedances and a differential signal is developed at the amplifier's input. This error signal cannot be separated from the desired signal. In the circuit in Figure 2 if $R_{s2} = 0$, $R_{s1} = 1k\Omega$, $e_{cm} + e_n = 10V$, and $Z_{cm} = 100M\Omega$, then the effect of unbalance is to generate a voltage.

$$e_2 - e_1 = 10V - 10V\frac{10^8}{10^8 + 10^3} = 10V\frac{10^3}{10^8 + 10^3} \cong \frac{10V}{10^5} = 0.1mV$$

If e_d full scale is 10mV then this error is:

$$\text{Error} = \frac{0.1mV}{10mV} = 1\% \text{ of full scale.}$$

Offset Voltage and Drift - Most instrumentation amplifiers are two stage devices - they have a variable gain input stage and a fixed gain output stage. If V_i and V_o are the offset voltages of the input and output stages respectively, then the amplifiers total offset voltage referred to the input (RTI) is E_{os} (RTI) = $V_i + V_o/G$ where G is the amplifier's gain. [Note that E_{os} (RTO) = E_{os} (RTI) x G]

The initial offset voltage is usually adjustable to zero and therefore, the voltage drift is the more signficant term since it cannot be nulled. The offset voltage drift also has two components - one due to the input stage of the amplifier and the other due to the output stage. When the amplifier is operated at high gain, the drift of the input stage predominates. At low values of gain, the drift of the output stage will be the major component of drift. When the total output drift is referred to the input, the effective input voltage drift is largest for low values of gain. Output voltage drift will always be lowest at low gains. If $\Delta V_i/\Delta T = 2\mu V/°C$ and $\Delta V_o/\Delta T = 500\mu V/°C$ and the amplifier in a gain of 1000V/V is nulled at 25°C, then at 65°C the offset voltage will be:

$$E_{os}\,(RTI)_{65^o} = 40^oC\,[2\mu V/^oC + (500\mu V/^oC/1000V/V)]$$
$$= 40^oC\,(2.5\mu V/^oC) = 100\mu V = 0.1mV$$

If the full scale input is 10mV then the error due to voltage drift is:

Error = 0.1mV/10mV = 1% of full scale.

Input Bias and Offset Currents - The input bias currents are the currents that flow out of (or into) either of the two inputs of the amplifier. They are the base currents for bipolar input stages and the JFET leakage currents for FET input stage. Offset currents are the difference of the two bias currents.

The bias currents flowing into the source resistances will generate offset voltages of $E_{os2} = I_{B2} \times R_{s2}$ and $E_{os1} = I_{B1} \times R_{s1}$. If $R_{s1} = R_{s2} = R_s/2$ the offset voltage at the input is $E_{os2} - E_{os1} = I_{os} \times R_x/2$. This input referred offset error may be compared directly with the input voltage to compute percent error. (Note that the source must be returned to power supply common or R_s will be infinite and the amplifier will saturate.)

APPLICATIONS OF INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are generally used in applications where extracting and accurately amplifying low level differential signals riding on high common-mode voltages (±10V) is very important. Such applications require high input impedance, high CMRR, low input noise, and excellent DC level stability (low offset voltage drift).

Instrumentation amplifiers are used as transducer amplifiers for various types of transducers such as strain gage bridges, load cells, thermistor networks, thermocouples, current shunts, biological probes, weather gages and so forth. Other applications include recorder preamplifiers, multiplexer buffers, servo error amplifiers, current sensors, signal conditioners in process control and data acquisition systems, and in general measurements of small differential signals riding on common-mode voltages.

The small size, low cost, and high performance of these amplifiers offer an attractive approach for data acquisition applications, that is, assigning a fixed-gain amplifier to each transducer and locating the amplifier physically near the transducer. This approach largely eliminates common-mode noise pickup problems since a high level signal (rather than a low level transducer signal) is then retransmitted to the data gathering station. The result is a higher signal/noise ratio at the output. Using one amplifier per point may well be more economical, as well as offering better performance and flexibility, than the approach of using low level multiplexers.

SELECTION GUIDE
Instrumentation Amplifiers

Description	Model	Gain: Range	Gain: Non-Linearity G = 100, max.	Rated Output (V/mA)	Input Parameters: CMR, DC to 60Hz, G = 10 1kΩ, Unbal., min	Input Parameters: Voltage vs Temp. max. (μV/°C)	Dynamic Response G = 100 ±3dB BW	Package		Page
PROGRAMMABLE GAIN										
Digitally* Controlled	3606A	1-1024	0.01%	±10/±5	86dB, G = 1	100μV/°C, typ.	15kHz	DIP		2-7
	3606B	1-1024	0.01%	±10/±5	86dB, G = 1	50μV/°C, typ.	15kHz	DIP		2-7
LOW DRIFT										
Lowest Drift	3620J	1-1000	±0.01%	±10/±10	74dB	±(10 + 2/G)	10kHz	Module		2-15
	3620J/16	1-1000	±0.01%	±10/±10	74dB	±(10 + 2/G)	10kHz	Module		2-15
	3620K	1-1000	±0.01%	±10/±10	74dB	±(10 + 0.5/G)	10kHz	Module		2-15
	3620K/16	1-1000	±0.01%	±10/±10	74dB	±(10 + 0.5/G)	10kHz	Module		2-15
	3620L	1-1000	±0.01%	±10/±10	74dB	±(10 + 0.25/G)	10kHz	Module		2-15
	3620L/16	1-1000	±0.01%	±10/±10	74dB	±(10 + 0.25/G)	10kHz	Module		2-15
Low Drift, Low Cost	3626AP	5-1000	±0.02%	±10/±5	74dB	±(6 + 10/G)	14kHz	DIP		2-22
	3626BP	5-1000	±0.01%	±10/±5	80dB	±(3 + 5/G)	14kHz	DIP		2-22
	3626CP	5-1000	±0.01%	±10/±5	80dB	±(1 + 5/G)	14kHz	DIP		2-22
	3629AM	5-1000	±0.007%	±10/±10	106dB	±(3 + 10/G)	30kHz	DIP		2-30
	3629AP	5-1000	±0.007%	±10/±10	106dB	±(3 + 10/G)	30kHz	DIP		2-30
	3629BM	5-1000	±0.004%	±10/±10	106dB	±(1.5 + 7.5/G)	30kHz	DIP		2-30
	3629BP	5-1000	±0.004%	±10/±10	106dB	±(1.5 +7.5/G)	30kHz	DIP		2-30
	3629CM	5-1000	±0.004%	±10/±10	106dB	±(0.75 + 5/G)	30kHz	DIP		2-30
	3629CP	5-1000	±0.004%	±10/±10	106dB	±(0.75 + 5/G)	30kHz	DIP		2-30
	3629SM	5-1000	±0.004%	±10/±10	106dB	±(1.5 + 7.5/G)	30kHz	DIP		2-30
Buffer, Unity-Gain	3627AM	1V/V, fixed	±0.001%[2]	±10/±5	90dB	30	800kHz	TO-99		2-26
Differential	3627BM	1V/V, fixed	±0.001%[2]	±10/±5	100dB	20	800kHz	TO-99		2-26
Very-High* Accuracy	3630AM	1-1000	±0.005%[3]	±10/±5	96dB	±(2 + 20/G)	25kHz	DIP		2-36
	3630BM	1-1000	±0.002%[3]	±10/±5	96dB	±(.75 + 10/G)	25kHz	DIP		2-36
	3630CM	1-1000	±0.002%[3]	±10/±5	96dB	±(.25 + 10/G)	25kHz	DIP		2-36
	3630SM	1-1000	±0.002%[3]	±10/±5	96dB	±(.75 + 10/G)	25kHz	DIP		2-36
General Purpose, Low Cost	3660J	1-1000	0.1%	±10/±10	76dB	±(10+1000/G)	72kHz	TO-100		2-42
	3660K	1-1000	0.03%	±10/±10	90dB	±(2 + 500/G)	72kHz	TO-100		2-42
	3660S	1-1000	0.03%	±10/±10	90dB	±(2 + 500/G)	72kHz	TO-100		2-42
	3662JP	1-1000	0.1%	±10/±10	76dB	±(5 + 1000/G)	72kHz	DIP		2-48
	3662KP	1-1000	0.05%	±10/±10	84dB	±(2 + 400/G)	72kHz	DIP		2-48

*New

1) Prices for 3620 family are for quantities (1-9) (10-24) (25-99). 2) Unity-gain. 3) G = 1-10.

GLOSSARY OF TERMS & DEFINITIONS
Instrumentation Amplifiers

COMMON-MODE INPUT IMPEDANCE
The effective impedance (resistance in parallel with capacitance) between either input of an amplifier and its common, or ground, terminal.

COMMON-MODE REJECTION (CMR)
When both inputs of a differential amplifier experience the same common-mode voltage (CMV), the output should, ideally, be unaffected. CMR is the ratio of the common-mode input voltage change to the differential input voltage (error voltage) which produces the same output change.

$$\text{CMR (in dB)} = 20 \log_{10} \text{CMV/Error Voltage}$$

Thus a CMR of 80dB means that 1V of common-mode voltage will cause an error of 100μV (referred to input).

COMMON-MODE REJECTION RATIO (CMRR)
The ratio of the differential voltage gain of an amplifier to its common-mode voltage gain.

COMMON-MODE VOLTAGE (CMV)
That portion of an input signal which is common to both inputs of a differential amplifier. Mathematically it is defined as the average of the signals at the two inputs:

$$\text{CMV} = e_1 + e_2/2$$

FEEDBACK
The return of a portion of the output signal from a device to the input of the device.

FULL POWER FREQUENCY RESPONSE
The maximum sinewave frequency at which a device can supply its peak-to-peak rated output voltage and current, without introducing significant distortion.

GAIN
The ratio of the output signal to the associated input signal of a device.

GAIN ERROR
The difference between the actual gain of an amplifier and the one predicted by the ideal gain expression.

INPUT BIAS CURRENT
The DC input current required at each input of an amplifier to provide zero output voltage when the input signal and input offset voltage are zero. The specified maximum is for each input.

INPUT BIAS CURRENT DRIFT
The rate of change of input bias current with temperature or time.

INPUT GUARDING
The use of an input shield that is sometimes driven to follow the voltage level of the input signal and, thereby, remove leakage and loss-inducing voltage differences between the input signal path and surrounding stray conduction paths.

INPUT OFFSET CURRENT
The difference of the two input bias currents in a differential amplifier.

INPUT OFFSET VOLTAGE
The DC input voltage required to provide zero voltage at the output of an amplifier when the input signal and input bias currents are zero.

INPUT PROTECTION
A means of protecting an input of a device from damage due to the application of excessive input voltage.

INSTRUMENTATION AMPLIFIER
A closed-loop differential input gain block exhibiting high input impedance and high common-mode rejection. Its primary function is to accurately amplify the voltage applied to its inputs.

NONLINEARITY
The peak deviation from a best straightline (curve fitting on input-output graph) expressed as a percent of peak-to-peak full scale output.

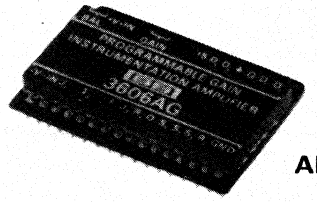
OVERLOAD RECOVERY TIME
The time required for the output of an amplifier to return from saturation to linear operation, following the removal of an input overdrive signal.

SETTLING TIME
The time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

SLEW RATE
The maximum rate of change of an output voltage when supplying the rated output.

BURR-BROWN

3606



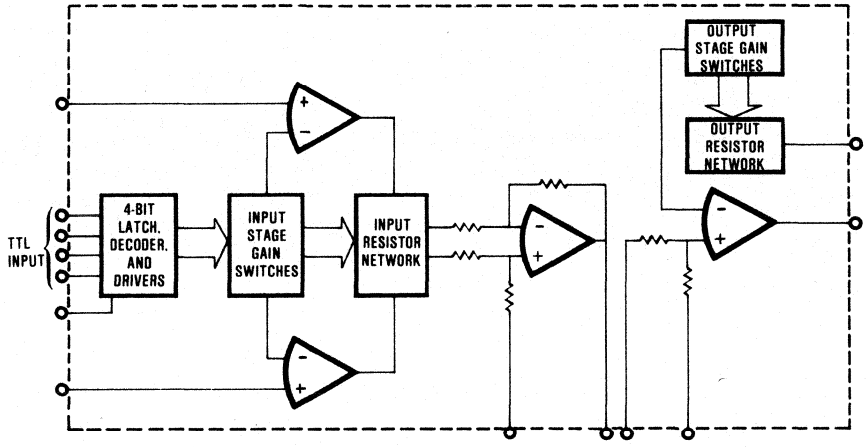
ADVANCE INFORMATION
Subject to Change

INST. AMP.

Digitally Controlled PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER

FEATURES

- 11 BINARY GAINS - 1, 2, 4, 8, 16, 32 64, 128, 256, 512, 1024 V/V
- 4-BIT TTL GAIN CONTROL
- EXCELLENT GAIN NONLINEARITY 0.01% max at G = 1024 V/V
- LOW GAIN ERRORS - 0.02% MAX
- LOW GAIN DRIFT - 10ppm/°C MAX
- LOW VOLTAGE DRIFT - 1µV/°C MAX RTI, G = 1024V/V
- HIGH CMR - 110dB MIN, G = 1024V/V
- HIGH INPUT IMPEDANCE - 10 x $10^9\Omega$
- LOW OFFSET VOLTAGE 22µV max RTI, G = 1024V/V 2mV max RTI, G = 1V/V



GIVES SYSTEM WIDE RANGE AND HIGH RESOLUTION

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-388 Printed in U.S.A. July, 1978

DESCRIPTION

The 3606 is a self-contained, Programmable Gain Instrumentation Amplifier (PGIA) whose gain can be changed in 11 binary weighted steps from 1 to 1024 V/V. The gain control is accomplished through a 4-bit TTL input.

The PGIA function allows the user to deal with wide dynamic range signals while maintaining high system resolution. For example: when used with a 10-bit A to D converter in a "floating point" system, the 2^{10} gain range of the 3606, plus the 2^{10} range of the converter produces a total system resolution of 2^{20} ($\cong$ 1,000,000:1).

Desirable characteristics of a high performance instrumentation amplifier are offered by the 3606: high input impedance (10GΩ), excellent gain nonlinearity (0.01% max, G = 1024V/V; 0.002% max, G = 1V/V), high common-mode rejection (110dB min, G $\geq$ 4V/V), low gain error (0.02% max with no trimming required), low gain temperature coefficient (10ppm/°C max), and low offset voltage drift vs temperature (1μV/°C max, RTI, G = 1024).

Added to these outstanding instrumentation amplifier characteristics is the ability to change the 3606's gain under control of a 4-bit TTL input word. An important characteristic of the 3606 PGIA is its low change in offset voltage when gain is changed. A unique design approach, plus laser trimming minimizes this change to a maximum of ±25mV with no external adjustments. With two simple offset adjustments the change can be limited to less than 2mV (1mV typ) at the output over the entire 1 to 1024V/V gain range.

A simplified schematic of the 3606 is shown in Figure 1. The circuit consists of a variable gain high input impedance voltage follower input stage (A1 and A2) followed by a unity gain difference amplifier (A3) with a variable gain output stage (A4).

Common-mode voltage is derived for active guard drive to improve system common-mode rejection. Two-pole, low pass filtering can easily be implemented on the output stage to reduce noise bandwidth and improve system signal-to-noise operation. A latch function is provided to inhibit gain changes while the digital gain control input is changed.

Burr-Brown's instrumentation grade monolithic operational amplifiers, high stability precision thin-film resistor networks and advanced laser trimming techniques are used by the 3606 to achieve a performance, size and cost combination never before achieved in a PGIA. It is available in a 32-pin dual-in-line package in either ceramic or metal (hermetic) configurations.

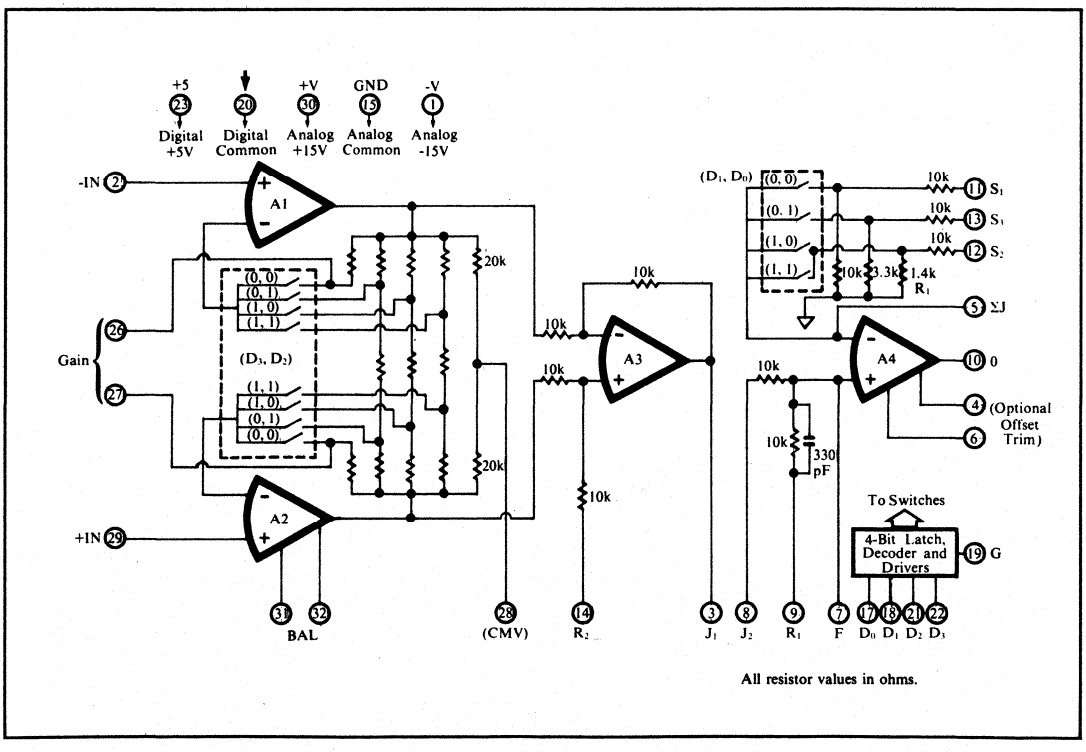


FIGURE 1. Simplified Schematic

ELECTRICAL SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

PARAMETER	Conditions	3606A(7)			3606B(7)			Units
		MIN	TYP	MAX	MIN	TYP	MAX	
GAIN, G(1)								
Inaccuracy	G = 1 to 1024, I_o = 1mA		±0.02	±0.05		±0.01	±0.02	%
Nonlinearity (2)	G = 1 to 16		0.001	0.002		*	*	%(5)
	G = 32 to 128		0.003	0.004		*	*	%
	G = 256 to 1024		0.005	0.01		*	*	%
Drift vs Temperature	G = 1 to 1024		±5	±10		*	*	ppm/°C
vs Time	G = 1 to 1024		±0.01			*		%/1000 hrs.
RATED OUTPUT								
Voltage	I_o = ±5mA	±10	±12		*	*		V
Current	V_o = ±10V	±5	±10		*	*		mA
Impedance			0.05			*		Ω
INPUT CHARACTERISTICS								
Absolute Max Voltage	No damage			$\pm V_{cc}$			*	V
Common-mode Voltage Range	Linear operation	±10	±10.5		*	*		V
Differential Impedance			10 ‖ 3			*		$10^9\Omega$ ‖ pF
Common-mode Impedance			10 ‖ 3			*		$10^9\Omega$ ‖ pF
OFFSET VOLTAGE, RTO(3)								
Initial at 25°C(4)			±(0.02G +1)	±(0.04G +2)		±(0.01G +1)	±(0.02G +2)	mV
vs Temperature	-25°C to +85°C		(±0.0015G ±0.03G_2)	(±0.003G ±0.05G_2)		(±0.0005G ±0.01G_2)	(±0.001G ±0.02G_2)	mV/°C
vs Time			(±0.001G ±0.01G_2)			*		mV/mo
vs Supply			(±0.002G ±0.04G_2)			*		mV/V
vs Gain (5)	With trimming		±1	±2		*	*	mV
INPUT BIAS CURRENT								
Initial	25°C		±15	±50		±5	±20	nA
vs Temperature	-25°C to +85°C		±0.3			*		nA/°C
vs Supply Voltage			±0.1			*		nA/V
INPUT DIFFERENCE CURRENT								
Initial	25°C		±15	±50		±5	±20	nA
vs Temperature	-25°C to +85°C		±0.5			*		nA/°C
vs Supply Voltage			±0.1			*		nA/V
INPUT NOISE								
Voltage	R source ≤ 5kΩ							
0.01Hz to 10Hz	G = 1024		1.4			*		μV p-p
10Hz to 1kHz			1.0			*		μV rms
Current								
0.01Hz to 10Hz			70			*		nA p-p
10Hz to 1kHz			20			*		nA rms
COMMON-MODE REJECTION								
DC, 1kΩ Source Imbalance								
G = 1, 2		80	90		90	100		dB
G = 4 to 16		90	100		100	110		dB
G = 32 to 1024		100	114		110	114		dB
60Hz, 1kΩ Source Imbalance								
G = 1, 2		80	86		*	*		dB
G = 4 to 16		90	96		*	*		dB
G = 32 to 1024		100	106		*	*		dB
DYNAMIC RESPONSE								
±3dB Response	Small Signal							kHz
G = 1			100			*		kHz
G = 32 to 128			40			*		kHz
G = 256 to 1024			10			*		kHz
±1% Response	Small Signal							
G = 1			40			*		kHz
G = 32 to 128			8			*		kHz
G = 256 to 1024			3			*		kHz
Slew Rate	G = 1	0.2	0.5		*	*		V/μs
Settling Time	G = 128							
to 1%			75			*		μs
to 0.1%			100			*		μs
to 0.01%			200			*		μs
LOGIC VOLTAGES								
"0" Level(6)			0	+0.4		*	*	V
"1" Level(6)		+2.4	+5.0		*	*		V
Absolute Max	No damage			+7			*	V
ANALOG SUPPLY								
Rated Voltage			±15			*		VDC
Voltage Range, Derated Performance		±8		±18	*		*	VDC
Current, quiescent			±10	±20		*	*	mA

ELECTRICAL SPECIFICATIONS CONTINUED

All specifications typical at 25°C unless otherwise noted.

PARAMETER	Conditions	3606A (7)			3606B (7)			Units
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL SUPPLY								
Rated Voltage			+5			*		VDC
Voltage Range		+4.5		+5.5	*		*	VDC
Current, quiescent			10			*		mA
TEMPERATURE RANGE								
Specification		-25		+85	*		*	°C
Storage		-40		+100	*		*	°C

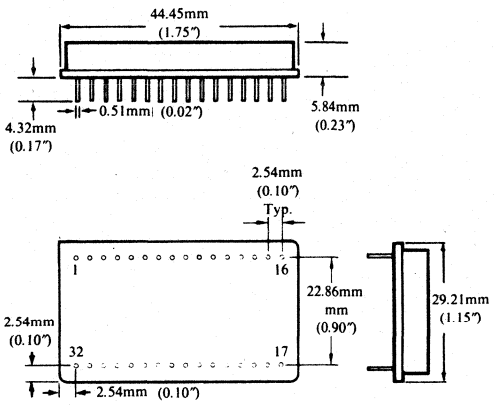
NOTES:

*Specifications same as 3606A.

1. $G = G_1 \cdot G_2$
2. Nonlinearity is the maximum peak deviation from the best straightline as a percent of full scale peak-to-peak output.
3. "RTO" = Referred To Output. May be referred to input by dividing by gain G.
4. May be adjusted to zero.
5. Trimmed according to Figure 8.
6. All digital inputs are 1TTL unit load.
7. Specify 3606AG or 3606BG for ceramic package and 3606AM or 3606BM for metal package - see below.

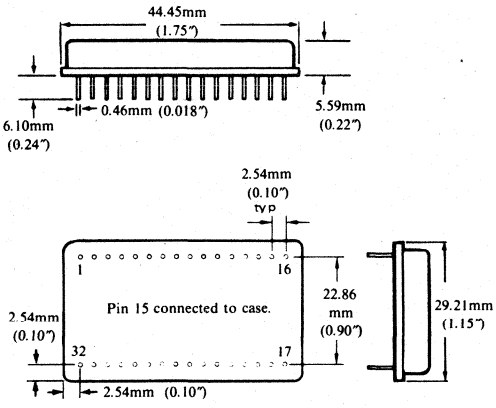
MECHANICAL

"G" PACKAGE



PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2). CASE: Ceramic MATING CONNECTOR: 2302MC - Set of two 16 pin strips. WEIGHT: 13 grams (0.46 oz.).

"M" PACKAGE



PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2). CASE: Metal MATING CONNECTOR: 2302MC - Set of two 16 pin strips. WEIGHT: 13 grams (0.46 oz.).

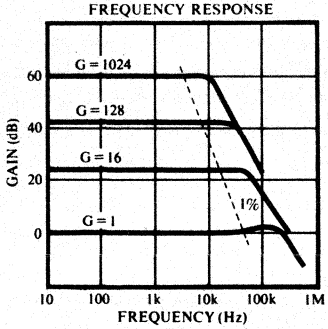
PIN DESIGNATIONS

PIN NO.	DESIG.	FUNCTION	PIN NO.	DESIG.	FUNCTION
1	-V	-15V Analog Supply	17	D_0	Digital Input, LSB
2	-IN	Inverting Input	18	D_1	Digital Input, next LSB
3	J_1	Output of A_3	19	G	Latch
4	(None)	Optional A_4 Offset Trim	20	⏚	Digital Common
5	ΣJ	Summing Junction of A_4	21	D_2	Digital Input, next MSB
6	(None)	Optional A_4 Offset Trim	22	D_3	Digital Input, MSB
7	F	Low Pass Filter Pin	23	+5	+5V Digital Supply
8	J_2	Input to A_4	24	(None)	No Internal Connection
9	R_1	Output Reference	25	(None)	No Internal Connection
10	O	Output	26	Gain	Optional External Gain
11	S_1	Sense G = 1	27	Gain	Optional External Gain
12	S_2	Sense G = 4	28	(None)	Input CMV
13	S_3	Sense G = 2	29	+IN	Noninverting Input
14	R_2	Output Reference	30	+V	+15V Analog Supply
15	GND	Analog Common	31	BAL	Optional Input Stage
16	(None)	No Internal Connection	32	BAL	Offset Null

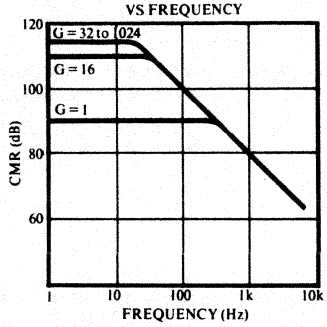
TYPICAL PERFORMANCE CURVES

All specifications typical at 25°C unless otherwise noted.

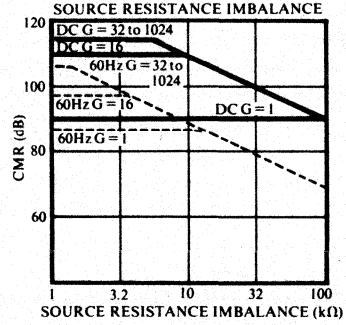
SMALL SIGNAL FREQUENCY RESPONSE



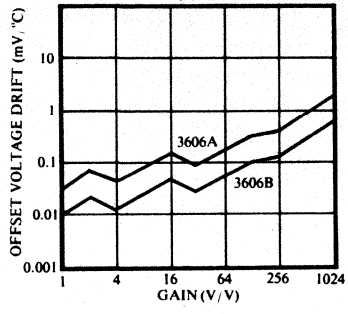
COMMON-MODE REJECTION VS FREQUENCY



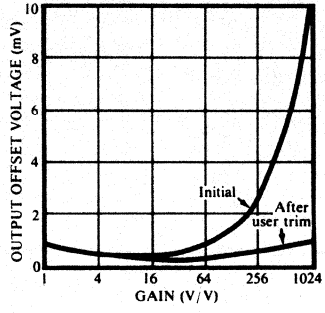
COMMON-MODE REJECTION VS SOURCE RESISTANCE IMBALANCE



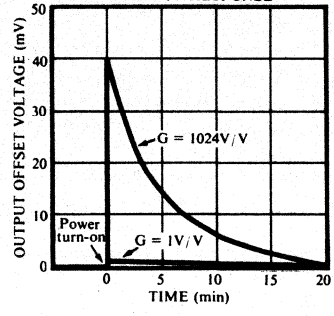
OUTPUT OFFSET VOLTAGE DRIFT VS GAIN



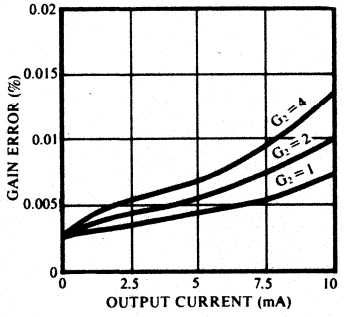
OUTPUT OFFSET VOLTAGE VS GAIN



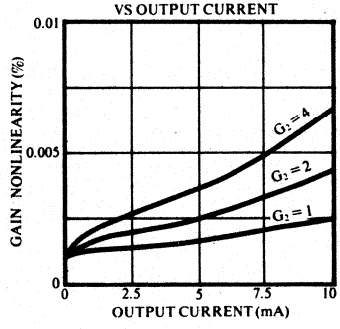
WARM-UP RESPONSE



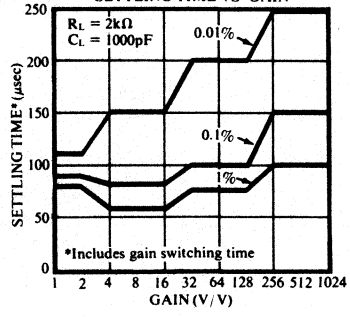
OUTPUT STAGE GAIN ERROR VS OUTPUT CURRENT



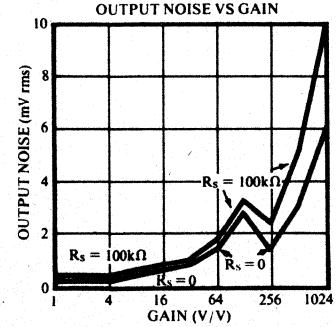
OUTPUT STAGE GAIN NONLINEARITY VS OUTPUT CURRENT



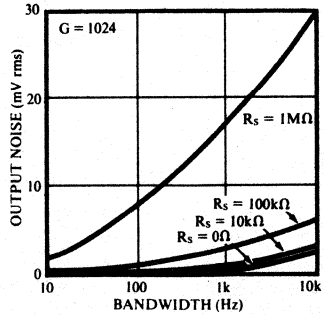
SETTLING TIME VS GAIN



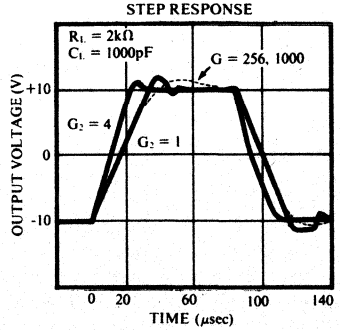
WIDEBAND OUTPUT NOISE VS GAIN



OUTPUT NOISE VS BANDWIDTH



STEP RESPONSE



INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

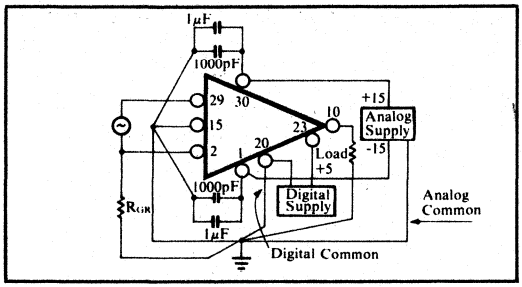


FIGURE 2. Power Supply and Ground Connections

Figure 2 shows the proper analog and digital power supply connections. The analog supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the amplifier as possible. Because the amplifier is direct-coupled it must have a ground return path for the bias currents associated with the amplifier inputs at pins 2 and 29. If the ground return path is not inherent in the signal source (floating source) it must be provided externally. The ground return resistance (R_{GR}) should be kept as low as practical. An upper limit of approximately 50MΩ is established by the input bias currents of the amplifier and its common-mode voltage.

SIGNAL CONNECTIONS

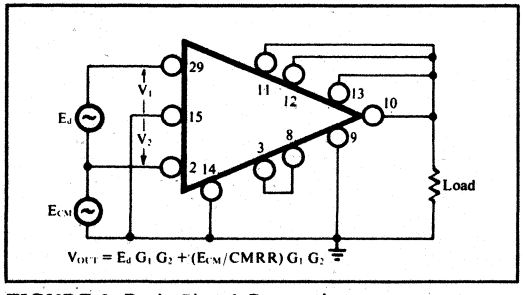


FIGURE 3. Basic Signal Connections

Basic signal connections are shown in Figure 3. The connection to pin 14 completes the difference amplifier of A_3 (see Figure 1). The 3 to 8 jumper connects the output stage. The pin 9 connection provides a divide-by-two attenuator for the A_4 stage. This is necessary to limit the signal on the output stage switches to maintain signal linearity. The pin 11, 12 and 13 connections to pin 10 close the feedback loop around A_4.

In the equation shown in Figure 3, G_1 is the input stage gain and G_2 is the output stage gain. CMRR is the common-mode rejection ratio [CMR (in dB) = 20 log CMRR (in V/V)]. Common-mode voltage shown as E_{CM} is actually the average of the two voltages appearing at the two inputs (pins 29 and 2) with respect to pin 15 (V_1 and V_2).

GAIN SETTING

Gain is determined by a 4-bit digital word applied to the input D_0 through D_3 (see Figure 1). Pin 19 provides a latch function for the inputs. When pin 19 is a logic 0, changes on the D_0 through D_3 inputs are inhibited. Pin 19 should be at +5V if the latch is not used.

A gain state truth table is shown in Table I. Gains are determined by the resistor networks shown in Figure 1. For the state D_3, D_2 = 0, 0, the input stage gain is a function of the gain setting resistor R_G connected between pins 26 and 27. If gains of 1, 2 and 4 are desired, no connection should be made to pins 26 and 27 and the resistance across these pins should be kept high with respect to 40kΩ (> 400MΩ).

Gain accuracy is established by laser-trimming the thin-film resistor networks during assembly. No external, user trimming is required.

OUTPUT OFFSET

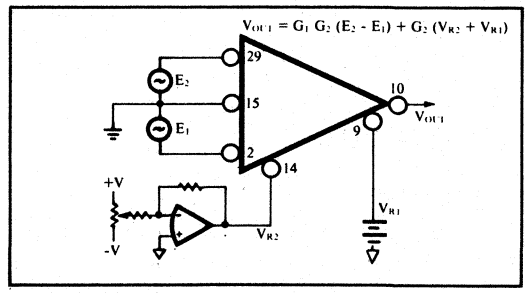


FIGURE 4. Output Offsetting

Output offset may be varied by either of two methods shown in Figure 4. Sources at pin 9 and pin 14 apply voltages to the noninverting inputs of A_4 and A_3 respectively (see Figure 1). Since the output stage gain occurs after these points, the output voltage bias established with V_{R1} and V_{R2} will vary with the output gain, G_2. Sources connected at pins 9 and 14 must have resistances low with respect to 10kΩ in order not to disturb gain accuracy and common-mode rejection.

Digital Inputs (G_1)		(G_2)		G_1 (A_1 and A_2) (Pins 2 & 29 to 3)	G_2 (A_4) (Pin 8 to Pin 10)	$G_1 \cdot G_2$ ($R_G^* = \infty$)	$G_1 \cdot G_2$ ($R_G^* \neq \infty$)
D_3	D_2	D_1	D_0				
0	0	0	0	1 + 40k/R_G	1	1	1(1 + 40k/R_G)
0	0	0	1		2	2	2(1 + 40k/R_G)
0	0	1	0		4	4	4(1 + 40k/R_G)
0	0	1	1		4	4	4(1 + 40k/R_G)
0	1	0	0	4	1	4	4
0	1	0	1		2	8	8
0	1	1	0		4	16	16
0	1	1	1		4	16	16
1	0	0	0	32	1	32	32
1	0	0	1		2	64	64
1	0	1	0		4	128	128
1	0	1	1		4	128	128
1	1	0	0	256	1	256	256
1	1	0	1		2	512	512
1	1	1	0		4	1024	1024
1	1	1	1		4	1024	1024

*R_G connected between pins 26 and 27.

TABLE I. Gain State Truth Table

LOW PASS FILTER

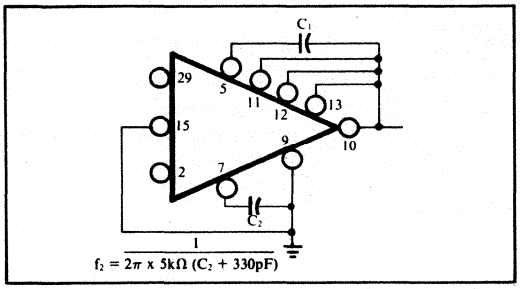


FIGURE 5. Low Pass Filter Connections

For low frequency signals, system performance may be improved by reducing noise bandwidth in the amplifier. This may be accomplished with the addition of one or two external capacitors as shown in Figure 5. C_2 is connected to a 10k/10k attenuator and C_1 is connected as a feedback element across A4 (see Figures 1 and 5). The transfer function is:

$$\frac{V_o}{V_{IN}} = \left[\frac{10 \times 10^3}{100 \times 10^6\ S\ (C_2 + 330 \times 10^{-12}) + 20 \times 10^3}\right]\left[1 + \frac{10 \times 10^3}{10 \times 10^3\ R_1\ SC_1 + R_1}\right]$$

The first term is a first order filter. The second term is more complex. R_1 varies with the output stage gain - 1.4k for $G_2 = 4$ (see Figure 1). The "1 + ..." nature of the transfer function prevents a true first order filter rolloff.

For most applications, the first order low pass filter obtained by C_2 provides sufficient filtering. The value of C_2 required for a desired cutoff frequency (f_2 in Hz) is obtained by the equation shown in Figure 5.

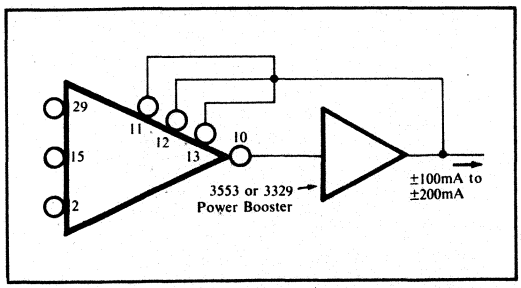


FIGURE 6. Output Current Booster

LARGER OUTPUT CURRENT

The output current rating of the 3606 is a minimum of ±5mA. The linearity of the gain is affected by output current. See TYPICAL PERFORMANCE CURVES. Optimum linearity is achieved with $I_o \leq 1mA$. $I_o \leq 5mA$ is acceptable. Above 5mA it may be desirable to use a power or current booster as shown in Figure 6. Burr-Brown's 3329 will provide ±100mA output while Burr-Brown's 3553 will supply ±200mA. When either booster is placed inside the feedback loop as shown, the booster's offset voltage produces no significant errors since it is divided by the open loop gain of the output stage.

GUARD DRIVE CONNECTIONS

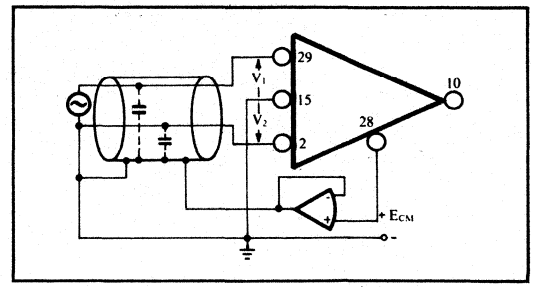


FIGURE 7. Guard Drive Connections

Use of the guard drive connection shown in Figure 7 can improve system common-mode rejection when the distributed capacitance of the input lines is significant. The common-mode voltage which appears on the input lines and on pins 29 and 2 is computed by the 3606 $[(V_1 + V_2)/2]$ and appears at pin 28. It is then fed back to the shield so that the voltage across the distributed capacitances is minimized. This reduces the common-mode current and improves common-mode rejection. The operational amplifier in the voltage follower configuration is used to supply more current than can be obtained from the 20k resistors connected internally to pin 28 (see Figure 1).

OFFSET TRIM

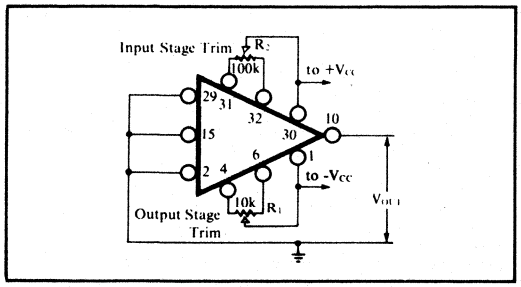


FIGURE 8. Optional Offset Trim

Offset voltages of the 3606 are reduced by laser-trimming during assembly. This reduces the initial offset voltage and the offset voltage change with gain change to levels that are acceptable for most applications. For more critical applications the offset voltages can be externally nulled to zero. The following steps should be followed (see Figure 8).

1. Adjust both R_1 and R_2 to mid range
2. Set the gain to minimum (1V/V)
3. Adjust R_1 to make V_{OUT} equal zero
4. Set the gain to maximum (1024 V/V)
5. Adjust R_2 to make V_{OUT} equal zero

By using this technique, the change in output offset voltage caused by a gain change of 1V/V to 1024V/V may be reduced to, typically 1mV instead of 10mV with no external trimming. Trimming may cause the offset voltage drift vs temperature to increase slightly.

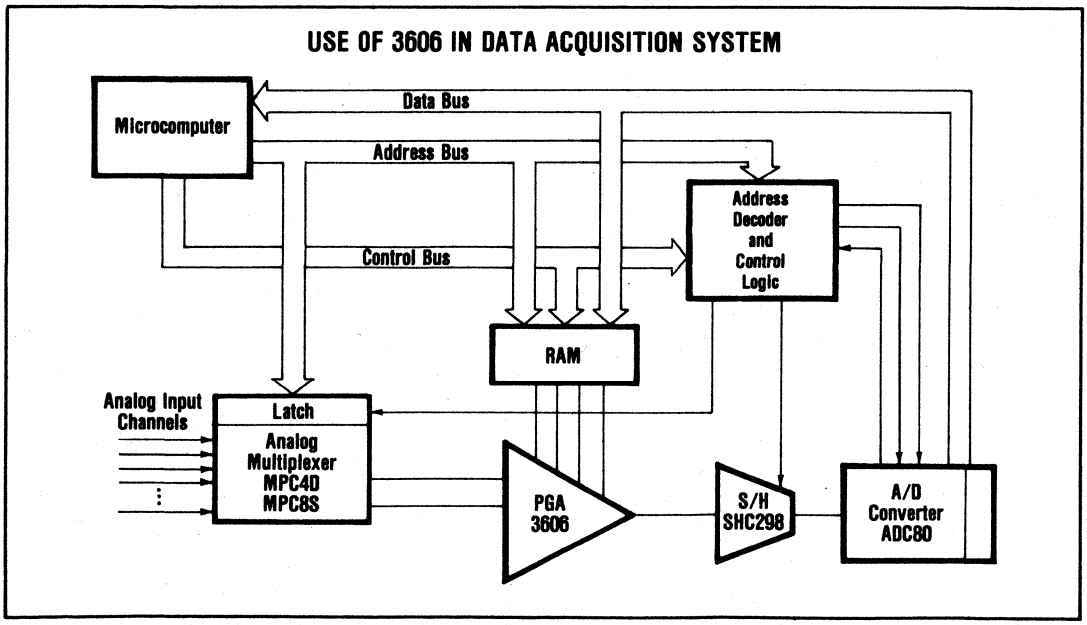
APPLICATIONS

A typical application of 3606 in a microcomputer based data acquisition system is shown in the block diagram below.

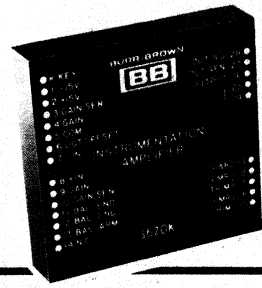
The purpose of this system is to be able to acquire data from a specific analog input channel, suitably condition it (amplify it and convert it to digital form) and store it or transmit it for further processing.

Initially the Microcomputer loads the RAM (random access memory) with the required coding for various desired gains via Data Bus. The coding associates the gain state truth table for 3606 with corresponding address locations in the computer memory. So when the computer puts out an instruction to multiplex a specific analog input channel through the multiplexer via the Address Bus, the RAM also receives the same address information and puts out corresponding gain code to the PGA 3606. The 3606 amplifies the multiplexed signal by the programmed gain value, and outputs it to S/H (sample and hold). The S/H holds the output value when it receives the control signal from the computer and the A/D converts it and outputs it to the computer via the Data Bus under computer control.

The PGA 3606 allows the system user to modify and reprogram gain values for different analog input channels merely by changing the software computer program. Since different dedicated instruments are not required for various input channels, the PGA also saves space and overall system costs.



BURR-BROWN



3620

Differential Input INSTRUMENTATION AMPLIFIER

FEATURES

- LOW DRIFT - ±0.25μV/°C
- LOW NOISE - 1μV peak-to-peak
- HIGH CMR - 100dB
- HIGH INPUT IMPEDANCE - 300MΩ Differential 1000MΩ Common mode
- LOW PROFILE - 0.4 Inch High
- WIDE GAIN RANGE - 1 to 10,000

DESCRIPTION

Model 3620 is a DC differential-input instrumentation amplifier designed for data acquisition and instrumentation use. The low drift, low noise, and high CMR make it possible to accurately amplify millivolt-level signals with gains of up to 1000. Two gain stages are used ... the input stage can be adjusted for any gain between 1 to 1000, and the output stage, which has a nominal gain of unity, can be easily adjusted for any gain from 0.1 to 10. So the overall gain can be varied from 0.1 to 10,000. A number of useful features are provided in the 3620.

CMR may be easily trimmed externally.

Common-mode voltage is sensed and is brought out for connection to signal shield or guard for improved noise rejection.

Active low-pass filtering can be added with one external capacitor.

The output amplifier feedback point is brought out so that power boosters may be added inside the feedback loop, thereby maintaining gain accuracy.

Output offset may be independently adjusted over the full ±10V output range.

Inputs are protected against overvoltages up to supply level, and the output is protected against damage due to shorting to common.

With this unusual versatility, outstanding electrical performance, and low cost, Burr-Brown's Model 3620 Instrumentation Amplifier is the best choice for your instrument or data acquisition system.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-260C

Printed in U.S.A. July, 1978

SPECIFICATIONS

ELECTRICAL | Typical at 25°C and ±15 Vdc power unless otherwise noted.

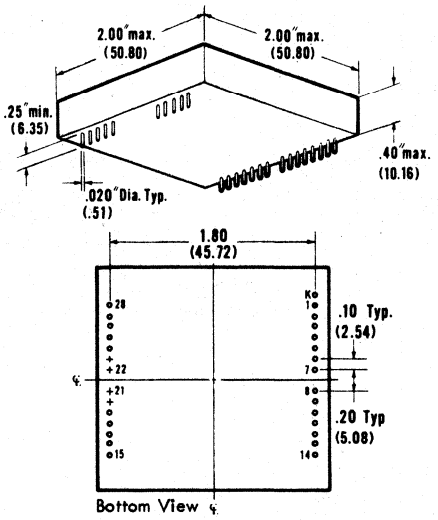
MODEL	3620J	3620K	3620L
GAIN			
Gain Equation (1)	$G = 1 + \frac{25\,k\Omega}{R}$		
Range of Gain (1)	1 to 1000		
Gain Nonlinearity, G = 100, max.	±0.01%		
Gain Stability			
vs. Temperature	±0.001%/°C		
vs. Time	±0.001%/mo.		
OUTPUT			
Rated Output	±10 V, ±10 mA		
Output Impedance, DC to 1 kHz	0.1 Ω		
Allowable Capacitive Load	1000 pF		
INPUT			
Input Impedance - Differential	300 MΩ		
- Common-Mode	1000 MΩ		
Input Voltage Range (2)	±10 V		
Absolute Max.	± Supply		
CMR, DC to 100 Hz			
at Gain of 10, 1 kΩ Source Unbal.	74 dB, min.		
at Gain of 1000, 1 kΩ Bal. Source	100 dB		
OFFSETS AND NOISE			
Input Offset, max.			
(may be externally zeroed)	±1 mV		
Output Offset, G = 1000			
vs. Temperature, max. Model J	±2 mV/°C		
Model K		±0.5 mV/°C	
Model L			±0.25 mV/°C
vs. Supply	±20 mV/V		
vs. Time	±3 mV/mo.		
Output Offset, at any gain G			
vs. Temperature, Model J, max	±(10 + 2 G) µV/°C		
Model K, max		±(10 + 0.5 G)µV/°C	
Model L, max			±(10 + 0.25 G)µV/°C
vs. Supply	±(100 +20 G) µV/V		
vs. Time	±(20 + 3 G) µV/mo.		
Bias Current (each input) @25°C, max.	±25 nA		
vs. Temperature, max.	±0.5 nA/°C		
Input Noise, G = 100			
Voltage, p-p, 0.01 Hz to 10 Hz	1 µV		
rms, 10 Hz to 1 kHz	0.6 µV		
Current, p-p, 0.01 Hz to 10 Hz	200 pA		
rms, 10 Hz to 10 kHz	35 pA		
Output Noise, G = 1			
Voltage, rms, 10 Hz to 10 kHz	6 µV		
DYNAMIC RESPONSE at G = 100			
Small-Signal Frequency Response			
for ±1%, min.	1.5 kHz		
for ±3 dB, min.	10 kHz		
Full Power, G = 10	5 kHz		
Settling Time to within ±10 mV			
of Output Final Value	200 µsec		
Slew Rate	0.3 V/µsec		
POWER SUPPLY			
Rated Supply Voltage	±15 Vdc		
Supply Range	±12 Vdc to ±18 Vdc		
Supply Drain, max.			
at Quiescent	±14 mA		
at Rated Output	±24 mA		
TEMPERATURE RANGE			
Specification	0°C to +70°C		
Operating	-40°C to +85°C		
Storage	-55°C to +100°C		

(1) The gain is set by one external resistor according to the gain equation $G = 1 + 25k\Omega/R$, where R is the external resistor. For gains from 1 to 100, the accuracy of this equation is ±0.1%. For a gain of 1000 it is typically accurate to ±0.5%. For higher values of gain, see the discussion under Wide-Range Gain Adjustments and Figure 12.

(2) The ±10V input range is subject to the limitation that $|E_{CM}| + |G\,E_d/2| \leq 10V$.

PACKAGE CONFIGURATION

NOTE: Dimensions in millimeters are shown in parentheses.



WEIGHT: 2 oz. max. (57 grams)
MATERIAL:
Case - Black Epoxy

Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).

PIN CONNECTIONS

K	KEY (No Con.)	
1	-15 Vdc	
2	+15 Vdc	
3	Gain Sense	
4	Gain	
5	Com.	
6	Output Offset	
7	Inverting Input	
8	Non-Inverting Input	
9	Gain	
10	Gain Sense	
11	Balance (end)	10 kΩ optional
12	Balance (end)	10 kΩ optional
13	Balance (arm)	10 kΩ optional
14	No Con.	
15	CMR 1	Trim
16	CMR 1	Trim
17	CMR 2	Trim
18	CMR 2	Trim
19	Guard	
20	No Pin	
21	No Pin	
22	No Pin	
23	No Pin	
24	Jumper	
25	Jumper	
26	Output	
27	Output Sense	
28	Output Summing Junction	

THEORY OF OPERATION

Burr-Brown pioneered in the field of modular instrumentation amplifiers with the popular Model 3061. This design is similar to the 3061 - two Burr-Brown low-bias-current IC op amps are used to make an input stage. Since these low-drift IC amplifiers are matched pairs, Burr-Brown can economically offer tested maximum drifts for the 3620 as low as $\pm 0.25\,\mu V/^{\circ}C$ (L Model). A third IC op amp converts the amplified differential signal to a single-ended signal, and a fourth amplifier is included for low-pass filtering, additional gain, or offsetting of the output. Wire-wound resistors are used throughout the 3620 to ensure good long-term stability of gain and CMR.

A simplified circuit diagram is shown in Figure 1. The two input voltages, E_{d1} and E_{d2} must be referenced to the system common.

The ±15 V power supply and output voltage must also be referenced to the same system common. Low-impedance floating signals, such as some thermocouple circuits, may be referenced to the common through a large-value resistor (typically 1 M Ω).

The common-mode input voltage E_{cm} is $(E_{d1} + E_{d2}) / 2$, and the differential input voltage E_d is $E_{d1} - E_{d2}$. When connected as shown in Figure 2, the output voltage E_o will be

$$E_o = \left(1 + \frac{25\text{ k}\Omega}{R}\right) E_d$$

Provisions are made for easily modifying this gain equation if desired. (See Wide-Range Gain Adjustments.)

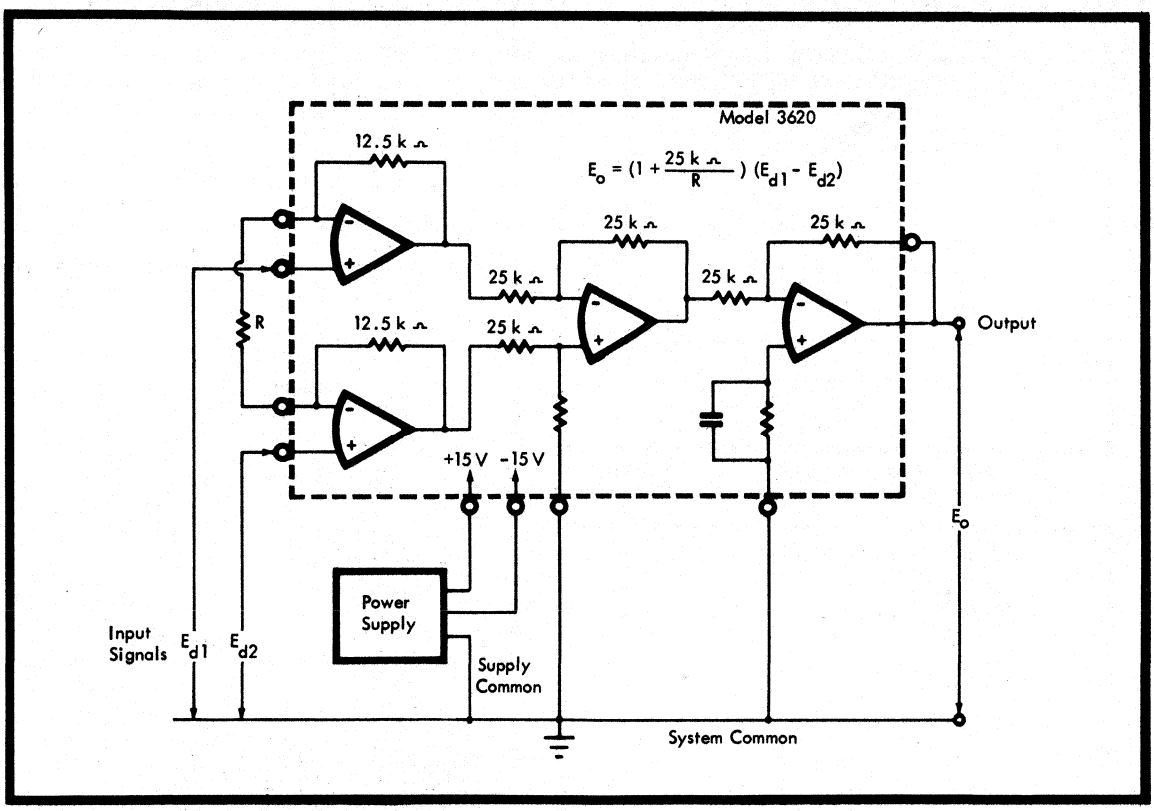


FIGURE 1. Simplified Diagram of the Model 3620 Instrumentation Amplifier.

APPLICATIONS INFORMATION

COMMON MODE REJECTION

CMR is a measure of an amplifier's ability to reject common-mode inputs while amplifying differential signal inputs. CMR varies with the differential gain setting. And at any given gain, the CMR will also vary with the frequency of the common-mode input. If the signal source impedance is unbalanced, this will also degrade the CMR. The effects of varying frequency and source impedance unbalance are shown in Figures 2, 3, 4 and 5.

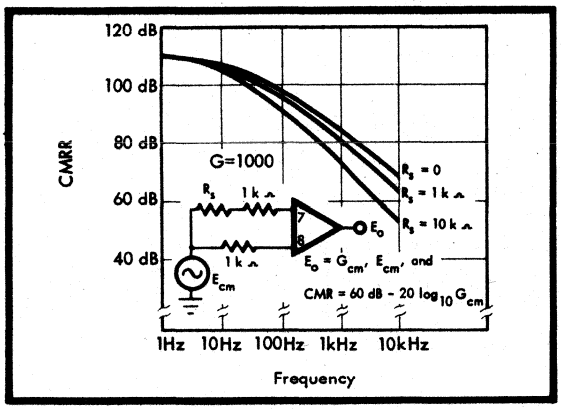


FIGURE 2. Typical Common-Mode Rejection with the Amplifier Connected for Gain of 1000.

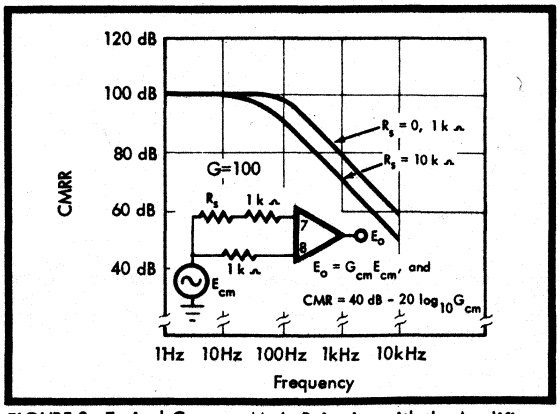


FIGURE 3. Typical Common-Mode Rejection with the Amplifier Connected for Gain of 100.

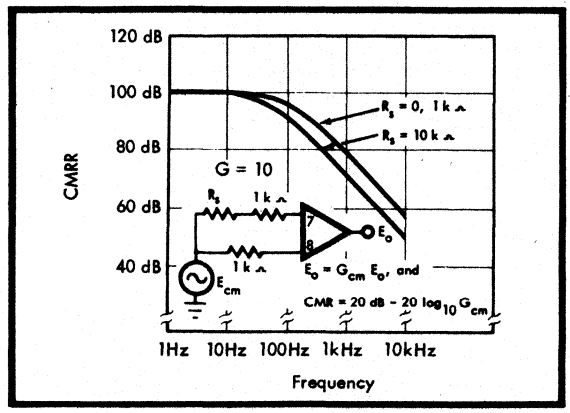


FIGURE 4. Typical Common-Mode Rejection with the Amplifier Connected for Gain of 10.

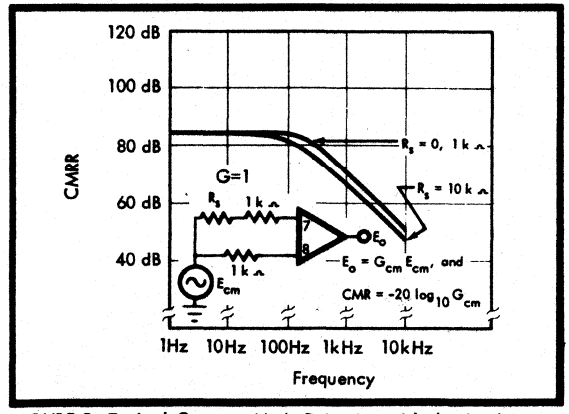


FIGURE 5. Typical Common-Mode Rejection with the Amplifier Connected for Unity Gain.

FREQUENCY RESPONSE

For small signals, the gain accuracy varies with frequency and the gain setting. For large signals, slew-rate limiting becomes important. Typical gain error, relating to the gain at DC, as a function of frequency is shown in Figure 6. Slew rate capability of the 3620 is independent of the gain setting, and is typically 0.3 V/μsec. Output impedance is very low for the 3620 under all conditions, but it varies somewhat with signal frequency as shown in Figure 7.

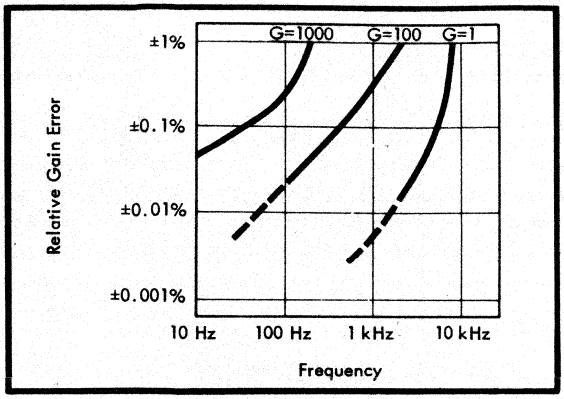


FIGURE 6. Typical Gain Error Variation with Frequency for Gains of 1, 100, and 1000.

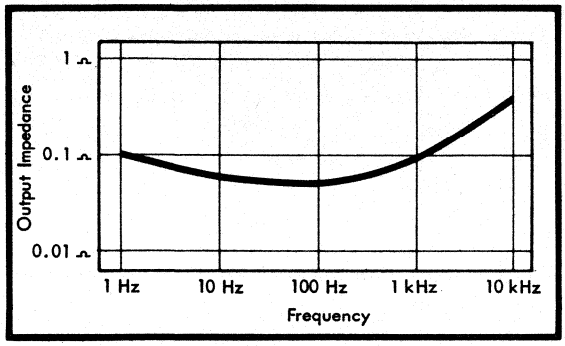


FIGURE 7. Output Impedance vs. Signal Frequency for a Typical 3620.

GAIN NONLINEARITY

Gain nonlinearity of the 3620 is specified to be less than ±0.02% at all gains from 1 to 1000. But gain nonlinearity varies with input signal amplitude and with the gain setting, so gain nonlinearity is better at lower gain settings. The variation in gain nonlinearity with gain setting will differ from unit-to-unit, but the typical variation is shown in Figure 8.

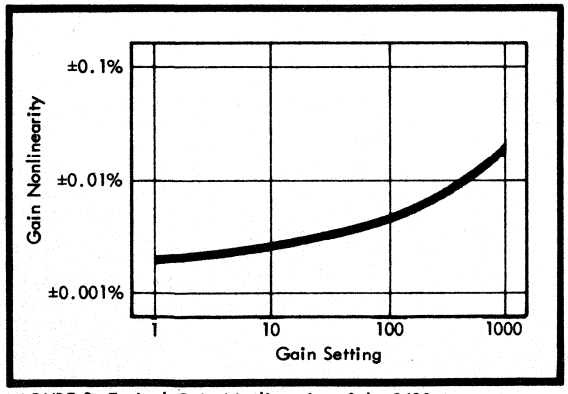


FIGURE 8. Typical Gain Nonlinearity of the 3620.

NOISE CHARACTERISTICS

For an amplifier with low voltage drift to be truly useful, it must also have low noise. The 3620 has very low voltage noise - both peak-to-peak and root-mean-square. Also, the input current noise is very low, so moderately high source impedance is not a problem. Noise referred-to-input is difficult to specify fully because it varies with gain setting and with the frequency range of interest. Some typical curves of voltage noise referred-to-input (RTI) for the 3620 are shown in Figure 9.

Peak-to-peak input voltage noise varies in a similar manner with the gain setting. Over a frequency range of 10 Hz to 1 kHz, the input noise typically varies from 5 μV p-p at gain of 1000 to 15 μV p-p at gain of 10. Low frequency flicker noise (0.01 Hz to 10 Hz) is typically 1 μV p-p for gain settings above 100, and is generally 10 to 40 μV p-p at unity gain.

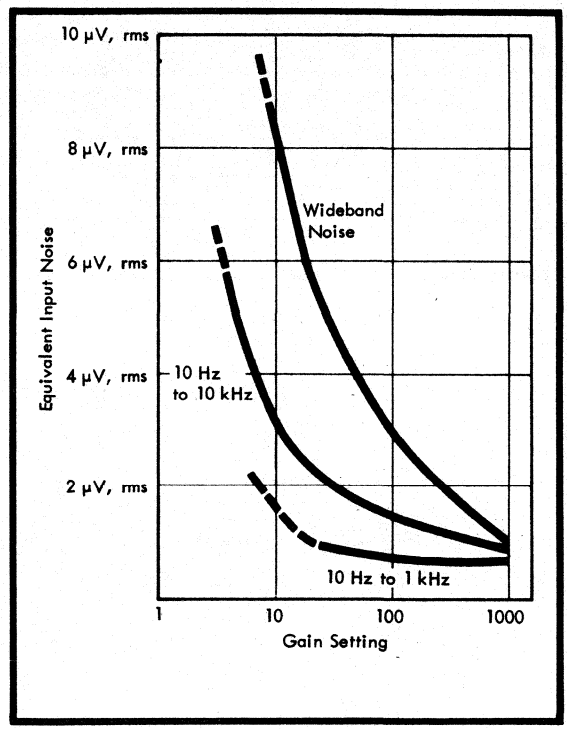


FIGURE 9. Equivalent Input Voltage Noise for Typical 3620's.

Input current noise needs to be considered when the input source impedance is over 100 ohms. In the 0.01 Hz to 10 Hz frequency range, input current noise is generally under 200 pA p-p. Wideband input current noise is typically 100 pA p-p. Since input current noise is essentially due to semiconductor shot noise, the RMS noise value is much less than the peak-to-peak noise value.

With the 3620, a capacitor C_o may be added between pins 27 and 28. This creates a one-pole, low-pass filter with a time-constant of 25 kΩ x C_o. Adding a low-pass filter will reduce the effect of high-frequency AC noise by 6 dB/octave, but at the expense of reduced bandwidth and increased settling time.

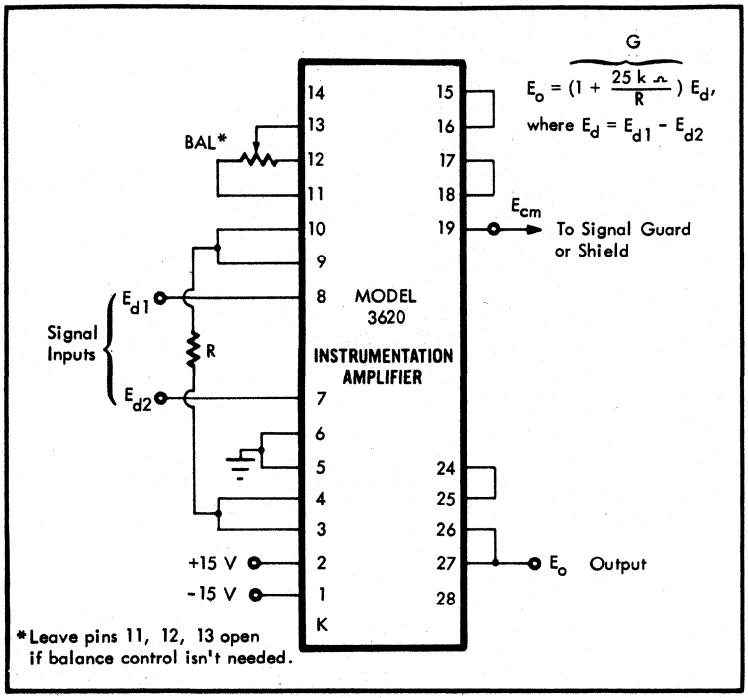


FIGURE 10. Pin Connections For Conventional Operation.

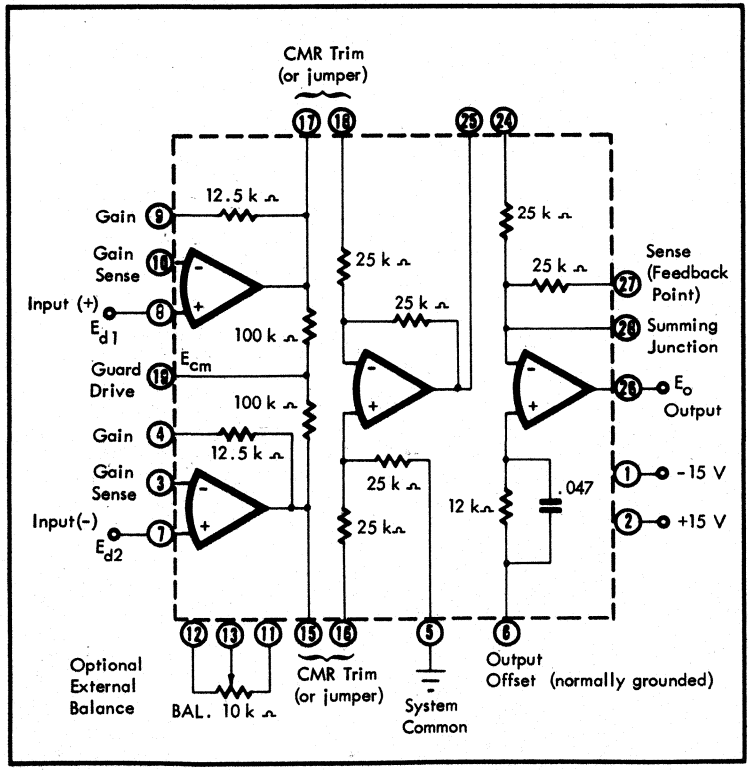


FIGURE 11. Simplified Pin-Connection Diagram of the Model 3620 Instrumentation Amplifier.

OPERATION

CONVENTIONAL OPERATION

Pin connections for conventional operation are shown in Figure 10. The gain is set by one external resistor. To balance the amplifier, simply connect both inputs (pins 7 and 8) to the system common (pin 5), and adjust the external balance potentiometer for zero volts at the output (pin 26). The balance adjustment is optional.

TRIMMING CMR

To externally trim CMR, just add a 100 Ω resistor between pins 17 and 18 and a 250 Ω potentiometer between pins 15 and 16. Adding the 100 Ω resistor deliberately unbalances the gain, then the 250 Ω potentiometer is varied to trim CMR. Gain nonlinearities and AC noise pickup make 120 dB the practical upper limit for CMR. For best stability, the resistor should be either the metal film or wirewound type. Adding the 100 Ω resistor will affect the gain equation slightly - the differential gain will be lowered by 0.8%. The gain can easily be raised by either making R smaller or by adding a 100 Ω resistor between pins 27 and 26 (see Figure 11).

WIDE-RANGE GAIN ADJUSTMENTS

Gain may be conveniently adjusted by two methods with the 3620. First, the gain resistor R can be varied to set the input stage gain. But the gain may also be varied by changing the feedback of the output op amp. With all other connections as shown in Figure 10, the circuit for varying gain over a wide range by varying the output stage gain is shown in Figure 12. For specified gain accuracy, a four-terminal connection to the gain-setting resistor R should be used.

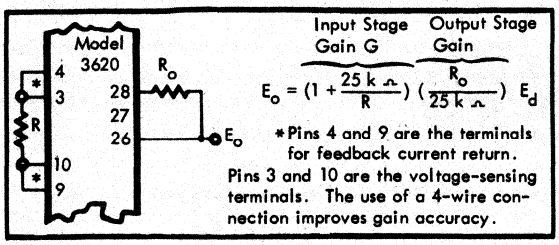


FIGURE 12.

For best performance, the input stage gain should be made as large as possible, and the output stage gain can then be used to make a linear gain adjustment. For example, an R of 25 Ω could be used for an input-stage gain of 1000, and R_o could be a potentiometer that varies between 12.5 k Ω to 125 k Ω. This would provide an overall gain of 500 to 5000 that would be linearily adjustable. So with the 2 stages of adjustable gain, it is feasible to operate the 3620 over a very wide range of gains - a range of 0.1 to 10,000 is practical.

LOW-PASS FILTERING

To filter out AC noise, simply add an external capacitor C_o between pins 27 and 28. The time constant of the low-pass, single-pole filter will be 25 k Ω x C_o. If an external gain resistor is being used, the time constant will be $R_o C_o$ with C_o connected between pins 26 and 28.

OUTPUT OFFSET

Output offset may be varied over the ±10 V output range by either of two methods:

1. Applying a voltage to pin 6. This point is connected to the non-inverting input of the output op amp.
2. Summing an offset current into the inverting input of the output op amp (pin 28) as shown in Figure 13.

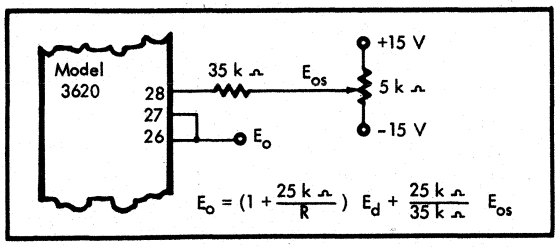


FIGURE 13.

ADDING A POWER BOOSTER

A power booster may be added inside the feedback loop of the output amplifier as shown in Figure 14.

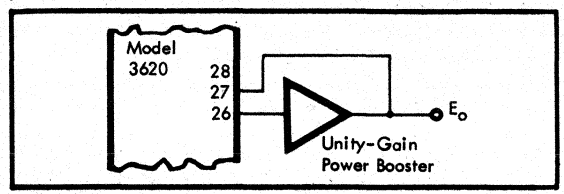


FIGURE 14.

The Burr-Brown hybrid IC power booster, Model 3329/03, is ideal for this circuit. The 3329/03 will provide an output of ±100 mA at ±10 V. The output protection of the 3329/03 allows it to operate without damage to itself under output short-circuit conditions at 85°C with full-scale input voltage applied.

SHIELDING PRACTICE

The common-mode input voltage is sensed and brought out on pin 19. To minimize AC noise pickup and maintain good CMR, connect pin 19 to a guard. If permissible from a systems viewpoint, the signal shield may also be connected to pin 19. The guarding system for minimum AC pickup is shown in Figure 15.

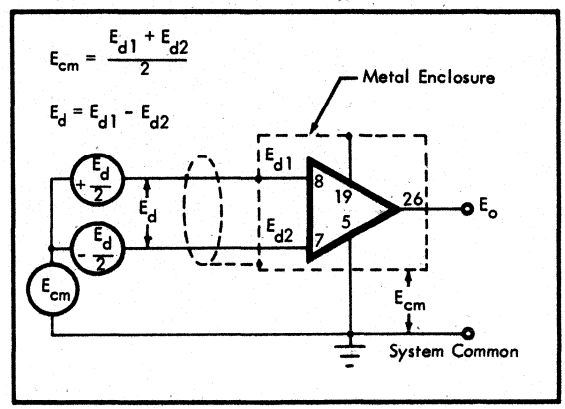
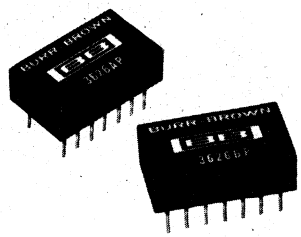


FIGURE 15.

The need for signal shielding and guarding depends on the amount of AC noise that is present, the gain, and the desired level of performance.

BURR-BROWN

3626



Low Drift INSTRUMENTATION AMPLIFIER

FEATURES

- LOW VOLTAGE DRIFT @ LOW GAIN
  2μV/°C @ G = 5 (3626CP)
- LOW NOISE - 2μV p-p
- HIGH CMR - >80dB @ = 1000
- LOW COST
- SMALL SIZE - DIP Package

DESCRIPTION

The 3626 is an integrated circuit instrumentation amplifier designed for amplifying low-level signals in the presence of high common-mode voltages. Its low drift, high input impedance ($5 \times 10^9\Omega$), easy gain adjustment (5V/V to 1000V/V) and high common-mode rejection eliminate the problems and compromises associated with using operational amplifiers to realize the same gain function.

Compared to other integrated circuit instrumentation amplifiers it has the unique feature of having low voltage drift versus temperature at low gains.

The 3626 offers many benefits to the user for his instrumentation applications:

Low voltage drift reduces temperature errors

High common-mode rejection preserves system accuracy

High input impedance prevents errors due to source loading and source impedance imbalance

Small, dual-in-line package conserves board space

Laser-trimmed offset requires no nulling

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PDS-350A

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DISCUSSION

An instrumentation amplifier is basically a closed-loop gain block that exhibits high input impedance and high common-mode rejection. Instrumentation amplifiers are committed devices with differential inputs and accurately predicatable input-to-output relationships – all necessary feedback networks are contained in the circuit package. These characteristics distinguish instrumentation amps from operational amplifiers – open-loop devices whose closed-loop performance depends upon the external networks supplied by the user.

In instrumentation amps parameters such as input and output impedances, frequency response, offset voltage drift and common-mode rejection are specified for the closed-loop, committed configuration. One of the few parameters that the user can vary is gain (by choosing the external gain-setting resistor value). Another important difference between an op amp and instrumentation amp is that the instrumentation amp has no summing junction available; you cannot make a summing amplifier or integrator out of an instrumentation amp.

In the past few years, choices in instrumentation amplifier designs have grown from a number of discrete modular units to include monolithic and hybrid integrated circuit versions which offer high performance at lower cost – and in smaller packages. Monolithic IC's were the first to break the price and performance barrier. Hybrid IC's, such as the 3626, are more expensive than monolithic IC's but they give better performance for the money.

Instrumentation amps normally require at least one external resistor – the gain-setting resistor R_G. Monolithic units usually require two additional – the output feedback resistor and a resistor between feedback common and ground. Since temperature coefficient differences between these two resistors will cause output offset voltage drift, they must be matched to meet the desired drift specification. Hybrid units, such as the 3626, have the advantage that all resistors except the gain-setting R_G can be included in the package.

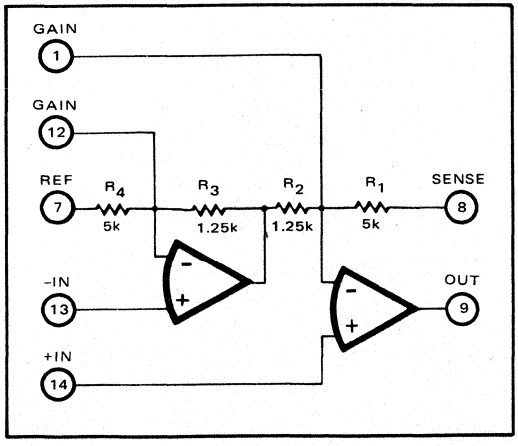


FIGURE 1. Simplified Circuit Diagram.

A simplified circuit diagram of the 3626 is shown in Figure 1. The circuit uses Burr-Brown's high performance bipolar integrated circuit amplifiers and a laser trimmed thin-film resistor network. The excellent initial matching and temperature tracking of these components provide a level of performance difficult to obtain with even expensive discrete amplifiers and resistors. The gain accuracy, linearity and temperature coefficient are particularly attractive.

One of the most outstanding features of the 3626 is its low voltage drift, especially at low and medium gains. Figure 2 shows the drift performance of the 3626 series comapred to monolithic integrated circuit instrumentation amplifiers. The guaranteed voltage drift performance is almost two orders of magnitude better at low gains.

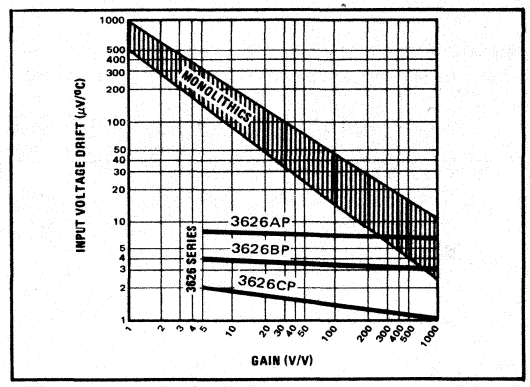


FIGURE 2. Input Offset Drift vs Gain.

The design of the 3626 is such that output biasing is easily accomplished. See Figure 3 for proper connections. The impedance of the reference source should be low compared to 5kΩ. A current booster such as the 3329 (100 mA) or 3553 (200 mA) can conveniently be used with the 3626 to increase its output current driving capability.

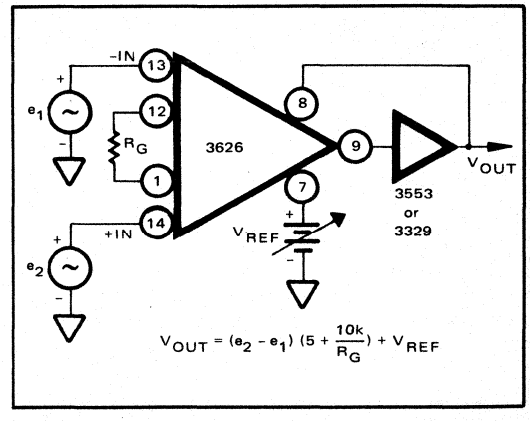


FIGURE 3. Output Offsetting and Power Boosting.

SPECIFICATIONS

ELECTRICAL

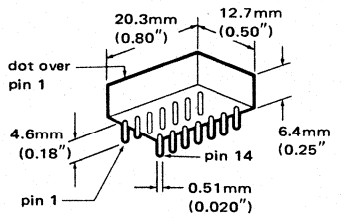
Specifications typical at 25°C and ±15 VDC Power Supply Unless Otherwise Noted.

MODELS	3626AP	3626BP	3626CP
GAIN			
Gain Equation	$G = 5 + \frac{10\ k\Omega}{R_G}$		
Error from Equation (1)	(±0.25 - 0.003G)%		
Range of Gain, min	5 to 1000		
Gain Temp. Coefficient:			
G = 5	2ppm/°C		
G = 10	25ppm/°C		
G = 100	35ppm/°C		
G = 1000	50ppm/°C		
Nonlinearity, max (%) (2)	±(0.02 +0.0003G)	±(0.01 + 0.0003G)	±(0.01 +0.003G)
OUTPUT			
Rated Output, min	±10V @ ±5mA		
Output Impedance, G = 100	2Ω		
INPUT			
Input Impedance, Diff. & CM	$5 \times 10^9\ \Omega \parallel 3$ pF		
Input Voltage Range, min	±10V		
CMR, DC to 60Hz	with 1kΩ source unbalance		
G = 5, min	68dB	74dB	74dB
G = 10 to 1000, min	74dB	80dB	80dB
INPUT OFFSET VOLTAGE			
Initial Offset, max(1)	$\pm(0.4 + \frac{0.4}{G})$mV	$\pm(0.2 + \frac{0.2}{G})$mV	$\pm(0.2 + \frac{0.2}{G})$mV
vs. Temperature, max	$\pm(6 + \frac{10}{G})\mu$V/°C	$\pm(3 + \frac{5}{G})\mu$V/°C	$\pm(1 + \frac{5}{G})\mu$V/°C
vs. Supply	40μV/V		
vs. Time	3μV/mo.		
INPUT BIAS CURRENTS			
Initial Bias Current, max	±50nA (either input)		
vs. Temperature, max	±0.7nA/°C		
vs. Supply	±0.1nA/V		
INPUT NOISE			
Voltage, p-p, 0.01Hz–10Hz	2μVp-p		
RMS, 10Hz - 10kHz	2μV RMS		
Current, p-p, 0.01Hz - 10Hz	150 pA p-p		
RMS, 10Hz - 10kHz	50 pA RMS		
DYNAMIC RESPONSE			
Small Signal, ±3dB Flatness:			
G = 5	400kHz		
G = 10	160kHz		
G = 100	14kHz		
G = 1000	1.4kHz		
Small Signal, ±1% Flatness;			
G = 5	76kHz		
G = 10	27kHz		
G = 100	2.1 kHz		
G = 1000	250 Hz		
Full Power, G = 5 - 100	19 kHz		
Slew Rate, G = 5 - 100	1.2 V/μs		
Settling Time (0.1%):			
G = 5	0.02 ms		
G = 10	0.03 ms		
G = 100	0.1 ms		
G = 1000	12 ms		
POWER SUPPLY			
Rated Voltage	±15 VDC		
Voltage Range	±5 to ±20 VDC		
Quiescent Supply Current	±6 mA, max		
TEMPERATURE RANGE			
Specifications, min	-25°C to +85°C		
Operation	-55°C to +125°C		
Storage	-65°C to +150°C		

(1) May be trimmed to zero.

(2) Nonlinearity is the maximum peak deviation from the best straightline as a percent of full scale peak-to-peak output.

MECHANICAL



Row Spacing: 7.6mm (0.300")
Weight: 3.4 grams (0.12 oz.)
Connector: 0145MC (14-pin DIP)

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std-202.

Pin Connections

1.	Gain	8.	Sense
2.	} No Internal	9.	Out
3.	} Connection	10.	$+V_{CC}$
4.	V_{OS}	11.	No Internal Connection
5.	V_{OS}	12.	Gain
6.	$-V_{CC}$	13.	-In
7.	Ref	14.	+In

Connection Diagram

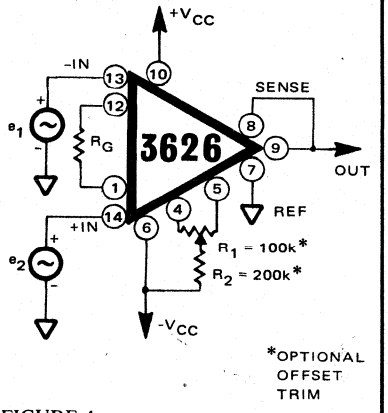
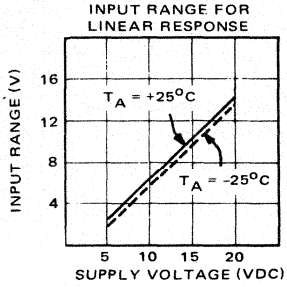
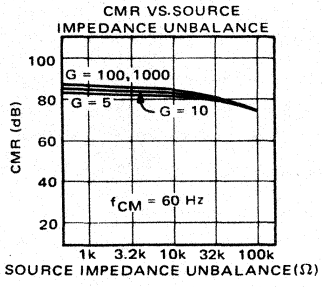


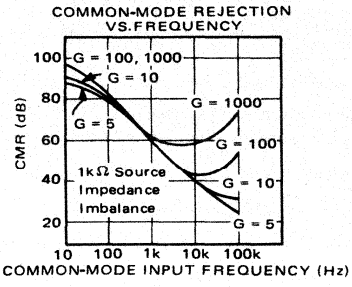
FIGURE 4

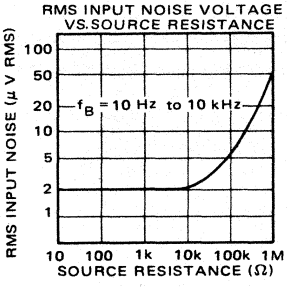
TYPICAL PERFORMANCE CURVES

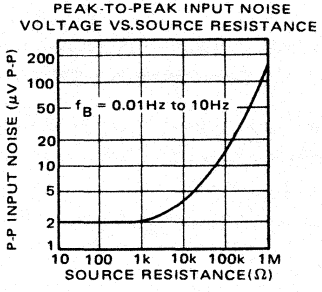
(TYPICAL @ 25°C and ±15 VDC POWER SUPPLIES UNLESS OTHERWISE NOTED)

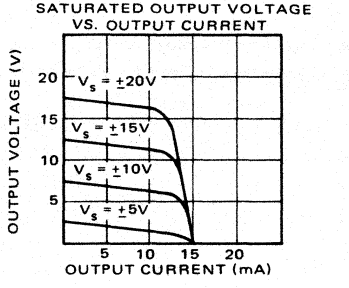


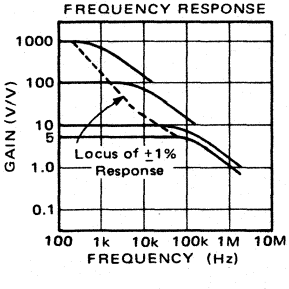


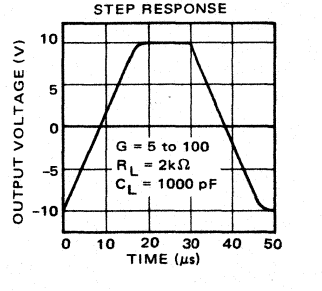


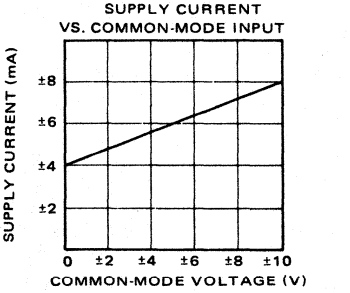












INSTALLATION AND OPERATING INSTRUCTIONS

SETTING THE GAIN

Figure 3 shows the normal operating connections for the 3626. The differential gain, G, is determined according to the equation

$$G = 5 + \frac{10k\Omega}{R_G}$$

where R_G is the resistor shown in Figure 4. This gain equation is typically accurate to 0.25%. The temperature coefficient of R_G will directly affect the stability of G. For high gains, R_G will be quite small (R_G = 10Ω for G = 1000); thus, the wiring impedance between pins 12 and 1 should be kept as low as possible. (Trimming of R_G will eliminate the effects of wiring impedances so long as this impedance is constant.) Also, note that V_{ref} source needs to be low impedance so as not to significantly affect the gain equation.

CMR TRIM

The 3626 meets its CMR specifications without additional trimming; however, for improved CMR in special situations (such as imbalanced source impedances), the circuit in Figure 5 may be used. In this circuit, R_1 is added to intentionally imbalance the inverting and noninverting gains of the amplifier. R_2 is then used to rebalance them, which overcomes the effects of any residual CMR degradation due to source impedance imbalance, etc. An improvement of approximately 6 to 10 dB can be typically realized at low gains.

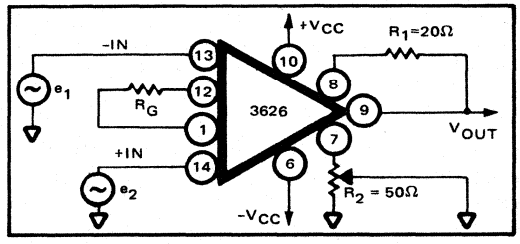
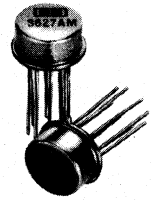


FIGURE 5. CMR Trim.

BURR-BROWN

3627



High Accuracy Unity-Gain DIFFERENTIAL AMPLIFIER

FEATURES

- LOW COST
- EASY TO USE
- COMPLETELY SELF-CONTAINED
- HIGH ACCURACY
  - Gain Error, 0.005%
  - Nonlinearity, 0.0005%
  - CMR, 106dB
- NO TRIMMING REQUIRED

DESCRIPTION

The 3627 is a high accuracy committed-gain differential amplifier. It consists of a high quality monolithic operation amplifier, a low drift thin-film resistor network and laser-trimmed offset circuitry - all inside a single integrated circuit package.

The fact that the 3627 is completely self-contained in a TO-99 package has several user benefits:

The total performance is guaranteed as a single component.
No gain adjustments are required.
No offset trimming is required.
The whole circuit, including the gain setting resistors and offset trim circuitry, is protected by the environmentally rugged hermetically sealed package.
The total amplifier function is very small in size (0.108 square inches of area and 0.025 cubic inches of volume).

The 3627 is offered in two grades: the 3627AM and the 3627BM. They differ only in common-mode rejection (94dB typ. vs 106dB typ.) and offset voltage drift (15μV/°C typ. vs 10μV/°C typ.).

The 3627 offers excellent total performance with no fuss and a very-low total installed cost.

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DISCUSSION

The 3627 is a new and unique approach to a widely occurring problem-how to get excellent performance at a low cost in a unity gain differential amplifier circuit. Burr-Brown's solution to this problem uses its wide range of integrated circuit expertise; a high quality monolithic amplifier, low drift high stability thin-film resistor network and state-of-the-art laser-trimming techniques. The result is a completely self-contained amplifier with total guaranteed 25°C accuracy of less than ±0.015% (gain error, nonlinearity, offsets and common-mode rejection).

The simplicity of the unity gain differential amplifier circuit may be deceiving when one considers an error analysis. Consider, for example, gain and common-mode rejection errors. The gain is determined by the ratio of R1 and R2 and the ratio of R3 and R4. The common-mode rejection of the total circuit is a function of the CMR of the operational amplifier and the matching of the resistors R1 to R3 and R2 to R4. Even if the operational amplifier is perfect (infinite CMR), in order to guarantee 100dB common-mode rejection would require resistor match of approximately 0.0005% (5ppm).

This matching (and especially maintaining the match over temperature) can be difficult and expensive to achieve. Packaged matched and tracking resistor networks are available but they are fairly expensive compared to the cost of the complete 3627 amplifier. Of course, matching can be obtained by trimming or padding some of the resistors, but this is difficult to do since each resistor effects both gain accuracy and common-mode rejection simultaneously. Unless care is used in choosing the trimming sequence a frustrating iterative trimming process can be encountered.

With the 3627 these problems no longer exist for the user. They are solved inside the package by Burr-Brown and the user has a completely self-contained plug-in-and-go amplifier to use. The excellent gain accuracy and common-mode rejection is obtained by using laser-trimming of a thin-film resistor network (R1 through R4). The outstanding gain and common-mode rejection temperature coefficients are a result of the excellent TCR tracking properties inherent in Burr-Brown's thin-film resistor networks.

The offset voltage is also laser-trimmed to a very low 250μV max value (100μV typical). This low value of offset eliminates the need for external offset adjust potentiometers which reduces cost and improves reliability.

The basic approach of the 3627 as a completely self-contained amplifier has several cost saving implications. It reduces design, purchasing and inventory cost. It reduces labor costs because the gain setting resistors do not require installation and adjustment. Also, no potentiometers are required.

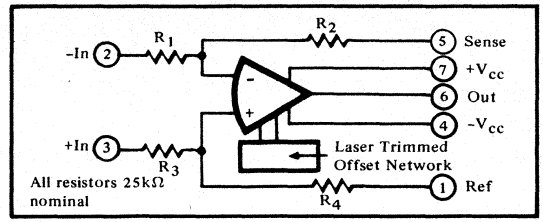
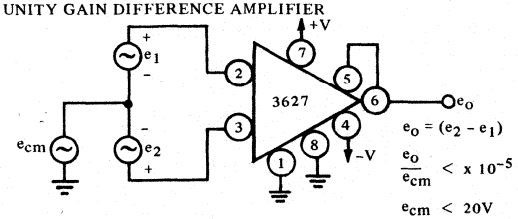
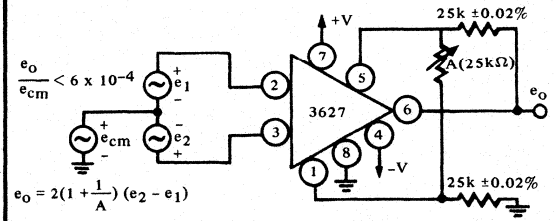


FIGURE 1. Simplified Circuit Diagram.

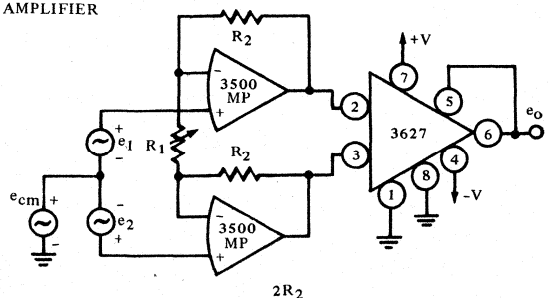
UNITY GAIN DIFFERENCE AMPLIFIER



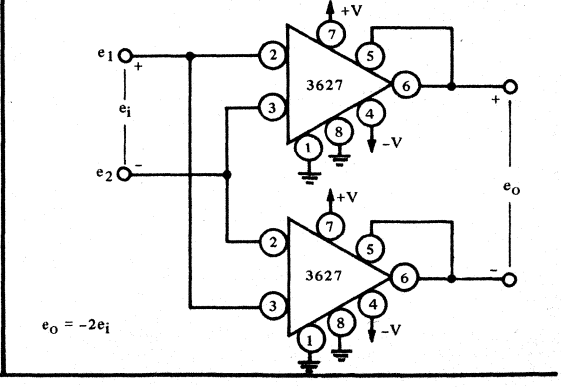
VARIABLE GAIN DIFFERENTIAL AMPLIFIER



HIGH INPUT IMPEDANCE, VARIABLE GAIN, INSTRUMENTATION AMPLIFIER



DIFFERENTIAL IN - DIFFERENTIAL OUT AMPLIFIER



SPECIFICATIONS

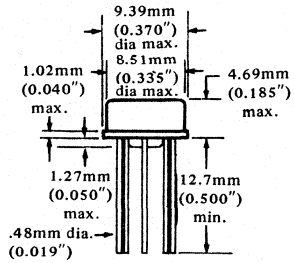
Specifications typical at 25°C and ±15VDC Power Supply Unless Otherwise Noted.

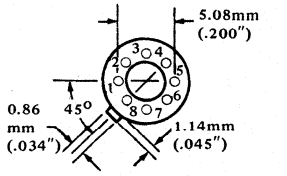
ELECTRICAL

MODELS	3627AM	3627BM
GAIN		
Gain Equation	G = 1 V/V[1]	
Gain Error	±0.01%, max (±0.005% typ)	
Gain Nonlinearity[2]	±0.001%, max (±0.0005% typ)	
Gain Temp. Coefficient, max	±0.0005%/°C (5ppm/°C)	
Gain Temp. Coefficient, typ	±0.0002%/°C (2ppm/°C)	
OUTPUT		
Rated Output, min	±10V at ±5mA	
Rated Output, typ	±12 at ±10mA	
Output Impedance	0.01Ω	
INPUT		
Input Impedance		
Differential	50k	
Common-mode	50k	
Input Voltge Range		
Differential	±20V	
Common-mode	±20V	
Common-mode Rejection, dc to 60 Hz[3]		
CMR, at 25°C	90dB, min(94 dB typ)	100 dB, min(106 dB typ)
CMR, -25°C to +85°C	80 dB, min(90 dB typ)	86 dB, min(94 dB typ)
OFFSET AND NOISE		
Offset Voltage, RTO[4][5]		
at 25°C	250μV (100μV typ)	
vs temperature, μV/°C	30 max (15 typ)	20 max (10 typ)
vs supply	20μV/V	
vs time	20μV/mo	
Noise Voltage, RTO[4][6]		
0.01Hz to 10Hz	2μV p-p	
10Hz to 100Hz	1.5μV rms	
DYNAMIC RESPONSE		
Small Signal, ±1% Flatness	5 kHz min (8 kHz typ)	
Small Signal, ±3 dB Flatness	0.8 MHz min (1.2 MHz typ)	
Full Power Bandwidth	14 kHz min (18 kHz typ)	
Slew Rate	0.6 V/μs min (1 V/μs typ)	
Settling time, 0.1% (±10mV)	20μsec	
.0.01% (±1 mV)	50 μsec	
POWER SUPPLY		
Rated Voltage	±15VDC	
Voltage Range	±5 to ±18VDC	
Quiescent Supply Current	±2mA	
TEMPERATURE RANGE		
Specifications, min	-25°C to +85°C	
Operation	-55°C to ±125°C	
Storage	-65°C to +150°C	

MECHANICAL

TO-99



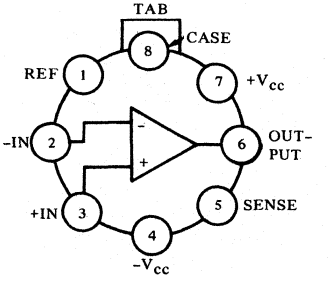


BOTTOM VIEW

Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).

CONNECTION DIAGRAM

TOP VIEW



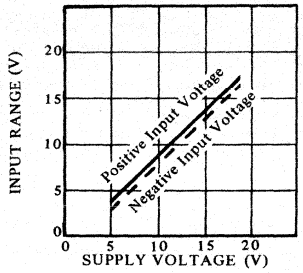
See Figure 1 for circuit diagram.

1. Connected as unity gain amplifier. Several other configurations are possible. See the figures in the "Discussion" and "Typical Applications."
2. Nonlinearity is the maximum peak deviation from the best straightline as a percent of full scale peak-to-peak output.
3. With zero source impedance unbalance.
4. Referred to output in unity gain difference configuration. Note that this circuit has a gain of 2 for the operational amplifiers offset voltage and noise voltage.
5. Includes effects of amplifiers input bias currents.
6. Includes effects of amplifiers input current noise.

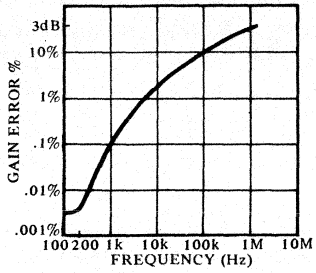
TYPICAL PERFORMANCE CURVES

(Typical at 25°C and ±15 VDC Power Supplies unless otherwise noted.)

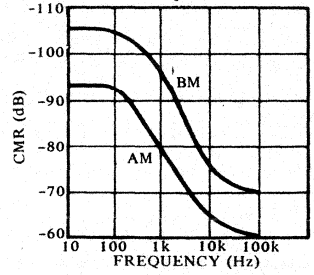
INPUT RANGE FOR LINEAR RESPONSE



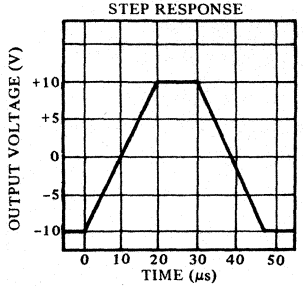
GAIN ERROR VS FREQUENCY



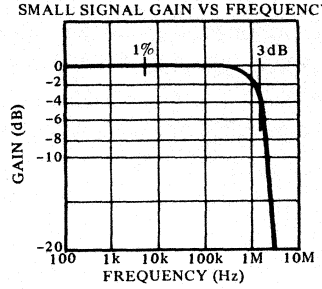
COMMON-MODE REJECTION VS FREQUENCY



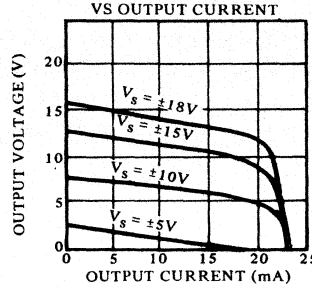
STEP RESPONSE



SMALL SIGNAL GAIN VS FREQUENCY

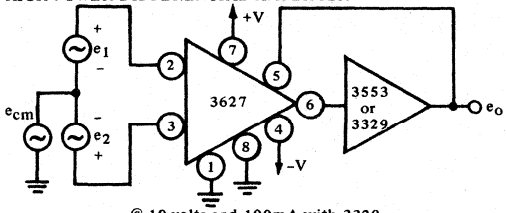


MAXIMUM OUTPUT VOLTAGE VS OUTPUT CURRENT



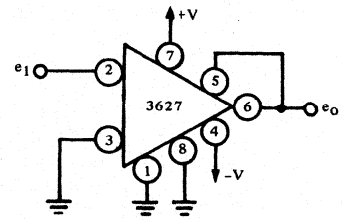
TYPICAL APPLICATIONS

HIGH POWER DIFFERENTIAL AMPLIFIER



$e_o = (e_2 - e_1)$ @ 10 volts and 100mA with 3329 @ 10 volts and 200mA with 3553

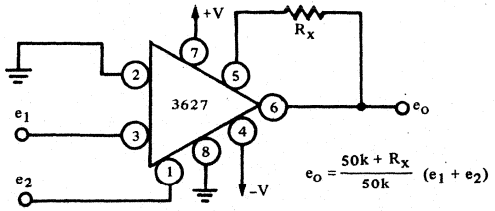
HIGH ACCURACY, LOW DRIFT, LOW OFFSET-UNIT GAIN INVERTER



$e_o = -e_1$

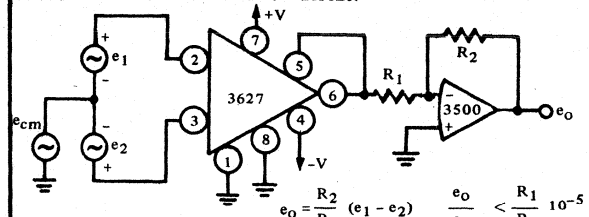
Accuracy .01%
Linearity .001%
Offset < 250μV at output
Offset Drift < 20μV/°C at output

NON-INVERTING SUMMER



$e_o = \frac{50k + R_x}{50k} (e_1 + e_2)$

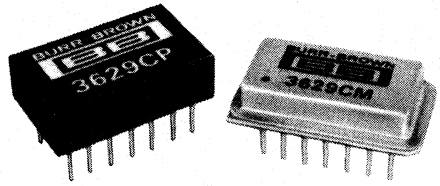
HIGHER GAIN DIFFERENCE AMPLIFIER



$e_o = \frac{R_2}{R_1} (e_1 - e_2)$ $\quad \frac{e_o}{e_{cm}} < \frac{R_1}{R_2} 10^{-5}$

BURR-BROWN

3629



Low Drift INSTRUMENTATION AMPLIFIER

FEATURES

- VERY-LOW VOLTAGE DRIFT 0.75μV/°C
- HIGH CMR - 90dB @ 60Hz
- LOW BIAS CURRENT - 20nA
- LOW NOISE - 1.2μV p-p
- SMALL SIZE - DIP Package

DESCRIPTION

Offering very-low voltage drift versus temperature even at low gains, the 3629 meets critical instrumentation requirements when amplifying low level signals in the presence of high common-mode voltages. This precision integrated circuit instrumentation amplifier offers low bias current and high input impedance ($10^{10}\Omega$). A single resistor sets gain from 5V/V to 1000V/V.

The 3629 exceeds the performance of other IC instrumentation amplifiers and offers many benefits for instrumentation applications:

Low voltage drift to reduce temperature errors
High common-mode rejection to preserve system accuracy
High input impedance to minimize errors caused by source loading and source impedance imbalance
Small, dual-in-line plastic or hermetically sealed metal package to conserve board space
Laser-trimmed offset to eliminate nulling

Use the 3629 to eliminate problems and compromises that arise when attempting to use operational amplifiers to achieve the same gain function.

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PDS-383 Printed in U.S.A. July, 1978

DISCUSSION

Instrumentation amplifiers are closed loop gain blocks whose committed circuitry accurately amplifies the voltage applied to their inputs. They respond only to the difference between the two input signals and exhibit extremely high input impedance, both differentially and common-mode. Feedback networks are packaged within the amplifier module. Only one external gain setting resistor must be added. An operational amplifier, on the other hand, is an open loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is difficult to reach the same level of performance. Using op amps often leads to design trade-offs when it is necessary to amplify low-level signals in the presence of common-mode voltages while maintaining high input impedances.

Figure 1 represents a simplified circuit diagram of the 3629. The circuit employs high performance bipolar IC amps and a laser trimmed thin-film resistor network.

The 3629 offers excellent performance. Its low voltage drift reduces temperature errors, especially at low and medium gains. Figure 2 illustrates the drift performance of the 3629 compared with competitive monolithic IC instrumentation amplifiers. Note that the drift does not increase at lower gains. Compare the 3629's input offset voltage drift vs temp at 1.75μV/°C with monolithic IC instrumentation amps in the range of 100μV/°C.

Because of its design, output biasing of the 3629 is easily accomplished. See Figure 3 for connections. The impedance of the reference source should be low compared to 10kΩ. Figure 3 also shows a current booster, such as Burr-Brown's 3329 (100mA) or 3553 (200mA), used with the 3629 to increase its output current driving capability while retaining its 5-1000 V/V gain characteristics. If power boosting is not required, connect pin 8 to pin 9.

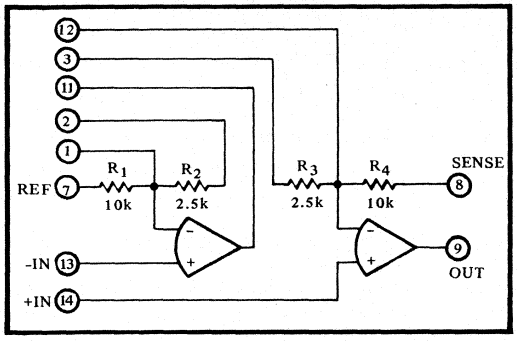


FIGURE 1. Simplified Circuit Diagram.

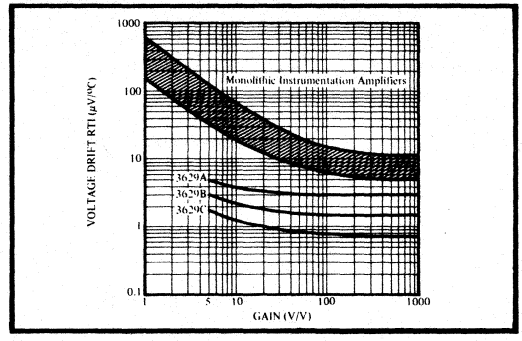


FIGURE 2. Input Offset Drift vs Gain.

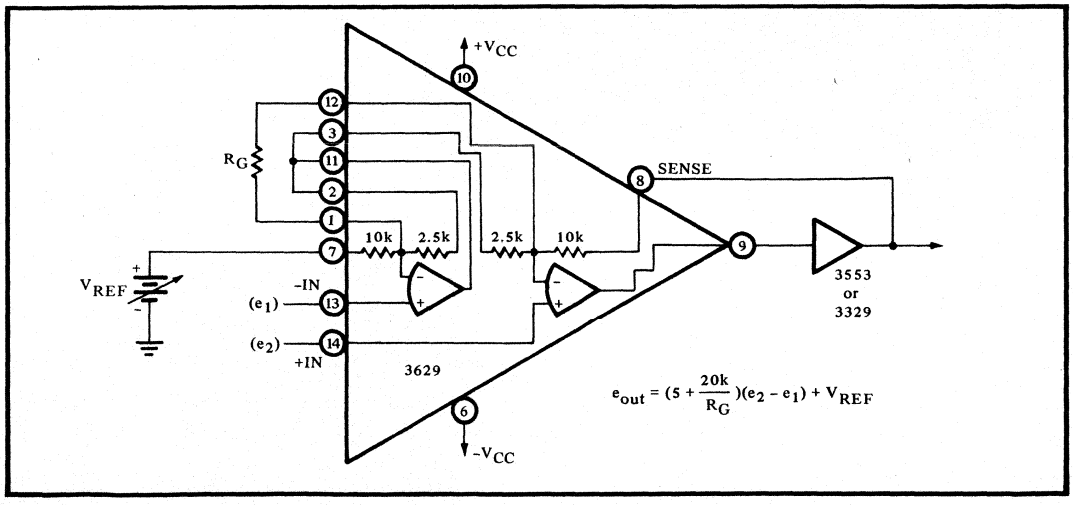


FIGURE 3. Output Biasing and Power Boosting.

DESIGN VERSATILITY

The 3629 offers additional application versatility. Its matched pair of amplifiers can be used as two independent, uncommitted op amps with a laser trimmed thin-film network present in one package.

When amplification must be extended to gains below 5, a 3629 used with a unity gain instrumentation amplifier (Burr-Brown's 3627) is recommended. This connection is shown in Figure 4.

DESIGN ALTERNATIVES

To amplify signals in the presence of common-mode voltages and noise while maintaining high input impedance, you can: 1) design and build an op amp circuit with a differential input configuration; 2) design and build an instrumentation amplifier made up of multiple op amps or; 3) purchase a ready-to-install, committed instrumentation amplifier. Only the third option provides an immediate solution with the elimination of in-house design, assembly and tuning steps. The growing range of lower cost, high quality IC instrumentation amps available has answered the build or buy question.

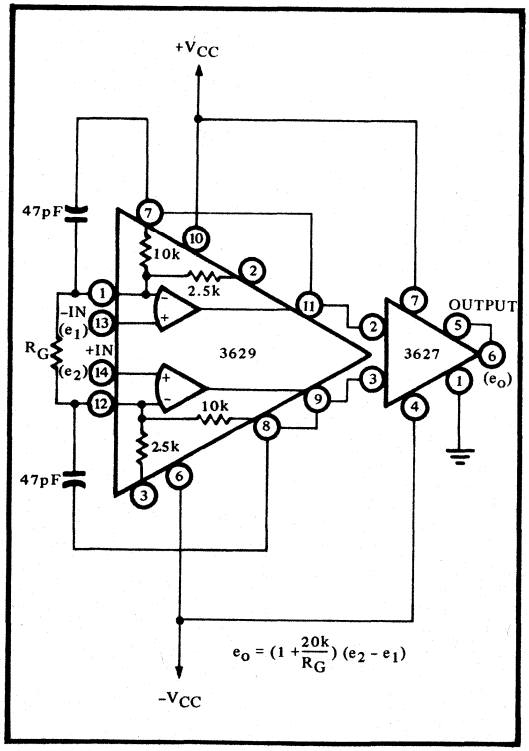


FIGURE 4. 3629 In A Composite Instrumentation Amplifier.

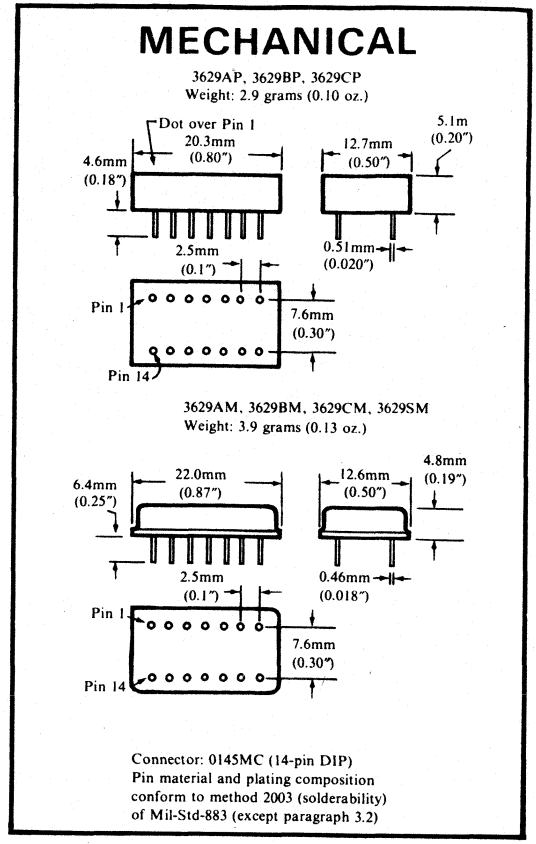


FIGURE 5. Mechanical Specifications

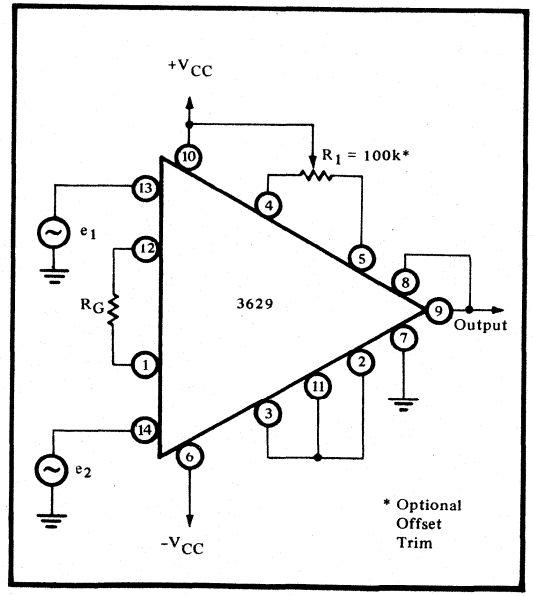


FIGURE 6. Connection Diagram

ELECTRICAL SPECIFICATIONS

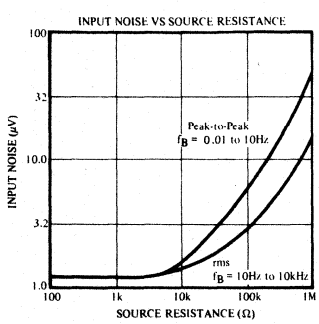
Specifications typical at 25°C with ±15VDC power supply unless otherwise noted.

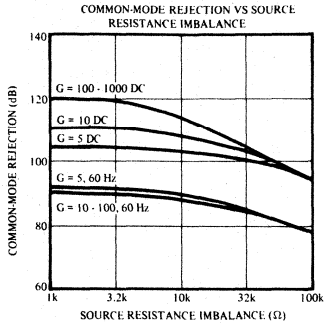
MODEL	3629AP, 3629AM			3629BP, 3629BM, 3629SM			3629CP, 3629CM			UNITS
	min	typ	max	min	typ	max	min	typ	max	
GAIN										
Range of Gain	5		1000	•		•	•		•	V/V
Gain Equation		G = 5 + 20k/R_G			•			•		V/V
Error From Equation, DC			(1)			•			•	
Gain Temp. Coefficient										
G = 5		2	5		•	•		•	•	ppm/°C
G = 10		12	25		•	•		•	•	ppm/°C
G = 100		20	45		•	•		•	•	ppm/°C
G = 1000		25	50		•	•		•	•	ppm/°C
Nonlinearity, DC		±(0.002 + 10^{-5}G)	±(0.005 + 2 x 10^{-5}G)		±(0.001 + 10^{-5}G)	±(0.003 + 10^{-4}G)		±(0.001 + 10^{-5}G)	±(0.003 + 10^{-4}G)	% p-p FS
RATED OUTPUT										
Voltage	±10	±12.5		•	•		•	•		V
Current	±10	±12.5		•	•		•	•		mA
Output Impedance G = 100		0.01			•			•		Ω
INPUT OFFSET VOLTAGE										
Initial Offset at 25°C		±25 ±200/G	±50 ±400/G		±10 ±100/G	±25 ±200/G		±10 ±100/G	±25 ±200/G	μV
vs. Temp.			±3 ±10/G			±1.5 ±7.5/G			±0.75 ±5/G	μV/°C
vs. Supply		5	10		•	•		•	•	μV/V
vs. Time		±0.4			•			•		μV/mo
INPUT BIAS CURRENT										
Initial Bias Current (each input)		±15	±35		±10	±25		±5	±20	nA
vs. Temp.		±0.30	±0.60		•	•		•	•	nA/°C
vs. Supply		±0.1	±0.2		•	•		•	•	nA/V
Initial Offset Current		±15	±50		±10	±30		±5	±20	nA
vs. Temp.		±0.6	±1.2		•	•		•	•	nA/°C
INPUT IMPEDANCE										
Differential		10 || 3			•			•		GΩ||pF
Common-mode		10 || 3			•			•		GΩ||pF
INPUT VOLTAGE RANGE										
Range	±10			•			•			V
CMR w/1kΩ Source Imbalance										
DC, G = 5	100	104		•	•		•	•		dB
, G = 10	106	110		•	•		•	•		dB
, G = 100 to 1000	110	120		•	•		•	•		dB
60 Hz All Gains	90	92		•	•		•	•		dB
INPUT NOISE										
Voltage, p-p, 0.01Hz - 10Hz		1.2			•			•		μV p-p
rms, 10Hz - 1.0 kHz		1.0			•			•		μV rms
Current, p-p, 0.01Hz - 10Hz		70			•			•		pA p-p
rms, 10Hz - 1.0kHz		20			•			•		pA rms
DYNAMIC RESPONSE										
Small Signal, ±3dB Flatness,										
G = 5		90			•			•		kHz
G = 10		60			•			•		kHz
G = 100		30			•			•		kHz
G = 1000		3.5			•			•		kHz
Small Signal, ±1% Flatness,										
G = 5		7.2			•			•		kHz
G = 10		3.8			•			•		kHz
G = 100		0.33			•			•		kHz
G = 1000		30			•			•		Hz
Full Power, G = 5 - 100		7.5			•			•		kHz
Slew Rate, G = 5 - 100	0.2	0.45		•	•		•	•		V/μsec
Settling Time (0.1%)										
G = 5		35			•			•		μsec
G = 100		85			•			•		μsec
G = 1000		350			•			•		μsec
Settling Time (.01%)										
G = 5		40			•			•		μsec
G = 100		120			•			•		μsec
G = 1000		400			•			•		μsec
POWER SUPPLY										
Rated Voltage		±15			•			•		V
Voltage Range	±5		±20	•		•	•		•	V
Current, Quiescent		±5	±7		•	•		•	•	mA
TEMPERATURE RANGE										
Specification(2)	-25		+85	•		•	•		•	°C
Operation	-55		+125	•		•	•		•	°C
Storage	-65		+150	•		•	•		•	°C

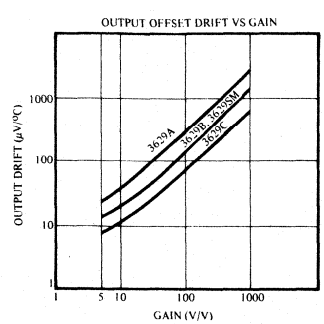
* Specifications same as for 3629AP/AM. (1) See Typical Performance Curves. (2) -55°C to +125°C for 3629SM.

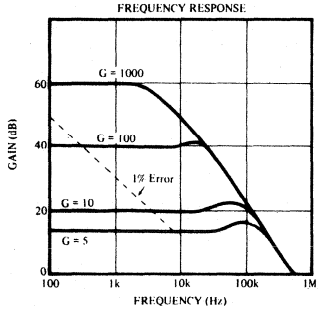
TABLE I.

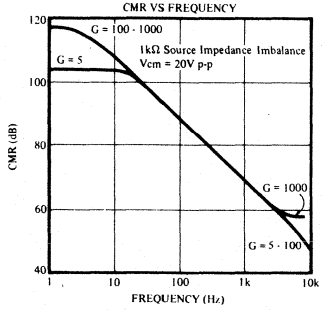
TYPICAL PERFORMANCE CURVES

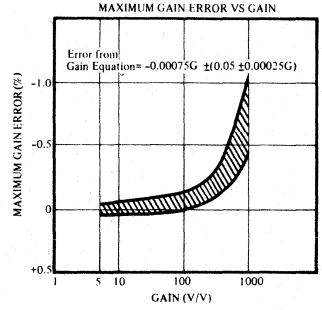


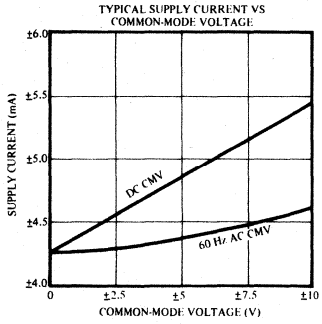


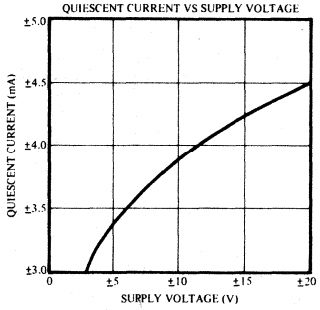


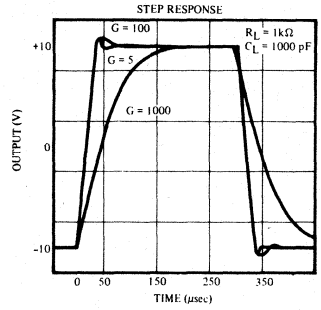












INSTALLATION AND OPERATING INSTRUCTIONS

OFFSET VOLTAGE ADJUSTMENT

Initial offset of the 3629 is trimmed to a very low value during production. In most applications further nulling will not be required. If it is necessary to null offset to the lowest possible value, a low cost single turn potentiometer can be connected between pins 4 and 5 as shown in Figure 6. Drift changes 0.33μV/°C for each 100μV of offset voltage nulled. Due to second order effects, the point of minimum offset drift does not occur at the point of zero offset voltage in approximately 25% of the cases. In these instances nulling the offset voltage may cause a slight increase in voltage drift.

A following stage should be used if large system offsets must be nulled. This method results in the lowest possible drift. In the circuit shown in Figure 7, the offset component of V_{OUT} due to V_1 is V_1R_2/R_1. Resistors R_1 through R_4 are selected to provide system scaling and to make the offset component of V_{OUT} due to V_2 cancel the component of V_{OUT} due to V_1.

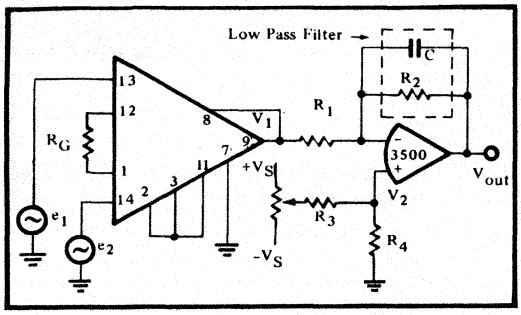


FIGURE 7. Multi-stage Amplifier For Offset Null and High Frequency Filtering.

NOISE

The 3629 offers very low noise at low and mid-frequencies. See specifications and performance curves. At frequencies above 100kHz, noise increases and may cause errors if the following circuitry responds to higher frequencies. When high frequency noise must be reduced, a low pass filter should be installed in a stage following the 3629. Figures 7 and 8 illustrate two high frequency filtering approaches.

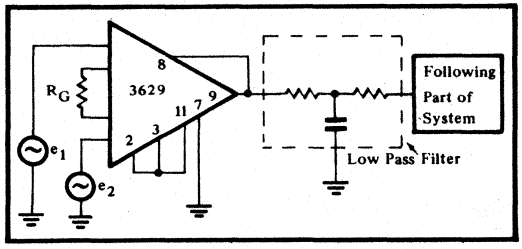


FIGURE 8. High Frequency Filter For Single Stage Amplifier.

APPLICATIONS

TRANSDUCER APPLICATION

A bridge transducer, Figure 9, with a 0 to 0.1V output requires amplification to interface with a 0 to 10V range system. The bridge introduces a 100Ω source imbalance and 0.25V of 60Hz noise is present on the ground return. Operating temperature range is 10°C to 50°C.

Absolute gain and offset errors can be trimmed to zero. The remaining error sources are tabulated in Table II as a % of Full Scale.

	Absolute Error		Resolution Error	
	Max	Typ	Max	Typ
Gain Nonlinearity	0.004%	0.002%	0.004%	0.002%
CMR	0.008%	0.0063%	0.008%	0.0063%
Noise 0.1 to 100Hz	0.0012%	0.0012%	0.0012%	0.0012%
Voltage Offset Drift	0.032%	0.020%		
Offset Current Drift	0.0048%	0.0024%		
Gain Drift	0.18%	0.08%		
TOTAL	0.230%	0.1119%	0.0132%	0.0095%

TABLE II. Transducer Application Error Analysis.

The 3629 Instrumentation Amplifier is, therefore, capable of 1/2LSB resolution in a 12 bit system over a 10°C to 50°C range and will produce 8 bit accuracy over the full temperature range.

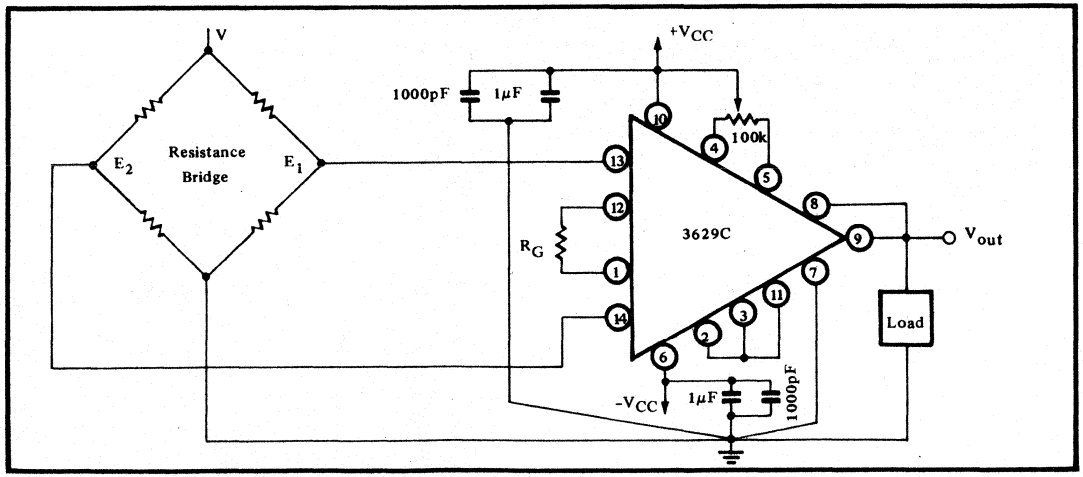
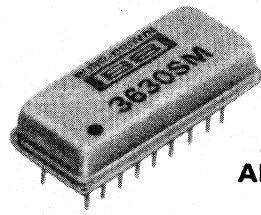


FIGURE 9. 3629 Used In A Transducer Application.

BURR-BROWN

3630



ADVANCE INFORMATION
Subject to Change

Very High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- ULTRA LOW VOLTAGE DRIFT - 0.25μV/°C
- LOW BIAS CURRENT - 20nA
- LOW NOISE - 1.2μV p-p
- HIGH INPUT IMPEDANCE - 10 x $10^9\Omega$
- HIGH CMR - 106dB @ 60Hz
- LOW OFFSET VOLTAGE - 25μV
- LOW NONLINEARITY - 0.002%

APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gages
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCERS
- LOW LEVEL SIGNALS

DESCRIPTION

The 3630 is a high accuracy, multi-stage, integrated circuit instrumentation amplifier designed for signal conditioning requirements where very high performance is desired.

A multi-stage design is used to provide excellent specifications and maximum versatility at reasonable cost. The input stage uses Burr-Brown's ultra-low drift low noise monolithic operational amplifiers to provide outstanding input characteristics.

All resistors are on a single network of Nichrome deposited on silicon. This provides high initial accuracy low TCR (temperature coefficient of resistance) and TCR matching, and outstanding stability as a function of time.

State-of-the-art laser-trimming techniques are used for reduction of offset voltage, offset voltage drift versus temperature, and for maximizing common-mode rejection.

In addition to providing an outstanding set of specifications, the 3630 offers convenience and ease of use in providing the following features: single capacitor active low pass filtering; easy output biasing (zero suppression and elevation); common-mode voltage generation for active guard drive; conveniently increased output current capability.

The unit is packaged in an 18-pin metal hermetic dual-in-line package which provides shielding, ease of installation, and environmental ruggedness.

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PDS-396 Printed in U.S.A. July, 1978

DISCUSSION

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are closed loop gain blocks whose committed circuitry accurately amplifies the voltage applied to their inputs. They respond only to the difference between the two input signals and exhibit extremely high input impedance, both differentially and common-mode. Feedback networks are packaged within the amplifier module. Only one external gain setting resistor must be added. An operational amplifier, on the other hand, is an open loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is difficult to reach the same level of performance. Using op amps often leads to design trade-offs when it is necessary to amplify low-level signals in the presence of common-mode voltages while maintaining high input impedances.

THE 3630

A simplified schematic of the 3630 is shown in Figure 1. It is a three-stage device which provides all the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found on integrated circuit instrumentation amplifiers.

The input stage (A1 and A2) consists of two of Burr-Brown's premium grade high accuracy bipolar operational amplifiers. They are connected in the noninverting configuration to provide the high input impedance (10 x $10^9\Omega$) desirable in the instrumentation amplifier function. The inherent low offset voltage and low offset voltage drift versus temperature of these amplifiers is improved even further by the state-of-the-art laser-trimming techniques.

The second stage (A3) consists of a high quality operational amplifier connected in a unity gain difference amplifier configuration. A critical part of this stage is the matching of the four 10k ohm resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to maintain excellent common-mode rejection. (The 106dB minimum at 60Hz for gains greater than 100V/V is a significant improvement compared to most other integrated circuit instrumentation amplifiers.)

All of the resistors shown in Figure 1 are part of a single thin-film network of Nichrome deposited on a passivated silicon substrate. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. The single network approach provides the excellent TCR (temperature coefficient of resistance) and TCR tracking desirable to provide gain accuracy and common-mode rejection when the 3630 is operated over wide temperature ranges.

The third stage (A4) of the 3630 adds a great deal of versatility and convenience to the amplifier. Its use allows easy implementation of active low pass filtering, output offsetting, and additional gain generation. The pin connections make the use of this stage optional but the effects are included in electrical specifications.

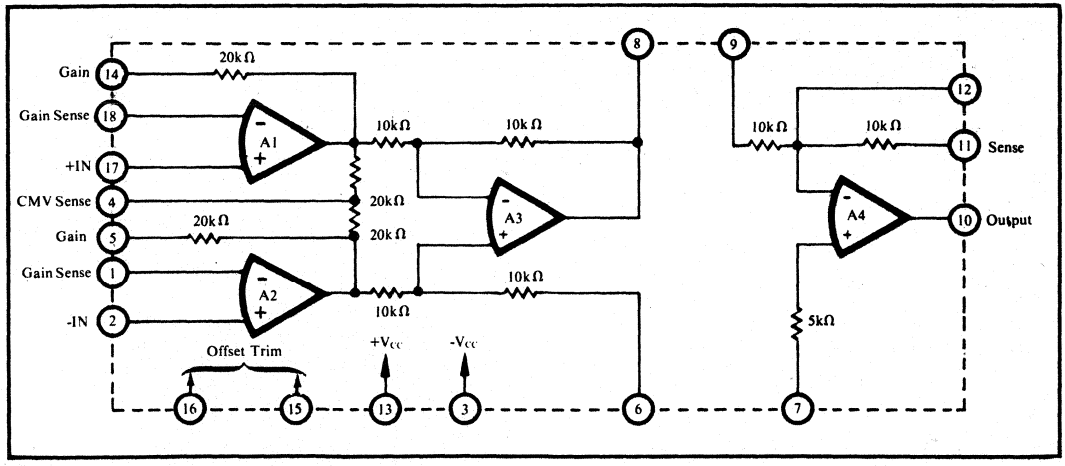


FIGURE 1. Simplified Schematic

USING THE 3630

Figure 2 shows the simplest configuration of the 3630. The gain is set by the external resistor R_G with a gain equation $G = 1 + 40k/R_G$. A low TCR resistor should be used for R_G since it contributes directly to the gain accuracy.

Pins 1, 5, 14 and 18 are accessible so that a four terminal connection can be made to R_G. (Pins 1 and 18 are the voltage sense terminals since no signal current flows into the operational amplifiers' inputs.) This may be useful at high gains where the value of R_G becomes small.

The optional offset null capability is shown in Figure 4. The adjustment affects only the input stage component of the offset voltage. Thus, the null condition will be disturbed when the gain is changed. Also, the input drift will be effected by approximately 0.33μV/°C per 100μV of input offset voltage nulled.

Output offsetting ("zero suppression" or "zero elevation") may be more easily accomplished with the 3630 than with most other IC instrumentation amplifiers.

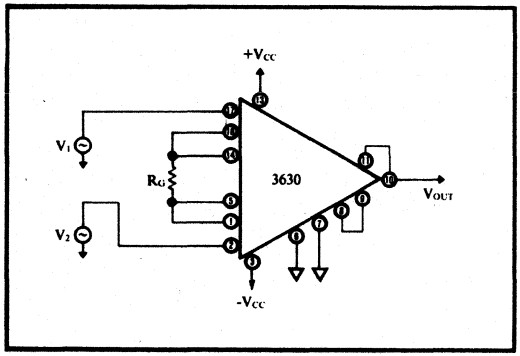


FIGURE 2. Basic Connections

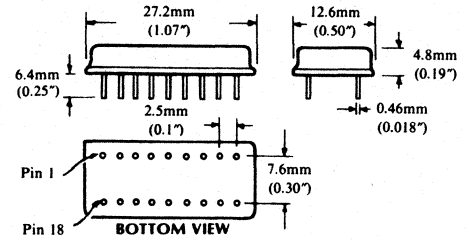
Figure 5 shows how this is done. The use of the noninverting input of the output stage means that CMR of the second stage is not disturbed and that any convenient value of variable resistor can be used.

The output stage also allows active low pass filtering to be implemented conveniently with a single capacitor. The effect this filtering has on noise reduction can be seen in the Typical Performance Curves.

The input stage contains extra resistors for the computation of input common-mode voltage. Figure 7 shows how this voltage, available at pin 4, can be used to drive the shield of the input cable. Since the cable is driven at the common-mode voltage the effects of distributed capacitance is reduced and the AC system common-mode rejection may be improved. Amplifier A1 is a buffer to supply larger currents than can be supplied by the 20kΩ resistors internally connected to pin 4.

Figure 8 shows how the output stage may be used to provide additional gain. If gains greater than 1000V/V are desired it is better to obtain them from the output stage than the input stage due to the low values of R_G required ($R_G < 40\Omega$ for $(1 + 40k/R_G) > 1000$).

MECHANICAL



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).

FIGURE 3. Mechanical Specifications

PIN DESIGNATIONS

1. Gain Sense
2. Inverting Input
3. Negative Supply
4. Common-mode Voltage Sense
5. Gain
6. Ground
7. Reference
8. Output of A_3
9. Input to A_4
10. Output
11. Sense
12. Summing Junction of A_4
13. Positive Supply
14. Gain
15. Offset Trim
16. Offset Trim
17. Noninverting Input
18. Gain Sense

ELECTRICAL SPECIFICATIONS

Specifications typical at 25°C with ±15VDC power supply and in circuit of Figure 2 unless otherwise noted.

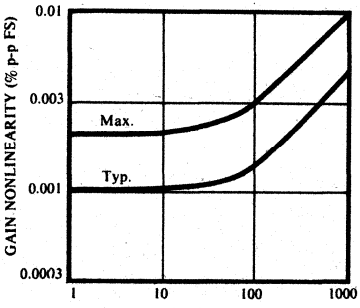
MODEL	3630AM			3630BM, 3630SM			3630CM			Units
	min	typ	max	min	typ	max	min	typ	max	
GAIN										
Range of Gain	1		1000	*		*	*		*	V/V
Gain Equation		G = 1 + 40k/R_G			*			*		V/V
Error From Equation, DC		(±0.05	(±0.1		(±0.02	(±0.05		(±0.02	(±0.05	%
		±0.0001G)	±0.0002G)		±0.00005G)	±0.0001G)		±0.00005G)	±0.0001G)	
Gain Temp. Coefficient[1]										
G = 1		2	5		*	*		*	*	ppm/°C
G = 10		20	50		*	*		*	*	ppm/°C
G = 100		22	55		*	*		*	*	ppm/°C
G = 1000		22	55		*	*		*	*	ppm/°C
Nonlinearity, DC		±(0.002	±(0.005		±(0.001	±(0.002		±(0.001	±(0.002	
		+ 10^{-5}G)	+ 2 x 10^{-5}G)		+ 4 x 10^{-6}G)	+ 10^{-5}G)		+4 x 10^{-6}G)	+ 10^{-5}G)	% of p-p FS
RATED OUTPUT										
Voltage	±10	±12.5		*	*		*	*		V
Current	±5	±12.5		*	*		*	*		mA
Output Impedance		0.01			*			*		Ω
INPUT OFFSET VOLTAGE										
Initial Offset at 25°C[2]		±25 ±200/G	±50 ±400/G		±10 ±100/G	±25 ±200/G		±10 ±100/G	±25 ±200/G	µV
vs. Temperature			±2 ±20/G			±0.75 ±10/G			±0.25 ±10/G	µV/°C
vs. Supply		±(1 + 20/G)			*			*		µV/V
vs. Time		±(1 + 20/G)			*			*		µV/mo
INPUT BIAS CURRENT										
Initial Bias Current (each input)		±15	±50		±10	±30		±5	±20	nA
vs. Temperature		±0.3			*			*		nA/°C
vs. Supply		±0.1			*			*		nA/V
Initial Offset Current		±15	±50		±10	±30		±5	±20	nA
vs. Temperature		±0.5			*			*		nA/°C
INPUT IMPEDANCE										
Differential		10 x 10^9 ‖ 3			*			*		Ω ‖ pF
Common-mode		10 x 10^9 ‖ 3			*			*		Ω ‖ pF
INPUT VOLTAGE RANGE										
Range, Linear Response	±10	±12		*	*		*	*		V
CMR w/1kΩ Source Imbal.										
DC to 60Hz, G = 1	80	90		*	*		*	*		dB
DC to 60Hz, G = 10	96	106		*	*		*	*		dB
DC to 60Hz, G = 100 to 1000	106	110		*	*		*	*		dB
INPUT NOISE										
Voltage, p-p, 0.01Hz - 10Hz		1.2			*			*		µV p-p
rms, 10Hz - 1.0kHz		1.0			*			*		µV rms
Current, p-p, 0.01Hz - 10Hz		70			*			*		pA p-p
rms, 10Hz - 1.0kHz		20			*			*		pA rms
DYNAMIC RESPONSE										
Small Signal, ±3dB Flatness,										
G = 1		150			*			*		kHz
G = 10		90			*			*		kHz
G = 100		25			*			*		kHz
G = 1000		2.5			*			*		kHz
Small Signal, ±1% Flatness,										
G = 1		20			*			*		kHz
G = 10		10			*			*		kHz
G = 100		1			*			*		kHz
G = 1000		200			*			*		Hz
Full Power, G = 1 - 100		7.5			*			*		kHz
Slew Rate, G = 1 - 100	0.2	0.5		*	*		*	*		V/µsec
Settling Time (0.1%)										
G = 1		60			*			*		µsec
G = 100		100			*			*		µsec
G = 1000		500			*			*		µsec
Settling Time (.01%)										
G = 5		100			*			*		µsec
G = 100		150			*			*		µsec
G = 1000		1000			*			*		µsec
POWER SUPPLY										
Rated Voltage		±15			*			*		V
Voltage Range	±5		±20	*		*	*		*	V
Current, Quiescent		±8	±14		*	*		*	*	mA
TEMPERATURE RANGE										
Specification[3]	-25		+85	*		*	*		*	°C
Operation	-55		+125	*		*	*		*	°C
Storage	-65		+150	*		*	*		*	°C

NOTES:
1. With R_G TCR = 0 ppm/°C
2. Trimmable to zero at any one gain.
3. -55°C to +125°C for 3630SM.

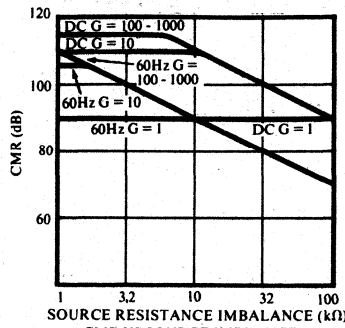
*Specifications same as for 3630AM

TYPICAL PERFORMANCE CURVES

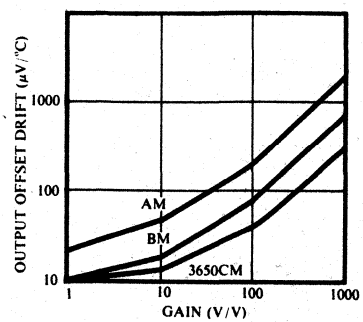
At 25°C and in circuit of Figure 2 unless otherwise noted.



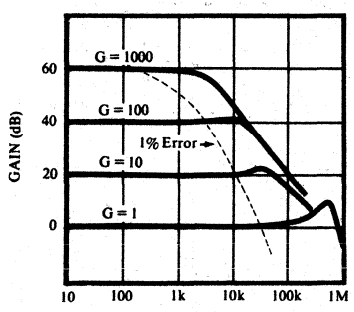
GAIN NONLINEARITY VS GAIN



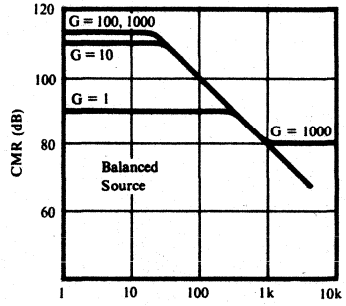
CMR VS SOURCE IMBLANCE



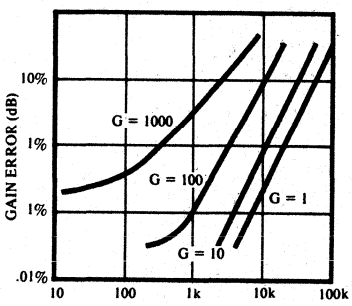
OUTPUT OFFSET DRIFT VS GAIN



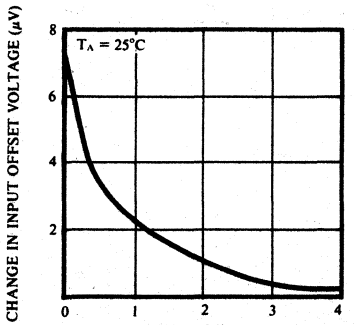
GAIN VS FREQUENCY



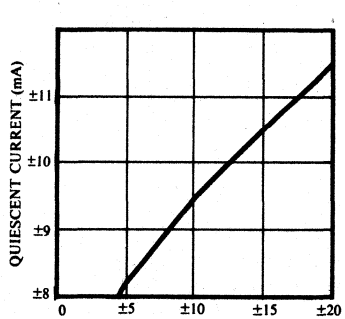
CMR VS FREQUENCY



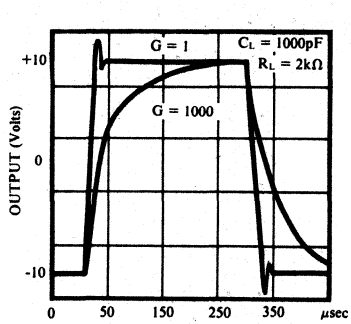
GAIN ERROR VS FREQUENCY



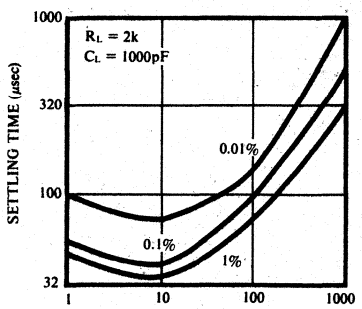
WARM-UP DRIFT VS TIME



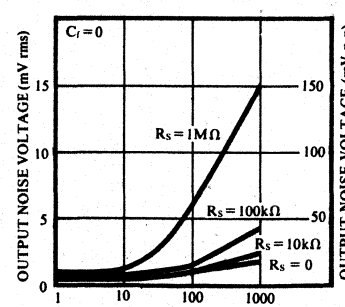
QUIESCENT CURRENT VS SUPPLY



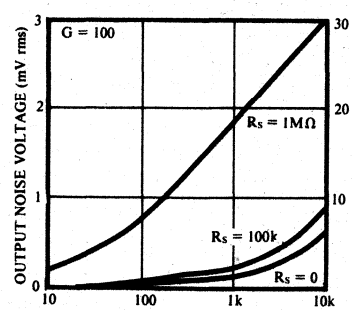
STEP RESPONSE



SETTLING TIME VS GAIN



OUTPUT NOISE VS GAIN



OUTPUT NOISE VS 3dB FREQUENCY

APPLICATIONS

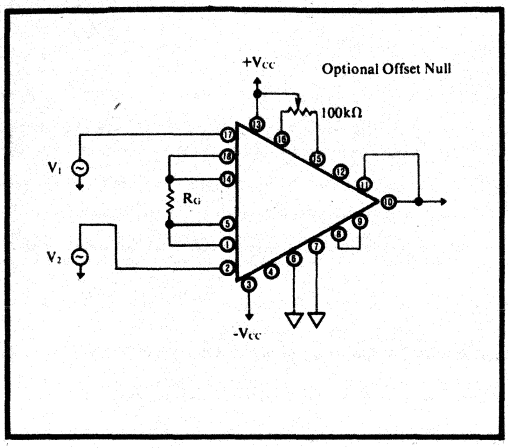


FIGURE 4. Optional Offset Null

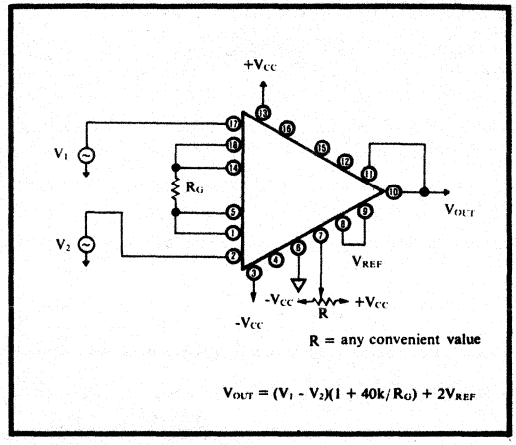


FIGURE 5. Output Offsetting

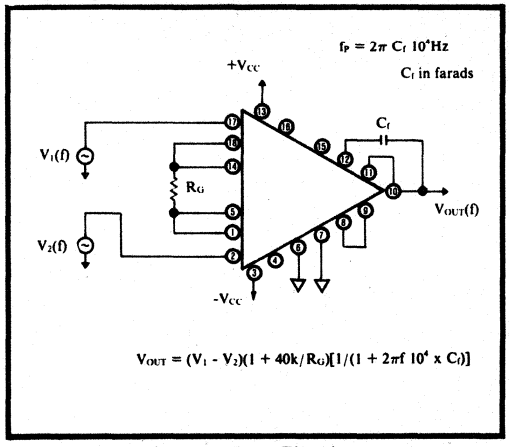


FIGURE 6. Active Low Pass Filtering

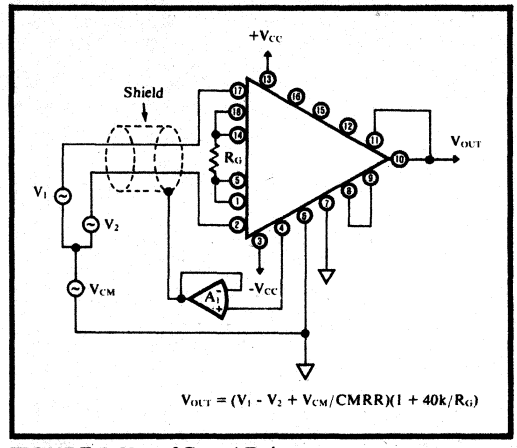


FIGURE 7. Use of Guard Drive

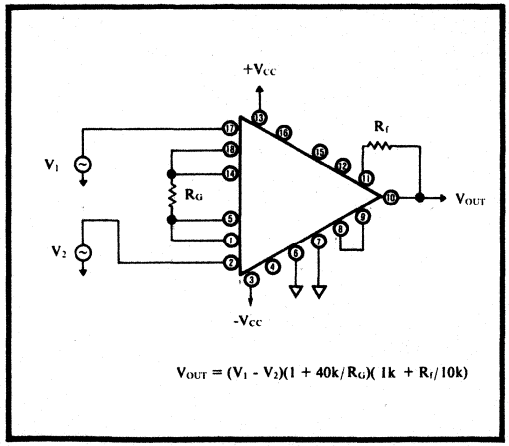


FIGURE 8. Additional Gain From Output Stage

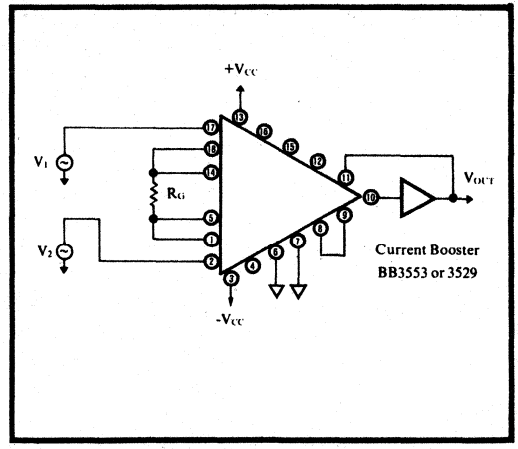
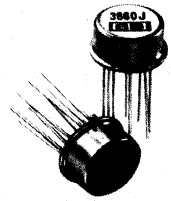


FIGURE 9. Output Power Boosting

BURR-BROWN

3660



Low Drift INSTRUMENTATION AMPLIFIER

FEATURES

- **PRESERVES SIGNAL INTEGRITY**
  - **Input Impedance 2 x $10^{10}\Omega$**
  - **Gain Nonlinearity < 0.03%**
  - **CMR > 110dB @ G = 1000**
- **REDUCES TEMPERATURE ERRORS**
  - **Voltage Drift < 2.5μV/°C @ G = 1000**
  - **Bias Current Drift < 2nA/°C**
- **EASY TO USE**
  - **Single Resistor Gain Adjust 1V/V to 1000V/V**
- **LOW COST**

DESCRIPTION

The 3660 is an integrated circuit instrumentation amplifier. It is a differential input amplifier with a transfer function of

$$V_{OUT} = (e_2 - e_1)\ 100k\Omega/R$$

where R is the single external gain setting resistor.

Instrumentation amplifiers differ from operational amplifiers in that they are committed closed-loop devices. As such they only (but very accurately) amplify and have no summing junction. Their high input impedance (2 x $10^{10}\Omega$), large gain (1000V/V), easy gain adjustment (1V/V to 1000V/V), high common-mode rejection (< 110dB at G = 1000V/V) and low voltage drift (< 2.5μV/°C at G = 1000) eliminate the problems and compromises of trying to use operational amplifiers to realize the same gain function. To achieve performance even close to that of the 3660 family using operational amplifiers would require a well matched pair of op amps and four matched and tracking precision resistors.

The excellent performance, small size, low cost, and integrated circuit reliability make the 3660 a natural choice for applications such as thermocouples, strain gages, bridges and other low level transducers.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-316A

Printed in U.S.A. July, 1978

DISCUSSION

NOT AN OP AMP

An instrumentation amplifier differs fundamentally from an operational amplifier. An op amp is an open loop uncommitted device whose closed loop performance depends on the external networks used to close the loop. While an op amp can be used to get the same basic transfer function as an instrumentation amplifier, it is generally difficult (often impossible) to achieve the same level of performance. The use of an op amp usually leads to design tradeoffs when it is necessary to amplify low level signals in the presence of common-mode voltages while maintaining high input impedances.

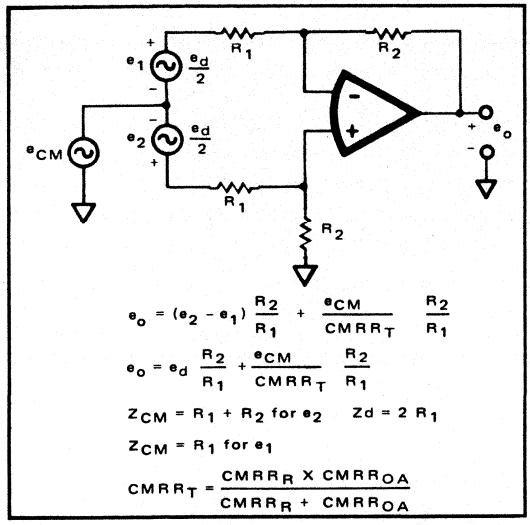


FIG. 1 Single Op Amp, Differential Input Configuration.

When a single op amp is used (see Figure 1), there are opposing constraints if there is a need for both high gain ($R_2 \div R_1 >> 0$, i.e. R_1 small) and high input impedances (R_1 large). Also, the common-mode rejection ratio of the total circuit, $CMRR_T$, is a function of the op amps rejection, $CMRR_{OA}$, and the effective rejection caused by resistor mismatches, $CMRR_R$. [For example, ±0.1% resistors in a gain of 10 circuit can have a CMR of only 69 dB (CMR (dB) = 20 $\log_{10}$ CMRR (V/V))].

INSTRUMENTATION AMPLIFIERS

The 3660 is a monolithic integrated circuit instrumentation amplifier. It is a closed loop differential input gain block. It is a committed circuit whose primary function is to accurately amplify the voltage applied to its inputs. Ideally, the instrumentation amplifier responds only to the difference between the two input signals ($e_2 - e_1$) and exhibits extremely high impedance between the two input terminals (differential input impedance) and from each input to ground (common-mode input impedance).

Figure 2 shows the simple model of an instrumentation amplifier which eliminates most of the problems of using op amps.

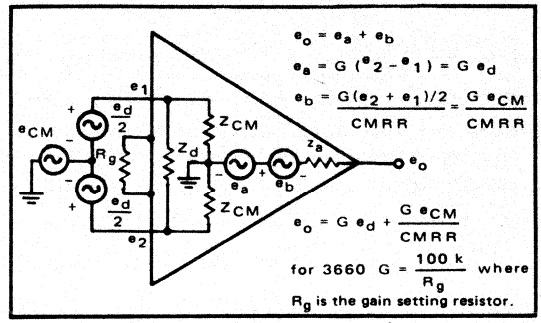


FIG. 2 Model of an Instrumentation Amplifier.

WHAT ARE THE ALTERNATIVES?

There are three basic alternatives available when you have a need to accurately amplify signals in the presence of common-mode voltages and noise and maintain high input impedances.

1. Build a single op amp circuit in a differential input configuration.
2. Build a circuit of multiple op amps interconnected to form an instrumentation amplifier.
3. Buy a committed instrumentation amplifier.

Some of the shortcomings of the first alternative were just discussed. One additional problem is that gain changes are difficult. Two resistors need to be changed and match and tracking must be maintained.

The second and third alternatives are usually the most realistic. There are a number of multiple op amp circuits, each with its own set of advantages and disadvantages(1), which might be suitable in a particular application. There are also available low drift op amps and matched pairs of amplifiers (Burr-Brown's 3500E and 3500MP) for use in such circuits.

The build or buy alternatives above, are swinging heavily towards buy. The appearance of the relatively low cost integrated circuit instrumentation amplifier is a step towards making the building at one's own instrumentation amplifiers as obsolete, as building one's own op amps.

MANY BENEFITS

The 3660 offers the user many benefits for his instrumentation applications:

High Common-Mode Rejection – to preserve system accuracy in the presence of common-mode voltage.

High Input Impedance – to prevent errors due to source loading and source impedance unbalance.

Input and Output Protection – output protected for shorts to ground and either supply. Input protect to ±VCC.

Small, Hermetically Sealed Packages – to take up less board space and to improve reliability.

Low Cost – to make it easy on the budget.

Internal Frequency Compensation – no large capacitors.

(1) J. Graeme, "Applications of Operational Amplifiers - Third Generation Techniques", McGraw-Hill, 1973.

SPECIFICATIONS

ELECTRICAL

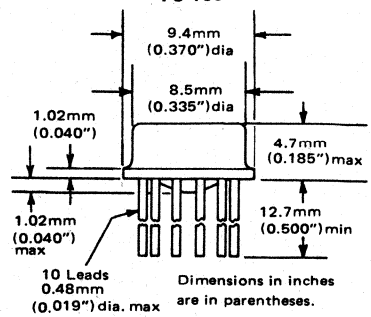
Specifications typical at 25°C and ±15 VDC Power Supply Unless Otherwise Noted.

MODELS	3660J	3660K	3660S
GAIN			
Range of Gain, min	G = 1 to 1000 V/V		
Gain Equation	$G = \frac{100\ k\Omega}{R}$ V/V		
Error from Equation (may be zeroed)	(±0.5 - 0.003G)%		
Gain temp. Coefficient	±(35 +0.05G)ppm/°C		
Nonlinearity			
G = 1-100, max	0.1%	0.03%	0.03%
G = 1000, max	0.1%	0.05%	0.05%
OUTPUT			
Rated output, min	±10 V, ±10 mA		
Output Impedance	0.15 Ω		
INPUT			
Input Impedance, Differential	$\frac{2 \times 10^{10}}{G}$ Ω ‖ 9 pF		
Common-Mode	2×10^{10} Ω ‖ 3 pF		
Input Voltage Range, min	±10 V		
CMR, DC to 60 Hz with 1 kΩ source unbalance			
G = 1, min	60 dB	70 dB	70 dB
G = 10, min	76 dB	90 dB	90 dB
G = 100, min	86 dB	100 dB	100 dB
G = 1000, min	96 dB	110 dB	110 dB
OFFSETS AND DRIFT(RTI)			
Input Offset, max (1) (may be zeroed)	$\pm(6 + \frac{600}{G})$ mV	$\pm(1 + \frac{300}{G})$ mV	$\pm(1 + \frac{300}{G})$ mV
vs. temperature, max	$\pm(10 + \frac{1000}{G})\mu V/°C$	$\pm(2 + \frac{500}{G})\mu V/°C$	$\pm(2 + \frac{500}{G})\mu V/°C$
vs. Supply	$\pm(8 + \frac{5000}{G})\mu V/V$		
vs. Time	$\pm(2 + \frac{1500}{G})\mu V/mo$		
Input Bias Current, max (either input)	200 nA		
vs. Temperature, max	-2 nA/°C		
vs. Supply	±0.25 nA/V		
Input Difference Current,max	±50 nA	±20 nA	±20 nA
vs. Temperature, max	±0.5 nA/°C	±0.2 nA/°C	±0.2 nA/°C
INPUT NOISE(RTI)(1)			
Voltage, p-p. 0.01 Hz - 10 Hz	$(3 + \frac{900}{G})\mu V$ p-p		
rms, 10 Hz - 10 kH	$(1 + \frac{130}{G})\mu V$ rms		
Current,p-p. 0.01Hz - 10Hz	150 pA p-p		
rms 10Hz - 10 kHz	50 pA rms		
DYNAMIC RESPONSE			
Small Signal, ±3 dB Flatness			
G = 1	800 kHz		
G = 10	95 kHz		
G = 100	72 kHz		
G = 1000	22 kHz		
Small Signal, ±1% Flatness			
G = 1	20 kHz		
G = 10	15 kHz		
G = 100	10 kHz		
G = 1000	3 kHz		
Full, Power, G = 1-100	28 kHz		
Slew Rate, G = 1-100	1.8 V/μs		
Settling Time (0.1%)			
G = 1	17 μs		
G = 10	19 μs		
G = 100	20 μs		
G = 1000	50 μs		
POWER SUPPLY			
Rated Voltage	±15 V		
Voltage Range	±7 VDC to ±20 VDC		
Quies. Supply Current, max	6 mA		
TEMPERATURE RANGE			
Specifications	0 to +70°C	0 to +70°C	-55 to +125°C
Operation		-55 to +125°C	
Storage		-65 to +150°C	

(1) RTI = referred to input. May be referred to output by multiplying by gain G.
(2) Check with factory for current prices.

MECHANICAL

TO-100



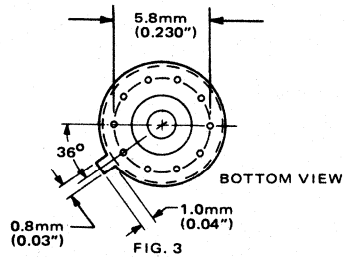


FIG. 3

PIN CONFIGURATION

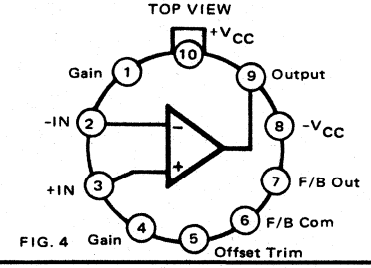
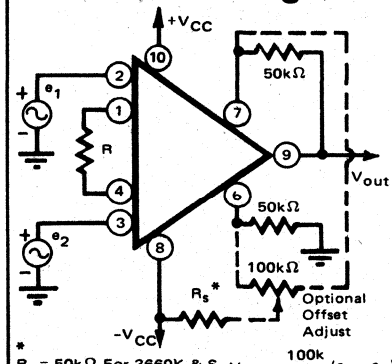


FIG. 4

Connection Diagram



* R_s = 50kΩ For 3660K & S
R_s = 3kΩ For 3660J

$V_{out} = \frac{100k}{R}(e_2 - e_1)$

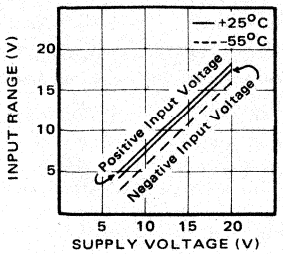
FIG. 5

(CONNECTOR: 1000 MC)

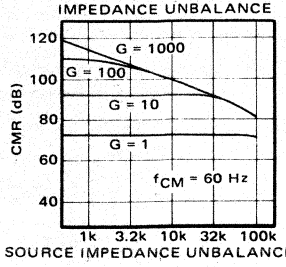
TYPICAL PERFORMANCE CURVES

(TYPICAL @ 25°C and ±15 VDC POWER SUPPLIES UNLESS OTHERWISE NOTED)

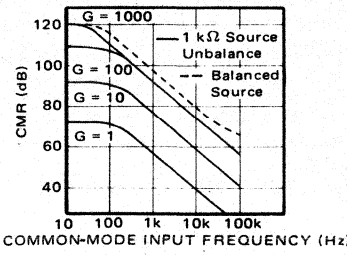
INPUT RANGE FOR LINEAR RESPONSE



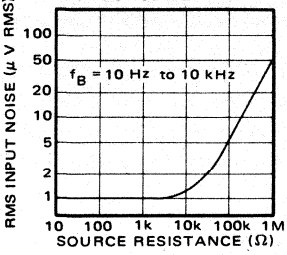
CMR VS.SOURCE IMPEDANCE UNBALANCE



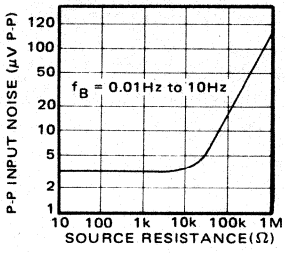
COMMON-MODE REJECTION VS.FREQUENCY



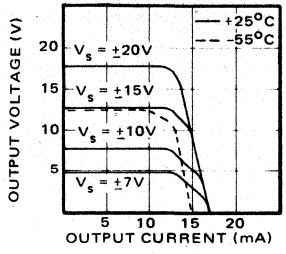
RMS INPUT NOISE VOLTAGE VS.SOURCE RESISTANCE



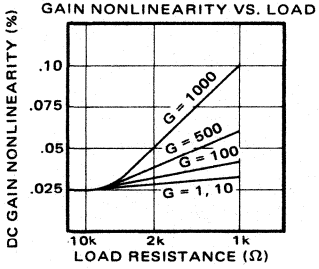
PEAK-TO-PEAK INPUT NOISE VOLTAGE VS.SOURCE RESISTANCE



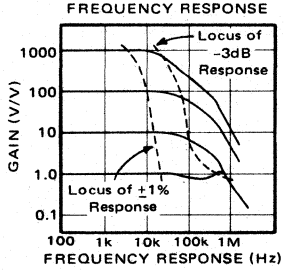
MAXIMUM OUTPUT VOLTAGE VS. OUTPUT CURRENT



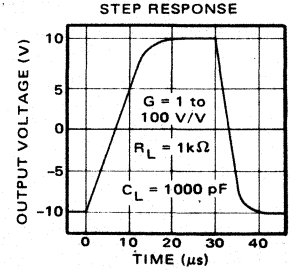
GAIN NONLINEARITY VS. LOAD



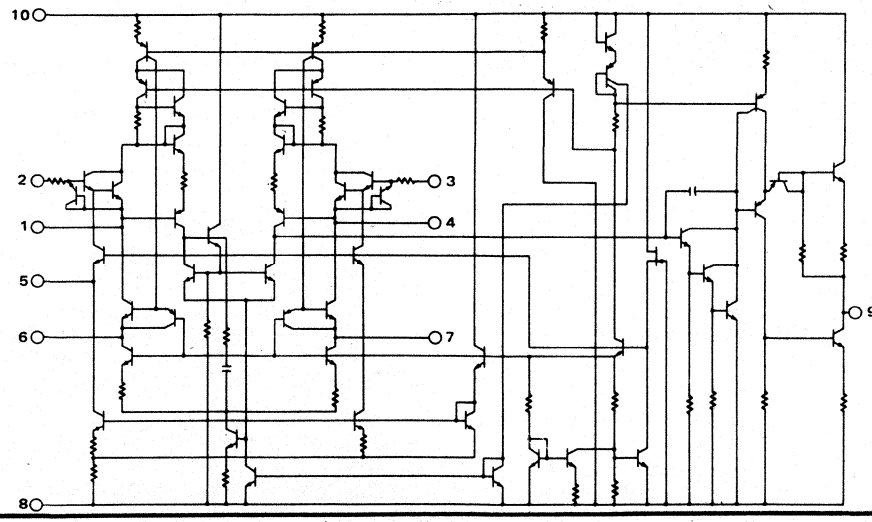
FREQUENCY RESPONSE



STEP RESPONSE



EQUIVALENT CIRCUIT



THEORY OF OPERATION

The 3660 is a single chip monolithic integrated circuit. The design has been optimized to provide excellent performance and maintain low cost.

Figure 6 is a simplified schematic of the 3660. It shows that the amplifier is basically a two stage device. It has a fixed gain output stage (shown as the op amp symbol) and a variable gain input stage (adjusted by R_g). The two stage nature of the design is the reason that many of the specifications consist of two components, one of which is a function of gain.

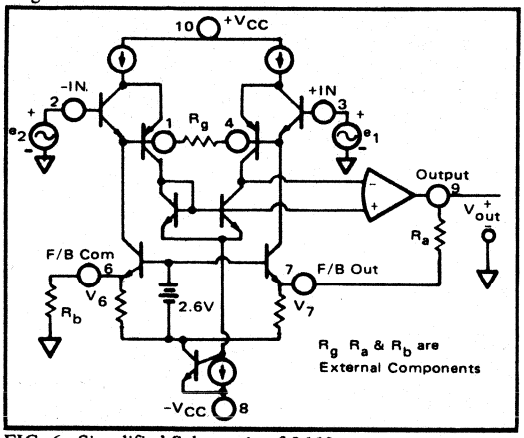


FIG. 6. Simplified Schematic of 3660.

An analysis of the circuit in Figure 6 is straight forward but lengthy even with simplifying assumptions. Therefore, only the results are given below:

$$V_{out} = (e_1 - e_2)\frac{2R_a}{R_g} + R_a\left(\frac{V_7}{R_a} - \frac{V_6}{R_b}\right) \quad (1)$$

Equation (1) consists of two parts. The first part is the desired gain equation where R_g is the gain setting resistor and R_a is the output stage feedback resistor (nominally 50 kΩ). The second part is an output component of offset voltage whose magnitude is dependent on the matching of R_a and R_b. V_6 and V_7 are voltages derived from -VCC. (If -VCC is -15V then $V_6 = V_7 \cong -13V$). The effect of unequal values of R_a and R_b is to generate an additional output component of offset voltage:

$$E_{os_{out}} = R_a\left(\frac{V_7}{R_a} - \frac{V_6}{R_b}\right) \cong -13V\,\frac{R_b - R_a}{R_a} \quad (2)$$

$E_{os_{out}}$ should be added to the output component of the amplifier itself (600 mV for J grade, 300 mV for K and S grades) to compute the total output component of offset voltage.

INSTALLATION AND OPERATING INSTRUCTIONS

SELECTION OF R_a AND R_b

The tolerance and TCR (Temperature Coefficient of Resistance) of R_a and R_b should be chosen to fit the particular application and grade of amplifier used. As explained in "Theory of Operation" the initial mismatch of R_a and R_b will generate an additional output component of offset voltage. If -VCC is -15V and M is the mismatch of R_a and R_b in percent.

$$E_{os_{out}} \cong \frac{13 \times M}{100} \text{ VDC}$$

Thus, 1% resistors in a worse case mismatch (M = 2) will generate approximately 260 mV of output offset. This can be trimmed to zero (see "Offset Voltage Adjustment").

A mismatch in TCR of R_a and R_b will generate an output voltage drift versus temperature of

$$\Delta E_{os_{out}}/\Delta T \cong 13 \times T\ \mu V/^oC$$

where T is the mismatch in TCR in ppm/°C. Thus, 20 ppm/°C resistors in a worse case condition (T = 40) will generate approximately 520 μV/°C of output offset voltage drift.

OFFSET VOLTAGE ADJUSTMENT

The 3660 will function without the offset voltage trim components installed. This would be suitable for applications where the offset is not critical – such as when the output is AC coupled to the following circuitry.

The simplest circuit to trim offset voltage is shown in Figure 5. It uses a single adjustment to compensate for both input and output components of offset voltage. Because of this the offset voltage will change if the gain is changed.

Figure 7 shows a more complete trim circuit which will make the offset voltage much less dependent on gain changes.

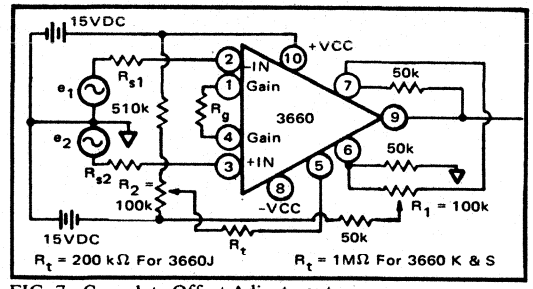


FIG. 7. Complete Offset Adjustment.

Nulling the offset voltage is a two step procedure:

Step 1. Set e_1 and e_2 to zero. Adjust R_g for maximum gain (R_g = 100Ω for G = 1000 V/V). Adjust R_1 for zero volts at pin 9.

Step 2. Adjust R_g for minimum gain (R_g = 100 kΩ for G = 1 V/V). Adjust R_2 for zero volts at pin 9.

The value of R_t in Figure 7 may be changed to trade range for resolution. The larger the value is, the smaller the trim range will be and the better the resolution will be.

INPUT BIAS AND OFFSET CURRENTS

The bias currents flowing through the source resistances (see Figure 7) will generate offset voltages of $E_{os2} = I_{B2} \times R_{s2}$ and $E_{os1} = I_{B1} \times R_{s1}$. If $R_{s1} = R_{s2} = R_s$ the offset caused by the offset current will be

$$(E_{os2} - E_{os1})\frac{100k}{R_a} = (I_{os} \times R_s)\frac{100k}{R_a}$$

For normal values of R_s this offset can be nulled with the circuits of Figure 5 or 7. (Note that the source must be returned to power supply common or the effective R_s will be infinite and the amplifier will saturate.)

APPLICATIONS

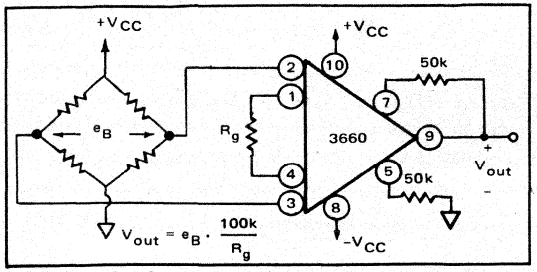


FIG. 8. Bridge Circuit Amplification.

The high gain, large common-mode rejection and moderate voltage drift of the 3660 make it well suited for most bridge circuit applications. In applications where the source impedance is high and the input bias currents of the 3660 cause objectionable errors, the FET input 3670 instrumentation should be considered. Request PDS-317.

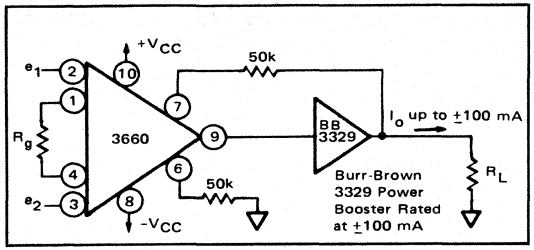


FIG. 9. Higher Output Current

Figure 9 shows how the 3660 can easily accomodate a power booster inside its output feedback loop to raise the output current capability above ±10 mA.

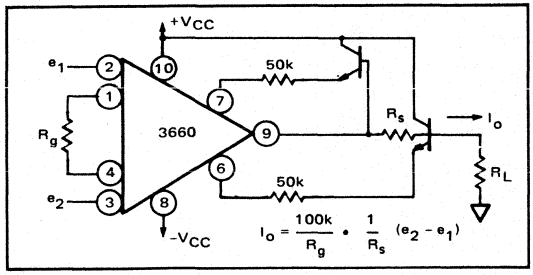


FIG. 10. Voltage-To-Current Circuit.

The 3660 may be operated in a voltage-to-current configuration as shown in Figure 10. R_S should be kept small since it is in series with the load and, therefore, reduces the output voltage swing.

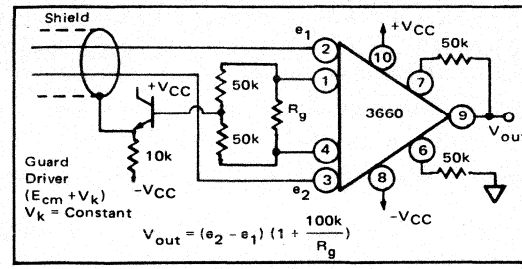


FIG. 11. Active Guard Drive.

The degeneration of common-mode rejection caused the capacitance of shielded cable can be reduced with the active guard drive circuit in Figure 11.

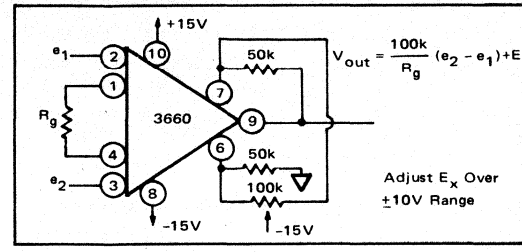


FIG. 12. Output Biasing.

When it is desired to bias the output over a large range (such a chart recorder bias) the circuit in Figure 12 may be used.

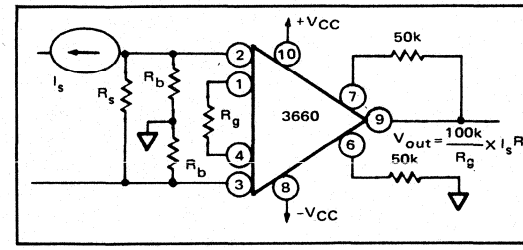
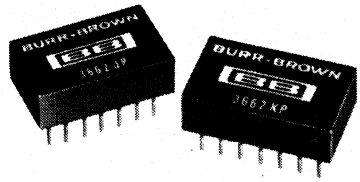


FIG. 13. Current Measuring Circuit.

When the parameter to be amplified is in the form of a current, a shunt resistor may be used to convert it into a voltage. The common-mode voltage limits of the amplifier must be observed and input bias current return paths must be used if the shut is floating.

BURR-BROWN

3662



Low Offset Voltage INSTRUMENTATION AMPLIFIER

FEATURES

- **PRESERVES SIGNAL INTEGRITY**
  - **Input Impedance 2 x $10^{10}\Omega$**
  - **Gain Nonlinearity < ±0.025%**
  - **CMR > 104dB @ G = 1000**
- **REDUCES TEMPERATURE ERRORS**
  - **Voltage Drift < 2.4μV/°C @ G = 1000**
  - **Bias Current Drift < 2nA/°C**
- **EASY TO USE**
  - **Single Resistor Gain Adjust 1V/V to 1000V/V**
  - **Usually No Trimming Needed**

DESCRIPTION

The 3662 is an integrated circuit instrumentation amplifier. It is a differential input amplifier with a transfer function of

$$V_{OUT} = (e_2 - e_1)\ 100k\Omega/R_g$$

where R_g is the single external gain settling resistor.

Instrumentation amplifiers differ from operational amplifiers in that they are committed closed-loop devices. As such they only (but very accurately) amplify and have no summing junction. Their high input impedance ($2 \times 10^{10}\Omega$), large gain (1000V/V), easy gain adjustment (1V/V to 1000V/V), high common-mode rejection (> 104dB at G = 1000V/V), and low voltage drift (< 2.4μV/°C at G = 1000) eliminate the problems and compromises of trying to use operational amplifiers to realize the same gain function. Modern hybrid integrated circuit design and state-of-the-art laser-trimming techniques reduce the offset voltage to a point where the need for additional nulling by the user is normally eliminated.

The excellent performance, small size, low cost, and integrated circuit reliability make the 3662 a natural choice for applications such as thermocouples, strain gages, bridges and other low level transducers.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-344A

Printed in U.S.A. July, 1978

DISCUSSION

NOT AN OP AMP

An instrumentation amplifier differs fundamentally from an operational amplifier. An op amp is an open loop uncommitted device whose closed loop performance depends on the external networks used to close the loop. While an op amp can be used to get the same basic transfer function as an instrumentation amplifier, it is generally difficult (often impossible) to achieve the same level of performance. The use of an op amp usually leads to design tradeoffs when it is necessary to amplify low level signals in the presence of common-mode voltages while maintaining high input impedances.

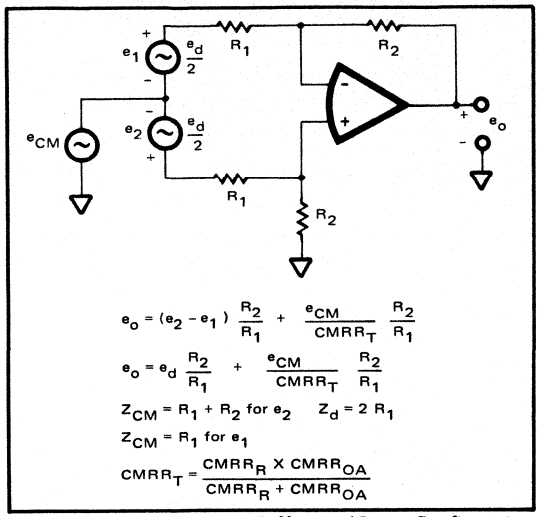


FIGURE 1 Single Op Amp, Differential Input Configuration.

When a single op amp is used (see Figure 1), there are opposing constraints if there is a need for both high gain ($R_2 \div R_1 >> 0$, i.e. R_1 small) and high input impedances (R_1 large). Also, the common-mode rejection ratio of the total circuit, $CMRR_T$, is a function of the op amps rejection, $CMRR_{OA}$, and the effective rejection caused by resistor mismatches, $CMRR_R$. [For example, ±0.1% resistors in a gain of 10 circuit can have a CMR of only 69 dB (CMR (dB) = 20 $\log_{10}$ CMRR (V/V))].

INSTRUMENTATION AMPLIFIERS

The 3662 is an integrated circuit instrumentation amplifier. It is a closed loop differential input gain block – a committed circuit whose primary function is to accurately amplify the voltage applied to its inputs. Ideally, the instrumentation amplifier responds only to the difference between the two input signals ($e_2 - e_1$) and exhibits extremely high impedance between the two input terminals (differential input impedance) and from each input to ground (common-mode input impedance). Figure 2 shows the simple model of an instrumentation amplifier which eliminates most of the problems of using op amps.

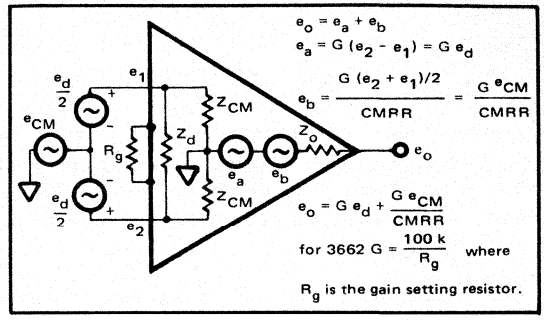


FIGURE 2. Model of an Instrumentation Amplifier.

THEORY OF OPERATION

Figure 3 is a simplified schematic of the 3662. It shows that the amplifier is basically a two stage device. It has a fixed gain output stage (shown as the op amp symbol) and a variable gain input stage (adjusted by R_g). The two stage nature of the design is the reason that many of the specifications consist of two components, one of which is a function of gain.

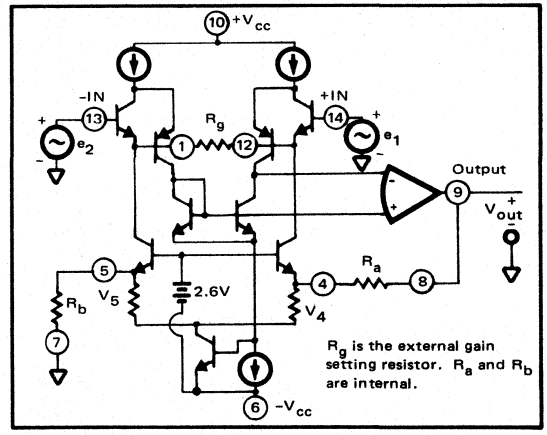


FIGURE 3. Simplified Schematic of 3662.

An analysis of the circuit in Figure 3 is straightforward but lengthy even with simplifying assumptions. Therefore, only the results are given below:

$$V_{out} = (e_1 - e_2)\frac{2R_a}{R_g} + R_a\left(\frac{V_4}{R_a} - \frac{V_5}{R_b}\right) \qquad (1)$$

Equation (1) consists of two parts. The first part is the desired gain equation where Rg is the gain setting resistor and R_a is the output stage feedback resistor (internal 50kΩ). The second part is an output component of offset voltage whose magnitude is dependent on the matching of R_a and R_b. In the 3662 this component of error is significantly reduced by the use of advanced laser trimming techniques and hybrid construction. In fact, the entire offset voltage is reduced to the point where the user nulling usually required with other instrumentation amplifiers is normally not necessary with the 3662.

SPECIFICATIONS

ELECTRICAL

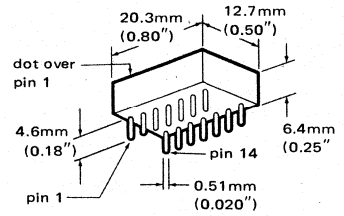
Specifications typical at 25°C and ±15 VDC Power Supply Unless Otherwise Noted.

MODELS	3662JP	3662KP
GAIN		
Range of Gain, min	G = 1 to 1000 V/V	
Gain Equation	$G = \frac{100\ k\Omega}{R}$ V/V	
Error from Equation (may be zeroed)	(±0.5 -0.003G)%	
Gain temp. Coefficient	±(50 +0.05G)ppm/°C	
Nonlinearity (1) G = 1 - 1000, max	0.1%	0.05%
OUTPUT		
Rated output, min	±10 V, ±10 mA	
Output Impedance	0.15 Ω	
INPUT		
Input Impedance, Differential	$\frac{2 \times 10^{10}}{G}$ Ω ‖ 9 pF	
Common-Mode	2×10^{10} Ω ‖ 3 pF	
Input Voltage Range, min	±10 V	
CMR, DC to 60 Hz with 1kΩ source unbalance		
G = 1, min	60 dB	66 dB
G = 10, min	76 dB	84 dB
G = 100, min	86 dB	94 dB
G = 1000, min	96 dB	104 dB
OFFSETS AND DRIFT (RTI)		
Input Offset, max (2) (may be zeroed)	$\pm(0.4 + \frac{100}{G})$mV	$\pm(0.2 + \frac{30}{G})$mV
vs temperature, max	$\pm(5 + \frac{1000}{G})\mu V/^{\circ}C$	$\pm(2 + \frac{400}{G})\mu V^{\circ}C$
vs Supply	$\pm(8 + \frac{5000}{G})\mu V/V$	
vs Time	$\pm(2 + \frac{1500}{G})\mu V/mo$	
Input Bias Current, max (either input)	+300nA	
vs Temperature, max	-2nA/°C	
vs Supply	±0.25nA/V	
Input Difference Current, max	±80nA	±30nA
vs Temperature, max	±0.8nA/°C	±0.3nA/°C
INPUT NOISE (RTI) (2)		
Voltage, p-p 0.01 Hz -10 Hz	$(3 + \frac{900}{G})\mu V$ p-p	
RMS, 10 Hz -10 kH	$(1 + \frac{130}{G})\mu V$ RMS	
Current, p-p 0.01 Hz -10 Hz	150 pA p-p	
RMS 10 Hz -10 kHz	50 pA RMS	
DYNAMIC RESPONSE		
Small Signal, ±3 dB Flatness		
G = 1	800 kHz	
G = 10	95 kHz	
G = 100	74 kHz	
G = 1000	27 kHz	
Small Signal, ±1% Flatness		
G = 1	20 kHz	
G = 10	15 kHz	
G = 100	10 kHz	
G = 1000	3 kHz	
Full Power, G = 1 - 100	28 kHz	
Slew Rate, G = 1 - 100	1.8V/μs	
Settling Time (0.1%)		
G = 1	17 μs	
G = 10	19 μs	
G = 100	20 μs	
G = 1000	50 μs	
POWER SUPPLY		
Rated Voltage	±15 V	
Voltage Range	±7 VDC to ±20 VDC	
Quies. Supply Current, max	6mA	
TEMPERATURE RANGE		
Specifications	0 to +70°C	
Operation	-55 to +125°C	
Storage	-65 to 150°C	

(1) Peak deviation from a best straightline, expressed as a percent of peak-to-peak full scale output.

(2) RTI = referred to input. May be referred to output by multiplying by gain G.

MECHANICAL



Row Spacing: 7.6mm (0.300")
Weight: 3.4 grams (0.12 oz.)
Connector: 14-pin DIP
0145MC

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std-202.

PIN CONNECTIONS

1. Gain	8. Sense
2. V_{OSI}	9. Out
3. V_{OSI}	10. $+V_{CC}$
4. V_{OSO}	11. Make No Connection
5. V_{OSO}	12. Gain
6. $-V_{CC}$	13. -In
7. Ref	14. +In

CONNECTION DIAGRAM

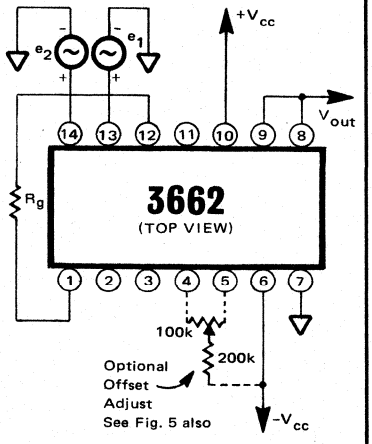
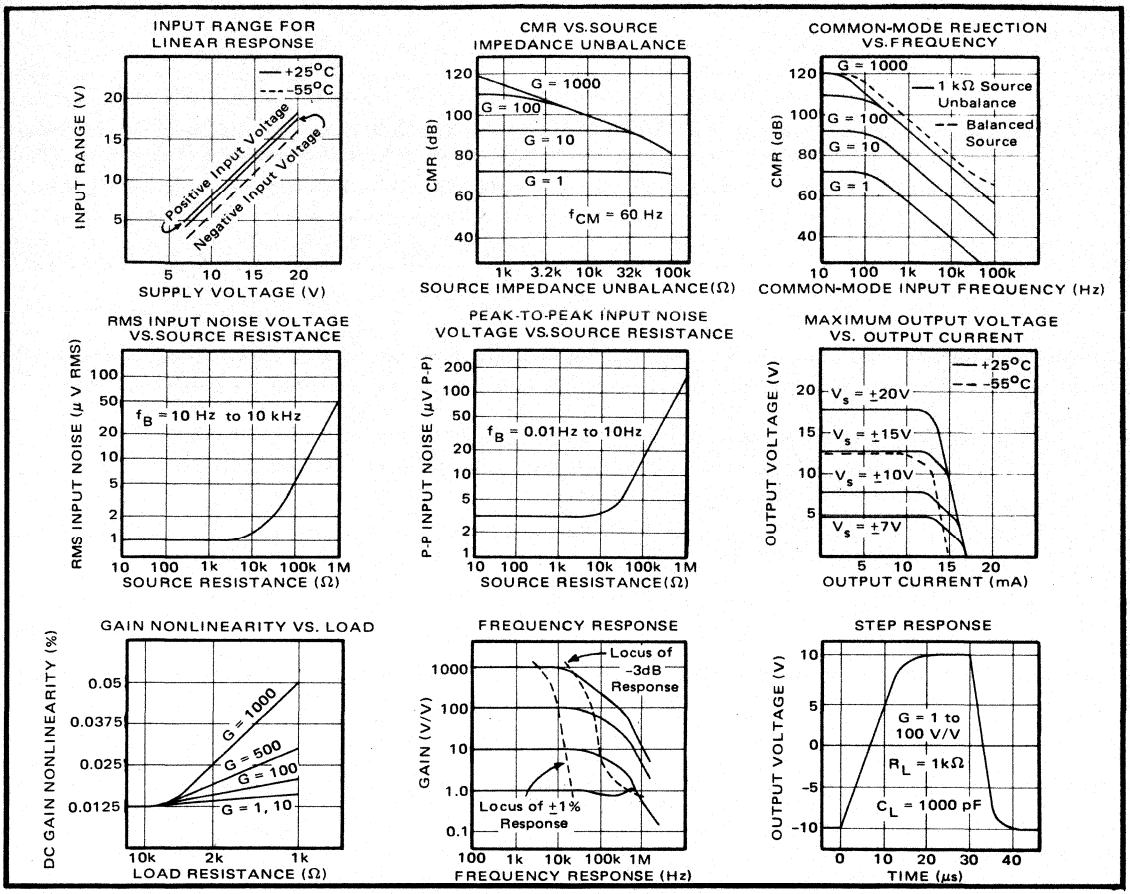


FIGURE 4

TYPICAL PERFORMANCE CURVES

(TYPICAL @ 25°C and ±15 VDC POWER SUPPLIES UNLESS OTHERWISE NOTED)



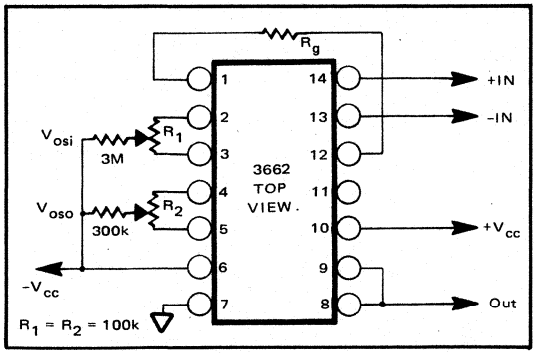


FIGURE 5. Alternate Optional Offset Voltage Adjustment.

The circuit in Figure 4 uses a single adjustment to trim both input and output components of offset voltage. Because of this the output voltage will change when the gain is varied. The circuit in Figure 5 trims the two components separately and minimizes the gain change problem. Adjust R_2 at minimum gain and then adjust R_1 at maximum gain.

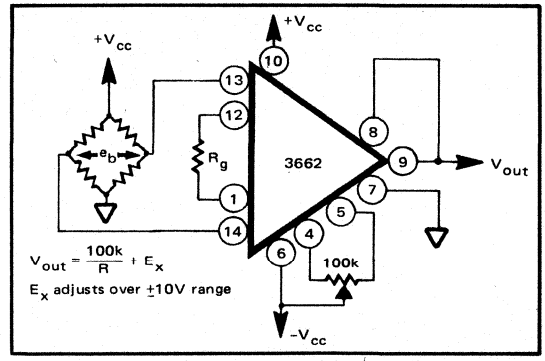


FIGURE 6. Output Biasing.

When it is desired to bias the output over a large range (such as chart recorder bias) the circuit in Figure 6 may be used.

3. ISOLATION AMPLIFIERS

WHAT IS AN ISOLATION AMPLIFIER?

An isolation amplifier is a device with the primary function of providing ohmic isolation (break the ohmic continuity of electrical signal) between the input signal/circuitry and the output of the amplifiers. It usually consists of an input operational amplifier or instrumentation amplifier followed by a unity-gain isolation stage. The sole purpose of the unity-gain isolation stage is to completely isolate the input from the output of the device. Ideally, the ohmic continuity of the input signal is broken (at the isolation barrier) yet accurate signal transfer without any attenuation is achieved across the unity-gain isolation stage. An important feature of an isolation amplifier is that it has a completely floating input which helps eliminate cumbersome connections to source ground in several applications.

Figure 1 shows a typical isolation amplifier application. The isolation-mode voltage V_{iso} is the voltage which exists across the isolation barrier. The contribution of the output referred error caused by V_{iso} is V_{iso}/IMRR, where IMRR is the Isolation Mode Rejection Ratio. V_d is the differential input signal and V_{cm} is the common-mode voltage. The "Leakage Current" is the current which flows across the isolation barrier with some specified isolation voltage applied between the input and the output.

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Glossary of Terms and Definitions 3-5
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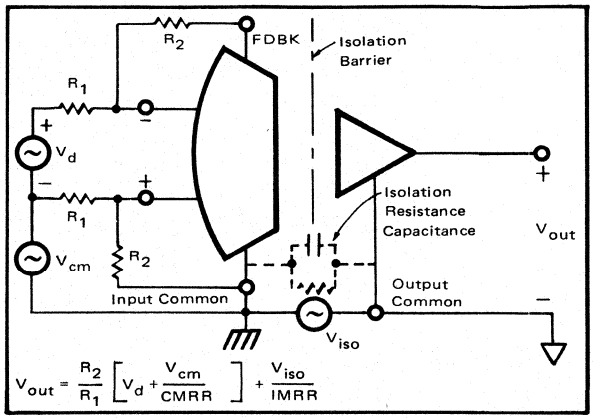


FIGURE 1. Typical Isolation Amplifier Application.

CHARACTERISTICS OF ISOLATION AMPLIFIERS

The following is a discussion of some of the characteristics and terms unique to isolation amplifiers.

Common-mode Voltage and Isolation Voltage - Some manufacturers (other than Burr-Brown) treat common-mode voltage and isolation voltage synonymously in describing the use and/or specifications of isolation amplifiers. It is important to understand the significance of these terms and the difference between them.

When the input common is grounded, the input signal V_d (see Figure 1) can be floated by the amount V_{cm} above the input ground. V_{cm} is the common-mode voltage (CMV) and is generally ±10V, limited by the CMV rating of the input stage amplifier. In applications involving higher system common-mode voltages, input common terminal is not grounded and the common-mode voltages are referenced across the isolation barrier to the output common terminal.

The isolation voltage V_{iso} as shown in Figure 1 is the potential difference between the input common and the output common terminals. The isolation voltage rating describes the amount of voltage that the isolation barrier can withstand without breakdown. This feature of the isolation amplifier allows two distinct ground connections to be made when necessary. It allows the isolation amplifier to be used in applications involving very-high common-mode voltages and in applications of breaking ground loops.

Many applications involve a large "system common-mode voltage." In such applications, the isolation amplifier's input common terminal is not connected to any ground but the output common terminal is connected to the system ground. In such a case, the term V_{cm} shown in Figure 1 becomes negligible and V_{iso} determines the safe limit for the system common-mode voltage. In this manner, the isolation amplifier can accommodate common-mode voltages of 2000V or more.

Common-mode Rejection and Isolation-mode Rejection - Isolation-mode rejection (IMR) is another term which some other manufacturers refer to as common-mode rejection (CMR). The above discussion on the common-mode voltage and isolation voltage helps recognize the difference between the CMR and the IMR. The CMR is the measure of the input stage amplifiers ability to reject common-mode input signals (referencing signals to the input common only) while amplifying only the differential input. The IMR is the measure of isolation amplifier's ability to reject common-mode input signals (common-mode with reference to the output common) while transmitting the signals across the isolation barrier. The isolation-mode rejection ratio (IMRR) is defined

by the equation shown in Figure 1. Thus, understanding the IMR capability of isolation amplifiers allows their meaningful use in applications requiring very high common-mode rejection ratios such as 100dB to 140dB.

Isolation Voltage Ratings, Test Voltage - It is important to understand the significance of the continuous derated isolation voltage specification and its relationship to the actual test voltage applied to the unit. Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration) it is generally accepted practice to perform a production test at a higher voltage (higher than the continuous rating) for some shorter length of time.

The important consideration is then "what is the relationship between actual test conditions and the continous derated minimum specification?" There are several rules of thumb used throughout the industry to establish this relationship. Burr-Brown has chosen a very conservation one: V_{test} = (2 x $V_{continuous\ rating}$) + 1000V. This relationship is appropriate for conditions where the system transient voltages are not well defined.* Where the real voltages are well defined or where the isolation voltage is not continuous the user may chose to use a less conservative derating to establish a specification from the test voltage.

APPLICATIONS OF ISOLATION AMPLIFIERS

When one or more of the following conditions/requirements are present in an application, an isolation amplifier would generally be the right choice as a signal conditioning device:

- When ohmic isolation between the signal source and the output is a requirement (isolation impedance between the input and the output > 10MΩ).
- When excellent common-mode noise and voltage rejection is a requirement (CMR > 100dB).
- When it is necessary to process signals in the presence of, or riding on, high common-mode voltages (CMV ⩾ 10V).

In general, most applications can be broadly categorized into the following four types:

- Amplifying and measuring low level signals in the presence of high common-mode voltages.
- Breaking ground loops and/or eliminating source ground connections. The isolation amplifier provides full floating input, eliminating the need for connections to source ground, and thus allows two-wire hook-up to the signal sources.
- Providing an interface between patient monitoring equipment and the transducer/devices which may be in physical contact with the patients. Such applications require high isolation voltage levels and very-low leakage currents.
- Providing isolation protection to electronic instruments/equipment. Large common-mode voltages occasionally cause hazardous electronic faults. Low leakage currents and high isolation voltage capability of isolation amplifiers help protect instruments against damage caused by such faults.

Isolation amplifier performance requirements vary signficantly, depending on the type of requirement. In applications where bandwidth and speed of response are more important than gain accuracy and linearity, the optically-coupled amplifiers will be the best choice. For applications where gain accuracy and linearity are key parameters, Burr-Brown's family of transformer-coupled amplifiers are the suitable choice.

*Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS I-109 and ICS I-111.

SELECTION GUIDE
Isolation Amplifiers

Description	Model	Input Voltage Common Mode (V)	Input Voltage Differential (V)	Input Impedance Common Mode (Ω)	Input Impedance Differential (Ω)	Isolation Voltage Continuous (V)peak	Isolation Voltage Pulse/Test (V)peak	Isolation Mode Rejection, min DC (dB)	Isolation Mode Rejection, min 60Hz (dB)	Leakage Current at Test Voltage (μA)	Gain Nonlinearity max. (%)	Gain Nonlinearity typ. (%)	±3dB Freq. kHz	External Isolation Power Required	Package		Page
TRANSFORMER COUPLED																	
Low Drift[1]	3450	±10	±15	5×10^9	10^7	±500	±2000	160	120	1	±0.01	±0.003	1.5	No	Module		3-6
Low Bias	3451	±10	±15	10^{11}	10^{11}	±500	±2000	160	120	1	±0.05	±0.01	2.5	No	Module		3-6
FET	3452	±10	±15	10^{11}	10^{11}	±2000	±5000	160	120	1	±0.05	±0.01	2.5	No[2]	Module		3-6
	3455	±10	±15	10^{11}	10^{11}	[3]	[3]	160	120	[3]	±0.05	±0.01	2.5	No[2]	Module		3-6
True 3-wire	3456A	±10	±15	5×10^9	10^7	±2000	±5000	160	130	25	±0.01	±0.02	2.5	No	Module		3-13
Inst. Amp	3456B	±10	±15	5×10^9	10^7	±2000	±5000	160	130	25	±0.01	±0.02	2.5	No	Module		3-13
OPTICALLY COUPLED																	
Balanced	3650HG	±10	±15	10^9	25[4]	±2000	±5000	140	120	.25[5]	±0.02	±0.05	15	Yes[6]	DIP		3-19
Current	3650JG	±10	±15	10^9	25[4]	±2000	±5000	140	120	.25[5]	±0.02	±0.05	15	Yes[6]	DIP		3-19
Input	3650KG	±10	±15	10^9	25[4]	±2000	±5000	140	120	.25[5]	±0.02	±0.05	15	Yes[6]	DIP		3-19
Balanced	3652HG	±10	[7]	10^{11}	10^{11}	±2000	±5000	140	120	.25[5]	±0.05	±0.1	15	Yes[6]	DIP		3-19
FET Input	3652JG	±10	[7]	10^{11}	10^{11}	±2000	±5000	140	120	.25[5]	±0.05	±0.1	15	Yes[6]	DIP		3-19

1) Biplar. 2) ±15V at ±15mA isolated power available to power external circuitry. 3) Isolation voltage tested at 2500V, rms, 60Hz; leakage current tested for 2μA max, at 240V, rms, 60Hz. 4) Model 3650 is a current input device; to reduce input errors, very low input impedance is desirable. 5) At 240V/60Hz. 6) Models 700 or 710 isolated DC/DC converters may be used to provide isolated power. 7) See Product Data Sheet.

GLOSSARY OF TERMS & DEFINITIONS
Isolation Amplifiers

ISOLATION AMPLIFIER
A device which provides ohmic isolation (breaks ohmic continuity of an electric signal) between the input and the output of the device. Method of coupling may be thermal, magnetic, optical, or any means other than direct ohmic coupling. Such a device allows the input circuit to be referenced separately and independent of the output circuitry.

ISOLATION BARRIER
A barrier or region between the input and the output stage of an isolation amplifier, where signal transfer is achieved between the input and the output.

ISOLATION IMPEDANCE
The effective impedance between the input common terminal and the output common terminal. It is the impedance of the isolation barrier. (It is usually specified as a typical parameter. Leakage current is related to isolation impedance and is usually specified with a maximum limit.)

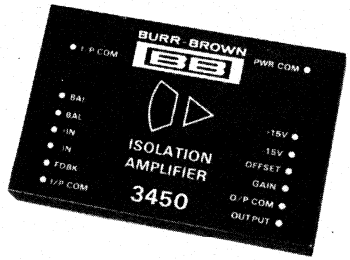
ISOLATION-MODE REJECTION (IMR)
The IMR is the measure of an isolation amplifier's ability to reject common-mode input signals (common-mode with reference to the output common). While transmitting the differential signals across the isolation barrier.

ISOLATION VOLTAGE
The potential difference between the input stage common and output stage common terminals of an isolation amplifier.

ISOLATION VOLTAGE RATING
The amount of voltage that can be impressed between the input common and the output common terminals (across the isolation barrier) without resulting in breakdown.

LEAKAGE CURRENT
The current that flows between the input common terminal and the output common terminal (across the isolation barrier) with a specified voltage applied across it. (It is usually 100% tested and specified with a maximum limit.)

BURR-BROWN



3450
3451
3452
3455

Precision Linear ISOLATION AMPLIFIERS

FEATURES

- 2000V ISOLATION (3452)
- 160dB ISOLATION-MODE REJECTION
- DIFFERENTIAL INPUT
- 0.005% GUARANTEED GAIN LINEARITY (3450)
- 1μV/°C INPUT VOLTAGE DRIFT (3450)
- 20pA INPUT BIAS CURRENT (3452)
- PRECISION WIRE-WOUND RESISTORS FOR LONG TERM STABILITY
- LOW INTERFERENCE PICKUP-PW. MODULATION

DESCRIPTION

The Models 3450, 3451 and 3452 are operational amplifiers with the unique feature of having the output completely isolated from the input. This is accomplished by a high accuracy modulation/demodulation stage which isolates the input from the output by $10^{12}\Omega$ in parallel with 12 pF of coupling capacitance and provides gain linearity and stability far superior to that offered by ordinary isolation amplifiers.

These devices differ from other isolation amplifiers in several respects. They are true differential input operational amplifiers where as other commercially available isolation amplifiers are simple unity-gain isolators or are capable of a few fixed gains. Thus they can be connected in all of the common op amp feedback circuits such as summing, inverting, differentiating, etc.

The 3452 differs from the 3450 and 3451 in that it has higher isolation voltage (2000 volts vs 500 volts) and has isolated ± 15 Vdc power available at the input.

The 3450 and 3451 differ from each other primarily in their input stage characteristics. The 3450 has a low drift (1 μV/°C) bipolar transistor input stage while the 3451 has a low bias current (25 pA) FET transistor input stage. The 3455 is identical to the 3452 except for additional isolation specifications more well suited for medical applications.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-305G Printed in U.S.A. July, 1978

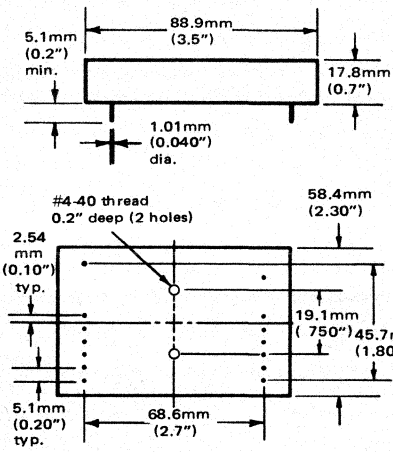
SPECIFICATIONS

Typical at 25°C and ±15 Vdc unless otherwise noted.

ELECTRICAL

MODEL		3450	3451	3452/3455[6]
INPUT STAGE SPECIFICATIONS [1]				
Open Loop Gain	dB, Min.	94	88	94
Input Offset Voltage @ 25°C[4]	mV, Max.	±0.55	±20	±0.30
vs. Temp.	µV/°C Max.	±1.0	±50	±5.0
vs. Supply	µV/V	±50	±50	±25
vs. Time	µV/mo	±10	±100	
Input Bias Current @ 25°C	Max.	±50 nA	−25 pA	−20 pA
vs Temp.	Max.	±0.5 nA/°C	doubles/10°C	
vs. Supply		±0.2 nA/V	±1 pA/V	
Input Offset Current @ 25°C		±30 nA Max.	±2 pA	
vs. Temp.	Max.	±0.3 nA/°C	doubles/10°C	
vs. Supply		±0.1 nA/V	±0.5 pA/V	
Input Impedance				
Differential		$10^7\Omega$	$10^{11}\Omega$	
Common Mode (2)		$5\times10^9\Omega \parallel 10pF$	$10^{11}\Omega \parallel 10pF$	
Input Noise				
Voltage, .01 Hz - 10 Hz	µV, p-p	0.8	2	4
10 Hz - 1 kHz	µV rms	1.2	3	2
Current, .01 Hz - 10 Hz	pA, p-p	30	0.3	0.3
10 Hz - 1 kHz	pA, rms	50	0.6	0.6
Input Voltage Range				
Common Mode (2) (operating)	V, Min.		±10	
Differential (w/o damage)	V, Min.		±15	
Common Mode (2) Rejection	dB @ 10V	100	80	90
Isolated Power Available				
Voltage		—	—	$\pm15V\ ^{+0}_{-10\%}$
Current,	Max.	—	—	±10mA
Ripple @ 100 kHz		—	—	100 mV p-p
ISOLATION STAGE SPECIFICATIONS				
Gain (without trimming) (4)	1 V/V, ±Max	±0.1%	±0.5 %	
vs. Temp.	ppM/°C Max	±10	±50	
Nonlinearity[7] @ ±10V	% Max/typ	±.005/±0.0015	±0.025/±.005	±0.025/±.005
Frequency Response, -3 dB (See Fig.9)		1.5 kHz	2.5 kHz	
Settling Time				
to 0.01%			5 msec	
to 0.1%			1 msec	
Isolation Impedance[3]			$10^{12}\Omega \parallel 16$ pf	
Isolation Leakage Current at 240V/60Hz			2.5µA max[6]	
Isolation Mode[3] Rejection				
DC			160 dB Min.	
60Hz			120 dB Min.	
Isolation[3] Voltage				
Rated, continuous, (min.)		±500 V Peak		±2000Vpk
Test voltage[5]		±2000V Peak		±5000Vpk[6]
Output Voltage			±10 V Min.	
Output Current			±5 mA Min.	
Output Impedance, DC			0.2 Ω	
Output Noise				
.01 Hz to 10 Hz			7 µV p-p	
10 Hz to 1 kHz			25 µV rms	
Output Offset Voltage @ 25°C[4]	mV, Max.	±2	±5	±5
vs. Temp.			±100µV/°C Max.	
vs. Supply			±500µV/V	
vs. Time			±100µV/Mo	
Input Power Requirements				
Voltage			±14 to ±16 VDC	
Current, quiescent			+30/-5 mA Max.	
, full load, max.		+35/-10mA		+55/-10mA[8]
TEMPERATURE RANGE				
Specification			-25°C to +85°C	
Storage			-55°C to +125°C	
Operating			-25°C to +85°C	

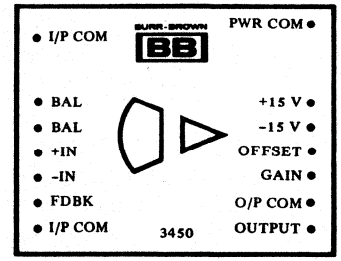
MECHANICAL



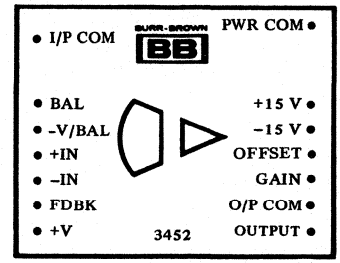
MATERIAL - Black Plastic
WEIGHT - 100g (3.5 oz)
PINS - Pin material and plating composition meet method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]
Mating Connector - 4400MC,

PIN CONNECTIONS

(TOP VIEW)



MODELS 3450 & 3451



MODEL 3452 & 3455

1) For 3450 and 3451 current drawn from FDBK pin must be ≤ 5mA. For 3452 the sum of the current drawn from FDBK pin and either "-V/Bal" or "+V" pins (i.e., + or - isolated current) must be ≤ 11mA.
2) Common-mode parameters are measured at the +IN and -IN pins with respect to the I/P COM pin.
3) Isolation mode parameters are measured at the I/P COM pin with respect to the PWR COM pin and O/P COM pin.
4) Errors may be trimmed to zero.
5) All units 100% tested for 1µA max leakage current at test voltage.
6) The 3455 is identical to the 3452 except for two additional specifications. Each unit is tested to withstand a 2500V rms, 60 Hz sinewave isolation voltage (Ref. Dielectric Withstand Voltage, paragraph 31.11 of UL 544). Each unit is specified at a maximum leakage current of 2µA with 240V rms, 60 Hz isolation voltage (Ref. Leakage Current, paragraph 27.5 of UL 544).
7) Nonlinearity is specified to be the peak deviation from a best straightline expressed as a percent of peak-to-peak full scale output.
8) Includes fully loaded input power.

CIRCUIT DESCRIPTION

The 3450,3451 and 3452 operate on the same principle, basically that of an operational amplifier followed by a high accuracy isolation stage (Figure 1a). The high accuracy of the isolation stage is achieved by use of a proprietary feedback technique in combination with high-stability components.

Isolated DC power for the input amplifier is provided by an internal DC-DC converter which derives its power from the external +15 Vdc supply.

Although a DC-DC converter and modulation techniques are used, the output noise is typically less than 1 mV (peak) as a result of careful design, internal filtering, and a shielded package. The frequency of this noise is approximately 100 kHz which makes it insignificant for many applications. Pulse width modulation minimizes pickup from adjacent units. The symbol shown in Figure 1b is used to represent the complete isolated operational amplifier.

The O/P COM pin must be connected to the PWR COM pin. Figure 10a shows the power supply connections and the optional offset and gain trims.

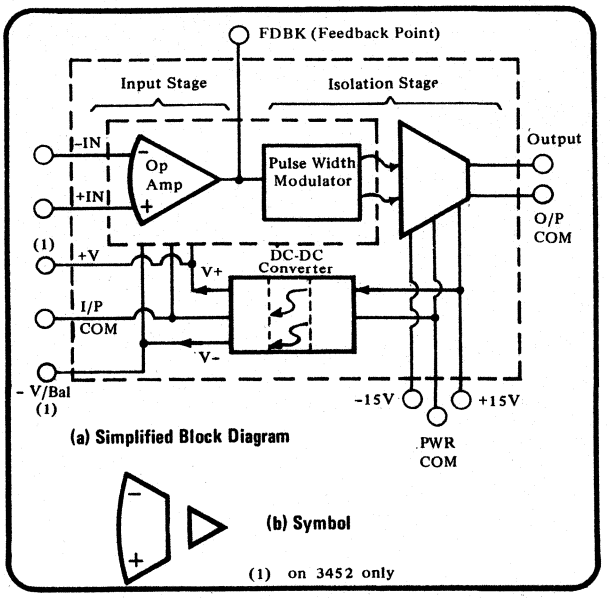


FIGURE 1. Block Diagram and Symbol

APPLICATIONS

The isolation amplifiers may be used in the same manner as any operational amplifier except that the feedback signal is taken from the FDBK pin rather than from the output pin. No connection is required or would normally be made from input common (I/P COM) to either the power common (PWR COM) or output signal ground pins. Some typical circuit applications are shown in the following.

NONINVERTING CIRCUITS

One of the most useful applications of these amplifiers is impedance buffering and pre-amplification of low-level signals. Such signals may be "riding" on several hundred volts of common mode potential or they may simply have a significant amount of common mode noise (power line "pickup," etc).

Figure 2 illustrates the correct signal and feedback connections for such noninverting circuits.

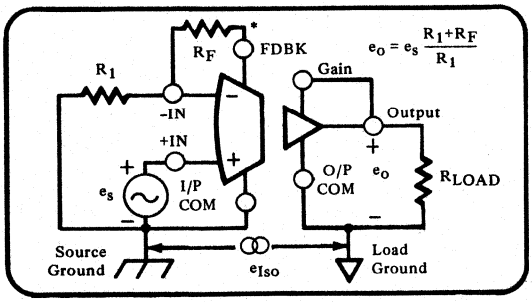


FIGURE 2. Noninverting Amplifier Circuit.

*See note (1) under Electrical Specifications.

For signal sources of millivolt levels and low internal impedance, the 3450 will usually be the best choice. Signal sources of this type include thermocouples, thermistors, etc. The 3451 will generally be the best choice for signal sources having large values of internal impedance. The pH cell is an example of this type of signal source.

INVERTING CIRCUITS

The isolation amplifiers can be used for a variety of inverting circuit applications. Figure 3 illustrates the proper circuit connections for summing a number of signals which are all at the same common mode level. An example of the use of such an amplifier is the computation of a weighted average of several temperature inputs.

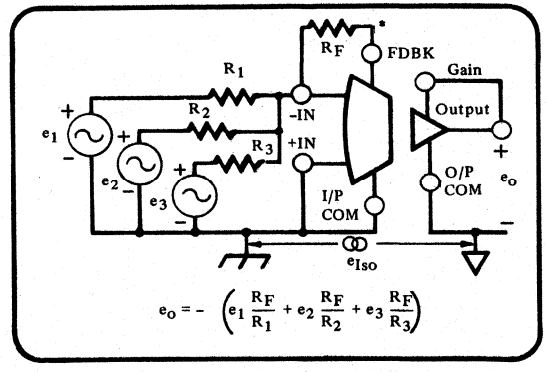


FIGURE 3. Summing Amplifier (or Weighted Averager).

DIFFERENTIAL INPUT CIRCUIT

The isolated operational amplifier can be operated in a fully differential mode as shown in Figure 4. The input impedance of the differential amplifier circuit is $2R_1$ and may cause undesirable loading of the signal source unless R_1 is much greater than the impedance of the signal sources.

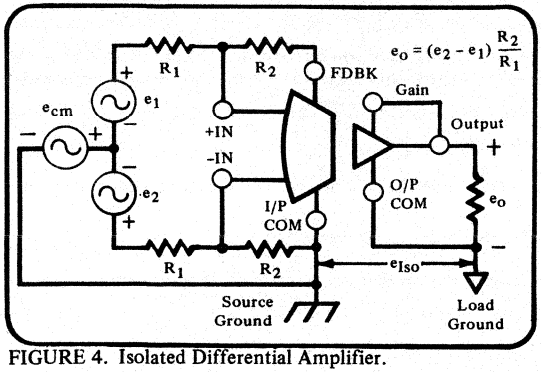


FIGURE 4. Isolated Differential Amplifier.

BRIDGE AMPLIFIER

The circuit in Figure 6 illustrates a method of amplifying a signal from a balanced bridge which cannot be conveniently used with a nonisolated amplifier. The circuit shown provides a high input impedance so that the bridge is not loaded. The common mode rejection of the bridge excitation voltage is not degraded by the external gain setting resistors as it would be with a difference amplifier. The gain can be changed conveniently by adjusting a single resistor (R_2). Also, the whole bridge circuit may be floated with respect to the output by a voltage equal to the isolation mode voltage specification without creating troublesome ground loop current.

ISOLATION AMPLIFIERS USED IN MEDICAL APPLICATIONS

When isolation amplifiers are used in patient monitoring medical application the considerations of 1) patient safety and 2) protection of the amplifier against defibrillator voltages require the use of additional circuitry.

The input resistors must be kept large in order to limit the leakage current in the event of a component failure in the input stage of the amplifier. The 1.2meg. ohm resistors will limit the current to 12.5μA (Figure 7).

The amplifier must be protected in two areas against possible damage from defibrillator over voltages. Diodes D_1 through D_4 protect the input stage from excessive voltages and currents. The gas filled surge voltage protection (SVP in Figure 7) will protect the isolation barrier of the amplifier from breakdown. A Siemens part number B2-B470 will limit the voltage across the isolation barrier to 470V and has high isolation resistance and low leakage capacitance characteristics.

CURRENT AMPLIFIER

As with nonisolated operational amplifiers, the isolation amplifiers can be used to convert current source or convert current signals to output voltage. However, with these amplifiers the input signal may have a large voltage associated with it which can be completely isolated from output ground. The circuit of Figure 5 illustrates this technique.

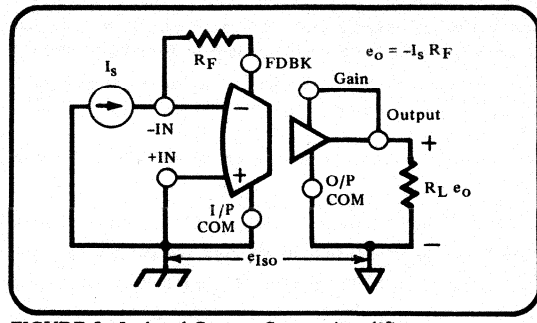


FIGURE 5. Isolated Current Source Amplifier.

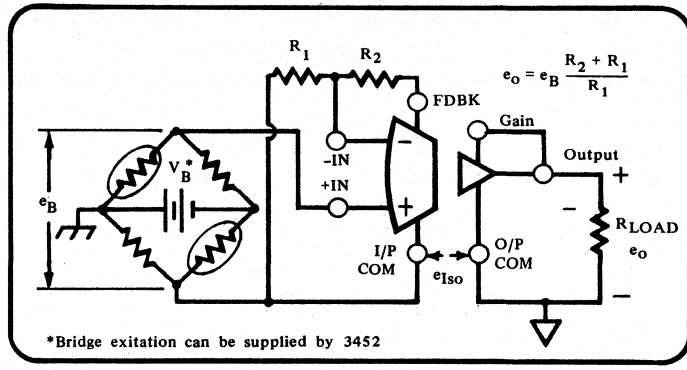


FIGURE 6. Bridge Circuit with Floating Input.

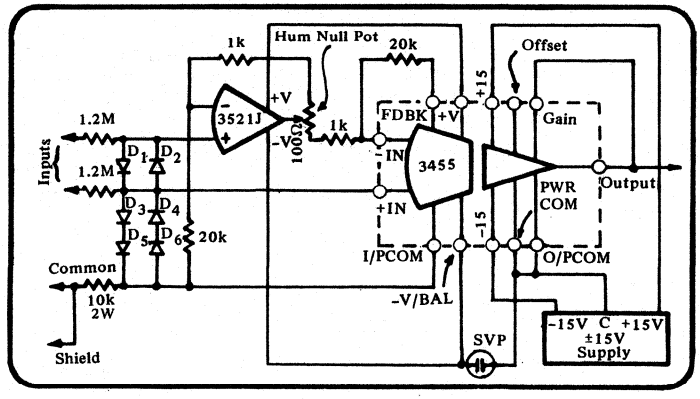


FIGURE 7. High Performance ECG Amplifier Gain = 20V/V

PERFORMANCE

OFFSET VOLTAGE and NOISE

The total error at the output of the isolation amplifiers may be computed by treating it as two amplifier stages in cascade. One stage (the input stage) has variable gain (G_1) and the other stage (the isolation stage) has a fixed gain of 1 V/V.

When this concept is applied to the circuit in Figure 2 as a typical example we see that the total DC offset voltage error at the isolation amplifier output is given by

$$V_{OS} = V_{OS1} \times G_1 + I_B R_1 \times G_1 + V_{OS2}$$

where V_{OS} = total offset voltage, referred to output (RTO)
V_{OS1} = offset voltage of input stage
V_{OS2} = offset voltage of isolation stage
I_B = input bias current
R_1 = input impedance
G_1 = gain of input stage, $\frac{R_1 + R_F}{R_1}$

A similiar expression may be used to compute the total offset voltage drift, RTO.

Total output noise may be calculated in much the same way.

$$E_N \text{ (rms)} = \sqrt{(E_{N1} \times G_1)^2 + (I_N R_1 \times G_1)^2 + (E_{N2})^2}$$

where E_N (rms) = total noise, RTO
E_{N1} = rms voltage noise of input stage
I_N = rms current noise of input stage
E_{N2} = rms voltage noise of output stage

The rms noise specifications shown in the Electrical Specifications are for a frequency band of 10Hz - 1kHz. If the bandwidth is reduced by filtering the noise will be decreased.

FREQUENCY RESPONSE

Because the isolation amplifiers are two stage amplifiers, the frequency response of both stages in cascade must be considered in determining the overall response. The curves of Figure 9 show the frequency response of each stage. Note that the frequency response of the input stage is shown under open loop conditions: As with conventional operational amplifiers, the actual closed loop response depends on the feedback network used.

GAIN ACCURACY and STABILITY

The overall gain accuracy of the isolation amplifier is determined by the gain accuracies of its two stages. The input stage accuracy is determined by the open loop gain and the feedback network (i.e. the loop gain) as with a conventional operational amplifier. The untrimmed accuracy of the isolation stage is given in the Electrical Specifications. Since these can be trimmed to zero the fundamental limitation on gain accuracy is the linearity and gain drift. When these limitations are considered the isolation amplifiers are quite capable of achieving gain accuracies of 0.01% and 0.1%. The achievement of such accuracies, as always, requires the use of high quality feedback components (such as wire-wound resistors) and careful calibration techniques (see Calibration Adjustments).

COMMON MODE REJECTION and ISOLATION MODE REJECTION

The use of the common mode rejection (CMR) and isolation mode rejection (IMR) specifications to calculate their respective error contribution is illustrated in Figure 8.

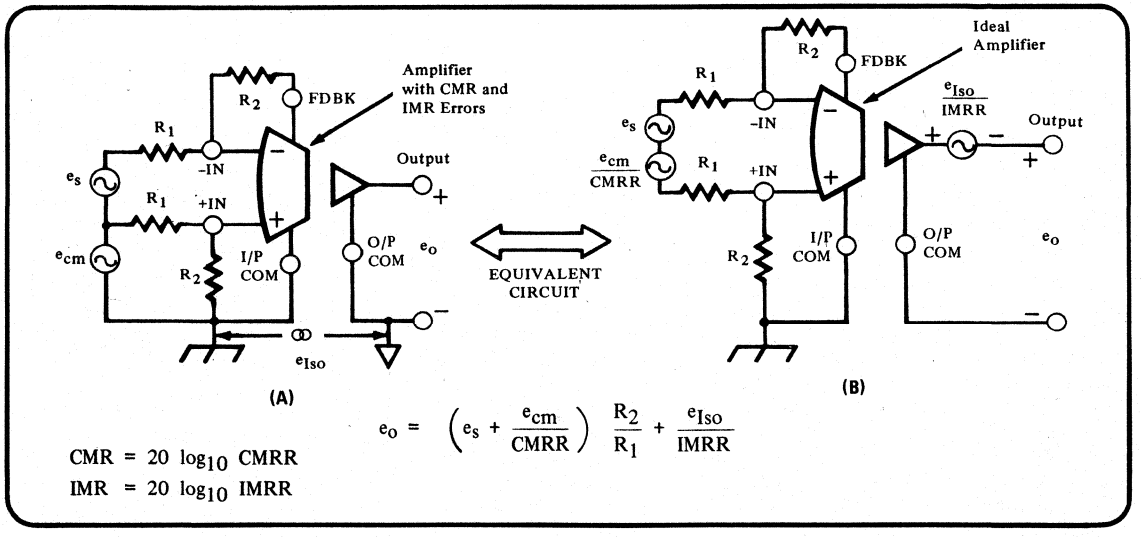


FIGURE 8. Common Mode and Isolation Mode Voltage Errors.

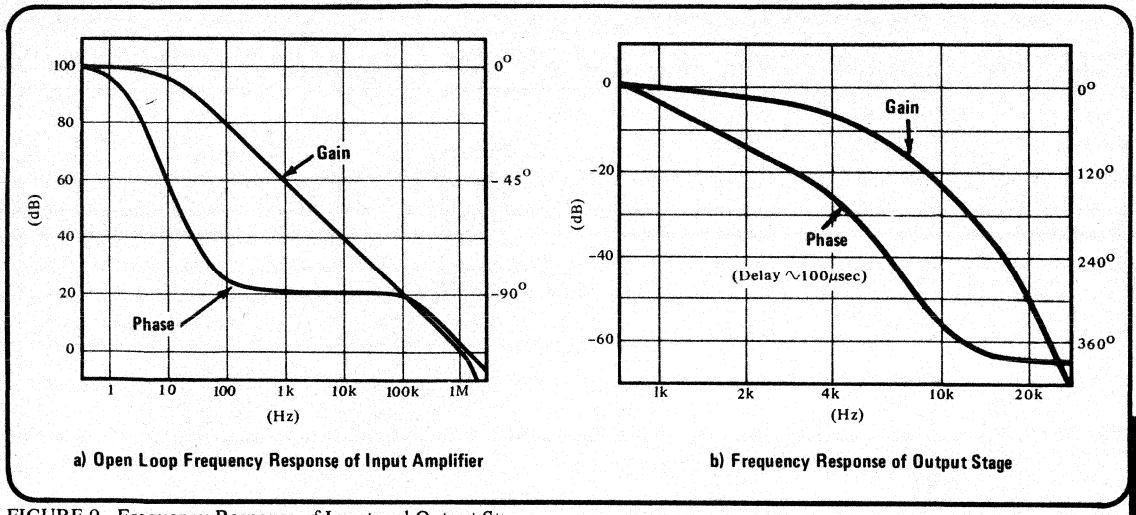


FIGURE 9. Frequency Response of Input and Output Stages.

INSTALLATION and OPERATING INSTRUCTIONS

MOUNTING

The isolation amplifiers are plastic cased modules suitable for soldering directly on to a printed circuit board. Alternatively they may be plugged into the 4400 MC mating connector which may be mounted on a panel or chassis.

POWER SUPPLY REQUIREMENTS

The isolation amplifiers have no unusual power supply requirements. A standard low-cost power supply such as the Burr-Brown 551 is recommended. The necessary isolated power for the input stage of the amplifier is derived internally by a DC-DC Converter operating from the externally applied +15VDC power.

CALIBRATION ADJUSTMENTS

Gain of the isolation amplifiers is determined primarily by the operational amplifier input stage. This allows a wide range of possible gains with the accuracy determined primarily by the feedback networks and the open loop gain of the operational amplifiers. $R_F \geqslant 10$ k is recommended for best linearity. The gain of the isolation stage is nominally unity but may be trimmed over a limited range to allow easy calibration.

Offset voltages of both input and output stages are adjustable by use of external components.

Figure 10 illustrates a typical amplifier circuit where gain and offset voltages are adjusted. Proper calibration procedure for this circuit would normally be as follows:

ISOLATION STAGE OFFSET VOLTAGE NULL

Set input signal to zero (connect +IN to I/P Com) connect I/P Com to O/P Com and measure the voltage between the FDBK and OUTPUT pins with a floating DVM. Null this voltage by adjusting R4. Remove the connection between I/P Com and O/P Com.

INPUT STAGE OFFSET VOLTAGE NULL

With the input signal set to zero, adjust R5 such that the voltage between the FDBK and I/P Com pins is zero. (This is best done at a high gain value i.e. $\frac{R_G + R_F}{R_G} \simeq 1000$).

OVERALL GAIN ACCURACY

With R_F and R_G at the proper values to produce the desired gain $G = \frac{R_G + R_F}{R_G}$, apply a known calibration voltage V_R as the input signal. Adjust R_3 for the desired output $V_O = V_R \times G$.

If it is unnecessary to adjust offset voltage of the output stage, R_1 and R_4 may be omitted. If no adjustment of input stage offset voltage is desired, omit R_5 and R_6. If the specified gain accuracy (see spec table) is adequate without further adjustment, both R_2 and R_3 may be omitted. The OUTPUT pin must then be connected to the GAIN pin for an output stage gain of unity. Omit R_7 if R_1 through R_4 omitted.

For all applications other than unity gain noninverting, R_2 is unnecessary and only R_3 is needed to trim the gain. However, it is then necessary to set the first stage gain slightly below the desired overall value and then use R_3 for the gain calibration.

For fixed gain applications it may be unnecessary to null offset voltage for both input and output stages. The offset voltage of the output stage, for instance, may be used to compensate for the input stage offset, thus giving an overall null. However, if gain is to be varied over a wide range it will usually be necessary to null both offset voltages.

Appropriate safety precautions should be taken when adjusting input stage offset voltage or gain. These points will be "floating" at the isolation mode voltage and appropriate precautions must be taken if this is a high voltage. In particular, any adjustment potentiometers used for input stage adjustment should have insulated shafts with voltage ratings in excess of any expected common mode potential.

The output stage can be adapted to drive capacitive load of up to 10,000 pF without sacrificing DC gain accuracy. Add R_8 = 100Ω as shown in Figure 10b; otherwise, R_8 = 0Ω.

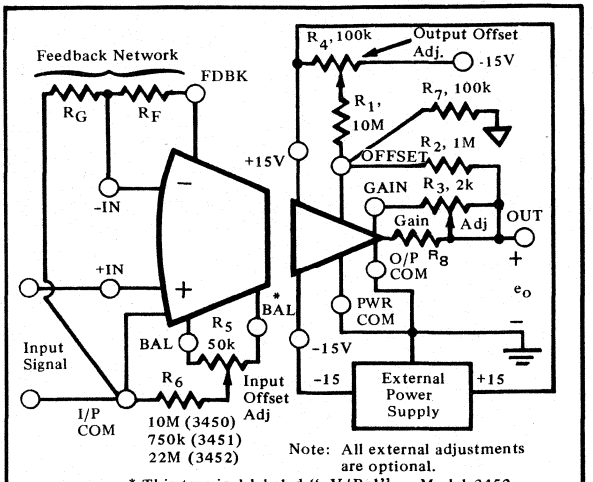


FIGURE 10a. External Connections for 3450, 3451 and 3452

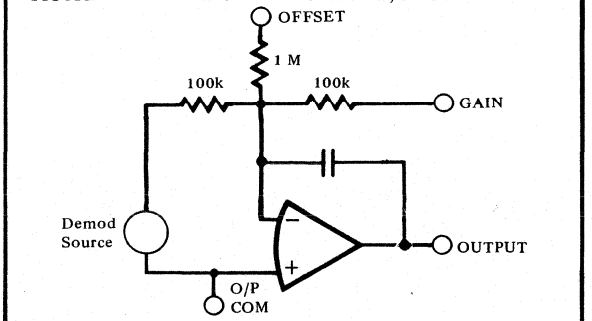


FIGURE 10b. Equivalent Circuit of O/P Stage.

WIRING SHIELDING and ISOLATION MODE REJECTION

The capacitive coupling from input common (I/P COM) to output common (O/P COM) for the isolation amplifiers is extremely low. This is an essential element in achieving the isolation mode rejection specifications. Therefore it is essential that care be used in wiring and printed circuit card layout to minimize stray capacitance between input and output circuits.

Proper shielding of input leads is also essential in preserving isolation mode rejection. When shielded cable is used the shield should be connected to the common mode potential at the signal-source.

Isolation mode rejection at high frequencies will be degraded by resistance in series between the signal source and the I/P COM pin (e.g. wire resistance). Figure11 illustrates the mechanism by which such degradation occurs. The isolation mode voltage "divides" across R_W and C_C creating an isolation mode error voltage Δe_{Iso} which appears as an unwanted differential input voltage adding to e_s. Note that this error occurs even if R_N and R_W are equal because the stray capacitance C_C exists only from the I/P COM pin to O/P COM. If this degradation of the isolation mode rejection becomes significant (for R_W = 1 kΩ and f = 60 Hz, the CMR is still in excess of 97 dB) a capacitance from the +IN pin to O/P COM will compensate the effect. A capacitor used in this manner must withstand whatever isolation mode potential exists.

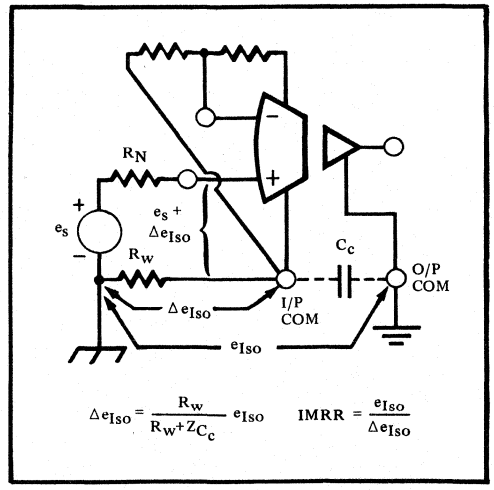
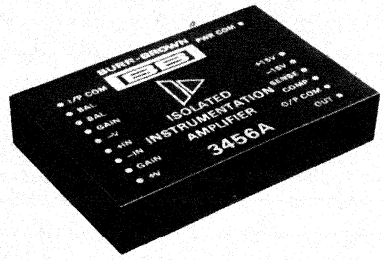


FIGURE 11. Degradation of Isolation Mode Rejection due to Wiring Impedance and Coupling Capacitance.

BURR-BROWN



3456

ISOLATED INSTRUMENTATION AMPLIFIER

FEATURES

- TRUE 3-WIRE INSTRUMENTATION AMPLIFIER INPUT
- TRUE INSTRUMENTATION GRADE ISOLATION AMPLIFIER
- 1μV/°C INPUT VOLTAGE DRIFT
- ADJUSTABLE GAIN, 1 to 1000
- LOW NONLINEARITY, 0.02% max
- ISOLATION VOLTAGE, 2000V PEAK RATED CONTINUOUS
- 160dB ISOLATION-MODE REJECTION
- ±20mA, VOLTAGE OR CURRENT PROGRAMMABLE OUTPUT
- 2.5kHz, FREQUENCY RESPONSE
- LOW INTERFERENCE PICKUP-PW. MODULATION
- FULLY SELF-CONTAINED

APPLICATIONS

- ISOLATED THERMOCOUPLE & RTD SENSING
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT AND INSTRUMENTS
- HIGH VOLTAGE INSTRUMENTATION AMPLIFIER
- CURRENT SHUNT MEASUREMENTS
- GROUND-LOOP ELIMINATION
- BIOMEDICAL PATIENT MONITORING

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PDS-377 Printed in U.S.A. July, 1978

DESCRIPTION

The Models 3456A and 3456B are high performance instrumentation amplifiers which have their outputs completely isolated from the input. The front end of the unit is a high performance, DC differential-input instrumentation amplifier stage, designed for data acquisition and instrumentation use. The low drift, low noise and high CMR make it possible to accurately amplify microvolt-level signals with gains of up to 1000. The input stage is followed by a high accuracy unity gain, pulse width modulation/demodulation isolation stage. This isolation stage isolates its input from the output by $10^{12}\Omega$|| 14 pF impedance. The 3456A and 3456B differ from other isolation amplifiers in several respects. They are true instrumentation amplifiers as opposed to differential input op amps or fixed gain isolators. They offer both, the single resistor programmable gain range as well as the true 3 wire instrumentation amplifier input.

THEORY OF OPERATION

Figure 1 shows block diagram of 3456. The true 3 wire instrumentation amplifier input section shown needs only one resistor to set the required gain level. It has high input impedance, high CMR and low bias current and allows the use of inverting, non-inverting and differential input configurations. The input offset adjustment shown is optional.

Isolated DC power for the input stage is provided by an internal DC/DC converter which derives its power from the external +15 VDC supply. The isolated power is also made available (on +V and -V pins) for external use.

The modulation/demodulation stage isolates the input from the output by $10^{12}\Omega$ in parallel with 14 pF of coupling capacitance. Pulse width modulation technique is used to minimize pickup from adjacent units. This technique combined with the use of wirewound and laser trimmed thin-film resistors provides high overall accuracy and excellent drift characteristics.

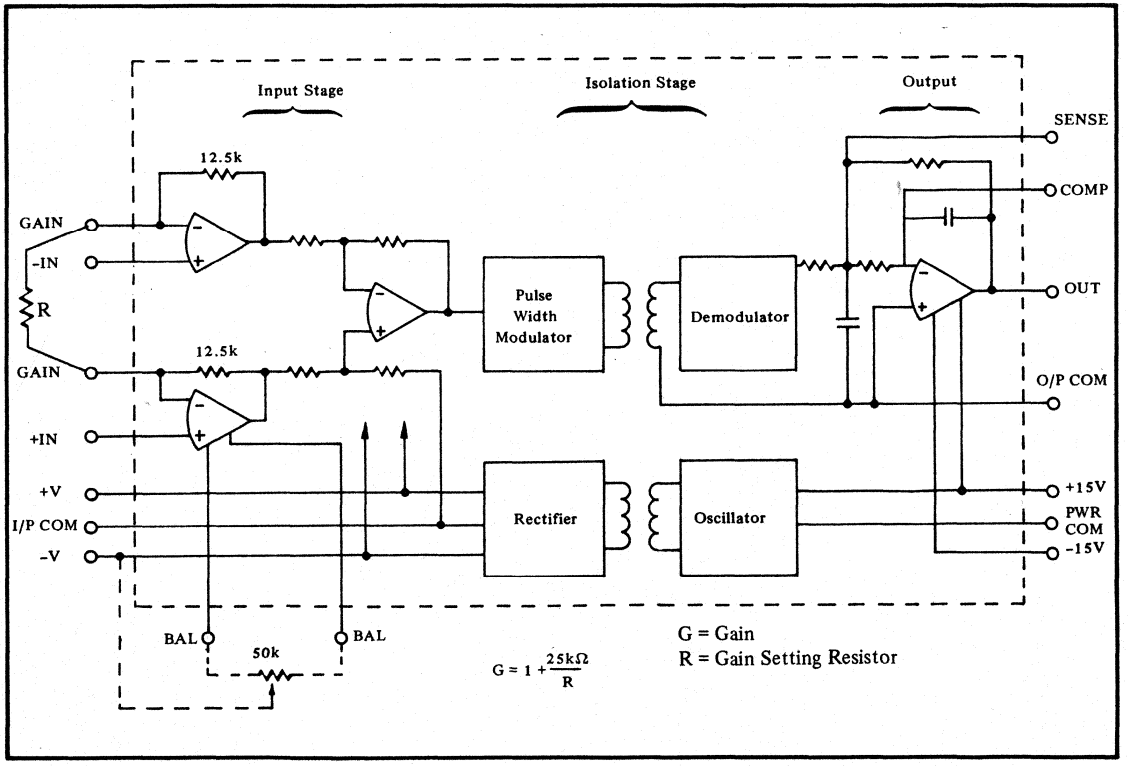


FIGURE 1. 3456 BLOCK DIAGRAM

SPECIFICATIONS

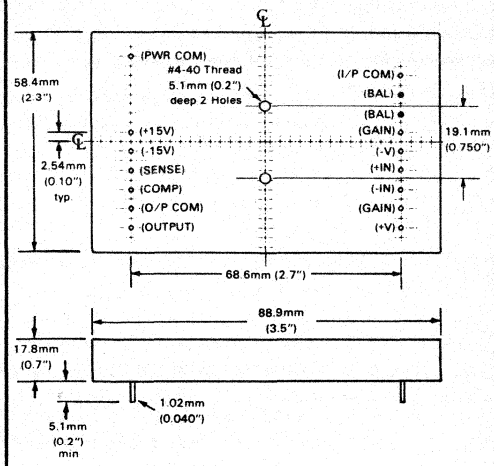
Typical at 25°C and ±15VDC supply voltage unless otherwise noted.

ELECTRICAL

MODEL	3456A	3456B
GAIN		
Gain Equation	$G = 1 + \frac{25k\Omega}{R}$	
Range of Gain	1 - 1000	
Gain Nonlinearity at G ≤ 100	±0.01% typ., ±0.02% max	
≤ 1000	±0.03% typ., ±0.08% max	
Gain Accuracy at G ≤ 100	±0.2% max	
G ≤ 1000	±0.5% typ.	
Gain vs Temperature at G ≤ 100	10 ppm/°C	
at G = 1000	50 ppm/°C	
INPUT		
Input Impedance - Differential	$10^7\Omega$ ‖ 3 pF	
Common-mode	$5 \times 10^9\Omega$ ‖ 3 pF	
Input Voltage Range[1]	±10V	
Absolute max	±Isolated Supply	
Common-mode Rejection, DC-100Hz		
at G = 1.5kΩ source unbal.	80dB, min	
at G = 100, 0Ω balanced source	110dB	
Input Bias Current, Initial	±50nA, max	
vs Temperature	0.3nA/°C typ, 0.6nA/°C, max	
vs Supply	±0.2nA/V	
Input Noise		
Voltage, 0.01Hz - 10 Hz	1.5μ p-p	
10Hz - 1.0kHz	1.4μV rms	
Current, 0.01Hz - 10Hz	200pA p-p	
10Hz - 1.0kHz	50pA rms	
ISOLATED POWER		
Voltage - No load	±15.3V, max	
Voltage - ±10mA	±13.5V, min	
Current	±10mA, max	
Ripple at 100kHz	100mV, p-p	
TOTAL OFFSET VOLTAGE		
Initial[2]	±(0.5 + 5/G)mV max	±(0.25 + 2/G)mV max
vs Temperature	±(2 + 150/G)μV/°C max	±(1 + 75/G)μV/°C max
vs Supply	±(30 + 500/G)μV/V	
vs Time	±(3 + 100/G)μV/mo	
ISOLATION		
Isolation Impedance[3]	$10^{12}\Omega$ ‖ 14 pF	
Isolation Mode Rejection, DC	160dB + I/P Gain (dB)	
,60Hz	130dB + I/P Gain (dB), min	
Isolation Voltage, Rated Continuous	±2000V Peak	
Test Voltage[4]	±5000V Peak	
FREQUENCY RESPONSE		
-3dB Response at G ≤ 400	2.5kHz	
-3dB Response for 400 ≤ G ≤ 1000	2.5kHz to 1kHz	
Setting Time to 0.01%	5msec	
to 0.1%	1msec	
OUTPUT		
Output Voltage	±10V at ±20mA, min	
Output Impedance, DC	0.04Ω	
Short Circuit Current, Duration	40mA, unlimited	
Output Noise, 0.01Hz - 10Hz	15μV p-p	
1Hz - 1kHz	25μV rms	
POWER SUPPLY		
Voltage	±14 to ±16VDC	
Current, Quiescent	+40/-8mA, max	
Full Load[5]	+85/-30mA, max	
TEMPERATURE RANGE		
Specification	-25°C to +85°C	
Operating	-25°C to +85°C	
Storage	-55°C to +125°C	

MECHANICAL

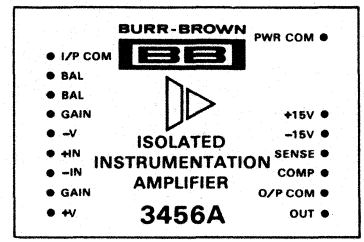
(BOTTOM VIEW)



MATERIAL: Black Plastic
WEIGHT: 100 grams (3.5 oz.)
PINS: Pin material and plating composition meet method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
MATING CONNECTOR: 4400MC

PIN CONNECTIONS

(TOP VIEW)



NOTES:
1. The ±10V input range is subject to the limitation that $|V_{common\ mode}| + |\text{Gain} \times V_{diff}/2| \leq 10V$.
2. Both the components (input and output) of the offset voltage may be trimmed to zero.
3. Isolation mode parameters are measured at the I/P COM pin with respect to the PWR COM pin.
4. All units are 100% tested for 25μA maximum leakage at test voltage.
5. Includes full isolated power supply.

VOLTAGE OUTPUT CONFIGURATION

The 3456, when connected as shown in Figure 2, will provide output signal capable of driving up to ±20mA load. Refer to the block diagram shown in Figure 2. Notice that the demodulated signal is referenced to the O/P COM pin. The O/P COM pin is connected to the output ground (PWR COM) for voltage output configuration as is shown in Figure 2. So with this configuration, the demodulated voltage signal is fully applied across the load impedance Z_L.

If roll-off at a lower frequency (lower than 2.5kHz) is desired, an optional compensation capacitor C_C may be connected as shown between the COMP pin and the OUT pin. See Figure 4 for the selection of C_C. The output offset controls shown in Figure 2 and Figure 3 are optional. They provide approximately ±15mV offset control at the output.

The SENSE and COMP pins are subject to electrostatic noise pick-up via stray capacitance. To minimize this noise pick-up these pins and connected circuits should be shielded. If these controls are not used, we recommend the unused pins be cut off flush to the 3456 surface. This would help minimize the degradation of Isolation Mode Rejection.

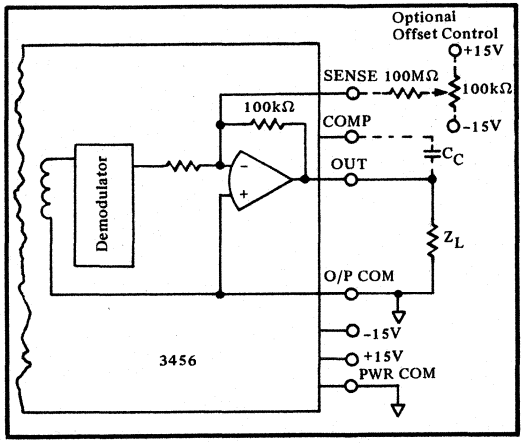


FIGURE 2. Voltage Output Configuration With Simplified Block Diagram.

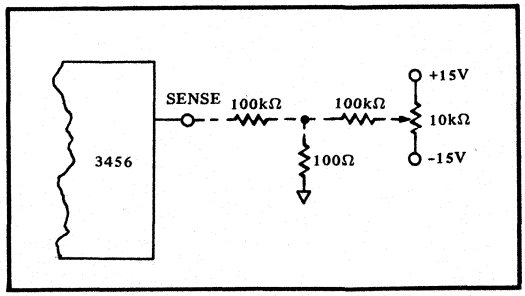


FIGURE 3. Alternate O/P Offset Control For Voltage Output Configuration.

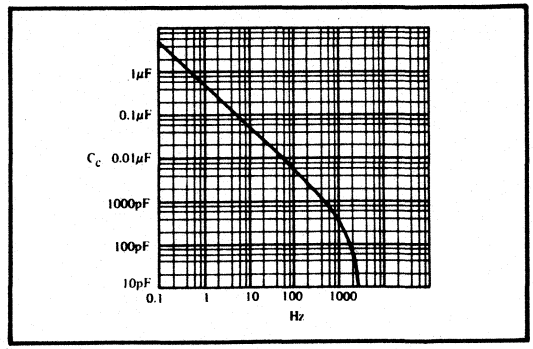


FIGURE 4. -3dB Frequency Vs C_C (Voltage Output).

ALTERNATE GAIN ADJUSTMENT

The gain adjustments are normally made by varying the gain setting resistor at the input. Since voltages at high potential may be present at the input side of the isolation barrier, some applications may require that gain adjustments or gain trimming be done at the output side of the isolation amplifier. For the voltage output configuration, such gain trimming can be done at the output. Figure 5 shows a recommended gain adjustment method. This method would provide a ±1% gain trim at the output.

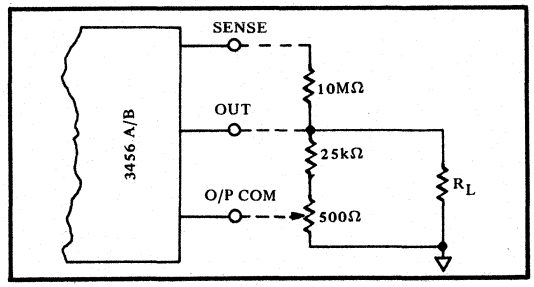


FIGURE 5. Alternate Gain Adjustment Method For Voltage Output Configuration.

CURRENT OUTPUT CONFIGURATION

Current output configuration is a configuration which gives an output current proportional to the input signal. The 3456 should be connected as shown in Figure 6 for current output configuration. In this configuration, the O/P COM pin is not connected to the output ground (PWR COM). The O/P COM pin is connected to R_L. The demodulated signal (voltage between the OUT pin and O/P COM pin) is thus applied across R_S. With a given demodulated signal and known feedback for the output amplifier, the voltage across R_S can be calculated. With known value of this voltage, the value of R_S can be fixed to give the desired output current to the load resistor R_L. The output current is thus programmed by R_S. It does not change with changes in the load resistor R_L. The feedback resistor R_F paralleled with the internal 100kΩ resistor (see Figure 6) helps achieve the required voltage rescaling at the output (the OUT pin).

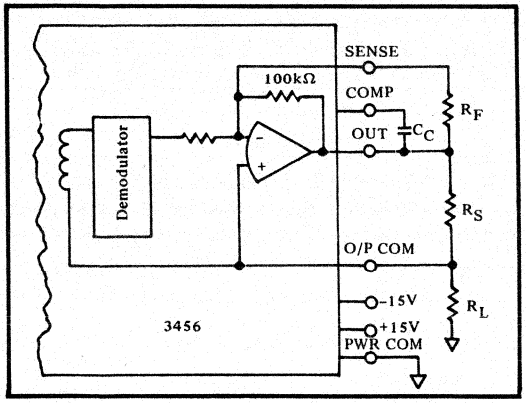


FIGURE 6. Current Output Configuration With Simplified Block Diagram

PROGRAMMING FOR CURRENT OUTPUT

The selection criteria discussed below is based on 3456 being gain programmed for ±10V full scale signal at the OUT pin (the signal as referenced to the PWR COM pin). With ±10V full scale signal, best overall accuracy is achieved.

R_L is defined as the maximum load impedance in ohms and I_o as the maximum peak output current in amperes. The common-mode voltage (an error producing term) is directly proportional to R_L. So, it is desirable to keep R_L to as minimum a value as is consistent with desired application's requirements.

Determine first the value of I_o and R_L suitable for the desired application. The values of R_S and R_F in ohms can be obtained by the expressions,

$$R_S = \frac{10 - I_o R_L}{I_o}$$

and

$$R_F = \frac{10^5 (I_o R_S 10^4 - R_S)}{10^5 - I_o R_S . 10^4 + R_S}$$

C_C, expressed in pF, can be calculated by the expression

$$C_C = \frac{220 . 10^5}{R_F}$$

where R_F is in ohms.

The above calculated value of C_C would maintain the -3dB frequency response at 2.5kHz. Roll-off at a frequency lower than 2.5kHz can be achieved by increasing the value of C_C.

The maximum allowable voltage across $R_S + R_L$ to maintain the specified accuracy, also known as "compliance" is limited to ±10V by the output swing capability of the output amplifier.

The current output configuration contains all error elements of the voltage output configuration plus additional common-mode errors introduced by raising the demodulated signal reference from output ground to the voltage developed across R_L. Hence, as discussed earlier, consistent with the requirements of desired application, it is best to keep the R_L to as minimum a value as is possible. Figure 7 shows the maximum additional peak nonlinearity errors in the current output configuration expressed as a percent of full scale peak to peak output (40mA) vs R_L/R_S.

The values of R_S and R_F as calculated above, would program the unit for the desired full scale output current I_o when the gain of 3456 is scaled for ±10V full scale ouptut. With these values of R_S and R_F the unit would comply with the performance curves shown in Figures 7, 8 and 9. Deviation from this selection procedure could result in degraded performance.

Due to the output amplifier bias currents and the demodulator currents, we recommend that the full scale output current value be ±1mA or higher (up to ±20mA).

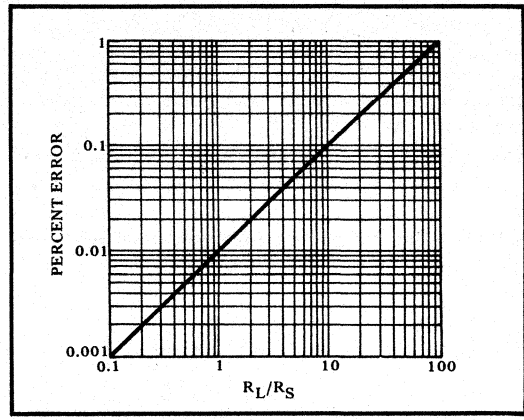


FIGURE 7. Maximum Additional Peak Nonlinearity Errors in Current Output Configuration Expressed as Percent of p-p Output Current Vs R_L/R_S.

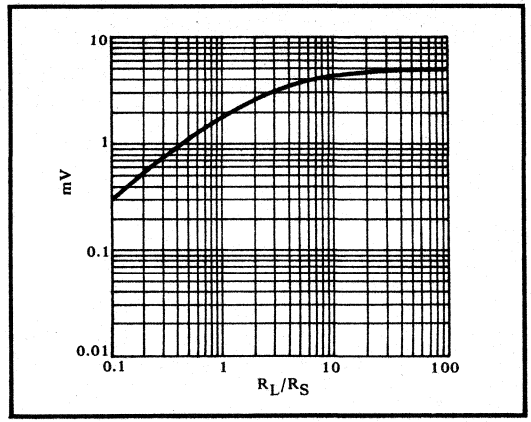


FIGURE 8. Typical Additional Offset in Current Output Configuration Vs R_L/R_S.

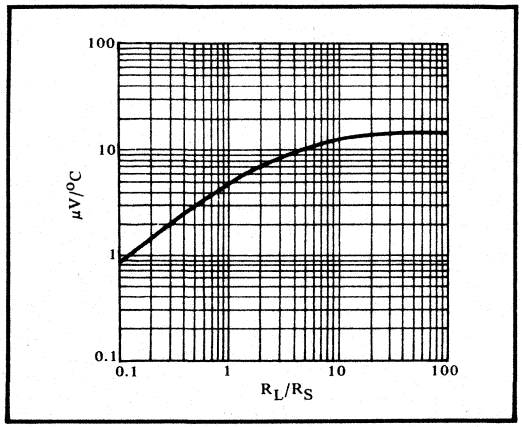


FIGURE 9. Typical Additional Temperature Drift in Current Output Configuration Vs R_L/R_S.

SPECIFICATIONS FOR CURRENT OUTPUT

When the above discussed current output configuration procedure is followed for selection of R_F, R_S, C_C and R_L, the following performance standards would be met by the configuration.

Gain accuracy would be maintained within a maximum of 0.1% above that specified for voltage output configuration. Gain nonlinearity would not exceed the voltage output specification by more than the value indicated in Figure 7.

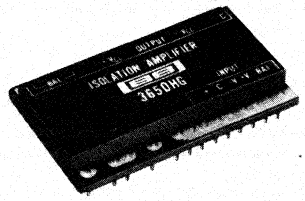
Current output offset and temperature drift are specified as a voltage quantity appearing across R_S. These parameters each contain two terms. The first term is the total offset voltage RTI (referred to input) specification for voltage output mode multiplied by the input gain setting, multiplied by $\frac{R_S}{R_S + R_L}$. The second term is the value found from Figure 8 for the offset voltage and from Figure 9 for the offset voltage drift. Adding these two terms would give the offset voltage and the offset voltage drift values appearing across the scaling resistor R_S. To obtain these parameters in terms of the offset current and the offset current drift, they have to be divided by R_S. In short,

$$\left(\begin{matrix}\text{Voltage Output Mode}\\ \text{Specification}\end{matrix}\right)\left(\begin{matrix}\text{Input}\\ \text{Gain}\end{matrix}\right)\left(\frac{R_S}{R_S + R_L}\right)+\left(\begin{matrix}\text{Value from}\\ \text{Fig. 8 or Fig. 9}\end{matrix}\right)$$
$$=\left(\begin{matrix}\text{Current Output Mode}\\ \text{Specification}\end{matrix}\right)$$

To obtain the offset or drift in units of current, divide the above equation by R_S.

BURR-BROWN

3650
3652



Optically-Coupled Linear ISOLATION AMPLIFIERS

FEATURES

- BALANCED INPUT
- LARGE COMMON-MODE VOLTAGES
  - ±2000V Continuous
  - 140dB Rejection
- ULTRA LOW LEAKAGE
  - 0.25μA max @ 240V/60Hz
  - 1.8pF Leakage Capacitance
- EXCELLENT GAIN ACCURACY
  - 0.05% Linearity
  - 0.05%/1000 Hours Stability
- WIDE BANDWIDTH
  - 15kHz ±3dB
  - 1.2V/μsec Slew Rate

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- DATA ACQUISITION
- INTERFACE ELEMENT
- BIO-MEDICAL MEASUREMENTS
- PATIENT MONITORING
- TEST EQUIPMENT
- CURRENT SHUNT MEASUREMENT
- GROUND-LOOP ELIMINATION
- SCR CONTROLS

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PDS-342B

Printed in U.S.A. July, 1978

THEORY OF OPERATION

Prior to the introduction of the 3650 family optical isolation had not been practical in linear circuits. A single LED and photo diode combination, while useful in a wide range of digital isolation applications, has fundamental limitations – primarily nonlinearity and instability as a function of time and temperature.

The 3650 and 3652 use a unique technique to overcome the limitations of the single LED and photo diode isolator. Figure 1 is an elementary equivalent circuit for the 3650 which can be used to understand the basic operation without considering the cluttering details of offset adjustment and biasing for bipolar operation.

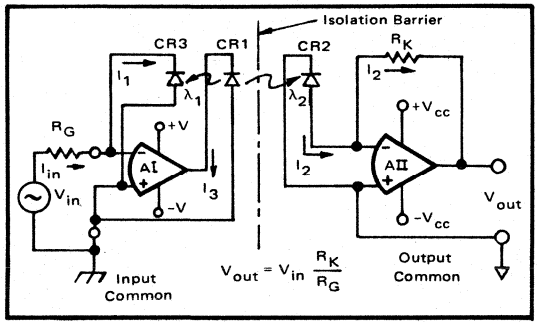

FIGURE 1. Simplified Equivalent Circuit of Linear Isolator.

Two matched photo diodes are used – – one in the input (CR3) and one in the output stage (CR2) – – to greatly reduce nonlinearities and time – temperature instabilities. Amplifier AI, LED CR1 and photo diode CR3 are used in a negative feedback configuration such that $I_1 = I_{in}/R_G$ (where R_G is the user supplied gain setting resistor). Since CR2 and CR3 are closely matched and since they receive equal amounts of light from the LED CR1 (i.e. $\lambda_1 = \lambda_2$), $I_2 = I_1 = I_{in}$. Amplifier AII is connected as a current-to-voltage converter with $V_{out} = I_2 R_K$ where R_K is an internal one megohm scaling resistor. Thus the overall transfer function is:

$$V_{out} = V_{in} \frac{10^6}{R_G}, \left(R_G \text{ in ohms}\right)$$

This improved isolator circuit overcomes the primary limitations of the single LED and photo diode combination. The transfer function is now virtually independent of any degradation in the LED output as long as the two photo diodes and optics are closely matched.* Linearity is now a function of the accuracy of the matching and is further enhanced by the use of negative feedback in the input stage. Advanced laser trimming techniques are used to further compensate for residual matching errors.

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* The only effect of decreased LED output is a slight decrease in full scale swing capability. See TYPICAL PERFORMANCE CURVES.

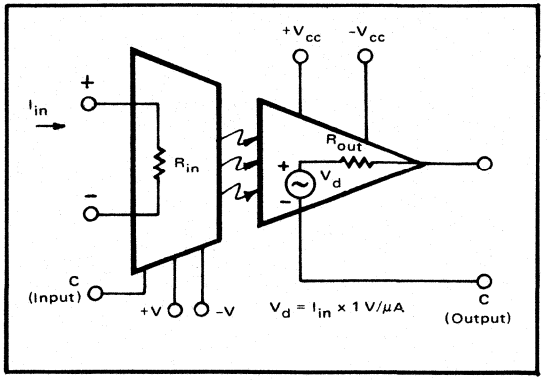


FIGURE 2. Simple Model of 3650.

A model of the 3650 suitable for simple circuit analysis is shown in Figure 2. The output is a current dependent voltage source, V_d, whose value depends on the input current. Thus, the 3650 is a transconductance amplifier with a gain of one volt per microamp. When voltage sources are used the input current is derived by using gain setting resistors in series with the voltage source. (See Installation and Operating Instructions for details). R_{in} is the differential input impedance. The common-mode and isolation impedances are very high and are assumed to be infinite for this model.

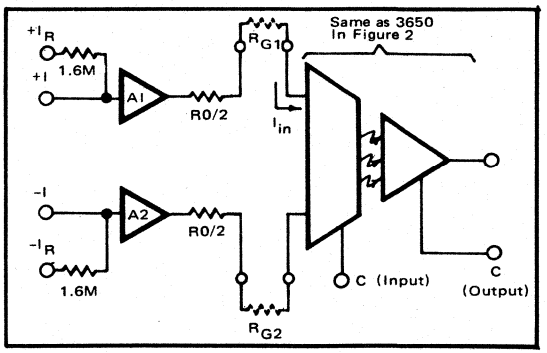


FIGURE 3. Simple Model of 3652.

A simplified model of the 3652 is shown in Figure 3. The isolation and output stages are identical to the 3650. Additional input circuitry consisting of FET buffer amplifiers and input protection resistors have been added to give higher differential and common-mode input impedance ($10^{11}\Omega$), lower bias currents (50pA) and overvoltage protection. The +IR and -IR inputs have a 10ms pulse rating of 6000V differential and 3000V common-mode. (See Definitions for a discussion of common-mode and isolation-mode voltages). The addition of the buffer amplifiers also creates a voltage-in voltage-out transfer function with the gain set by R_{G1} and R_{G2}.

SPECIFICATIONS

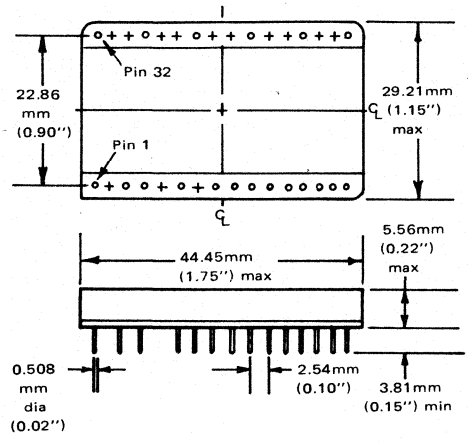
ELECTRICAL

Specifications typical at 25°C and ±15V supply voltages unless otherwise noted.

MODEL		3650HG	3650JG	3650KG	3652HG	3652JG
ISOLATION	Isolation Voltage					
	Rated Continuous, (min)[7]	2000Vp or VDC				
	Test Voltage, (min)[7] 10 sec duration	5000Vp				
	Isolation Mode Rejection, G = 10					
	DC	140dB				
	60 Hz, 5000 ohm source unbalance	120dB				
	Leakage Current, 240V/60 Hz	0.25 μA, max				
	Isolation Impedance					
	Capacitance	1.8pF				
	Resistance	$10^{10}\Omega$				
GAIN	Gain Equation					
	for current sources	$G_I = 10^6$ Volt/Amp			$G_I = 1.0057 \times 10^6$ Volt/Amp[6]	
	for voltage sources	$G_V = \frac{10^6}{R_{G1} + R_{G2} + R_{IN}}$			$\frac{10^6}{R_{G1} + G_{G2} + R_{IN} + R_O}$	
	Input Rsistance, R_{IN}, max	25Ω			25Ω	
	Buffer Output Impedance, R_O	Not applicable			90Ω ±30Ω	
	Gain Equation Error, max[2][7]	1.5%	0.5%	0.5%	1.5%[1]	0.5%[1]
	Gain Nonlinearity[7]	±0.05% typ. ±0.2% max	±0.03% typ. ±0.1% max	±.02% typ. ±.05% max	±0.05% typ. ±0.2% max	±0.05% typ. ±0.1% max
	Gain vs Temperature	±0.03%/°C	±0.01%/°C	±.005%/°C	±0.03%/°C[1]	±0.02%/°C[1]
	Gain vs Time	±0.05%/1000 hrs.			±0.05%/1000 hrs.	
	Frequency Response					
	Slew Rate	0.7V/μs min. 1.2V/μs typ.				
	±3dB Frequency	15 kHz				
	Settling Time					
	to ±0.01%	400 μs				
	to ±0.1%	200 μs				
INPUT STAGE[3]	Input Offset Voltage					
	at 25°C, max[2]	±5mV	±1mV	±0.5mV	±5mV	±2mV
	vs Temperature, max[7]	±25 μV/°C	±10 μV/°C	±5 μV/°C	±50 μV/°C	±25 μV/°C
	vs Supply	100 μV/V			100 μV/V	
	vs Time	50 μV/1000 hrs.			100 μV/1000 hrs.	
	Input Bias Current					
	at 25°C	10 nA typ. 40 nA max			10 pA typ, 50 pA max	
	vs Temperature	0.3 nA/°C			doubles every +10°C	
	vs Supply	0.2 nA/V			1 pA/V	
	Input Offset Current				10 pA	
	vs Temperature	effects included			doubles every 10°C	
	vs Supply	in output offset			1 pA/V	
	Input Impedance					
	Differential	"R_{IN}" = 25Ω max			$10^{11}\Omega$	
	Common-mode	$10^9\Omega$			$10^{11}\Omega$	
	Input Noise					
	Voltage, 0.05 to 100 Hz	8 μV p-p			4 μV p-p	
	10 Hz to 10 kHz	4 μV rms			5 μV rms	
	Input Voltage Range					
	Common-mode, linear operation,	±(|V|-5)V			±(|V|-5)	
	w/o damage, at +, -	±V			±V	
	at +I, -I	Not applicable			±300V for 10ms[4]	
	at +IR, -IR	Not applicable			±3000V for 10ms[4]	
	Differential, w/o damage, at +, -	±V			±V	
	Differential, w/o damage, at ±I, -I	Not applicable			±600V for 10ms[4]	
	Differential, w/o damage, at +IR, -IR	Not applicable			±6000V for 10ms[4]	
	Common-mode Rejection, 60 Hz	90 dB at 60 Hz, 5k imbalance			80 dB at 60 Hz, 5k imbalance	
	Power Supply (Input Stage Only)					
	Voltage (at "+V" and "-V")	±8V to ±18V			±8V to ±18V	
	Current					
	Quiescent	±1.2 mA[5]			±3 mA[5]	
	with ±10V output[5]	+6.5 mA or -6.5 mA typ.			+8.5 mA or -8.5 mA typ.	
		+12 mA or -12 mA max			+16 mA or -16 mA max	
OUTPUT STAGE	Output Voltage, min	±10V			±10V	
	Output Current, min	±5 mA			±5 mA	
	Output Offset Voltage					
	at 25°C max[2]	±25 mV	±10 mV	±10 mV	±25 mV	±10 mV
	vs Temperature, max	±900 μV/°C	±450 μV/°C	±300 μV/°C	±900 μV/°C	±450 μV/°C
	vs Supply	±500 μV/V			±500 μV/V	
	vs Time	±1 mV/1000 hrs.			±1 mV/1000 hrs.	
	Output Noise Voltage					
	0.05 to 100 Hz	50 μV p-p			50 μV p-p	
	10 Hz to 1 kHz	65 μV rms			65 μV rms	
	Power Supply (Output Stage Only)					
	Voltage ("$+V_{cc}$" and "$-V_{cc}$")	±8V to ±18V				
	Current					
	Quiescent	±2.3 mA typ. ±6 mA max				
	with ±5 mA output, max	±11 mA				
TEMPERATURE RANGE[8]	Specification	0°C to 85°C				
	Operating	-40°C to +100°C				
	Storage	-55°C to +125°C				

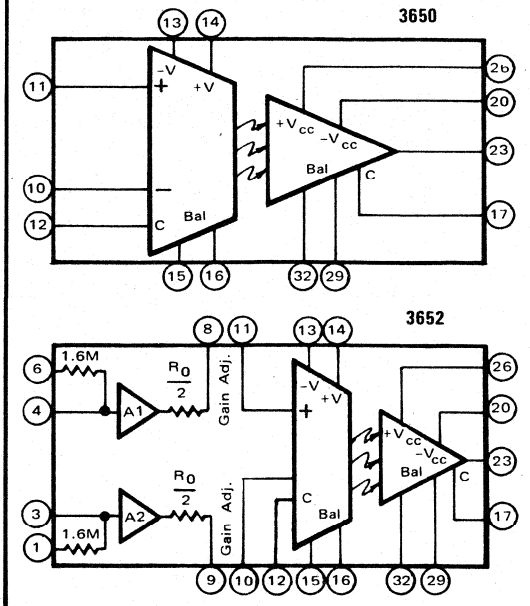
1) Gain error terms specified for inputs applied through buffer amplifiers (i.e., ±I or ±IR pins).
2) Trimmable to zero.
3) Input stage specifications at +I and -I inputs for 3652 unless otherwise noted.
4) Continuous rating is 1/3 pulse rating.
5) Load current is drawn from only supply lead at a time, other supply current at quiescent level, for 3652 add 0.2mA/V of pos. CMV.
6) If used as 3650, see discussion "Input Configurations" under Installation & Operating Instructions.
7) Contact factory for higher voltages or tighter specifications.
8) $dT_j/dt > 1°C_j$/minute below 0°C, and long term storage above 100°C is not recommended.

MECHANICAL



Material: Alumina (Ceramic)
Weight: 14 grams (0.5 oz)
Pins: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std 883 (except paragraph 3.2).
Mating Connector: 2302MC (Set of two, 16 pin strips)

PIN CONNECTIONS



DEFINITIONS

ISOLATION MODE VOLTAGE, V_{ISO}

The isolation mode voltage is the voltage which appears across the isolation barrier, i.e., between the input common and the output common. (See Figure 4.)

Two isolation voltages are given in the electrical specifications; "rated continuous" and "test voltage." Since it is impractical on a production basis to test a "continuous" voltage (infinite test time is implied), it is generally accepted practice to test at a significantly higher voltage for some reasonable length of time. For the 3650 and the 3652 the "test voltage" is equal to 1000 volts plus two times the "rated continuous" voltage. Thus, for a continuous rating of 2000 volts each unit is tested at 5000 volts. Specifically, each unit is tested with a 60 Hz 5000 volt peak sine wave with an acceptance criteria of 3.7μA maximum leakage current I_L (equivalent to 0.25μA @ 240V/60Hz).

COMMON-MODE VOLTAGE, V_{CM}

The common-mode voltage is the voltage midway between the two inputs of the amplifier measured with respect to input common. It is the algebraic average of the voltage applied at the amplifiers input terminals. In the circuit in Figure 5, $(V_+ + V_-)/2 = V_{CM}$ (Note: Many applications involve a large system "common-mode voltage." Usually in such cases the term defined here as "V_{CM}" is negligible and the system "common-mode voltage" is applied to the amplifier as "V_{ISO}" in Figure 4.)

ISOLATION MODE REJECTION

The isolation mode rejection is defined by the equation in Figure 4. The isolation mode rejection is not infinite because there is some leakage across the isolation barrier due to the isolation resistance and capacitance.

NONLINEARITY

Nonlinearity is specified to be the peak deviation from a best straightline, expressed as a percent of peak-to-peak full scale output (i.e., $\pm$10mV @ 20Vpp $\approx$ 0.05%).

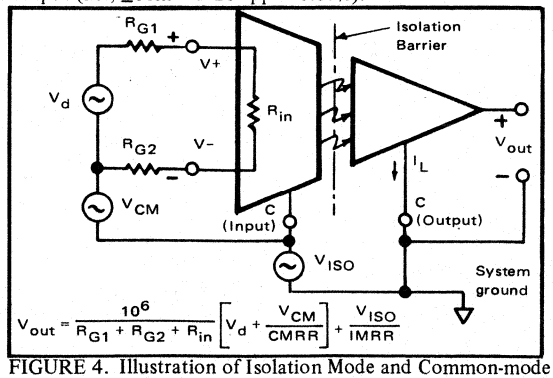
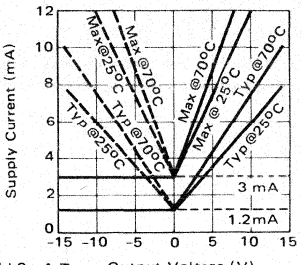


FIGURE 4. Illustration of Isolation Mode and Common-mode Specifications.

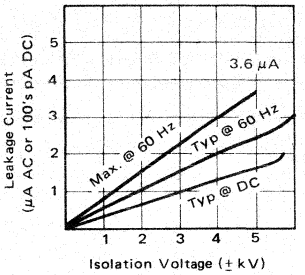
TYPICAL PERFORMANCE CURVES

Typical @ 25°C and ±15 V power supplies unless otherwise noted.

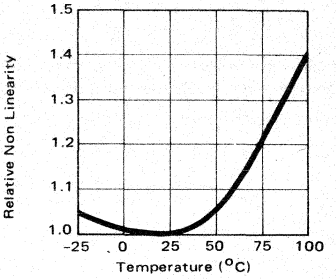
INPUT STAGE SUPPLY CURRENT VS. OUTPUT VOLTAGE



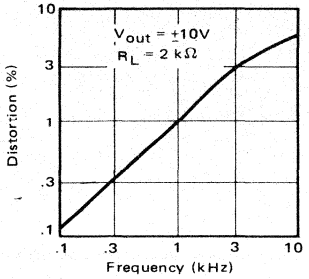
ISOLATION LEAKAGE CURRENT VS. ISOLATION VOLTAGE



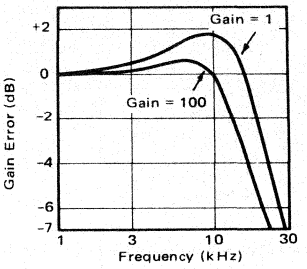
NORMALIZED LINEARITY VS. TEMPERATURE



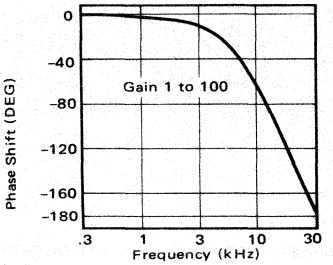
DISTORTION VS. FREQUENCY



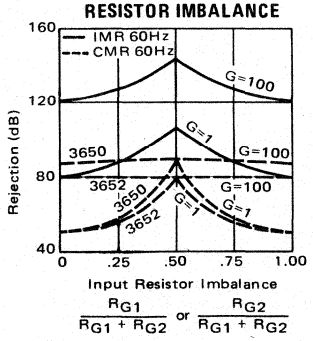
GAIN ERROR VS. FREQUENCY



PHASE SHIFT VS. FREQUENCY

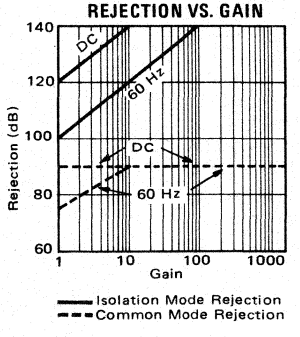


REJECTION VS. RESISTOR IMBALANCE

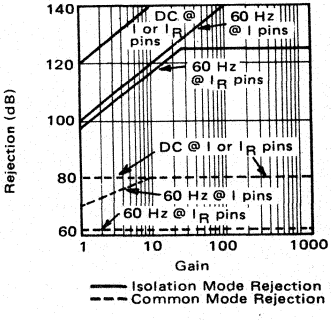


$$\frac{R_{G1}}{R_{G1} + R_{G2}} \text{ or } \frac{R_{G2}}{R_{G1} + R_{G2}}$$

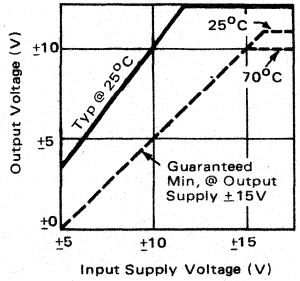
3650 COMMON-MODE AND ISOLATION MODE REJECTION VS. GAIN



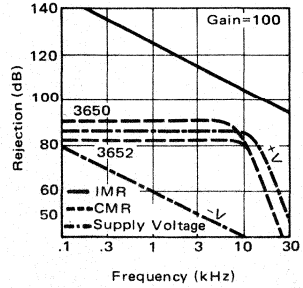
3652 COMMON-MODE AND ISOLATION MODE REJECTION VS. GAIN



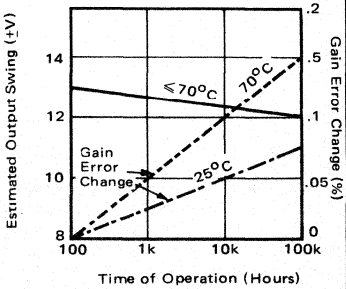
OUTPUT VOLTAGE SWING VS. INPUT SUPPLY VOLTAGE



REJECTION VS. FREQUENCY



OUTPUT VOLTAGE AND GAIN ERROR VS. TIME



ISO. AMP.

INSTALLATION & OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

The power supply connections for the 3650 and 3652 are shown in Figure 5. When a DC to DC converter is used for isolated power it is placed in parallel with the isolation barrier of amplifier. This can lower the isolation impedance and degrade the isolation mode rejection of the overall circuit. Therefore, a high quality, low leakage DC to DC converter such as the Burr-Brown Model 700 should be used.

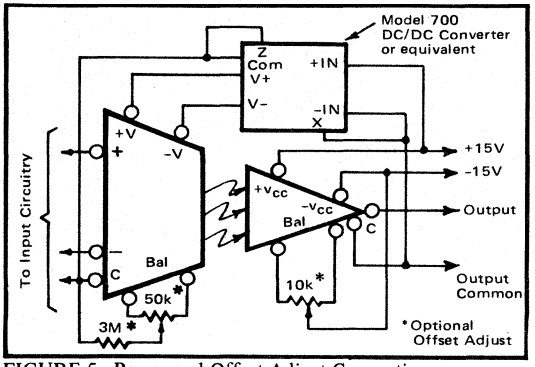


FIGURE 5. Power and Offset Adjust Connections.

OFFSET VOLTAGE ADJUSTMENTS

The offset nulling circuits are identical for the 3650 and 3652 and are shown in Figure 5. The offset adjust circuitry is optional and the units will meet the stated specifications with the BAL terminals unconnected. Provisions are available to null both the input and output stage offsets. If the amplifier is operated at a fixed gain normally only one adjustment will be used; the output stage (10kΩ adjustment) for low gains and the input stage (50kΩ adjustment) for high gains. (> 10)

Use the following procedure if it is desired to null both input and output components (for example, if the gain of the amplifier is to be switched). The input stage offset is first nulled (50kΩ adjustment) with the appropriated input signal pins connected to input common and the amplifier set at its maximum gain. The gain is then set to its minimum value and the output offset is nulled (10kΩ adjustment).

INPUT CONFIGURATIONS

Some possible input configurations for the 3650 and 3652 are shown in Figure 6. Differential input sources are used in these examples. For situations with nondifferential inputs the appropriate source term should be set to zero in the gain equations and replaced with a short in the diagrams.

Figure 6a shows the 3650 connected as a transconductance amplifier with input current sources. Voltage sources are shown in Figure 6b. In this case the voltages are converted to currents by R_{G1} and R_{G2}. As shown by the equations they perform as gain setting resistors in the voltage transfer function. When a single voltage source is used it is recommended (but not essential) that the gain setting resistor remain split into two equal halves in order to minimize errors due to bias currents and common-mode rejection (see typical performance curves).

Figure 6c illustrates the connections for the 3652 when the FET buffer amplifiers A1 and A2 are used. This configuration provides an isolation amplifier with high input impedance (both common-mode and differential) and good common-mode and isolation mode rejection. It is a true isolated instrumentation amplifier which has many benefits for noise rejection when source impedance imbalances are present.

In the 3652 the voltage gain of the buffer amplifiers is slightly less than unity, but the gain of the output stage has been raised to compensate for this so that the overall transfer function from the ±I or ±IR inputs to the output is correct. It should be noted that A1 and A2 are buffer amplifiers. No summing can be done at the ±I or ±IR inputs. Figure 6c shows the +I and -I inputs used. If more input voltage protection is desired, then the +IR and -IR inputs should be used. This will increase the input noise due to the contribution from the 1.6 megohm resistors, but will provide additional differential and common-mode protection (10ms rating of 3kV).

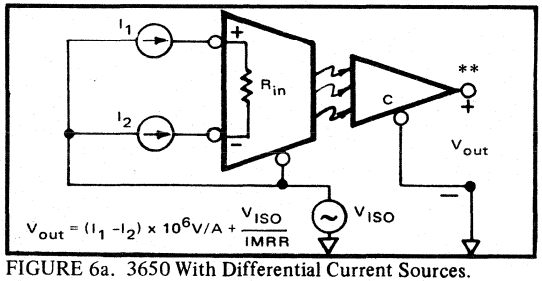


FIGURE 6a. 3650 With Differential Current Sources.

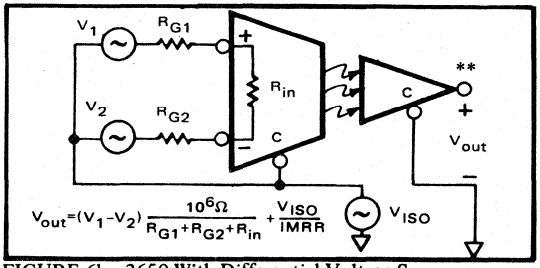


FIGURE 6b. 3650 With Differential Voltage Source.

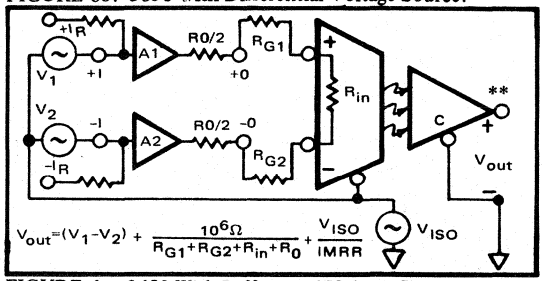


FIGURE 6c. 3652 With Differential Voltage Source.

** The offset adjustment circuitry and power supply connections have been omitted for simplicity. Refer to Figure 5 for details.

ERROR ANALYSIS

A model of the 3650 suitable for DC error analysis of offset voltage, voltage drift vs. temperature, bias current, etc., is shown in Figure 7.

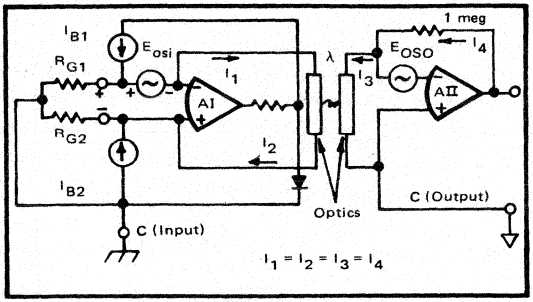


FIGURE 7. DC Error Analysis Model for 3650.

AI and AII, the input and output stage amplifiers, are considered to be ideal. Separate external generators are used to model the offset voltages and bias currents. R_{in} is assumed to be small relative to R_{G1} and R_{G2} and is therefore omitted from the gain equation. The feedback configuration, optics and component matching are such that $I_1 = I_2 = I_3 = I_4$. A simple circuit analysis gives the following expression for the total output error voltage due to offset voltages and bias currents.

$$V_{out\text{-}total} = \frac{10^6}{R_{G1} + R_{G2}} \left[E_{osi} + (I_{B1} R_{G1} - I_{B2} R_{G2})\right] + E_{oso} \quad (1)$$

Offset current is defined as the difference between the two bias currents I_{B1} and I_{B2}. If $I_{B1} = I_B$ and $I_{B2} = I_B + I_{os}$,

then, for $R_{G1} = R_{G2}$, $V_{out} - I_B = \frac{10^6 \cdot I_{os}}{2}$.

This component of error is not a function of gain and is therefore included as a part of E_{oso} specifications. The output errors due to the output stage bias current are also included in E_{oso}. This results in a very simple equation for the total error:

$$V_{out\text{-}total} = \frac{10^6 E_{osi}}{2 R_{G1}} + E_{oso} \text{ (for } R_{G1} = R_{G2}) \quad (2)$$

In summary it should be noted that equation (2) should be used only when $R_{G1} = R_{G2}$. When $R_{G1} \neq R_{G2}$, equation (1) applies.

The effects of temperature may be analyzed by replacing the offset terms with their corresponding temperature gradient terms:

$V_{out} \rightarrow \Delta V_{out}/\Delta T$, $E_{osi} \rightarrow \Delta E_{osi}/\Delta T$, etc.

OUTPUT NOISE

The total output noise is given by

$$E_n\,(RMS) = \sqrt{(E_{nI}\ G)^2 + (E_{nO})^2}$$

where E_n (RMS) = total output noise
E_{nI} = RMS noise of the input stage
E_{nO} = RMS noise of the output stage
$G = 10^6/(R_{G1} + R_{G2})$

E_{nO} includes the noise contribution due to the optics and the noise currents of the output stage. Errors created by the noise current of the input stage are insignificant compared to other noise sources and are therefore omitted.

COMMON-MODE and ISOLATION MODE REJECTION

The expression for the output error due to common-mode and isolation mode voltage is:

$$V_{out} = G \cdot \frac{V_{cm}}{CMRR} + \frac{V_{iso}}{IMRR}$$

See Definitions for explanation of CMRR, IMRR terms.

GUARDING & PROTECTION

To preserve the excellent inherent isolation characteristics of these amplifiers, the following recommended practice should be noted:

1. Use shielded,twisted pair of cable at the input as with any instrumentation amplifier;
2. Care should be taken to minimize external capacitance. A symmetrical layout of external components to achieve balanced capacitance from the input terminals to output common will preserve high IMR;
3. External components and conductor patterns should be at a distance equal to or greater than the distance between the input and output terminals, to prevent HV breakdown.
4. Though not an absolute requirement, the use of laminated or conformally coated printed circuit boards is recommended.

APPLICATIONS

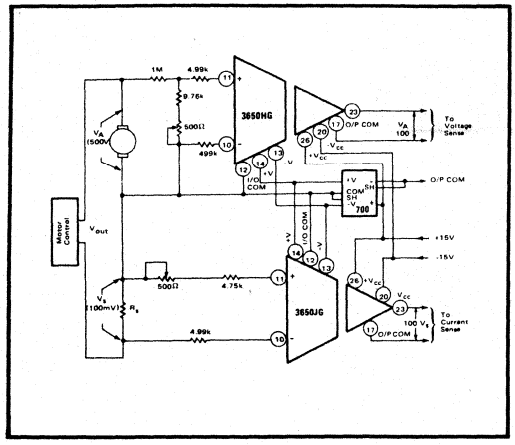


FIGURE 8. Isolated Armature Current and Voltage Sensor.

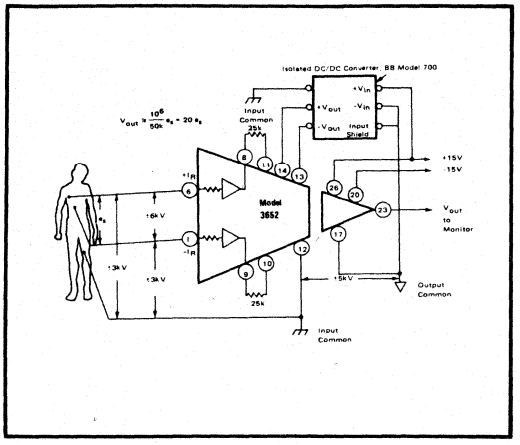


FIGURE 9. 3652 Used in Patient Monitoring Application (ECG, VCG, EMG Amplifier).

Figure 8 shows a system where isolation amplifiers (3650) are used to measure the armature current and the armature voltage of a motor.

The armature current of the motor is converted to a voltage by the calibrated shunt R_S and then amplifier (adjustable gain) and isolated by the 3650.

The armature voltage is sensed by the voltage divider (adjustable) shown and then amplified and isolated by the 3650.

The 3650 provides the advantage of accurate current measurement in the presence of high common-mode voltage. Both 3650s' provide the advantage of isolating the motor ground from the control system ground. Isolated power is provided by an isolated DC/DC converter (BB Model 700 or equivalent).

The 3652 is ideally suited for patient monitoring applications as shown in Figure 9. The fact that it is a true balanced input instrumentation amplifier with very high differential and common-mode impedance means that it can greatly reduce the common-mode noise pick up due to imbalance in lead impedances that often appear in patient monitoring situations. The 3kV and 6kV shown in Figure 9 are the 10ms pulse ratings of the +IR and -IR inputs for the common-mode and differential input voltages with respect to input common. The rating of the isolation barrier is 2000Vp continuous. The non recurrent pulse rating of the isolation barrier is 5000Vp since each unit is factory tested at 5000Vp. If the isolation barrier is to be subjected to higher voltages a gas filled surge voltage protection device can be used. For multichannel operation, four 3652s can be powered by one model 700, isolated DC/DC converter. The total leakage current for all four channels at 240V/60Hz would still be less than 2μA.

The block diagram in Figure 10 shows the use of isolation amplifiers in SCR control application.

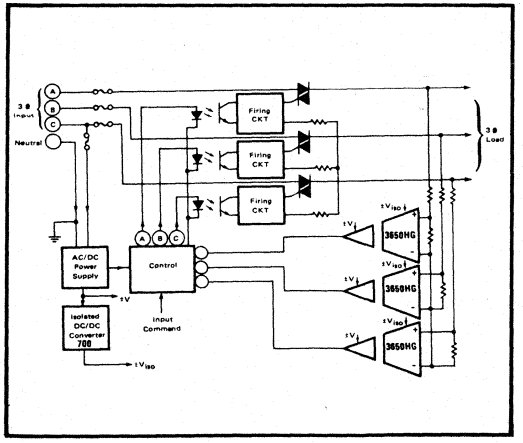
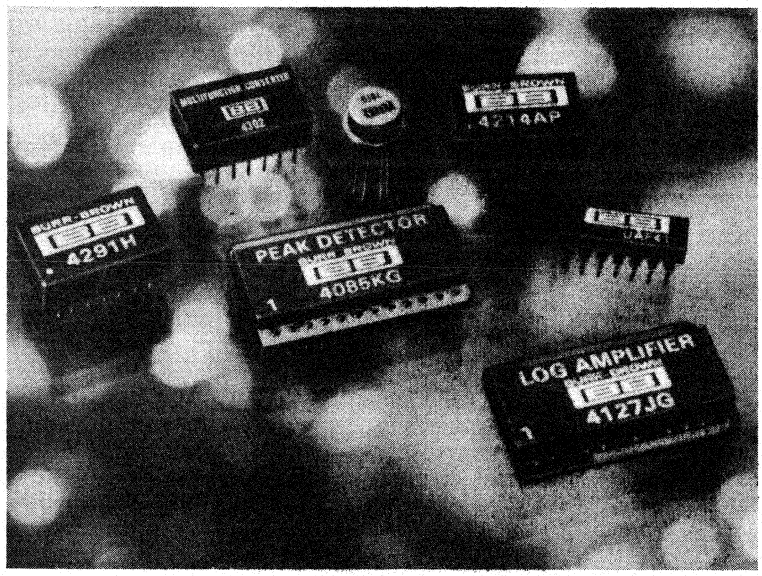


FIGURE 10. 3 Phase Bi-Directional SCR Control with Voltage Feedback.

4. ANALOG CIRCUIT FUNCTIONS



Analog circuits act as building blocks with which to perform a variety of instrumentation, computation, and control functions. They provide a broad range of versatile, proven, and ready to use computational function circuits for the designer to use in developing simple or complex systems. The analog circuit functions include multipliers, dividers, multifunction converters, true rms-to-DC converters, logarithmic amplifiers, voltage and window comparators, peak detectors, precision oscillators, and filters. The multifunction converter also provides multiply, divide, square, square root, exponentiate, roots, sine, cosine, arctangent, vector magnitude RMS-to-DC and logarithmic amplifier functions.

The availability of these relatively complex functions as precise, versatile, easy-to-use, low-cost building blocks has broadened the scope of practical analog circuit systems and greatly simplified analog circuit designs. The names of most analog circuit functions are self-explanatory and describe the main functions they perform.

These functions are used mostly for processing (handling) and/or conditioning of analog signals, and usually (though not always) for simulation of algebraic and/or trigonometrically expressed analog computations. The variety of applications these functions are effectively used for, are limited only by the designers' creative imagination. Some of the interesting applications where analog circuit functions have found wide acceptance are listed in the table on the following page.

TABLE OF CONTENTS

Introduction 4-1
Selection Guide 4-3
Glossary of Terms and Definitions 4-5
Product Data Sheets 4-7

Types of Applications	Recommended Analog Circuit Function
Analog simulation. Algebraic and trigonometric computations. Power series approximation, function fitting and linearizing Analog wave shaping.	Multiplier, Divider, Multifunction Converter, Logarithmic Amplifier, Oscillator.
VCO and AGC applications.	Multiplier, Divider.
Vector computation.	Multifunction Converter, Multiplier.
Power and energy measurements.	Multiplier, RMS-to-DC Converter.
Moduation and demodulation.	Multiplier, Divider.
Signal compression.	Logarithmic Amplifier.
Log-antilog-log ratio computations.	Logarithmic Amplifier.
Light-related measurements.	Logarithmic Amplifier.
Analog signal conditioning.	All circuit functions.
Instrumentation and control systems.	All circuit functions.
Variety of test equipment.	All circuit functions.
Transducer excitation	Oscillator.
Signal reference.	Oscillator.
Alarm circuits.	Voltage and Window Comparators.
Bang-bang control applications.	Voltage and Window Comparators.
Control of limit stops.	Voltage and Window Comparators.
Analog memory and peak detection.	Peak Detection.
Fixed-frequency tuned filters.	ATF-76 Filters.

SELECTION GUIDE
Analog Circuit Functions

MULTIPLIER/DIVIDERS

Accuracy at 25°C	Model	Specification Temp. Range (°C)	Operating Temp. Range (°C)	Package		Page
0.25% max., no trimming required. 0.1% typical, externally trimmed.	4206K	0 to +70	-25 to +85	DIP		4-41
	4204K	-25 to +85	-55 to +125	DIP		4-31
	4204S	-55 to +125	-55 to +125	DIP		4-31
0.50% max., no trimming required. 0.2% typical, externally trimmed.	4206J	0 to +70	-25 to +85	DIP		4-41
	4204J	-25 to +85	-55 to +125	DIP		4-31
	4213BM	-25 to +85	-55 to +125	TO-100		4-47
	4214BP	-25 to +85	-55 to +125	DIP		4-51
	4204S	-55 to +125	-55 to +125	DIP		4-31
	4213SM	-55 to +125	-55 to +125	TO-100		4-47
	*4214SM	-55 to +125	-55 to +125	DIP		4-51
1% max., no trimming required.	4203K	0 to +70	0 to +70	TO-100		4-26
	4205K	0 to +70	0 to +70	TO-100		4-37
	4213AM	-25 to +85	-55 to +125	TO-100		4-47
	*4214RM	-55 to +125	-55 to +125	DIP		4-51
	*4214AP	-25 to +85	-55 to +125	DIP		4-51
	4203S	-55 to +125	-55 to +125	TO-100		4-26
	4205S	-55 to +125	-55 to +125	TO-100		4-37
2% max., no trimming required.	4203J	0 to +70	0 to +70	TO-100		4-26
	4205J	0 to +70	0 to +70	TO-100		4-37

SPECIAL FUNCTIONS

Function	Model	Comments	Package		Page
Divider	4291H	±1% to ±0.25% untrimmed	DIP		4-55
	4291J	accuracy. ±0.1% by external	DIP		4-55
	4291K	trimming.	DIP		4-55
Multifunction Converter (multiply, divide, square, square root, exponentiate, sineθ, cosineθ, etc.)	4301	4301 is hermetically sealed and	DIP		4-59
	4302	shielded in a metal package; 4302 is in a plastic package. Both units are pin-for-pin compatible. Functions shown in parenthesis can be obtained by connecting 4301/4302 with a few external components as is shown in the detailed Product Data Sheets.	DIP		4-65
Logarithmic	4127JG	4127JG (1% accuracy) and 4127KG	DIP		4-19
	4127KG	(0.5% accuracy) provide logarithmic transfer function for input signals (2 current or 2 voltage input signals) and antilog transfer function for current or voltage inputs.	DIP		4-19
True RMS-to-DC Conversion	4340	Laser-trimmed, requires no external trimming for rated accuracy. Pin-for-pin compatible with 4341. Hermetically sealed in metal package.	DIP		4-71
	4341	External trimming required. Lower cost in plastic package.	DIP		4-75

*New

SPECIAL FUNCTIONS (CONT)					
Function	Model	Comments	Package		Page
Oscillator	4023/25	Fixed-frequency (customer-specified, 10Hz to 20kHz) provides low distortion, stable amplitude sine wave output.	Module		4-7
	4423	Very-low cost in plastic package. Provides resistor programmable quadrature outputs (sine and cosine wave outputs simultaneously available).	DIP		4-79
Fixed-Frequency Active Filter	ATF76 Series	More than 60 complete 2-pole active filters in this series. Low cost makes them especially suitable for OEM applications. Cascading the units provides complex filter response. Bandpass, band-reject, and low-pass transfer functions.	DIP		4-83
Universal Active Filter	UAF41 UAF31 UAF21 UAF21H UAF11 UAF11H	Complete 2-pole active filters. Cascading the units provides complex filter response. 3 or 4 external resistors provide easy control of Q-factor. Low-pass, high-pass, and bandpass transfer functions.	DIP DIP DIP DIP DIP DIP		4-106 4-98 4-90 4-90 4-90 4-90
Comparator	4115/04 (window) 4082/03 (voltage)	Provides 2-state logic output that indicates whether one analog voltage is > or < another. 4115/04 provides a window or dual limit for comparison. Unit has 3 inputs - one for a voltage that sets upper limit, one for a voltage that sets lower limit, and one for a signal input. The 3 outputs are capable of sinking up to 200mA of current, indicating if the input voltage is above, below, or in the window.	Module Module		4-17 4-9
Peak Detector	4085BM 4085KG 4085SM	These are analog memory circuits which hold and provide read-out of a DC voltage equal to peak value of a complex input waveform. Digital mode control provides reset capability and allows selection of peaks within a desired time interval.	DIP DIP DIP		4-11 4-11 4-11

1) Prices are for quantities (1-9) (10-24) (25-99).

GLOSSARY OF TERMS & DEFINITIONS
Analog Circuit Functions

ABSOLUTE-VALUE CIRCUIT
A circuit that produces a unipolar output signal equal to the magnitude or absolute value of a bipolar input signal.

ACCURACY
The deviation from the ideal output voltage defined as a percent of full scale output voltage.

COMPARATOR
A device with two stable output states which signal if an input current or voltage has crossed a threshold. The threshold may be set by one or more other currents or voltages, either fixed or variable.

CREST FACTOR
The ratio of the peak value of a time-varying signal to its rms value.

CURRENT LIMITING
Limiting the output current supplied by a circuit for protection purposes.

FEEDBACK
The return of a portion of the output signal from a device to the input of the device.

FEEDTHROUGH
The input offset parameter applicable to multipliers. It is the output voltage when voltage is applied to one input of the multiplier and the other input is at zero.

FULL POWER FREQUENCY RESPONSE
The maximum frequency at which the output will swing full scale peak-to-peak voltage into a rated load without significant distortion of the output.

HYSTERESIS
The transfer response lag of comparators controlled by positive feedback and resulting in different trip points for the two directions of output transition.

LOGARITHMIC AMPLIFIER
An amplifier which develops an output voltage that is proportional to the logarithm of the input signal.

OUTPUT OFFSET
The output voltage when the inputs are grounded.

RMS
The root-mean-square value of a time-varying signal E(t) over a time period of T is

$$E_{rms} = \sqrt{1/T \int_o^T [E(t)]^2 \, dt}$$

RMS CONVERTER
A circuit that develops a DC output voltage equal in rms value to an input signal of arbitrary waveform.

SETTLING TIME
The time required for the output to respond to a step input and to settle within some specified error band around the output final value.

SLEW RATE
The maximum rate of change of an output voltage when supplying the rated output.

SMALL SCALE FREQUENCY RESPONSE
The -3dB output frequency for a small AC signal (normally 1V, p-p) input. For multipliers, one input may be held at +10VDC or -10VDC and the other input held at small AC signal.

WINDOW COMPARATOR
A compartor that detects levels within a set range or window rather than simply distinguishing between levels above and below a set point.

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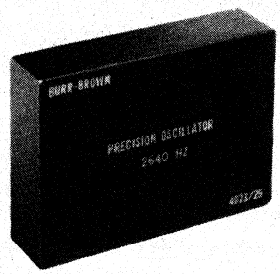

4023/25

PRECISION OSCILLATOR

FEATURES

- FIXED FREQUENCY - 10Hz to 20kHz
- STABLE AMPLITUDE
- SINE WAVE OUTPUT
- LOW DISTORTION

DESCRIPTION

Model 4023/25 is an all solid-state, ultra-stable sine-wave oscillator. Both output amplitude and frequency are constant, and the stability of both with time and temperature variations is excellent. Internal high-performance Burr-Brown IC operational amplifiers are used to form a Wien bridge oscillator circuit and to regulate the output amplitude. The frequency of oscillation is within ±1% of the customer-specified value. If desired, external components may be added to trim the frequency to an exact value. Adding two external resistors will raise the output frequency and adding two external capacitors will lower the output frequency. With its small size, low distortion, and excellent frequency and amplitude stability, the Model 4023/25 is ideal for use as a reference oscillator in airborne or mobile equipment, special-purpose test equipment, and in telemetry systems. To order, specify Model 4023/25 and frequency.

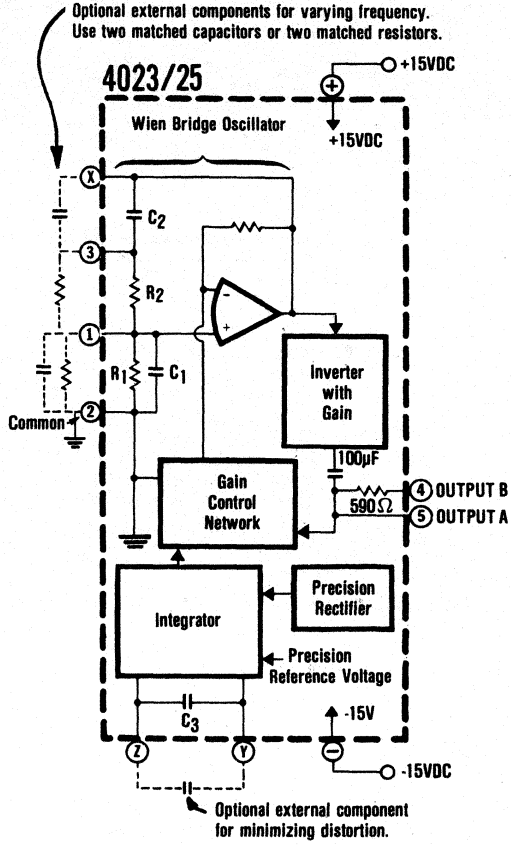

Figure 1. Simplified Schematic Diagram - Model 4023/25.

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PDS-209D

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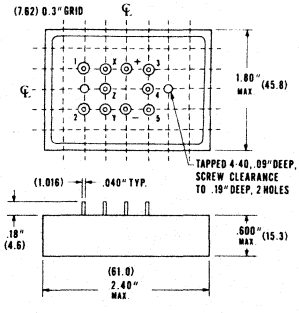
ELECTRICAL SPECIFICATIONS

Typical performance at 25°C and with rated supply unless otherwise noted.

FREQUENCY	
Range (1)	Customer specified, may be any value from 10 Hz to 20 kHz.
Accuracy	±1%, (May be trimmed by the user to less than ±1%)
Stability vs. Temperature	0.04%/°C (max.)
OUTPUT (3)	
Amplitude - Output A	6 Vrms
- Output B	3 Vrms (with 600 Ω load)
Amplitude Accuracy	±2%
Impedance - Output A	1 Ω
- Output B	600 Ω
Rated Load - Output A	1.2 k Ω
- Output B	600 Ω
Distortion (max.)	0.1%
AMPLITUDE STABILITY	
vs. Temperature (max.)	0.02%/°C
Noise and Jitter (max.)	0.02%
Long Term (max.)	0.1%
TEMPERATURE RANGE	
Operating, Rated Specifications	-25°C to +85°C
Storage	-55°C to +100°C
POWER REQUIREMENTS	
Rated Supply	±15 Vdc
Voltage Range at 25°C (2)	±12 Vdc to ±18 Vdc
Supply Drain (max.)	±40 mA

(1) To order, specify Model 4023/25 and frequency.
(2) The positive and negative supplies must be balanced within 2% of each other.
(3) The output may be taken from either Output A or Output B (not both).

MECHANICAL SPECIFICATIONS



Dimensions in millimeters are shown in parentheses.

Weight: 4 oz. maximum (120 grams)

Mating Connector: 1500MC (Optional)

OPERATING INSTRUCTIONS

With $R_1 = R_2$ and $C_1 = C_2$, the Wien-Bridge oscillator will provide a sine-wave oscillation of frequency:

$f_o = 1/2\pi RC$, where $R = R_1 = R_2$ and $C = C_1 = C_2$.

The frequency of oscillation, f_o, will be within ±1% of the nominal value specified by the customer. The frequency may be lowered by externally paralleling the internal capacitors C_1 and C_2; and the frequency may be raised by paralleling the internal resistors R_1 and R_2. The nominal values of C_1 and C_2 will be as follows:

Frequency f_o	C_1 and C_2
10Hz to 100Hz	0.1μF
101Hz to 1000Hz	0.01μF
1001Hz to 20kHz	0.001μF

It is important to pad both R_1 and R_2 or C_1 and C_2 by an equal amount to keep distortion within specifications.

If the frequency is lowered by a significant amount, it may be necessary to externally parallel the integrator capacitor C_3 to lower distortion of the output.

The range of frequency adjustment is approximately 2 decades (within 10kHz and 20kHz). For example, a 10Hz unit may be trimmed for a frequency of up to 1kHz or a 10kHz unit may be varied down to 100Hz. However, the distortion and amplitude stability specifications are guaranteed and tested only for the nominal frequency of oscillation. In general, the degradation in distortion and amplitude stability as the frequency is varied over a wide range is very small.

INSTALLATION

The Model 4023/25 is designed for installation on a flat mounting surface such as a chassis or printed circuit board. The gold-flashed pins may be hand or dip soldered; for plug-in installation, the Model 1500MC mating connector may be installed on the chassis. The unit may be secured to the mounting surface by means of two 4-40 machine screws inserted through the mounting surface not more than 3/16" into the tapped holes in the bottom.

Pin 1 and pin 3 must be shielded from external sources of electrical noise. The module is particularly sensitive to periodic noise near the resonant frequency. Also, if external bridge components are added to the Wien bridge terminals they must be physically near the 4023/25 module.

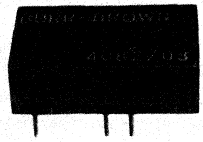
EXTERNAL CONNECTIONS

External connections are made to the gold-flashed pins on the unit. These connections include the Wien bridge, integrator feedback, output, and power supply termination and are made as follows:

Pin 1	Wien Bridge Terminals
Pin 2 Common	Wien Bridge Terminals
Pin 3	Wien Bridge Terminals
Pin X	
Pin 4	Output B
Pin 5	Output A
Pin Y	Integrator Feedback Terminals
Pin Z	Integrator Feedback Terminals
(+)	Positive Power, +15VDC
(-)	Negative Power, -15VDC

BURR-BROWN

4082/03



GENERAL PURPOSE COMPARATOR

FEATURES

- RELAY AND LAMP-DRIVING CAPABILITY
  Up to 100mA LOAD
- TRANSIENT PROTECTION TO 400mA
- RESPONSE TIME AND HYSTERESIS ADJUST

DESCRIPTION

Model 4082/03 is a low cost hybrid integrated circuit comparator in a dual-in-line package. It combines a low-cost differential input comparator with an open collector transistor output stage capable of sinking 100mA. With transient protection of 400mA, this unit is an excellent choice to drive lamps, relays, and other devices with high transient requirements. In addition, the open collector output will accept up to +30VDC making the 4082/03 compatible with MOS circuitry and high noise immunity logic as well as TTL and DTL devices. The 4082/03 operates from ±15VDC power. Additional outputs are provided for response time control and hysteresis feedback.

OPERATION

Model 4082/03 will function when power is applied and the output load is connected between Pin 9 and Pin 13. The load may be resistor, lamp, or relay. A simplified diagram in shown in Figure 1.

Either input may be connected to common or to some reference voltage. Whenever the (+In) input is positive with respect to the (-In) input, the output transistor is switched ON. The load power ($+V_R$) may be any voltage up to +30VDC.

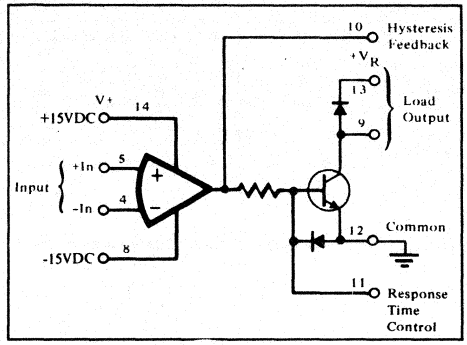


FIGURE 1. Simplified Diagram of Model 4082/03 Comparator.

HYSTERESIS

Hysteresis may be added by means of positive feedback as shown in Figure 2. The amount of hysteresis is approximately:

$$\text{Hysteresis} \approx 26V\ R_o/R_f + R_o,\ R_f \geq 10k\Omega$$

Adding hysteresis provides better noise immunity, but at the price of decreased switching resolution.

RESPONSE TIME

Response time can be decreased if desired by adding capacitance between Pin 11 and Pin 12 (common). This will limit the rise and fall times of the output voltage, which in turn limits turn-on surge currents when driving lamps.

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ELECTRICAL SPECIFICATIONS

Typical performance at 25°C and with rated supplies unless otherwise noted.

MODEL	4082/03	Units
INPUT		
Signal Levels		
Either (or both) Inputs	±10	V
Absolute Maximum	±15	V
Impedance (both Inputs)		
Differential, small signal	300	kΩ
Differential, large signal	10	kΩ
Common-mode	100	MΩ
Bias Current at 25°C	400	nA
Over Temperature Range, (max)	700	nA
Differential Offset Current at 25°C	±30	nA
Over Temperature Range, (max)	±80	nA
OUTPUT		
Switched Current Sink		
Impedance to common from output		
OFF state	1	MΩ
ON state	3	Ω
Load Voltage Supply (V_R)	0 to +30	V
Load Current (sinking)	Up to +100	mA
Transient (absolute maximum)	+400	mA
ACCURACY		
Sensitivity, (min)	±0.1	mV
Offset		
Over Temperature (max)[1]	±12	mV
at 25°C	±3	mV
vs Power Supply	±50	μV/V
FREQUENCY RESPONSE		
Total Switching Time[2]		
at 20mV Step Input	7	μsec
TEMPERATURE RANGE		
Operating, Rated Specification	-25 to +85	°C
Operating, Derated Performance	-40 to +85	°C
Storage	-55 to +100	°C
POWER SUPPLY REQUIREMENTS		
(-V and +V)		
Rated Supply Voltage	±15	V
Voltage Range	-14 to +16	V
Supply Drain, (max)	±12	mA

1. This offset is referred to the input and includes offset due to common-mode effects.
2. With load supply of +15VDC and with output load of 300Ω. Total switching time includes delay time and rise time. The input E_{IN} is a sine wave of frequency f_N.

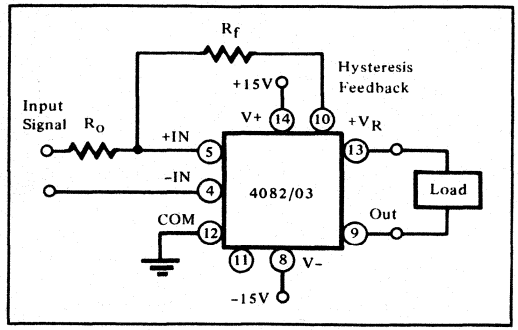
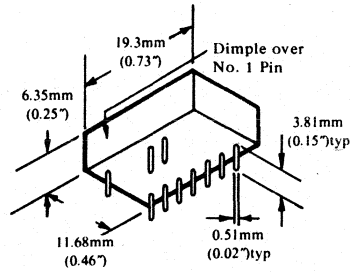
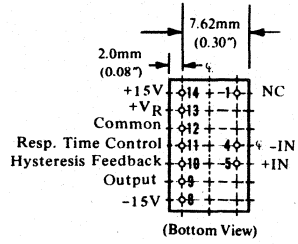


FIGURE 2. Connections for Adding Hysteresis.

MECHANICAL SPECIFICATIONS

MODEL 4082/03





WEIGHT: 0.12 oz. (3.40 grams)
GRID SPACING: 0.1" (2.5)
MATERIAL: Black Epoxy
PIN: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
CONNECTOR: Standard 14 pin DIP socket

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4085

HYBRID MICROCIRCUIT PEAK DETECTOR

FEATURES

- STORES TRANSIENT VOLTAGES
- COMPLETELY SELF-CONTAINED
- ACCURATE TO ±0.01%
- LOW DROOP ERRORS
- SMALL DIP PACKAGE

DESCRIPTION

The 4085 is a specialized sample/hold amplifier that tracks an input signal until a maximum amplitude is reached. That maximum value is held at the analog output, and the digital STATUS output indicates that a peak has been detected. The unit can then be commanded to hold that value, ignoring additional peaks, or reset to a user-specified reference voltage. The 4085 detects positive-going peaks from -10V to +10V and is available in a hermetic metal package and a low-cost ceramic package. Three models are available, specified for temperature ranges 0 to +70°C (4085KG), -25 to +85°C (4085BM), and -55 to +125°C (4085SM).

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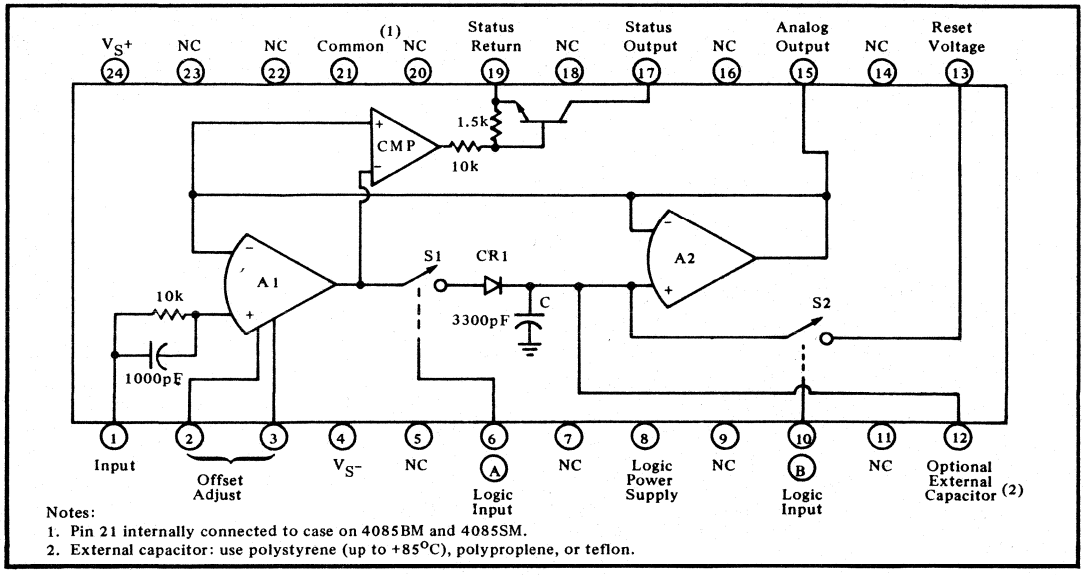
THEORY OF OPERATION

In the PEAK DETECT mode (S1 closed, S2 open), the analog output tracks the analog input until a peak value is reached. When the input voltage falls below the magnitude of the peak voltage, CR1 becomes reversed biased, and the feedback loop between A1 and A2 is broken. At this point, the status output transistor turns on and the magnitude of the peak voltage is held on the analog output. In the HOLD mode (S1 open, S2 open), the current charging path from the output of A1 to the capacitor is opened. The output voltage is equal to the voltage stored in the capacitor even though the input voltage may become larger than the peak voltage. In the RESET mode (S1 open, S2 closed), the voltage on the capacitor will charge to whatever voltage is applied to the RESET voltage input. If both S1 and S2 are closed at the same time, the output of A1 will be connected to the reset voltage input through a low impedance. This represents an illegal mode of operation, but will cause no damage to the unit.



Notes:
1. Pin 21 internally connected to case on 4085BM and 4085SM.
2. External capacitor: use polystyrene (up to +85°C), polypropelene, or teflon.

FIGURE 1. 4085 Functional Diagram and Pin Configuration.

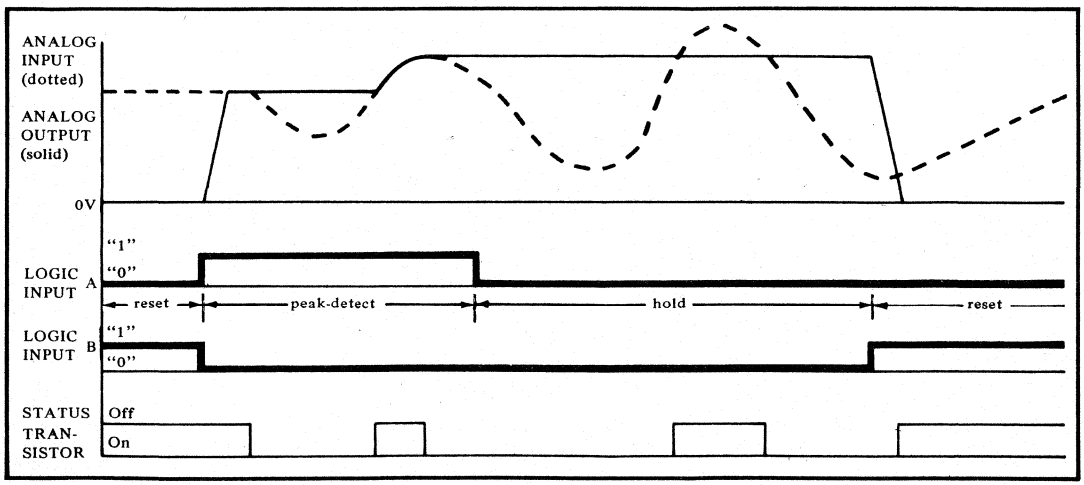


FIGURE 2. Timing Diagram For Peak-Detect Operation

ELECTRICAL SPECIFICATIONS

Specifications at T_A = +25°C and ±15VDC and +5VDC power supplies unless otherwise noted.

MODEL	4085 MIN	4085 TYP	4085 MAX	UNITS
ANALOG INPUT				
Signal Inputs				
Operating Range	±10	|V| -3		V
Absolute Maximum Range			±Supply	V
Input Offset Voltage (adjustable to zero)			2	mV
Input Offset Voltage Drift		15	50	µV/°C
Input Bias Current		15	50	pA
Input Resistance		1		GΩ
Input Capacitance		8		pF
DIGITAL INPUT				
Logic Levels				
Logic "1"	+2.4 at 50nA max			V
Logic "0"			+0.8 at 100µA max	V
Truth Table	Logic Input A		Logic Input B	
Peak Detect Mode	1		0	
Hold Mode	0		0	
Reset	0		1	
TRANSFER CHARACTERISTICS				
Voltage Gain		1.0		V/V
ACCURACY				
DC Voltage Gain Error			±0.01	% of FSR[3]
Dynamic Accuracy to 300Hz		±0.01	±0.02	% of FSR
100Hz			±0.01	% of FSR
Temperature Coefficient of Gain Error		±3		ppm/°C
Feedthrough			±0.05	% of Step
Droop (all units at T_A = +25°C)[5]			±0.06	mV/ms
T_A = +70°C, 4085KG			±0.5	mV/ms
T_A = +85°C, 4085BM			±1.2	mV/ms
T_A = +125°C, 4085SM			±12.0	mV/ms
Power Supply Sensitivity, $\pm V_S$			±0.005	%/% Supply Variation
Logic Supply			±0.005	%/% Supply Variation
DYNAMIC PERFORMANCE				
Acquisition Time (BM, SM)			500	µsec
(KG)			800	µsec
Slew Rate		0.5		V/µsec
Charge Offset[4]		0.5	1	mV
Status Delay at 500Hz		0.7	1	ms
at 100Hz		1.2	2	ms

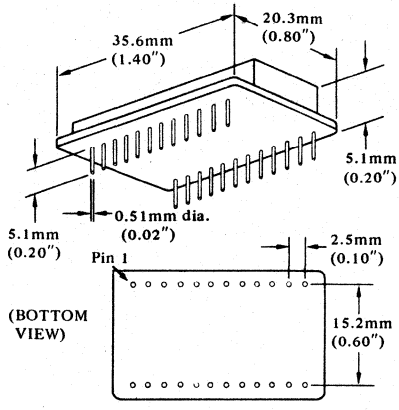
MODEL	4085 MIN	4085 TYP	4085 MAX	UNITS
ANALOG OUTPUT				
Voltage Range	±10	|V| -3		V
Output Current	5			mA
Output Resistance		0.2	0.5	Ω
Output Noise 10Hz to 100kHz		30		µV rms
Output Load Capacitance	50	100		pF
STATUS OUTPUT				
Collector-emitter Voltage			+30	V
Collector Current			20	mA
DC Current Gain	50	100		mA/mA
V_{BE}		0.65		V
RESET VOLTAGE				
Operating Range	±10	|V| -3		V
Absolute Maximum Range			±Supply	V
Discharge Current[1]	5		30	mA
POWER SUPPLY REQUIREMENTS				
Rated Voltage		±15		V
Operating Range	±8		±18	V
Current Drain (i_{out} = 0)			±20	mA
Rated Logic Supply Voltage[2]		+5.0 ±0.5		V
Logic Supply Current				
(Logic A & B high)		3.0 ±0.3		mA
(Logic A & B = 0V)		4.4 ±0.5		mA
TEMPERATURE RANGE				
Specification				
4085KG	0		+70	°C
4085BM	-25		+85	°C
4085SM	-55		+125	°C
Operating				
4085KG	-25		+85	°C
4085BM	-55		+90	°C
4085SM	-55		+125	°C
Storage				
4085KG	-30		+90	°C
4085BM	-60		+100	°C
4085SM	-60		+150	°C

Notes:

1. Any circuitry connected to the reset pin should be capable of sinking the desired discharge current of the internal 3300pF holding capacitor plus any external capacitor. The discharge current range is the current limit imposed by an internal FET switch. It does not imply that the I_{DSS} of external circuitry must be designed to limit current to this range.
2. Logic Supply, pin 8, may be connected to higher supply voltages for operation with MOS or CMOS logic. Refer to OPERATING INSTRUCTIONS.
3. FSR = Full Scale Range, 20V for the 4085.
4. Charge Offset is the charge transferred from the holding capacitor when the 4085 is switched to the hold mode.
5. Equation for droop: $\text{Droop (mV/ms)} = \frac{100\text{pA} \times 2^{\left(\frac{T - 25^{\circ}C}{11}\right)}}{3300\text{pF} + C_{ext}\,(\text{pF})}$

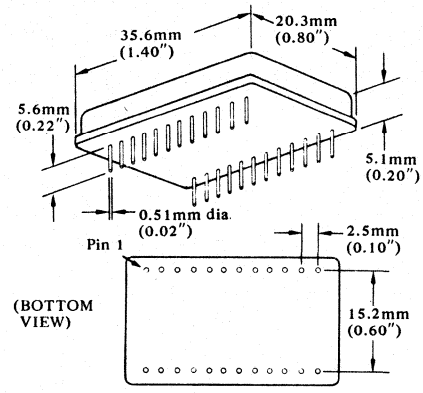
MECHANICAL SPECIFICATIONS

CERAMIC PACKAGE 4085KG



CASE: Black Ceramic (alumina)
Mating Connector 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to Mil-Std-883, method 1014. Gross leak (condition C, step 1, Fluorocarbon).

METAL PACKAGE 4085BM, 4085SM



CASE: Kovar, Gold or Nickel Plated
Mating Connector 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to Mil-Std-883, method 1014. Gross leak (condition C, step 1, Fluorocarbon) Fine leak (condition A, Helium, 5 x 10^{-7} cc/sec).

TYPICAL PERFORMANCE CURVES

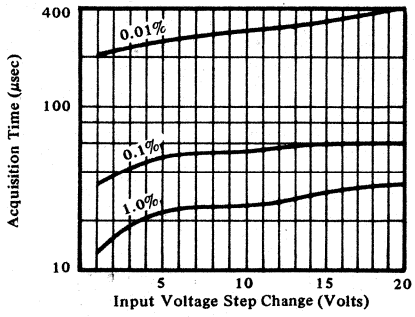


FIGURE 3. Acquisition Time

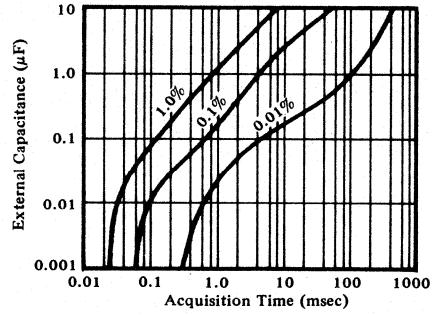


FIGURE 4. Acquisition Time

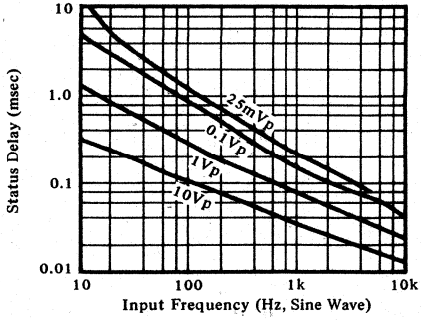


FIGURE 5. Status Output Delay

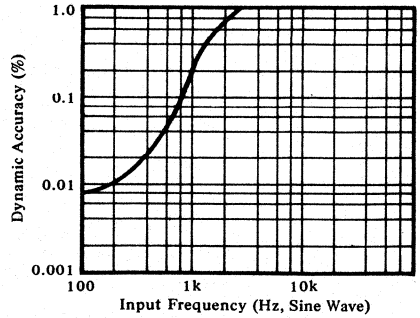


FIGURE 6. Dynamic Accuracy

OPERATING INSTRUCTIONS

OFFSET VOLTAGE ADJUSTMENT

The ±2mV input offset voltage of the 4085 may be nulled to zero by using the circuit shown in Figure 7. With the 4085 in the PEAK DETECT mode (logic input A = "1", logic input B = "0") apply zero volts to pin 1. Adjust the potentiometer until the output voltage is zero volts. Disconnect pin 12 after adjustment is made.

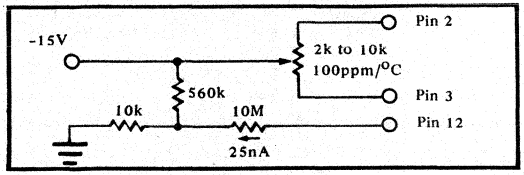


FIGURE 7. Offset Adjust Circuit

POWER SUPPLY CONSIDERATIONS

The 4085 will operate as specified with power supplies from ±8VDC to ±18VDC. To minimize noise pickup, the supply inputs should be decoupled with 1μF tantalum capacitors located physically close to the unit.

DIGITAL INPUTS AND LOGIC SUPPLY

The digital inputs may be driven with TTL or CMOS logic. Pin 8 should be tied to the logic supply. The logic supply voltage (V_L) may also be provided by connecting pin 8 through a resistor of value R(kohms) = 1.67 (V_S - V_L)/V_L to the +V_S supply ($V_S \geq V_L$). The logic threshold voltage is equal to 0.4 V_L - 0.7 volts.

INPUT FREQUENCY BANDWIDTH LIMITING

It is recommended that the input bandwidth be limited as much as possible by an RC section such as that shown in Figure 8. This is to limit noise spikes at the input that may cause erroneous readings. If detecting large pulse heights, a 5 μsecond time constant should be used. This will not degrade acquisition time or tracking accuracy for frequencies up to 500 Hz. For input frequencies greater than 500 Hz, a smaller time constant may be used.

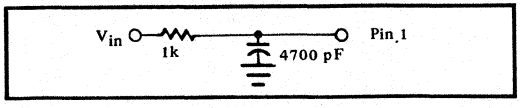


FIGURE 8. Input Bandwidth Limiting

STATUS OUTPUT CHARACTERISTICS

The open-collector, open-emitter output transistor is a small signal, medium speed switching transistor similar to a 2N2222. To facilitate driving a variety of devices, the configuration of the status output has been left to the user's discretion.

The internal comparator shown in the block diagram (Figure 1) has an output characteristic as follows. Input signal track: $Z_{out} \approx \infty$; peak hold: V_{out} = +V_S - 0.5 volts. Several configurations are illustrated in Figures 9 through 11. "Inverting" means logic "0" = peak has been detected, "Noninverting" means logic "1" = peak has been detected.

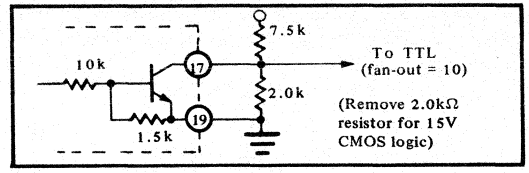


FIGURE 9. Inverting TTL (CMOS) STATUS Output.

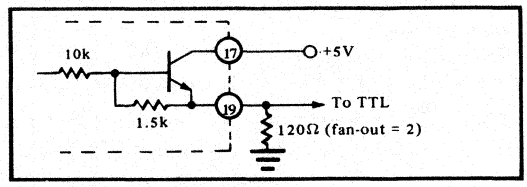


FIGURE 10. Noninverting TTL STATUS Output.

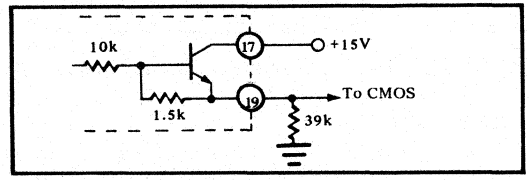


FIGURE 11. Noninverting CMOS STATUS Output

DESIGNING IN HYSTERESIS

It may be desirable in some situations to have hysteresis in the circuit such that small peaks will not be detected, eliminating jitter in the STATUS output. This is possible through external components connected as shown in Figure 12. After a peak is detected, the input voltage must be slightly greater (determined by R1/R2) than the previous peak to cause the output to resume tracking the input. This hysteresis voltage is expressed by:

$$V_H = \frac{(V_{in} - V_E - 0.9V)\ R1}{R1 + R2}$$

The emitter voltage of the status transistor should be tied to a voltage sufficiently lower than the lowest expected peak to allow proper operation.

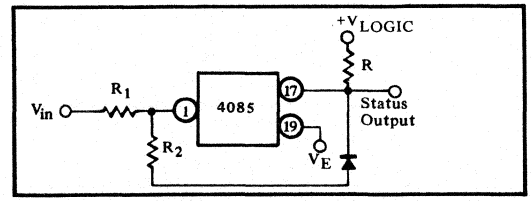


FIGURE 12. Hysteresis

APPLICATIONS

PEAK CATCHER

This circuit detects and holds the first peak it encounters. After the first peak is detected, it automatically is switched to the hold mode. To reset the circuit for catching another peak, a 10 μsec or longer positive logic pulse should occur at the "RELEASE" input. This will reset the peak detector to the desired voltage and put it in the peak-detect mode.

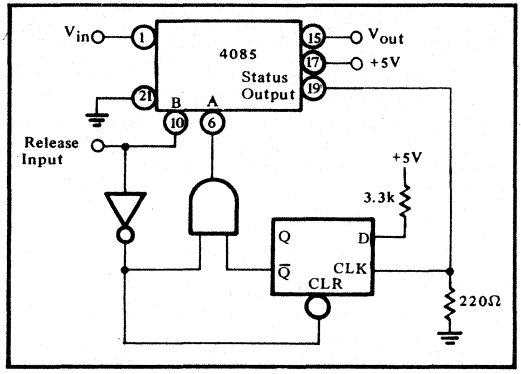


FIGURE 13. Peak Catcher

NO-RIPPLE, FAST SETTLING RMS-DC CONVERTER

If a waveform is known, the RMS value of the signal may be computed from the peak value. In this circuit, the RMS value is computed by the output amplifier from the peak value held by the 4085. The output in the circuit shown is updated manually. It may be updated automatically by replacing the switch circuit with an oscillator plus timing logic.

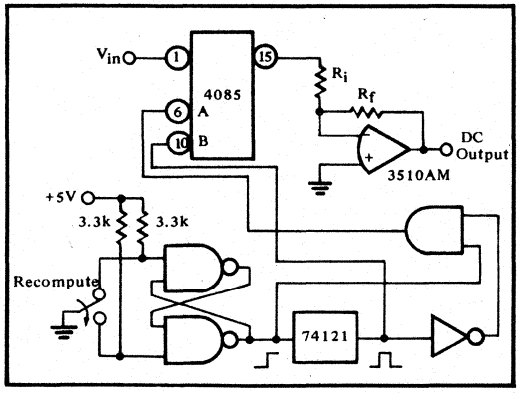


FIGURE 14. RMS-DC Converter

INTERFACING TO A/D CONVERTER

Interfacing to an A/D converter is straightforward. The gating of the A/D converter command allows a conversion only if a peak has been detected and permits completion of each conversion. If a peak occurs while the A/D is converting, it will not be detected.

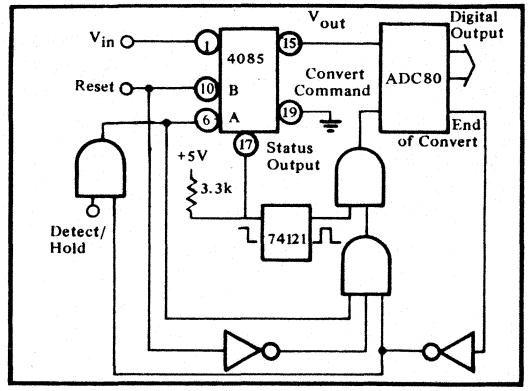


FIGURE 15. A/D Converter Interface

PEAK-TO-PEAK DETECTOR

Figure 16 shows a circuit that will display the peak-to-peak voltage of an input waveform. The STATUS output indicates that both positive and negative peaks have been detected and that the output is valid. The resistors around A3 should be matched to insure good common-mode rejection.

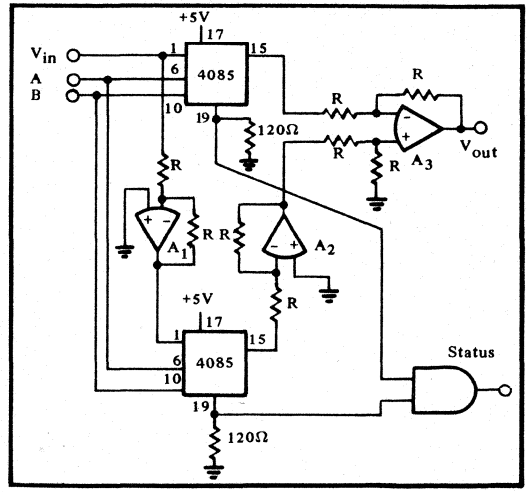
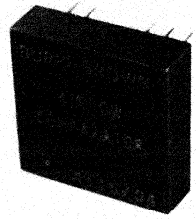


FIGURE 16. Peak-to-Peak Detector

BURR-BROWN



4115/04

WINDOW COMPARATOR

FEATURES

- ADJUSTABLE LIMITS FOR "HIGH", "LOW", AND "GO"
- UP TO 200mA LOAD CAPABILITY (each output)
- INPUT PROTECTION

APPLICATIONS

- PRODUCTION LINE TESTING
- TEMPERATURE CONTROLS
- INDUSTRIAL ALARMS
- LEVEL DETECTORS/CONTROLS

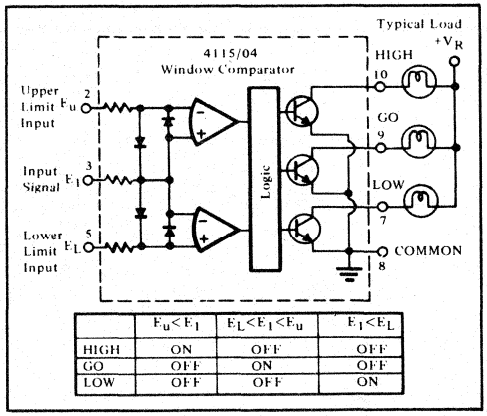
DESCRIPTION

Model 4115/04 is a hybrid IC window comparator in a double width DIP. The unit has three inputs - one for a voltage that sets the upper limit, another for a voltage that sets the lower limit, and a signal input. There are three mutually exclusive outputs - HIGH, LOW and GO. When an output is ON it will sink up to 200mA of current. This input diode protected device is designed to work with input voltages of up to ±10V, and will not be harmed by voltages to ±15V. The 4115/04 will drive a variety of loads including lamps, relays, MOS circuitry, and high noise immunity logic as well as DTL and TTL devices.

INSTALLATION

Separate connections should be made from each power supply common (+15VDC, -15VDC and V_R) to the 4115/04 common (pin 8).

To avoid unwanted pickup or chattering it may be necessary to include bypass capacitors from the ±15V supply pins (13 and 14) to the module common pin (8).



	$E_u<E_I$	$E_L<E_I<E_u$	$E_I<E_L$
HIGH	ON	OFF	OFF
GO	OFF	ON	OFF
LOW	OFF	OFF	ON

Model 4115/04 Transfer Characteristics.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-400

Printed in U.S.A. July, 1978

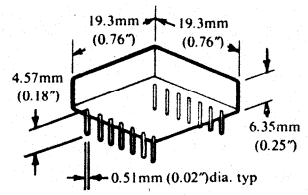
ELECTRICAL SPECIFICATIONS

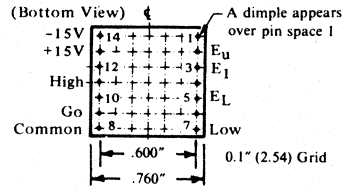
Typical performance at 25°C and with rated supply unless otherwise noted.

MODEL	4115 04	Units
INPUT		
All Inputs	±10V into 6kΩ (min)	
Maximum Safe Input	±15	V
ACCURACY		
D.C. Resolution (min)	±0.2	mV
Voltage Offset (referred to input)		
at 25°C (max)	±2	mV
vs Temperature (max)	±30	μV °C
Over Temperature Range (max)	±7	mV
vs Power Supply	±50	μV V
Switching Speed		
Total Switching Time at 30mV		
Overdrive	300	μsec
OUTPUT		
Impedance to COMMON from all Outputs		
OFF state	> 1	MΩ
ON state	3	Ω
Load Supply Voltage (V_R)	0 to +30	V
Load Current		
Steady State	+200	mA
Transient (absolute maximum)		
1 Second Duration	+400	mA
Saturation Voltage (V_{C1}) (max)		
at 200mA	0.7	V
TEMPERATURE RANGE		
Rated Specifications	-25 to +85	°C
Derated Performance	-40 to +85	°C
Storage	-55 to +100	°C
POWER SUPPLY REQUIREMENTS		
Rated Supply Voltage	±15	VDC
Derated Performance	-12 to ±18	VDC
Quiescent Drain (max)	±15	mA

To achieve best results use stable quiet reference sources and drive signal input from low impedance source. Noise and drift in input sources readily masks the inherently high resolution of the device.

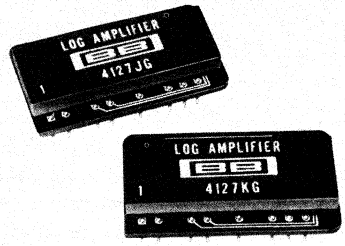
MECHANICAL SPECIFICATIONS





WEIGHT: 0.24 oz. (6.80 grams)
MATERIAL: Black Exoxy
PIN: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
CONNECTOR: Fits any commercial dual-in-line connector.

BURR-BROWN



4127

LOGARITHMIC AMPLIFIER

FEATURES

- ACCEPTS INPUT VOLTAGES OR CURRENTS OF EITHER POLARITY
- WIDE INPUT DYNAMIC RANGE
  - 6 Decades of current
  - 4 Decades of voltage
- VERSATILE
  - Log, antilog, and log ratio capability
- SMALL SIZE
  - Doublewide DIP
- LOW COST

DESCRIPTION

Packaged in a ceramic doublewide DIP, the 4127 is the first hybrid logarithmic amplifier that accepts input signals of either polarity from current or voltage sources. A special purpose monolithic chip, developed specifically for logarithmic conversions, functions accurately for up to six decades of input current and four decades of input voltage. In addition, a newly-developed current inverter and a precise internal reference allow pin programming of the 4127 as a logarithmic, log ratio, or antilog amplifier.

To further increase its versatility and reduce your system cost the 4127 has an uncommitted operational amplifier in its package that can be used as a buffer, inverter, filter, or gain element.

The 4127 is available with initial accuracies (log conformity) of 0.5% and 1.0%, and operates over an ambient temperature range of -10°C to +70°C.

With its versatility and high performance, the 4127 has many applications in signal compression, transducer linearization, and phototube buffering. Manufacturers of medical equipment, analytical instruments, and process control instrumentation will find the 4127 a low-cost solution to many signal processing problems.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-346B Printed in U.S.A. July, 1978

GENERAL DESCRIPTION

The 4127 is a complete logarithmic amplifier that can be pin-programmed to accept input currents or voltages of either polarity. By making use of the internal current inverter, reference current generator, log ratio element, and uncommitted op amp, you can generate a variety of logarithmic functions, including the log ratio of two signals, the logarithm of an input signal, or the antilog of an input signal. The unique FET-input current-inverting element removes the polarity limitations present in most conventional log amplifiers.

Utilizing the inherent exponential characteristics of transistor functions, the 4127 calculates accurate log functions for input currents from 1 nA to 1 mA, and input voltages from 1 mV to 10 V. Carefully-matched monolithic quad transistors and temperature sensitive gain elements are used to produce a log amplifier with excellent temperature characteristics.

THEORY OF OPERATION

A functional diagram of the 4127 circuit is shown in Figure 1. Besides the basic log amplifier, the 4127 contains a separate internal current source, a current inverter, and an uncommitted operational amplifier. The current inverter accurately converts negative input current to a positive current of equal magnitude.

The 4127 is capable of accurately logging input current over a 120dB range, but to use this full range good shielding practice must be followed. A current source input is, by definition, a high impedance source, and is therefore subject to electrostatic pickups.

The input op amps A_1 and A_3 have FET input stages for low noise and very low input bias current. The op amp A_1 will make the collector current of Q_1 equal to the signal input current I_S, and the collector current of Q_2 will be the reference input current I_R.

From the semiconductor junction characteristics, the base-to-emitter voltage will be

$$V_{BE} \approx \frac{m\,K\,T}{q} \ln \frac{I_C}{I_L}$$, where I_C = Collector current
I_L = Reverse saturation current
q, m, K = Constants
T = Absolute temperature

$$\text{So } E_1 = -\frac{m\,K\,T_1}{q} \ln \frac{I_S}{I_{L1}} \quad \text{and } E_2 - E_1 = \frac{m\,K\,T_2}{q} \ln \frac{I_R}{I_{L2}}$$

If the transistors Q_1 and Q_2 are at the same temperature and have matched characteristics then

$$E_2 = \frac{m\,K\,T}{q}\left[\ln \frac{I_R}{I_L} - \ln \frac{I_S}{I_L}\right]$$

$$E_2 = \frac{-m\,K\,T}{q} \ln \frac{I_S}{I_R}$$

The output op amp A_2 provides a voltage gain of approximately $(R_T + R_2)/R_T$, and the value of m K T/q is about 26mV at room temperature. Since resistor R_T varies with temperature to compensate for gain drift, the output voltage E_o expressed as a log will be

$$E_o = -A \log_{10} \frac{I_S}{I_R}$$

$$\text{where } A \approx \frac{R_T + R_2}{R_T}\ (26\text{ mV})\ \frac{1}{0.434},\ R_T \approx 520\Omega$$

The external resistor R_1 sets the reference current I_R and resistor R_2 sets the scale-factor "A". The two resistors must be trimmed to the desired values, but graphs in Figures 2 and 3 show the approximate relationships.

Figures 4 and 5 illustrate the relationship between the input current I_S and the output voltage E_o in terms of the externally adjusted parameters I_R and "A". This relationship is, of course, restricted to values of I_S between 1 nA to 1 mA and output voltages of less than ±10V.

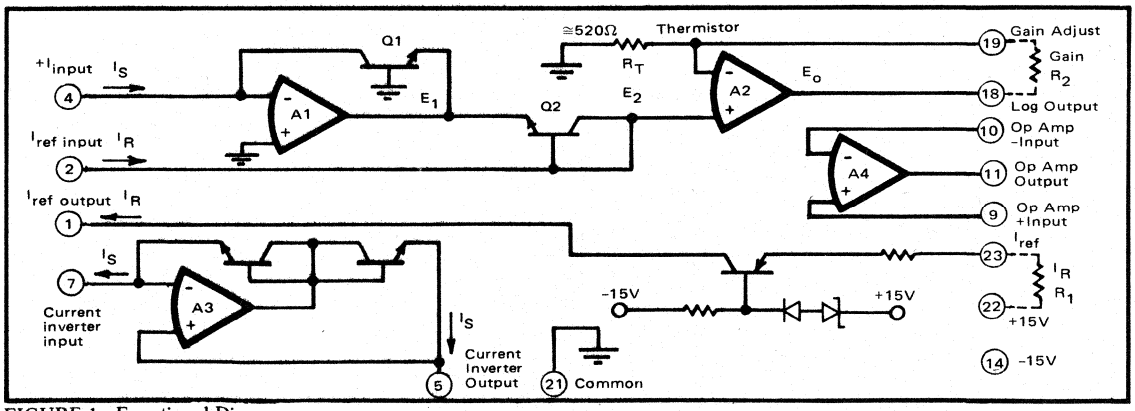


FIGURE 1. Functional Diagram.

SPECIFICATIONS

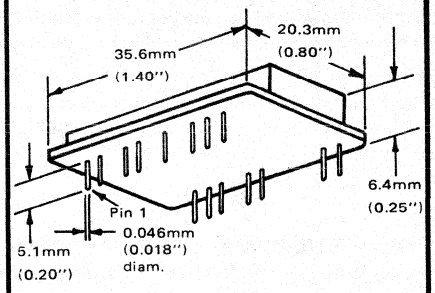
Typical specifications at +25°C with rated supplies unless otherwise specified.

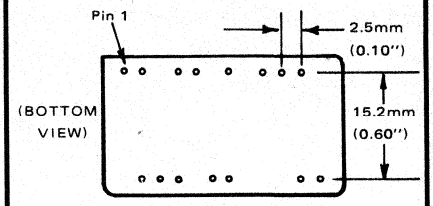
ELECTRICAL

	4127KG	4127JG
ACCURACY, (1) % of FSR		
Current Source Input: 1nA to 1mA	0.5% max	1% max
Voltage Input: 1mV to 10V	0.5% max	1% max
INPUT		
Current Source Input, Pin 4	+1nA to +1mA	
Pin 7	-1nA to -1mA	
Reference Current Input, Pin 2	+1μA to +1mA	
Absolute Maximum Inputs	±10mA or ±Supply Volts	
OUTPUT		
Voltage	±10V	
Current	±5mA	
Impedance	10 Ω	
FREQUENCY RESPONSE		
-3dB Small Signal at Current Input		
of 100μA	90kHz	
10μA	50kHz	
1μA	5kHz	
100nA	250Hz	
10nA	80Hz	
Step Response to within ±1% of Final Value (I_R = 1μA, A = 5)	10msec	
STABILITY		
Scale Factor Drift (Δ A/°C)	±0.0005A/°C	
Reference Current Drift (Δ I_R/°C)	±0.001 I_R/°C for $I_R \geq$ 1μA	
	±0.003 I_R/°C for 400nA < I_R < 1μA	
Input Offset Current Drift (Δ I_S/°C)	10pA at +25°C, Doubles Every 10°C	
Input Offset Voltage Drift	±10μV/°C	
Accuracy vs. Supply Variation		
Reference Current	±0.001 I_R/V	
Input Offset Voltage	±300μ V/V	
Input Noise - Current Input	1pA RMS, 10Hz to 10kHz	
Voltage Input	10μV RMS, 10Hz to 10kHz	
UNCOMMITTED OP AMP CHARACTERISTICS		
Input Offset Voltage	5mV	
Input Bias Current	40nA	
Input Impedance	1MΩ	
Large Signal Voltage Gain	85dB	
Output Current	5mA	
TEMPERATURE RANGE		
Specification	0°C to +60°C	
Operating	-10°C to +70°C	
Storage	-55°C to +125°C	
POWER SUPPLY REQUIREMENTS		
Rated Supply Voltages	±15VDC	
Supply Voltage Range	±14VDC to ±16VDC	
Supply Current Drain		
at Quiescent (max.)	±20mA	
at Full Load (max.)	±26mA	

(1) Log conformity at 25°C

MECHANICAL





CASE: Black Ceramic
Mating Connector 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
WEIGHT: 56 grams, (2 oz.)

PIN DESIGNATIONS

1. I_{REF} Output
2. I_{REF} Input
3. No Pin Present
4. +I Input
5. Current Inverter Output
6. No Pin Present
7. Current inverter Input
8. No Pin Present
9. Op Amp +Input
10. Op Amp -Input
11. Op Amp Output
12. No Pin Present
13. Make No Connection
14. Negative Supply
15. No Pin Present
16. No Pin Present
17. No Pin Present
18. Log Output
19. Gain Adjust
20. No Pin Present
21. Common
22. Positive Supply
23. I_{REF} Bias
24. No Pin Present

TYPICAL PERFORMANCE CURVES

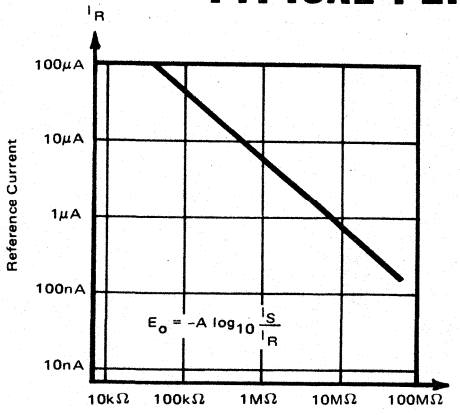


FIGURE 2. Relationship of Reference Current I_R and external resistor R_1.

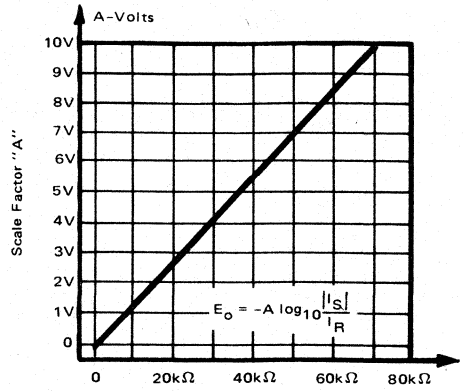


FIGURE 3. Relationship of scale factor "A" to gain-setting resistor R_2.

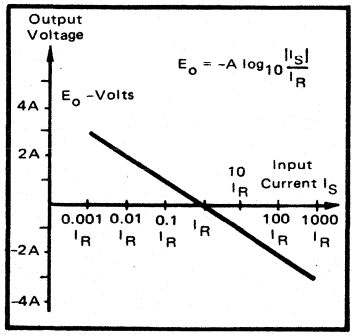


FIGURE 4. Log Relationship of $\frac{|I_S|}{I_R}$ and output voltage in terms of "A".

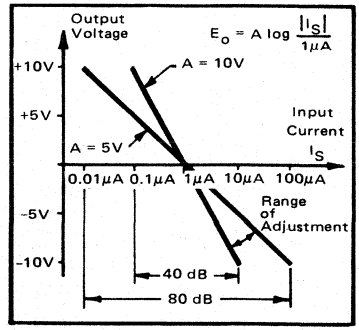


FIGURE 5. Relationship of $\frac{|I_S|}{I_R}$ to output voltage for I_R = 1μA and A = 5V and 10V.

DISCUSSION OF SPECIFICATIONS

ACCURACY

The deviation from the ideal output voltage defined as a percent of the full scale output voltage.

INPUT/OUTPUT RANGE

The log relationships of $-A \log \frac{I_S}{I_R}$ and $-A \log \frac{E_S}{I_R R}$ are subject to the constraints specified. The 4127 can be operated with inputs lower than those given, but the accuracy will be degraded.

FREQUENCY RESPONSE

The small-signal frequency response varies considerably with signal level and scaling, so the frequency response is specified under several different operating conditions.

STABILITY

The use of a monolithic transistor quad and low-drift op amps minimizes drift, but some drift remains in the scale-factor, reference current, and input offset. Input offset consists of a bias current plus the op amp input voltage offset divided by the signal source resistance. Also, there is some slight drift in conformity to the log function and in output amplifier offset, but this is generally negligible.

SCALE FACTOR A AND REFERENCE CURRENT I_R.

Refer to CHOOSING THE OPTIMUM SCALE FACTOR AND REFERENCE CURRENT.

CHOOSING THE OPTIMUM SCALE FACTOR AND REFERENCE CURRENT

To minimize the effects of output offset and noise, it is usually best to use the full ±10V output range. Once an output range of ±10V has been chosen, then "A" and I_R can be determined from the min/max of the input current I_S.

$$E_O = -A \log \frac{I_S}{I_R}, \text{ where } I_{min} < I_S < I_{max}$$

The output range of ±10V for an input range of I_{min} to I_{max} means that

$$+10 = -A \log \frac{I_{min}}{I_R} \text{ and } -10 = -A \log \frac{I_{max}}{I_R}$$

Adding these two equations together

$$\log \frac{I_{max} I_{min}}{I_R^2} = 0, \text{ or } I_R = \sqrt{I_{max} I_{min}}$$

The value for A can be found from:

$$10 = A \log \frac{I_{max}}{\sqrt{I_{max}\, I_{min}}}$$

In terms of the input current range for I_S, the values for I_R and A that will provide a full ±10V output swing are:

$$I_R = \sqrt{I_{max} I_{min}} \text{ and } A = \frac{10}{\log \frac{I_{max}}{I_R}}$$

Example: Assume that I_{min} is +10nA and I_{max} is +100μA.

This is an 80 dB range.

$$I_R = \sqrt{I_{max} I_{min}} = \sqrt{(10^{-4})\ (10^{-8})} = 10^{-6}, \text{ or } 1\mu A.$$

$$\frac{I_{max}}{I_R} = \frac{10^{-4}}{10^{-6}} = 100$$

$$\log \frac{I_{max}}{I_R} = 2 \quad \text{So } A = 5$$

For an I_R of 1μA and A of 5,

$$E_O = -5 \log \frac{I_S}{1\mu A}$$

*Single resistor recommended. Voltage divider network difficult to use due to amplifier offset voltage. RF500-108, 1k meg resistor available from Burr-Brown.

CONNECTION DIAGRAMS

Transfer function is $E_O = -A \log \frac{I_1}{I_R}$ where I_1 is a positive input current and I_R is the resistor-programmed internal reference current.

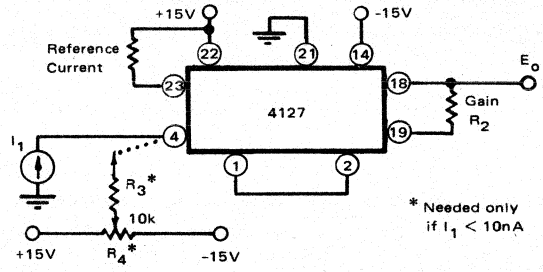


FIGURE 6.

ADJUSTMENT PROCEDURE

1. Refer to top of page for choosing optimum scale factor and reference current.
2. Apply $I_1 = I_R$, adjust R_1 such that $E_O = 0$.
3. Apply $I_1 = I_{max}$, adjust R_2 for the proper output voltage.
4. Repeat steps 2 and 3 if necessary.
5. Ignore this step if $I_{1min} \geq 10nA$. Otherwise, apply $I_1 = 1nA$, make $R_3 = 1k\Omega$* and adjust R_4 for the proper output voltage.

Transfer function is $E_O = -A \log \frac{|I_1|}{I_R}$ where I_1 is a negative input current and I_R is the resistor-programmed internal reference current.

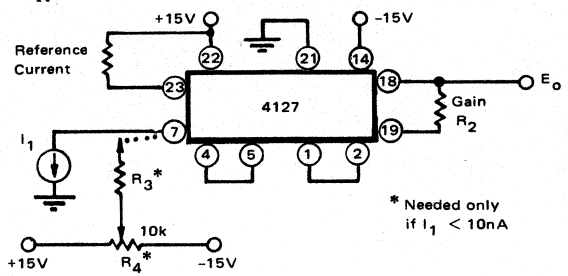


FIGURE 7.

ADJUSTMENT PROCEDURE

1. Refer to top of page for choosing optimum scale factor and reference current.
2. Apply $|I_1| = I_R$ adjust R_1 such that $E_O = 0$.
3. Apply $|I_1| = I_{max}$, adjust R_2 for the proper output voltage.
4. Repeat steps 2 and 3 if necessary.
5. Ignore this step if $|I_{1min}| \geq 10nA$. Otherwise, apply $|I_1| = 1nA$, make $R_3 = 1k\Omega$* and adjust R_4 for the proper output voltage.

CONNECTION DIAGRAMS

Transfer function is $E_0 = -A \log \frac{E_1}{R_4 I_R}$, where E_1 is a positive input voltage and I_R is the resistor-programmed internal reference current.

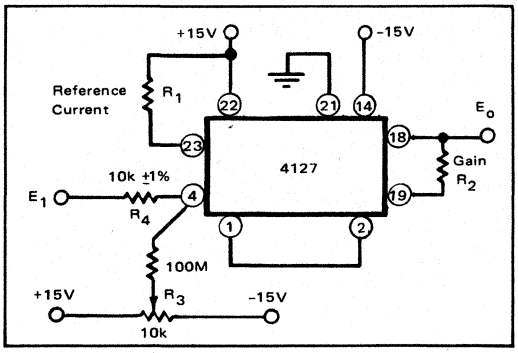


FIGURE 8.

ADJUSTMENT PROCEDURE

1. Refer to CHOOSING OPTIMUM SCALE FACTOR AND REFERENCE CURRENT.
2. Apply $E_1 = I_R$ (10kΩ), adjust R_1 such that $E_0 = 0$.
3. Apply $E_1 = E_{max}$, adjust R_2 for the proper output voltage.
4. Apply $E_1 = E_{min}$, adjust R_3 for the proper output.
5. Repeat steps 2 through 4 if necessary.

Transfer function is $E_0 = -A \log \frac{|E_1|}{R_4 I_R}$, where E_1 is a negative input voltage and I_R is the resistor-programmed internal reference current.

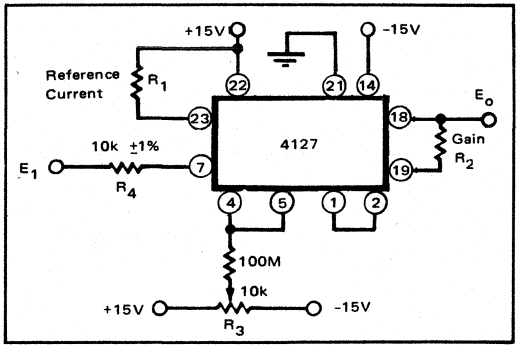


FIGURE 9.

ADJUSTMENT PROCEDURE

1. Refer to CHOOSING OPTIMUM SCALE FACTOR AND REFERENCE CURRENT.
2. Apply $|E_1| = I_R$ (10kΩ), adjust R_1 such that $E_0 = 0$.
3. Apply $|E_1| = E_{max}$, adjust R_2 for the proper output voltage.
4. Apply $|E_1| = E_{min}$, adjust R_3 for the proper output.
5. Repeat steps 2 through 4 if necessary.

Transfer function is $E_0 = -A \log \frac{|I_1|}{|I_2|}$ with I_1 and I_2 negative; $|I_1| \geq 1nA, |I_2| \geq 1\mu A$.

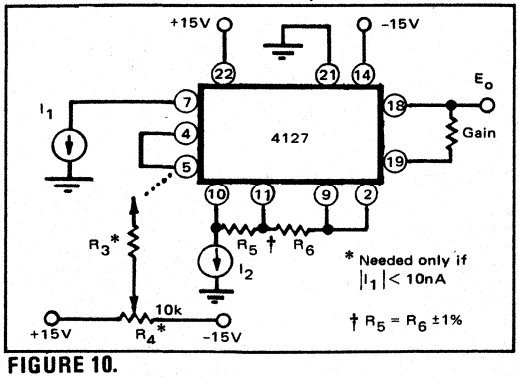


FIGURE 10.

ADJUSTMENT PROCEDURE

1. Refer to CHOOSING OPTIMUM SCALE FACTOR AND REFERENCE CURRENT.
2. No further adjustment is necessary if I_1 min ≥ 10nA, otherwise connect the R_3 and R_4 network, with R_4 = 10k and $R_3 = 10^9\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of ±5mV, it is not practical to use a T - network to replace R_3.

Transfer function is $E_0 = -A \log \frac{|I_1|}{I_2}$ with I_1 negative, I_2 positive; $|I_1| \geq 1nA$, $I_2 \geq 1\mu A$.

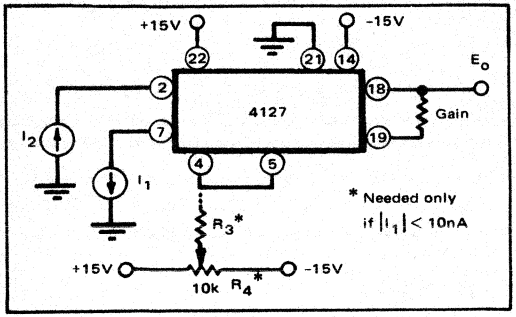


FIGURE 11.

ADJUSTMENT PROCEDURE

1. Refer to CHOOSING OPTIMUM SCALE FACTOR AND REFERENCE CURRENT.
2. No further adjustment is necessary if $|I_1|$min $\geq$ 10nA, otherwise connect the R_3 and R_4 network, with R_4 = 10k and $R_3 = 10^9\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of $\pm$5mV, it is not practical to use a T - network to replace R_3.

Transfer function is $E_0 = -A \log \frac{I_1}{I_2}$ with I_1 and I_2 positive; $I_1 \geq 1nA$, $I_2 \geq 1\mu A$.

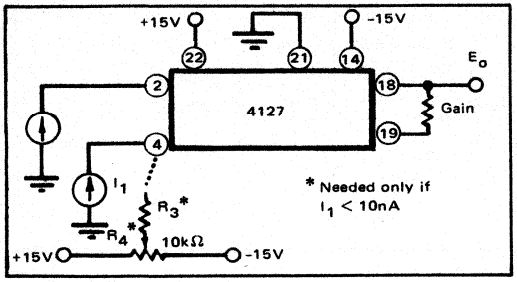


FIGURE 12.

ADJUSTMENT PROCEDURE

1. Refer to CHOOSING OPTIMUM SCALE FACTOR AND REFERENCE CURRENT.
2. No further adjustment is necessary if I_1 min $\geq$ 10nA, otherwise connect the R_3 and R_4 network, with R_4 = 10k and $R_3 = 10^9\Omega$. Adjust R4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of $\pm$5mV, it is not practical to use a T - network to replace R_3.

ANTILOG OPERATION

The 4127 can also perform the antilog function. The output is connected through a resistor R_0 into the current input, pin 4. The input signal is connected through a gain resistor to pin 19 as shown in Figure 13.

These connections form an implicit loop for computing the antilog function. From the block diagram of Figure 1, the voltage at the inverting input of the output amplifier A2 must equal E_2, so

$$E_2 \approx \frac{R_T}{R_T + R_2} E_S, \quad R_T \cong 520\Omega$$

Since the output is connected through R_0 to pin 4, the current I_S will equal E_0/R_0 and E_2 will be

$$E_2 = -\frac{m K T}{q} \ln \frac{E_o}{R_o I_R}$$

Combining expressions for E_2 gives the relationship

$$\frac{R_T}{R_T + R_2} E_S = -\frac{m K T}{q} \ln \frac{E_o}{R_o I_R}$$

$$-\frac{E_S}{A} = \log \frac{E_o}{R_o I_R}$$

where

$$A \approx \frac{R_T + R_2}{R_T} (26mV) \frac{1}{0.434}$$

$$E_o = R_o I_R \text{ Antilog} - \frac{E_S}{A}$$

Setting R_0 and I_R will set the scale factor. For example, an R_0 of 1MΩ and I_R of 1μA will give a scale factor of unity and

$$E_o = \text{Antilog} - \frac{E_S}{A}$$

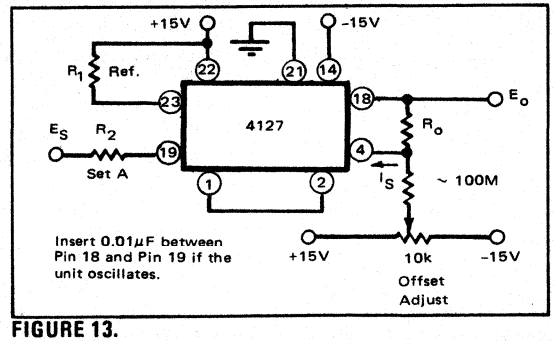
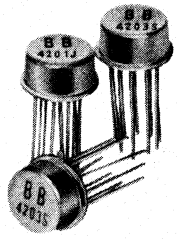


FIGURE 13.

BURR-BROWN



4203

Integrated Circuit MULTIPLIER-DIVIDER

FEATURES

- **LASER-TRIMMED**
  Requires no adjustment
- **GUARANTEED ACCURACY - 1% or 2%**
- **SELF-CONTAINED**
  No Additional Amplifiers
- **FAST SLEWING - 25V/μsec**
- **SMALL PACKAGE - TO-100**

DESCRIPTION

Burr-Browm Model 4203 is an integrated circuit multiplier-divider designed for general-purpose usage. In addition to four-quadrant multiplication it also performs division and square-rooting of analog signals, requiring no additional amplifiers in performing the above functions. The 4203 is laser-trimmed prior to final packaging and is guaranteed to its rated accuracy with no external components. This is a distinct advantage from the standpoints of cost and reliability.

This multiplier contains its own zener-regulated reference and, as a result, is much less sensitive to supply voltage variation than were earlier IC multipliers. The fast (25V/μsec) slew rate and 1MHz bandwidth are key performance factors for applications where delay phase shift must be minimized. Harmonic distortion of the 4203 remains low for frequencies well above 100kHz, an important asset in modulation applications.

Other desirable features of the 4203 are hermetic TO-100 package (10-pin version of TO-99) and wide temperature range of operation. The 4203S is specified for operation over the full Mil temperature range.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-292E

Printed in U.S.A. July, 1978

SPECIFICATIONS

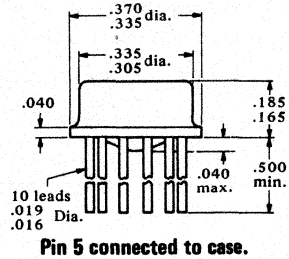
Typical performance at +25°C with rated power supplies unless otherwise noted.
Per cent specifications refer to % of full scale (10V).

ELECTRICAL

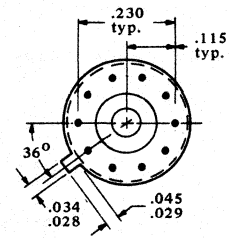
MODEL	4203J	4203K	4203S
OUTPUT FUNCTION	XY/10		
TOTAL ERROR*			
Internal trim	2%, max.	1%, max.	1%, max.
External trim	1%	0.6%	0.6%
vs. Temperature	0.04%/°C		
vs. Supply	0.2%/%		
INDIVIDUAL ERRORS			
Output Offset @ 25°C (X=Y=0)	20 mV	20 mV	20 mV, max.
vs. Temperature (Operating Range)	0.4 mV/°C		
vs. Supply	10 mV/%		
Scale Factor Error	1%	0.6%	0.6%
vs. Temperature (Operating Range)	0.04%/°C		
vs. Supply	0.1%/%		
Non-Linearity			
X (X=20 V p-p, Y=±10VDC)	0.8%	0.5%	0.5%
Y (Y=20 V p-p, X=±10VDC)	0.2%	0.2%	0.2%
Feedthrough @ 50 Hz			
X=0, Y=20V p-p (Internal Trim)	50 mV p-p	50 mV p-p	
(External Trim)	20 mV p-p		
vs. Temperature	1 mV p-p/°C		
Y=0, X=20V p-p (Internal Trim)	50 mV p-p	50 mV p-p	
(External Trim)	20 mV p-p		
vs. Temperature	2 mV p-p/°C		
AC PERFORMANCE			
Slew Rate	25 V/μsec		
-3 dB Small Signal Bandwidth	1 MHz		
1% Amplitude Error	40 kHz		
1% Vector Error (0.57° phase shift)	10 kHz		
Settling Time (2% of final value, 20V, step)	1 μsec		
Overload Recovery Time	3 μsec		
OUTPUT NOISE (X=Y=0)			
10 kHz to 10 MHz	3 mV rms		
10 Hz to 10 kHz	600 μV rms		
INPUT CHARACTERISTICS			
Input Voltage Range			
Rated Operation	±10 V		
Absolute Max.	±15 V		
Input Impedance, X	10 MΩ	10 MΩ	10 MΩ
Y	10 MΩ	10 MΩ	10 MΩ
Z	36 KΩ	36 KΩ	36 KΩ
OUTPUT CHARACTERISTICS			
Rated Output	±10 V @ ±5 mA		
Output Impedance	1 Ω		
POWER SUPPLY REQUIREMENTS			
Rated Voltage	±15 VDC		
Operating Range	±12 VDC to ±18 VDC		
Quiescent Current	±4 mA		
TEMPERATURE RANGE			
Operating, Rated Performance	0°C to 70°C		-55° to +125°C
Storage	-65°C to +150°C		

* Total error is a tested maximum at +25°C and represents the maximum allowed value for the sum of the individual errors.

TO-100

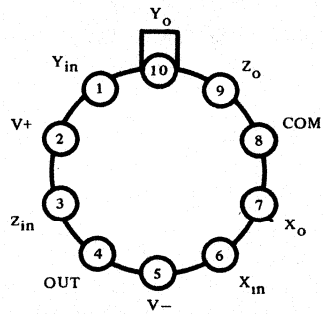


Pin 5 connected to case.



(BOTTOM VIEW)

CONNECTION DIAGRAM



(TOP VIEW)

MULTI. DIV.

TYPICAL PERFORMANCE CURVES

Typical Performance @ 25°C and ±15 VDC

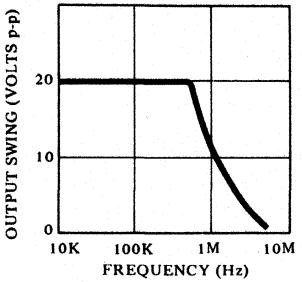


FIGURE 1. Large Signal Frequency Response.

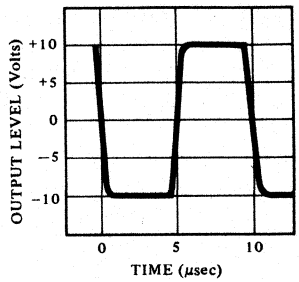


FIGURE 2. Step Response

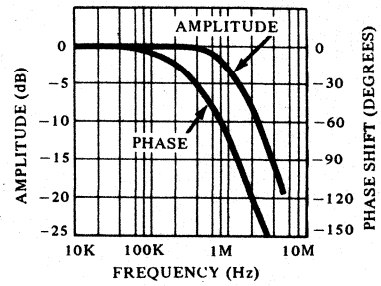


FIGURE 3. Small Signal Frequency Response.

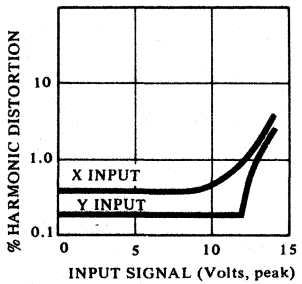


FIGURE 4. Output Distortion vs. Peak Input Signal.

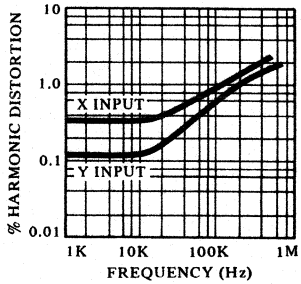


FIGURE 5. Output Distortion vs. Frequency.

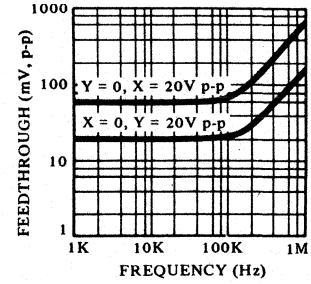


FIGURE 6. AC Feedthrough vs. Frequency.

LARGE SIGNAL FREQUENCY RESPONSE

The response curve describes the output voltage capability of the 4203 as a function of frequency. The measurement is made with one input at +10 VDC or -10 VDC, and with a sine wave applied at the other input. An output distortion of 2% is allowed.

STEP RESPONSE

Step response is measured with one input at +10 or −10 VDC and with a 20 volt p-p square wave applied at the other input.

SMALL SIGNAL FREQUENCY RESPONSE

These curves are the amplitude and phase response of the transfer function, when one input is held at +10 or −10 VDC. A sine wave signal is applied to the other input. Small signal response requires that the amplitude of the input sine wave be adjusted so that the output signal does not reach the slew rate limitation.

OUTPUT DISTORTION

The output distortion is of most interest in modulator applications. The curves of Figures 4 and 5 characterize this distortion with one input held at +10 or −10 VDC. In Figure 4, frequency is held constant at 100 Hz while the amplitude of the input sine wave is varied. In Figure 5 the sine wave amplitude is held constant at 20 volts p-p while frequency is varied.

AC FEEDTHROUGH

The variation of feedthrough as a function of frequency is illustrated by Figure 6. One of the inputs is at zero while a 20 volt p-p sine wave is applied at the other input. The output feedthrough generally has substantial harmonic content and is measured in millivolts, peak-to-peak.

APPLICATIONS

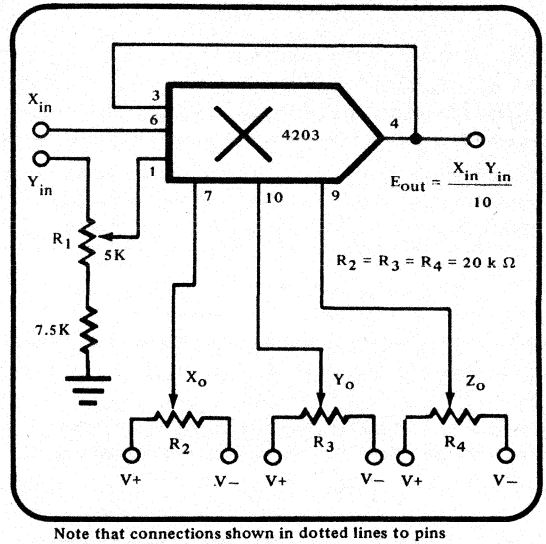
MULTIPLICATION

The general procedures given below for external adjustment of the 4203 are designed to minimize the peak value of total error over the entire operating range (±10 V) of both inputs. If reduced signal range or unipolar operation is anticipated, the accuracy may be improved by suitably restricting the X_{in} and Y_{in} voltages when making the recommended adjustments.

MULTIPLICATION - 4203

To operate the 4203 as a multiplier, connect it as shown in Figure 7 (connections shown in dotted lines to pins 7, 10 and 9 are optional). Note that no external adjustments are required in order to meet the specified accuracy. If it is desired to reduce the output offset voltage and feedthrough below their specified values, the trimpots R_2, R_3 and R_4 of Figure 7 may be added. If these optional trimpots are used, the proper adjustment procedure consists of the following steps.

1) Let $X_{in} = Y_{in} = 0$ volts, adjust R_4 for $E_{out} = 0$ volts.
2) Let $Y_{in} = 20$ volts p-p (at f=50 Hz) and $X_{in} = 0$ volts, adjust R_2 for minimum peak-to-peak output.
3) Let $X_{in} = 20$ volts p-p (at f=50 Hz) and $Y_{in} = 0$ volts, adjust R_3 for minimum peak-to-peak output.
4) Readjust R_4 if necessary.



Note that connections shown in dotted lines to pins 7, 10 and 9 are optional

Figure 7. Multiplier Connections - 4203.

MULTIPLIERS

DIVISION

The 4203 may be used as a two-quadrant divider without the need for an external operational amplifier. It should, however, be noted that, in this type of divider, the maximum output error is approximately given by

$$\text{divider error} \approx \frac{10 \in_m}{X_{in}}$$

where $\in_m$ is the total error specification for the multiply mode. Obviously, divider error becomes excessively large for small values of X_{in}. A 10:1 denominator range is usually the practical limit. If accurate division is required over a wide dynamic range of denominator voltage, the Burr-Brown Model 4291 is recommended (0.25% max error over 100:1 range).

To operate the 4203 as a divider, connect it as shown in Figure 8. The following adjustment procedure is suggested.

1) Set R_1 at mid-scale.
2) Set X_{in}= -10 VDC adjust R_2 such that E_o (@ Z_{in} = +10V) = E_o (@ Z_{in} = -10V).
3) Set X_{in} at the minimum expected denominator voltage, adjust R_1 such that E_o (@$Z_{in} = X_{in}$) = E_o (@$Z_{in} = X_{in}$).
4) Repeat steps 2 and 3.

Typically the error will be less than ±100 mV @ X_{in} = -10V and less than ±500 mV @ X_{in} = -1V.

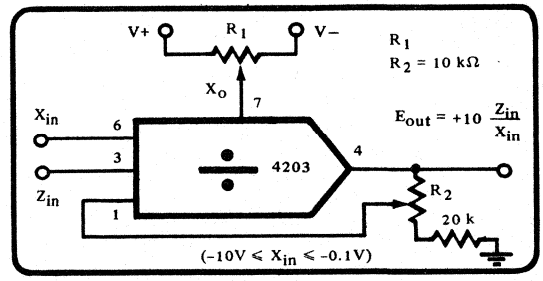


Figure 8. Divider Connections.

SQUARE ROOT

The pin connections for the Square Root mode of operation are similar to those for division, except that the denominator input is connected to the output node, thus,

$$E_o = -\sqrt{10\,Z_{in}}\ (+0.1V \leq Z_{in} \leq +10V)$$

Errors in the Square Root mode of operation become troublesome for small values of Z_{in}. However, the output error does not increase so rapidly as in the divide mode. The actual output for small values of Z_{in} is given approximately by

$$E_{out} \approx -\sqrt{10Z_{in} + 10\in_m}$$

where $\in_m$ is the total error specified for Multiply mode. This equation can be used to determine the feasibility of using the 4203 as a square rooter for a given application. For operation over a much wider dynamic range, with improved accuracy, Models 4302 or 4301 are recommended.

Figure 9 shows that proper connections for operation of the 4203 as a square rooter. The output offset should be nulled for best performance. The procedure for this is quite simple:

1) Let Z_{in} be equal to its smallest expected value.
2) Adjust R4 for $E_{out} = -\sqrt{10Z_{in}}$.

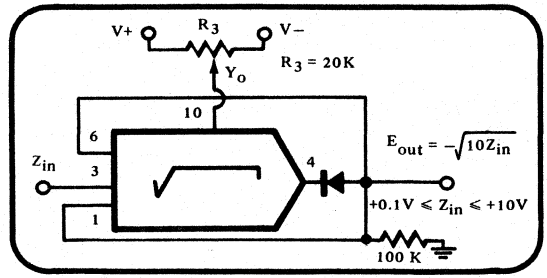
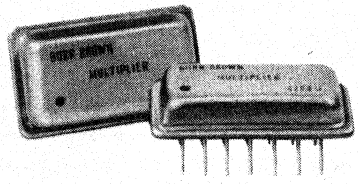


Figure 9. Square Root Connections.

BURR-BROWN

4204



ANALOG MULTIPLER-DIVIDER

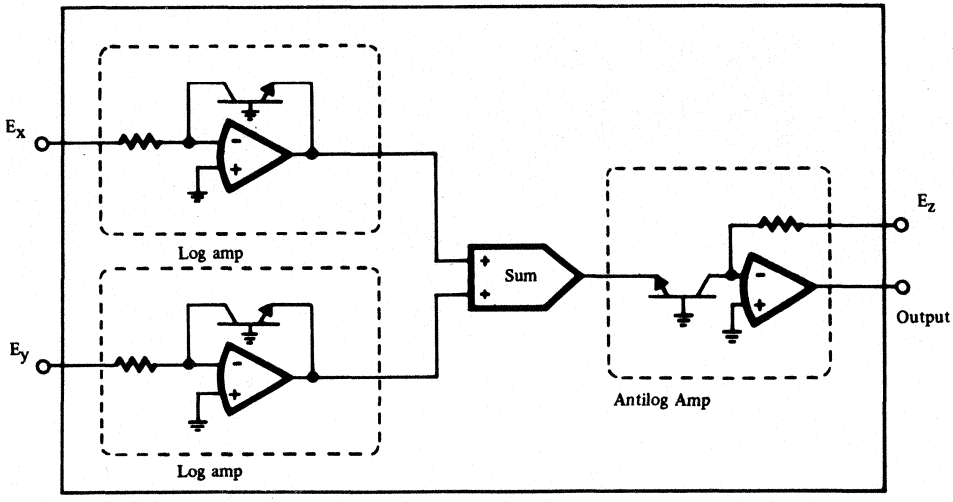
FEATURES

IMPROVE SYSTEM ACCURACY
±0.25% and ±0.5% units

LOW COST
0.5% accuracy

IMPROVE ACCURACY
OVER TEMPERATURE - ±0.02%/°C max

SIMPLIFY ASSEMBLY
Laser-trimmed at the factory
No external components required



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PDS-311A
Printed in U.S.A. July, 1978

DESCRIPTION

The 4204 is an internally trimmed four quadrant analog multiplier/divider using the log/antilog technique. This method yields excellent accuracy, low noise and moderate bandwidth–at low cost. No external components or amplifiers are required with the 4204. Accuracy specifications are guaranteed without external adjustments and are verified at Burr-Brown by an automatic tester which scans the X-Y plane. Maximum error at any point in the plane is required to be less than the specified values.

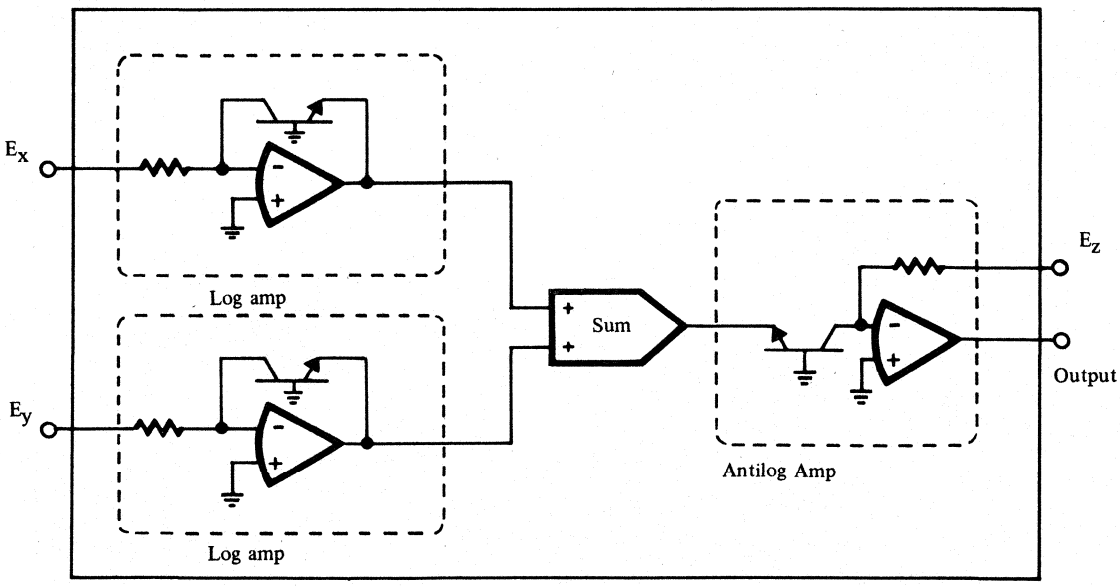
The laser trimmed 4204 is the first high accuracy hybrid IC multiplier/divider ever offered. Just as Burr-Brown was first to offer internally laser trimmed IC multipliers with accuracies of 1% and 2% (Model 4203), we have now extended this money saving technology into the accuracy areas where only higher priced modules were previously available. The excellent tracking characteristics of adjacent monolithic transistors is a key element in maintaining the 4204's high accuracy performance over the temperature range. By variation of external pin connections, the 4204 may be used as a divider or square rooter. No external amplifiers are required for either operation.

THEORY OF OPERATION

The 4204's log-antilog multiplication technique is based upon the logarithmic voltage-current relationship in a semiconductor junction. This action is shown by this simplified equation: $V_{be} = (\frac{KT}{q})(\ln I_c - \ln I_s)$

where V_{be} is the transistor's emitter base voltage, I_c is the transistor collector current, I_s is the collector saturation current, K is Boltzmann's constant, q is the charge of one electron and T is the absolute temperature in degrees Kelvin. As can be seen from the equation, the logarithmic function is extremely temperature sensitive. The 4204, however, has excellent temperature characteristics because the log and antilog circuitry have equal and opposite temperature drifts which cancel to a first order approximation. The log and antilog circuits will compensate each other to the extent that the various logging transistors are matched to each other. In the 4204 these transistors are placed adjacently on a monolithic chip to obtain the best possible matching and so the best possible performance.

BLOCK DIAGRAM



Functional Diagram of Model 4204.

SPECIFICATIONS

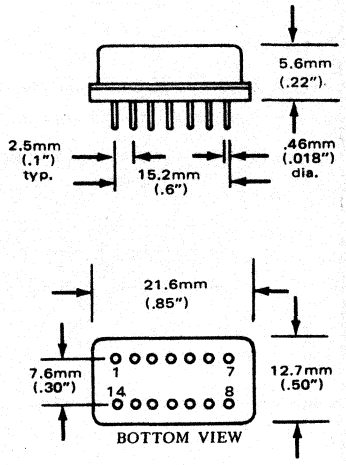
Typical performance at +25°C with rated power supplies unless otherwise noted.
Per cent specifications refer to % of full scale (10V).

ELECTRICAL

MODEL	4204J	4204K	4204S
OUTPUT FUNCTION	$\frac{E_x E_y}{10}$	*	*
TOTAL ERROR**			
Internal trim †	0.5% max	0.25% max	0.25%,max
External trim, typ	0.2%	0.1%	0.1%
vs. Temperature	0.01%/°C	*	0.02%/°C,max
vs. Supply	0.02%/%	*	*
INDIVIDUAL ERRORS			
Output Offset X=Y=0	15 mV	5 mV	5 mV
Scale Factor Error	0.2%	0.1%	0.1%
Non-Linearity			
X = 20 V, p-p Y = −10 VDC Y = 20 V, p-p X = −10 VDC	0.005%	*	*
X = 20 V, p-p Y = +10 VDC Y = 20 V, p-p X = +10 VDC	0.05%	*	*
Feedthrough @ 50 Hz			
X = 20 V, p-p Y = 0	10 mV p-p	5 mV p-p	5 mV p-p
Y = 20 V, p-p X = 0	10 mV p-p	5 mV p-p	5 mV p-p
AC PERFORMANCE		*	*
Slew Rate	1 V/μsec		
−3 dB Small Signal Bandwidth	250 kHz		
1% Amplitude Error	33 kHz		
1% Vector Error (0.57° phase shift)	2.5 kHz		
Full Power Response	20 kHz		
OUTPUT NOISE X = Y = 0.0V		*	*
DC to 10 kHz	300 μV rms		
INPUT CHARACTERISTICS		*	*
Input Voltage			
Maximum for Rated Specifications X,Y,Z	±10 V		
Maximum Safe Level X,Y,Z	±Supply		
Input Impedance X/Y/Z	25kΩ/25kΩ/100kΩ		
OUTPUT CHARACTERISTICS		*	*
Rated Output			
Voltage, min	±10 V		
Current, min	±5 mA		
Output Impedance	1 Ω		
POWER SUPPLY REQUIREMENTS		*	*
Rated Supply	±15 VDC		
Operating Range	±14 to ±16 V		
Quiescent Current	+15 mA, −8.5 mA		
TEMPERATURE RANGE		*	
Specification	−25°C to +85°C		−55°C to +125°C
Operating	−55°C to +125°C		*
Storage	−65°C to +125°C		*

*Same as for 4204J.
** Total error is a tested maximum and does not represent a sum of the maximum individual errors as the maximum individual errors do not occur at the same X, Y operating point.
† With output loading of 10 kΩ or less.

MECHANICAL



PIN 1 IS IDENTIFIED BY A BLACK DOT ON THE TOP SURFACE

Pin material and plating composition meet Method 2003 (solderability) of Mil-Std-883 [except for paragraph 3.2.]

PIN CONNECTIONS

1	E_Z
2	Output
3	$-V_S$
4	Feedthrough Adj.
5	Make No Connection
6	Make No Connection
7	E_X
8	Internal Reference
9	Make No Connection
10	Ground
11	Feedthrough Adj.
12	Offset Adj.
13	E_Y
14	$+V_S$

MULTI. DIV.

TYPICAL PERFORMANCE CURVES

Typical Performance @25°C and ±15 VDC

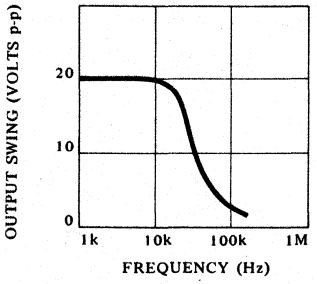


FIGURE 1. Large Signal Frequency Response

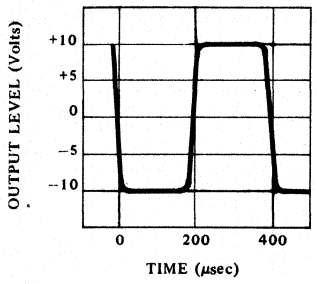


FIGURE 2. Step Response

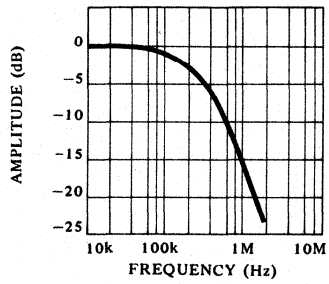


FIGURE 3. Small Signal Frequency Response

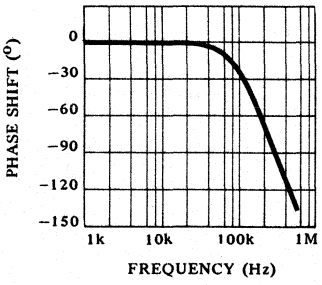


FIGURE 4. Small Signal Frequency Response

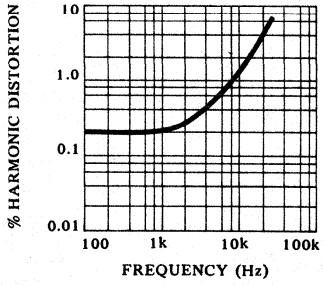


FIGURE 5. Output Distortion vs. Frequency

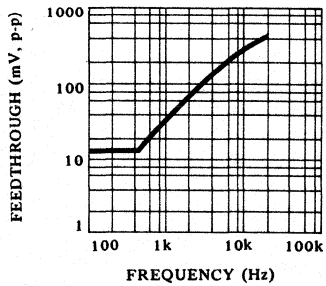


FIGURE 6. AC Feedthrough vs. Frequency

DISCUSSION OF PERFORMANCE CURVES

LARGE SIGNAL FREQUENCY RESPONSE

This response curve describes the output voltage capability of the 4204 as a function of frequency. The measurement is made with one input at +10 or −10 VDC, and with a sine wave applied at the other input. An output distortion of 0.5% is allowed.

STEP RESPONSE

Step response is measured with one input at +10 or −10VDC and with a 20 volt p-p square wave applied at the other input.

SMALL SIGNAL FREQUENCY RESPONSE

These curves are the amplitude and phase response of the 4204's transfer function, when one input is held at +10 or −10 VDC. A sine wave signal is applied to the other input. Small signal response requires that the amplitude of the input sine wave be adjusted so that the output signal does not reach the slew rate limitation.

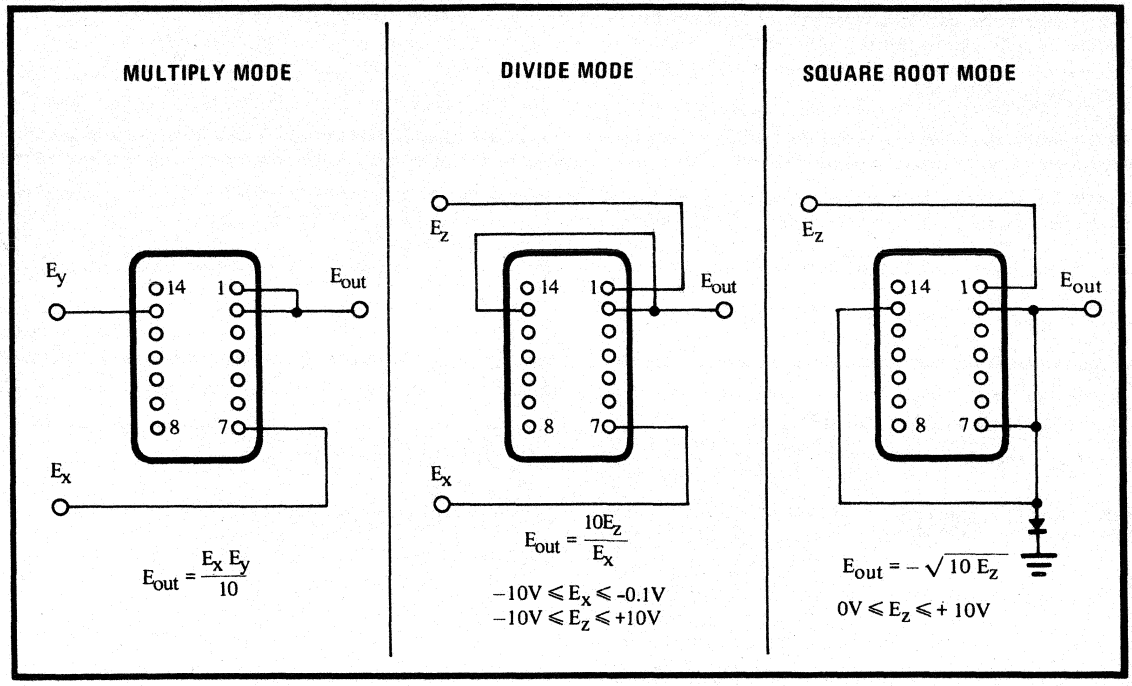
OUTPUT DISTORTION

The output distortion of the 4204 is of most interest in modulator applications. The curve of Figure 5 characterizes this distortion with one input of the 4204 held at +10 or −10 VDC. A sine wave is applied to the other input. The sine wave amplitude is held constant at 20 volts p-p while frequency is varied.

AC FEEDTHROUGH

The variation of feedthrough as a function of frequency is illustrated by Figure 6. One of the inputs is a zero while a 20 volt p-p sine wave is applied at the other input. The output feedthrough generally has substantial harmonic content and is measured in millivolts, peak-to-peak.

OPERATING MODES



MULTI. DIV.

ADJUSTMENTS

Although the 4204 will achieve specified performance in the multiply mode with no external trimming, optimized performance can be achieved with external adjustments. The proper connections and the trim procedures are explained below.

The 4204 will operate within specification with any combination of input signals. The best performance, however, will be obtained in the 2nd, 3rd and 4th quadrants. That is if four quadrant operations are not needed, the performance of the 4204 can be optimized by constraining operation to quadrants 2, 3 and 4 rather than 1.

MULTIPLICATION

MULTIPLICATION TRIM PROCEDURE (FIG. 7)

1) Set E_x = 0 and apply a 10 volt peak-peak sine wave (50 Hz) to E_y: Adjust R_1 for minimum output.
2) Set E_y = 0 and apply a 10 volt peak-to-peak sine wave (50 Hz) to E_x: Adjust R_2 for minimum output.
3) Set $E_x = E_y$ = 0: Adjust R_3 for E_{out} = 0.000 V.
4) Set $E_x = E_y$ = +10.000 V ±1 mV: Adjust R_4 for E_{out} = +10.000 V ±2 mV.

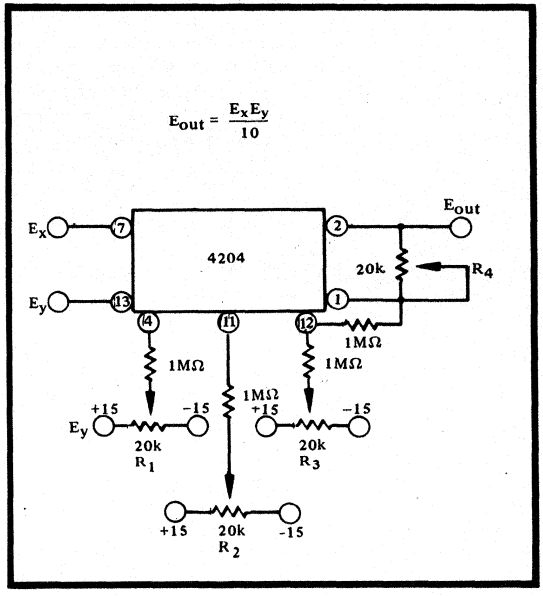


FIGURE 7. Multiplication Trim Procedure.

DIVISION

The 4204 may be used as a two-quadrant divider without the need for an external operational amplifier. It should, however, be noted that the maximum output error is approximately given by

$$\text{divider error} \approx \frac{10\epsilon_m}{Ex}$$

where ϵ_m is the total error specification for the multiply mode. Obviously, divider error becomes excessively large for small values of E_X. A 10:1 denominator range is usually the practical limit. If accurate division is required over a wide dynamic range of denominator voltage, the Burr-Brown Model 4291 is recommended (0.5%, max., over a 100:1 range).

DIVISION TRIM PROCEDURE (FIG. 8)

1) Set all potentiometers @ about mid-scale.
2) Set E_Z = 0 volt, $E_X \approx -10$ V, adjust R_2 such that E_O = 0.000 V ±2 mV.
3) Set $E_X = E_Z = -10.000$VDC ±2 mV, adjust R_3 such that $E_O = +10.000$VDC ±2 mV.
4) Set $E_X = E_Z \approx$ minimum value required by application, adjust R_1 such that $E_O = +10.000$VDC ±5 mV.
5) Repeat steps (2) through (4) if necessary.

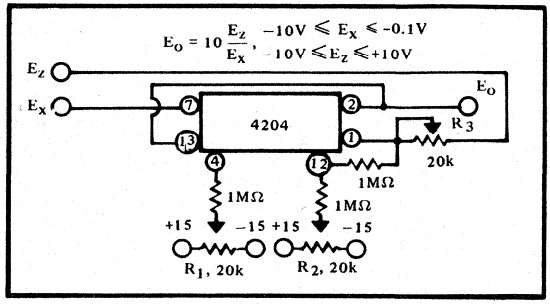


FIGURE 8. Division Trim Procedure.

SQUARE ROOT

The pin connections for the Square Root mode of operation are similar to those for division, except that the denominator input is connected to the output node. Errors in the Square Root mode of operation become troublesome for small values of E_Z. However, the output error does not increase so rapidly as in the divide mode. The actual output for small values of E_Z is given approximately by

$$E_{out} \approx -\sqrt{10E_Z + 10\epsilon_m}$$

where ϵ_m is the total error specified for Multiply mode. This equation can be used to determine the feasibility of using the 4204 as a square rooter for a given application. For operation over a much wider dynamic range, with improved accuracy, the Model 4302 multifunction converter is recommended.

SQUARE ROOT TRIM PROCEDURE (FIG. 9)

1) Set E_Z = +10.000VDC ±2 mV, adjust R_2 such that E_O = -10.000VDC ±2 mV.
2) Set $E_Z \approx$ minimum value required by application (E_{Zm}) adjust R_1 such that $E_O = -\sqrt{10E_{Zm}}$ ±2 mV.
3) Repeat steps (1) and (2) if necessary.

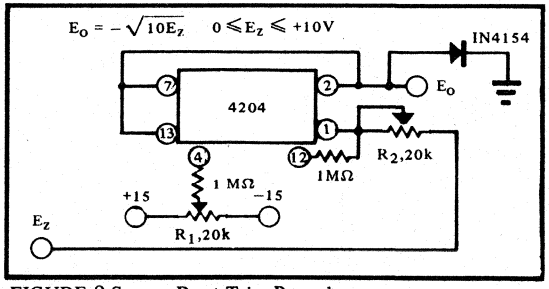
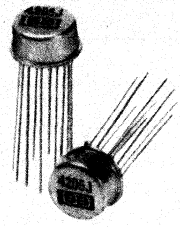


FIGURE 9. Square Root Trim Procedure.

BURR-BROWN



4205

MULTIPLIER-DIVIDER

FEATURES

- **DIFFERENTIAL INPUTS**
- **LASER-TRIMMED**
  Requires no adjustment
- **GUARANTEED ACCURACY**
  1% or 2%
- **SELF-CONTAINED**
  No additional amplifiers

DESCRIPTION

Burr-Brown Model 4205 is a differential input monolithic multiplier/divider designed for general-purpose usage. In addition to four-quadrant multiplication it also performs division and square-rooting of analog signals. It does not require the use of additional amplifiers in performing the above functions. The 4205 is laser trimmed prior to final packaging and is guaranteed to its rated accuracy with no external components.

This multiplier contains its own zener-regulated references and, as a result is much less sensitive to supply voltage variation than were earlier IC multipliers. The fast (25 V/μsec) slew rate and 1 MHz bandwidth are key performance factors for applications where delay or phase shift must be minimized. Harmonic distortion remains low for frequencies well above 100 kHz, an important asset in modulation applications.

Other desirable features of the 4205 are hermetic TO-100 package (10-pin version of TO-99) and wide temperature range of operation. The 4205S is specified for operation over the full Mil temperature range.

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PDS-312A

Printed in U.S.A. July, 1978

SPECIFICATIONS

Typical performance at +25°C with rated power supplies unless otherwise noted.
Per cent specifications refer to % of full scale (10V).

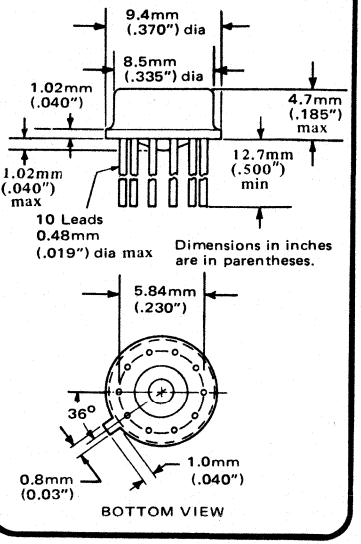
ELECTRICAL

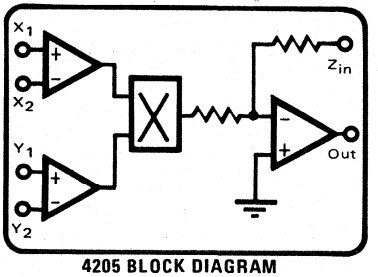
MODEL	4205J	4205K	4205S
OUTPUT FUNCTION		$(X_1 - X_2)(Y_1 - Y_2)/10$	
TOTAL ERROR*			
Internal Trim	2% max	1% max	1%, max
Error vs. Temperature		0.04%/°C	
Error vs. Supply		0.2%/%	
INDIVIDUAL ERRORS			
Output Offset @ 25°C (X=Y=0)	20 mV	20 mV	20 mV, max
vs. Temperature (Operating Range)		0.4 mV/°C	
vs. Supply		10 mV/%	
Scale Factor Error	1%	0.6%	0.6%
vs. Temperature (Operating Range)		0.04%/°C	
vs. Supply		0.1%/%	
Non-Linearity			
X (X=20 V p-p, Y=±10 Vdc)	0.8%	0.5%	0.5%
Y (Y=20 V p-p, X=±10 Vdc)	0.2%	0.2%	0.2%
Feedthrough @ 50 Hz			
X=0, Y=20V p-p (Internal Trim)		50 mV p-p	
(External Trim)		20 mV p-p	
vs. Temperature		1 mV p-p/°C	
Y =0, X=20V p-p (Internal Trim)		50 mV p-p	
(External Trim)		20 mV p-p	
vs. Temperature		2 mV p-p/°C	
AC PERFORMANCE			
Slew Rate		25 V/μsec	
-3 dB Small Signal Bandwidth		1 MHz	
1% Amplitude Error		40 kHz	
1% Vector Error (0.57° phase shift)		10 kHz	
Settling Time (2% of final value, 20V, step)		1 μsec	
Overload Recovery Time		3 μsec	
OUTPUT NOISE (X=Y=0)			
10 kHz to 10 MHz		3 mV rms	
10 Hz to 10 kHz		600 μV rms	
INPUT CHARACTERISTICS			
Input Voltage Range			
Rated Operation		±10 V	
Absolute max		±15 V	
Input Impedance, between X_1, X_2		10 MΩ	
between Y_1, Y_2		10 MΩ	
Z_{in}		36 kΩ	
OUTPUT CHARACTERISTICS			
Rated Output		±10 V @ ±5 mA	
Output Impedance		1 Ω	
POWER SUPPLY REQUIREMENTS			
Rated Voltage		±15 Vdc	
Operating Range		±12 Vdc to ±18 Vdc	
Quiescent Current		4.5 mA	
TEMPERATURE RANGE			
Operating, Rated Performance	0° to +70°C		-55° to +125°C
Storage		-65°C to +150°C	

*Total error is a tested maximum at +25°C and represents the maximum allowed value for the sum of the individual errors.

MECHANICAL

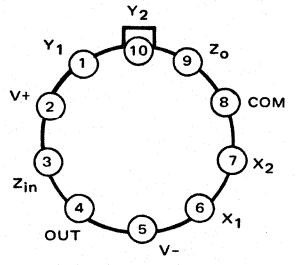
TO-100





4205 BLOCK DIAGRAM

CONNECTION DIAGRAM



(TOP VIEW)

TYPICAL PERFORMANCE CURVES

Typical Performance @ 25°C and ±15 Vdc

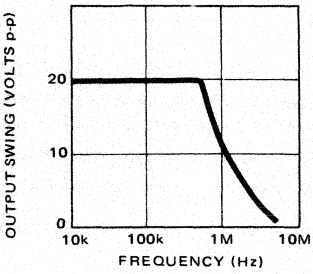


FIGURE 1. Large Signal Frequency Response.

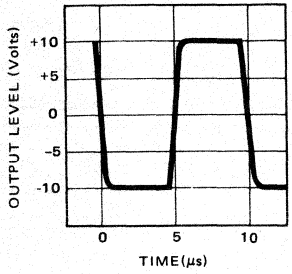


FIGURE 2. Step Response.

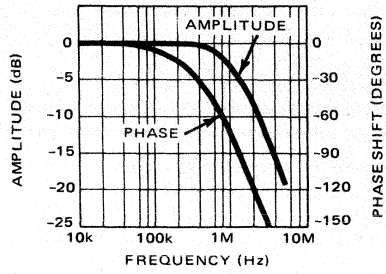


FIGURE 3. Small Signal Frequency Response.

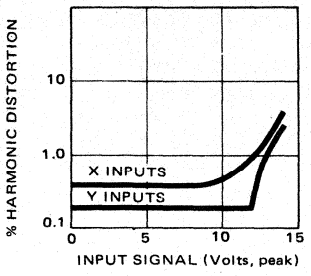


FIGURE 4. Output Distortion vs. Peak Input Signal.

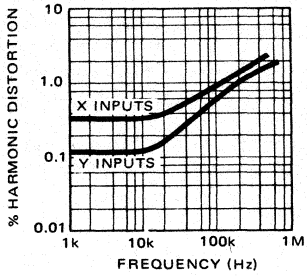


FIGURE 5. Output Distortion vs. Frequency.

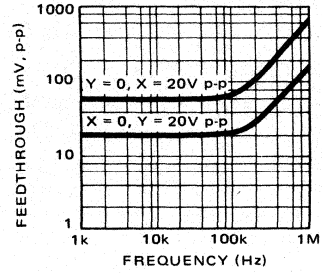
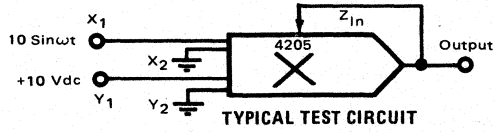


FIGURE 6. AC Feedthrough vs. Frequency.



TYPICAL TEST CIRCUIT

DISCUSSION OF PERFORMANCE CURVES

LARGE SIGNAL FREQUENCY RESPONSE

Figure 1 describes the output voltage capability of the 4205 as a function of frequency. The measurement can be made with a sine wave applied to the X_1 input and +10 or -10 Vdc applied to the Y_1 input (the X_2 and Y_2 inputs should be grounded). Similar results will be obtained with the signals applied to the X_2 and Y_2 inputs. An output distortion of 2% is allowed.

STEP RESPONSE

Step response can be measured with a 20 volt peak-peak square wave applied to the X_1 input and +10 or -10 Vdc applied to the Y_1 input (with the X_2 and Y_2 inputs grounded). Similar results will be obtained with the signals applied to the X_2 and Y_2 inputs.

SMALL SIGNAL FREQUENCY RESPONSE

Figure 3 shows the amplitude and phase response of the transfer function with a sine wave applied to the X_1 input and +10 or -10 Vdc applied to the Y_1 input (with the X_2 and Y_2 inputs grounded). Similar results will be obtained with the signals applied to the X_2 and Y_2 inputs. Small signal response requires that the amplitude of the input sine wave be adjusted so that the output signal does not reach the slew rate limitation.

OUTPUT DISTORTION

The output distortion is of most interest in modulator applications. The curves of Figures 4 and 5 characterize this distortion with +10 or -10 Vdc applied across one set of inputs. In Figure 4, frequency is held constant at 100 Hz while the amplitude of the input sine wave is varied. In Figure 5 the sine wave amplitude is held constant at 20 volts p-p while frequency is varied.

AC FEEDTHROUGH

The variation of feedthrough as a function of frequency is illustrated by Figure 6. One set of inputs is at zero while a 20 volt peak-peak sine wave is applied across the other set of inputs. The output feedthrough generally has substantial harmonic content and is measured in millivolts, peak-to-peak.

OPERATING MODES

The general procedures given below for external adjustments are designed to minimize the peak value of total error over the entire operating range (±10 V) of both inputs. If reduced signal range or unipolar operation is anticipated, the accuracy may be improved by suitably restricting the X_{in} and Y_{in} voltage when making the recommended adjustments.

MULTIPLICATION

To operate the 4205 as a multiplier, connect it as shown in Figure 7. No external adjustments are required in order to meet the specified accuracy. If it is desired to reduce the output offset voltage below its specified value, the optional offset adjustment may be used. The proper offset adjustment procedure is to ground all inputs and adjust E_{out} = 0 V.

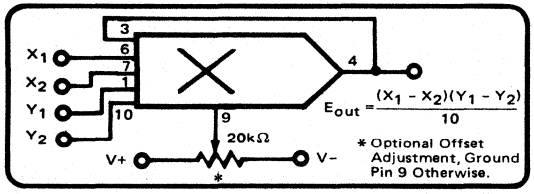


FIGURE 7. Multiplier Connections - 4205.

DIVISION

The 4205 may be used as a two-quadrant divider without the need for an external operational amplifier. It should, however, be noted that, in this type of divider, the maximum output error is approximately given by

$$\text{divider error} \approx \frac{10 \in_m}{X_{in}}$$

where $\in_m$ is the total error specification for the multiply mode. Obviously, divider error becomes excessively large for small values of X_{in}. A 10:1 denominator range is usually the practical limit. If accurate division is required over a wide dynamic range of denominator voltage, the Burr-Brown Model 4290 is recommended (0.5%, max., over a 100:1 range).

To operate the 4205 as a two quadrant divider connect it as shown in Figure 8. The following adjustments should be made to achieve best performance:

1) Set R_1 at about mid-scale.
2) Set X_1 = -10.000 V, adjust R_2 such that $|E_{out}|$ with Z_{in} = +10V is equal to $|E_{out}|$ with Z_{in} = -10V.
3) Let $Z_{in} = X_1$ = minimum expected denominator voltage. Adjust R_1 such that $|E_{out}|$ = 10V.
4) Repeat steps 2) and 3) if necessary.

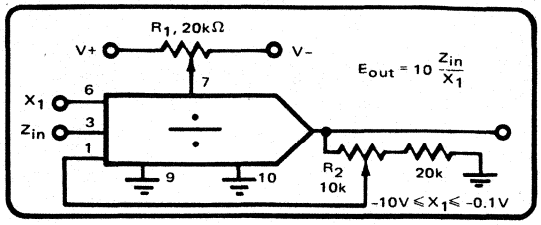


FIGURE 8. Divider Connections - 4205.

SQUARE ROOT

The pin connections for the Square Root mode of operation are similar to those for division, except that the denominator input is connected to the output node, thus,

$$E_o = -\sqrt{10\,Z_{in}} \quad (+0.1V \leq Z_{in} \leq +10\ V)$$

Errors in the Square Root mode of operation become troublesome for small values of Z_{in}. However, the output error does not increase so rapidly as in the divide mode. The actual output for small values of Z_{in} is given approximately by

$$E_{out} \approx -\sqrt{10\,Z_{in} + 10 \in_m}$$

where $\in_m$ is the total error specified for Multiply mode. This equation can be used to determine the feasibility of using the 4205 as a square rooter for a given application. For operation over a much wider dynamic range, with improved accuracy, the Model 4301 multifunction converter is recommended.

Figure 9 shows the proper connections for operation of the 4205 as a square rooter. The output offset should be nulled for best performance. The procedure for this is quite simple:

1) Let Z_{in} be equal to its smallest expected value.
2) Adjust R_3 for $E_{out} = -\sqrt{10\,Z_{in}}$.

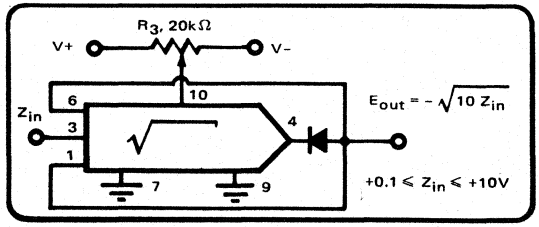
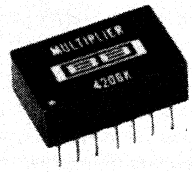


FIGURE 9. Square Root Connections - 4205.

BURR-BROWN

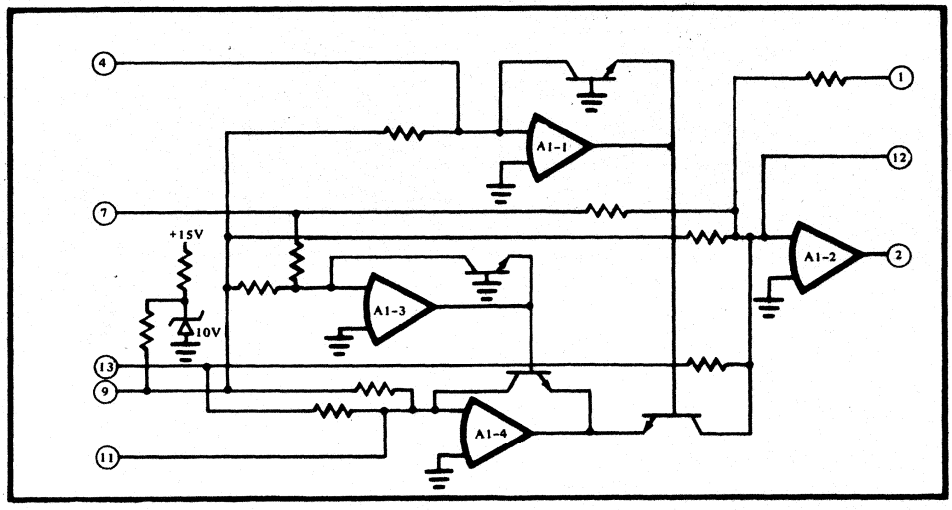
4206



ANALOG MULTIPLIER-DIVIDER

FEATURES

- HIGH TOTAL ACCURACY
  0.25% and 0.5% max, no external trims
  0.1% and 0.2% typ. with external trims
- LOW TEMPERATURE DRIFT
  100ppm/°C from 0°C to +70°C
- SMALL PACKAGE
  Dual-in-line saves board space
- LOW COST



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PDS-330A

Printed in U.S.A. July, 1978

DESCRIPTION

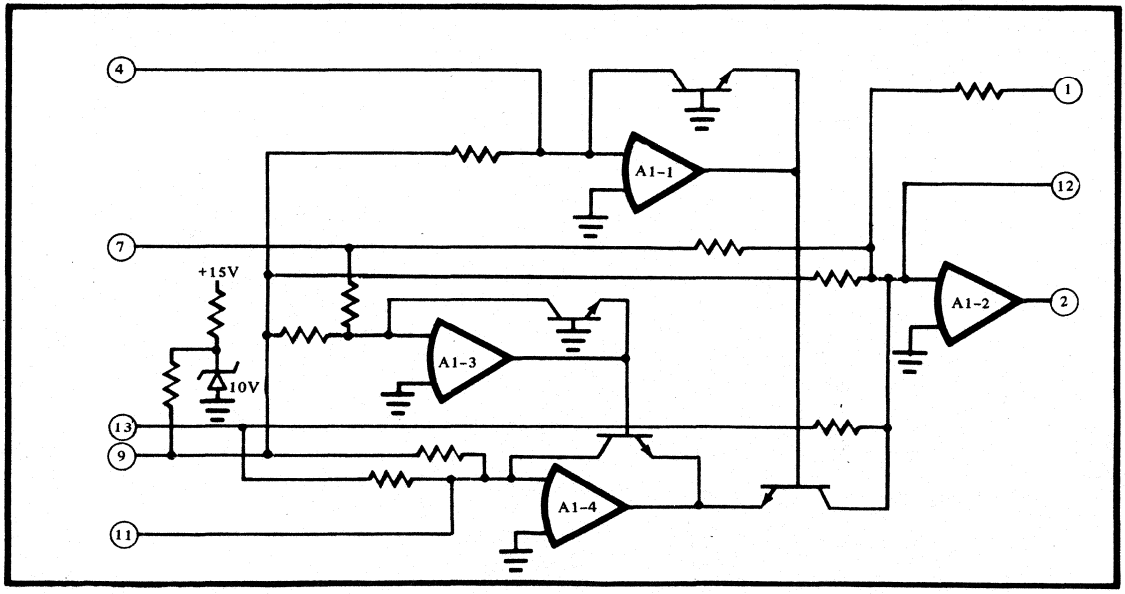
The 4206 is a four quadrant analog multiplier offering high accuracy, low noise, and moderate bandwidth at low cost. It uses the log/antilog technique and is internally laser trimmed and multiply mode accuracies of 1/4% and 1/2% max, are guaranteed with no external components. By following the external trim procedure, accuracies can be improved to 0.1% and 0.2% typ. Accuracy specifications are verified at Burr-Brown by an automatic tester which scans the X-Y plane. Maximum error at any points in the plane is required to be less than the specified values.

The 4206 also performs the divide function in two quadrants and the square root function in one quadrant with no external components required. Detailed instructions for these operations are given under discussions titled DIVISION and SQUARE ROOT.

THEORY OF OPERATION

The 4206's log-antilog multiplication technique is based upon the logarithmic voltage-current relationship in a semiconductor junction. This action is shown by the simplified equation: $V_{be} = (\frac{KT}{q})(\ln I_c - \ln I_s)$

where V_{be} is the transistor's emitter-base voltage, I_c is the transistor collector current, I_s is the collector saturation current, K is Bolzmann's constant, q is the charge of one electron and T is the absolute temperature in degrees Kelvin. As can be seen from the equation, the logarithmic function is extremely temperature sensitive. The 4206, however, has excellent temperature characteristics because the log and antilog circuitry have equal and opposite temperature drifts which cancel to a first order approximation. The log and antilog circuits will compensate each other to the extent that the various logging transistors are matched to each other. In the 4206 these transistors are placed adjacently on a monolithic chip to obtain the best possible matching and so the best possible performance.



SPECIFICATIONS

Typical performance at +25°C with rated power supplies unless otherwise noted.
Per cent specifications refer to % of full scale (10V).

ELECTRICAL		
MODEL	**4206J**	**4206K**
OUTPUT FUNCTION	$\frac{E_x E_y}{10}$	*
TOTAL ERROR (Multiply Mode)**		
Internal trim, max †	0.5% max	0.25% max
External trim, typ	0.2%	0.1%
vs. Temperature	0.01%/°C	*
vs. Supply	0.02%/%	*
INDIVIDUAL ERRORS (Multiply Mode)		
Output Offset X=Y=0	15 mV	5 mV
Scale Factor Error	0.2%	0.1%
Non-Linearity		
X = 20 V, p-p Y = −10 VDC Y = 20 V, p-p X = −10 VDC	0.005%	*
X = 20 V, p-p Y = +10 VDC Y = 20 V, p-p X = +10 VDC	0.05%	*
Feedthrough @ 50 Hz		
X = 20 V, p-p Y = 0	10 mV p-p	5 mV p-p
Y = 20 V, p-p X = 0	10 mV p-p	5 mV p-p
AC PERFORMANCE		*
Slew Rate	1 V/μsec	
−3 dB Small Signal Bandwidth	250 kHz	
1% Amplitude Error	33 kHz	
1% Vector Error (0.57° phase shift)	2.5 kHz	
Full Power Response	20 kHz	
OUTPUT NOISE X = Y = 0.0V		*
DC to 10 kHz	300 μV rms	
INPUT CHARACTERISTICS		*
Input Voltage		
Maximum for Rated Specifications X,Y,Z	±10 V	
Maximum Safe Level X,Y,Z	±Supply	
Input Impedance X/Y/Z	25kΩ/25kΩ/100kΩ	
OUTPUT CHARACTERISTICS		*
Rated Output		
Voltage, min	±10 V	
Current, min	±5 mA	
Output Impedance	1 Ω	
POWER SUPPLY REQUIREMENTS		*
Rated Supply	±15 VDC	
Operating Range	±14 to ±16 V	
Quiescent Current	+15 mA, −8.5 mA	
TEMPERATURE RANGE		*
Specification	0°C to +70°C	
Operating	−25°C to +85°C	
Storage	−55°C to + 125°C	

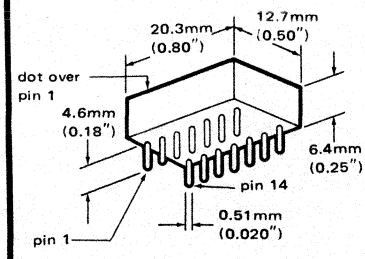
The information in this publication has been carefully checked and is believed to be reliable; however, no responsibility is assumed for possible inaccuracies or omissions. Prices and specifications are subject to change without notice. No patent rights are granted to any of the circuits described herein.

* Same as for 4206J

** Total error is a tested maximum and does not represent a sum of the maximum individual errors as the maximum individual errors do not occur at the same X, Y operating point.

† With output loading of 10 kΩ or less.

MECHANICAL



Pin Spacing: 2.5mm (0.1")
Row Spacing: 7.6mm (0.300")
Weight: 3.4 grams (0.12 oz.)
Connector: 14-pin DIP

0145MC

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std-202.

PIN CONNECTIONS

1	E_Z
2	Output
3	$-V_S$
4	Feedthrough Adj.
5	Make No Connection
6	Make No Connection
7	E_X
8	Internal Reference
9	Make No Connection
10	Ground
11	Feedthrough Adj.
12	Offset Adj.
13	E_Y
14	$+V_S$

TYPICAL PERFORMANCE CURVES

Typical Performance @25°C and ±15 VDC

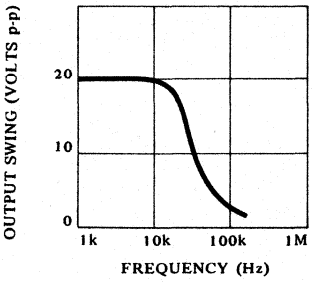


FIGURE 1. Large Signal Frequency Response

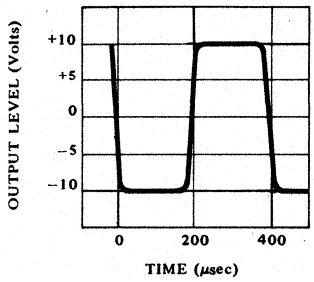


FIGURE 2. Step Response

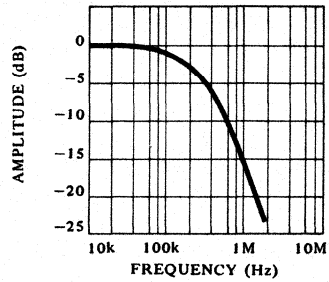


FIGURE 3. Small Signal Frequency Response

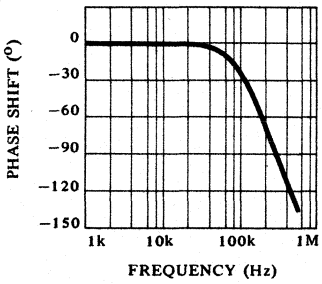


FIGURE 4. Small Signal Frequency Response

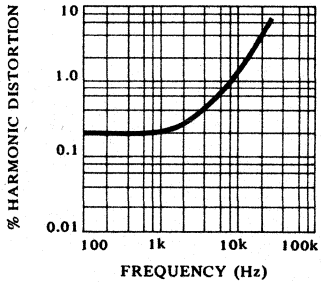


FIGURE 5. Output Distortion vs. Frequency

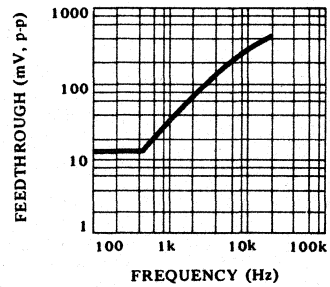


FIGURE 6. AC Feedthrough vs. Frequency

DISCUSSION OF PERFORMANCE CURVES

LARGE SIGNAL FREQUENCY RESPONSE

This response curve describes the output voltage capability of the 4206 as a function of frequency. The measurement is made with one input at +10 or −10 VDC, and with a sine wave applied at the other input. An output distortion of 0.5% is allowed.

STEP RESPONSE

Step response is measured with one input at +10 or −10VDC and with a 20 volt p-p square wave applied at the other input.

SMALL SIGNAL FREQUENCY RESPONSE

These curves are the amplitude and phase response of the 4206's transfer function, when one input is held at +10 or −10 VDC. A sine wave signal is applied to the other input. Small signal response requires that the amplitude of the input sine wave be adjusted so that the output signal does not reach the slew rate limitation.

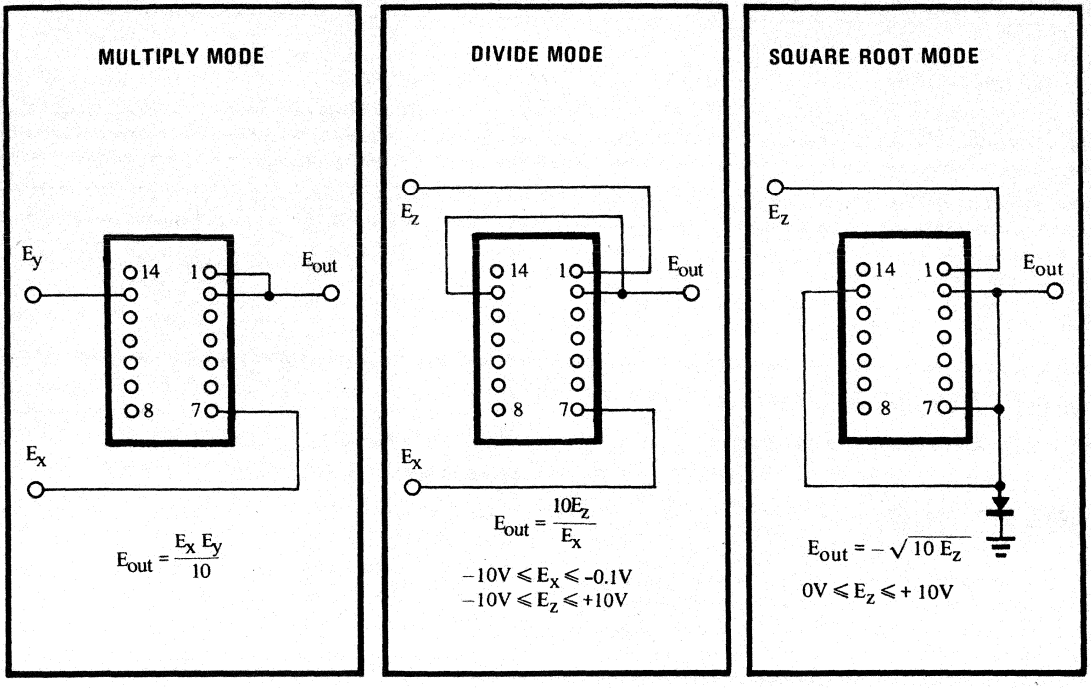
OUTPUT DISTORTION

The output distortion of the 4206 is of most interest in modulator applications. The curve of Figure 5 characterizes this distortion with one input of the 4206 held at +10 or −10 VDC. A sine wave is applied to the other input. The sine wave amplitude is held constant at 20 volts p-p while frequency is varied.

AC FEEDTHROUGH

The variation of feedthrough as a function of frequency is illustrated by Figure 6. One of the inputs is a zero while a 20 volt p-p sine wave is applied at the other input. The output feedthrough generally has substantial harmonic content and is measured in millivolts, peak-to-peak.

OPERATING MODES



MULTI DIV

ADJUSTMENTS

Although the 4206 will achieve specified performance in the multiply mode with no external trimming, optimized performance can be achieved with external adjustments. The proper connections and the trim procedures are explained below.

The 4206 will operate within specification with any combination of input signals. The best performance, however, will be obtained in the 2nd, 3rd and 4th quadrants. That is if four quadrant operations are not needed, the performance of the 4206 can be optimized by constraining operation to quadrants 2, 3 and 4 rather than 1.

MULTIPLICATION

MULTIPLICATION TRIM PROCEDURE (FIG. 7)

1) Set E_x = 0 and apply a 10 volt peak-peak sine wave (50 Hz) to E_y: Adjust R_1 for minimum output.
2) Set E_y = 0 and apply a 10 volt peak-to-peak sine wave (50 Hz) to E_x: Adjust R_2 for minimum output.
3) Set $E_x = E_y$ = 0: Adjust R_3 for E_{out} = 0.000 V.
4) Set $E_x = E_y$ = +10.000 V ±1 mV: Adjust R_4 for E_{out} = +10.000 V ±2 mV.

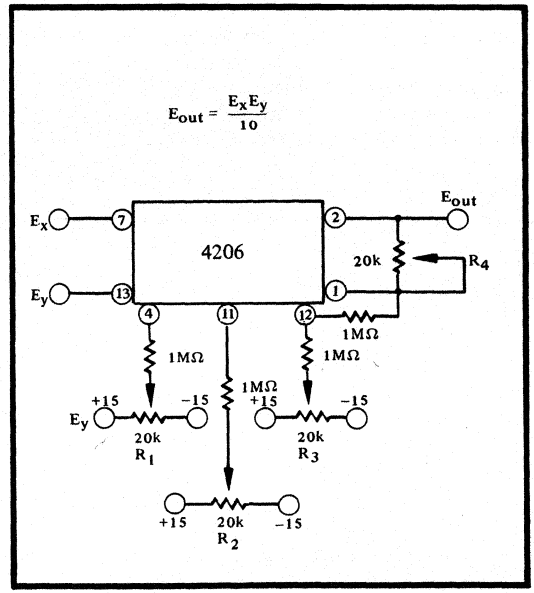


FIGURE 7 Multiplication Trim Procedure

DIVISION

The 4206 may be used as a two-quadrant divider without the need for an external operational amplifier. It should, however, be noted that the maximum output error is approximately given by

$$\text{divider error} \approx \frac{10\epsilon_m}{Ex}$$

where ϵ_m is the total error specification for the multiply mode. Obviously, divider error becomes excessively large for small values of E_X. A 10:1 denominator range is usually the practical limit. If accurate division is required over a wide dynamic range of denominator voltage, the Burr-Brown Model 4291 is recommended (0.5%, max., over a 100:1 range).

DIVISION TRIM PROCEDURE (FIG. 8)

1) Set all potentiometers near mid-scale.
2) Set E_Z = 0 volt, $E_X \approx -10$ V, adjust R_2 such that E_O = 0.000 V ±2 mV.
3) Set $E_X = E_Z$ = -10.000VDC ±2 mV, adjust R_3 such that E_O = +10.000VDC ±2 mV.
4) Set $E_X = E_Z \approx$ minimum value required by application, adjust R_1 such that E_O = +10.000VDC ±5 mV.
5) Repeat steps (2) through (4) if necessary.

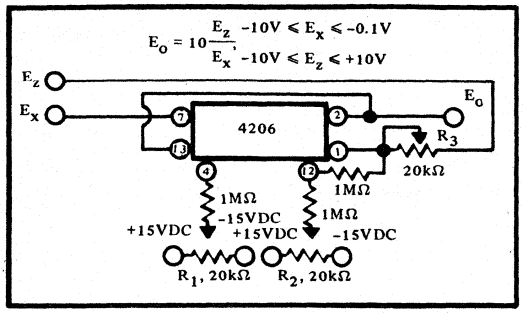


FIGURE 8 Division Trim Procedure

SQUARE ROOT TRIM PROCEDURE (FIG. 9)

1) Set E_Z = +10.000VDC ±2 mV, adjust R_2 such that E_O = +10.000VDC ±2 mV.
2) Set $E_Z \approx$ minimum value required by application (E_{Zm}) adjust R_1 such that $E_O = -\sqrt{10\,E_{Zm}}$ ±2 mV.
3) Repeat steps (1) and (2) if necessary.

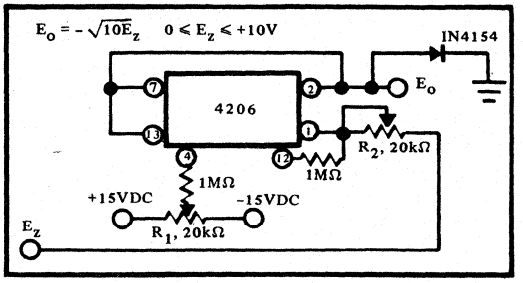


FIGURE 9 Square Root Trim Procedure

SQUARE ROOT

The pin connections for the Square Root mode of operation are similar to those for division, except that the denominator input is connected to the output node. Errors in the Square Root mode of operation become troublesome for small values of E_Z. However, the output error does not increase so rapidly as in the divide mode. The actual output for small values of E_Z is given approximately by

$$E_{out} \approx -\sqrt{10E_Z + 10\epsilon_m}$$

where ϵ_m is the total error specified for Multiply mode. This equation can be used to determine the feasibility of using the 4206 as a square rooter for a given application. For operation over a much wider dynamic range, with improved accuracy, the Model 4302 multifunction converter is recommended.

BURR-BROWN

4213

MULTIPLIER-DIVIDER

FEATURES

- DIFFERENTIAL INPUTS
- LASER-TRIMMED
- GUARANTEED ACCURACY
  0.5% and 1%
- LOW NOISE
  120μV rms, 10Hz to 10kHz
- SELF-CONTAINED
  No additional amplifiers
- SMALL SIZE
  Hermetic TO-100 package
- LOW COST

DESCRIPTION

The 4213 family of multipliers are low cost integrated circuit multiplier/dividers designed for general purpose usage. In addition to four quadrant multiplication, they also perform division and square rooting of analog signals. They do not require use of additional amplifiers to perform the above functions. The 4213 is laser-trimmed prior to final packaging and is guaranteed to its rated accuracy with no external components. This is a distinct advantage from standpoints of cost and reliability.

The 4213 contains its own zener regulated references and, as a result is much less sensitive to supply voltage variation than were earlier IC multipliers. Hermetic TO-100 package, wide temperature range of operation (4213SM is specified for operation over the full MIL temperature range), low output noise (120μV, rms, for 10Hz to 10kHz) and low cost are some of the other desirable features of 4213 family.

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PDS-366B

Printed in U.S.A. July, 1978

SPECIFICATIONS

Typical performance at +25°C with rated power supplies unless otherwise noted.

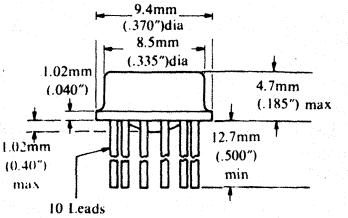
ELECTRICAL

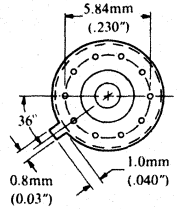
MODEL	4213AM	4213BM	4213SM
OUTPUT FUNCTION	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$		
TOTAL ERROR[1]			
Without Trimming	1% max	0.5% max	0.5% max
Error vs Temperature (-25°C to +85°C)	0.008%/°C typ., 0.02%/°C max		
(-55°C to +125°C)			0.025%/°C typ 0.05%/°C max
Error vs Supply	0.05%/%		
INDIVIDUAL ERRORS			
Output Offset	10mV typ 50mV max	7mV typ 25mV max	
vs Temperature	0.7mV/°C typ 2mV/°C max	0.3mV/°C typ 0.7mV/°C max	
vs Supply	0.25mV/%		
Scale Factor Error	0.12%		
vs Temperature	0.008%/°C		
vs Supply	0.05%/%		
Nonlinearity			
X(X = 20V p-p, Y = ±10VDC)	±0.08%		
Y(Y = 20V p-p, X = ±10VDC)	±0.01%		
Feedthrough at 50 Hz			
X = 20V p-p, Y = 0	30mV p-p		
Y = 20V p-p, X = 0	6mV p-p		
vs Temperature	0.1mV p-p/°C		
vs Supply	0.15mV p-p/%		
AC PERFORMANCE			
Small Signal ±3dB Flatness	610 kHz		
Small Signal ±1% Flatness	90 kHz		
Small Signal ±1% Vector Error (0.57° Phase Shift)	7.5 kHz		
Full Power Bandwidth	330 kHz		
Slew Rate	23V/μs		
Settling Time to 1% (20V step)	1.7μs		
OUTPUT NOISE (X = Y = 0)			
10 Hz to 10 kHz	120μV rms		
10 Hz to 10 MHz	700μV rms		
INPUT CHARACTERISTICS			
Input Voltage Range			
Rated Operation, min.	±10V		
Absolute max	±V_s		
Input Impedance, X, Y, Z[2]	10 MΩ		
Input Bias Current, X, Y, Z	1.4μA		
OUTPUT CHARACTERISTICS			
Rated Output	±10V at ±5mA min		
Output Impedance	1.5Ω		
POWER SUPPLY REQUIREMENTS			
Rated Voltage	±15V		
Operating Range	±8.5VDC to ±20VDC		
Quiescent Current	±5.5mA		
TEMPERATURE RANGE			
Rated Performance (specification)	-25°C to +85°C		-55°C to +125°C
Operation	-55°C to +125°C		
Storage	-65°C to +150°C		

1. Total error is the maximum allowed value of the sum of the individual errors.
2. Z_2 input impedance is 10 MΩ typ with Pin 9 open circuit. If pin is grounded or used for optional offset adjustment the Z_2 input impedance may become as low as 25kΩ.

MECHANICAL

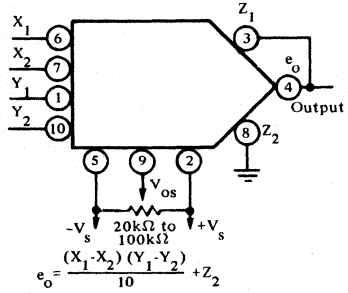
TO-100





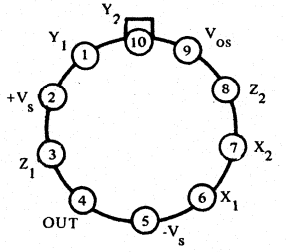
BOTTOM VIEW

CONNECTION DIAGRAM



NOTE: $-V_{os}$ adjustment optional, not normally recommended. Pin 9 may be left open or be grounded.

PIN CONFIGURATION



(TOP VIEW)

TYPICAL PERFORMANCE CURVES

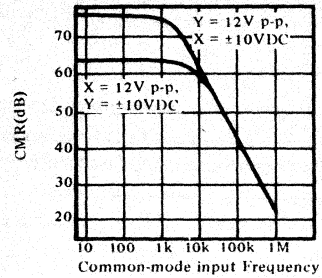


FIGURE 1. Common-mode Rejection vs. Frequency.

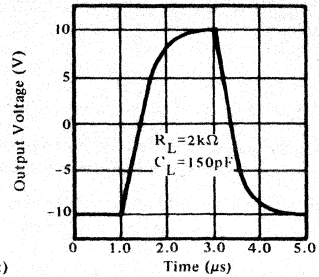


FIGURE 2. Step Response.

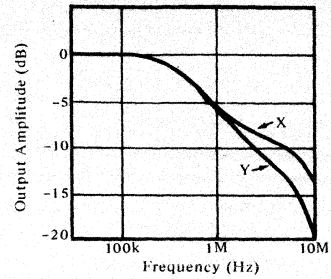


FIGURE 3. Small-signal Frequency Response.

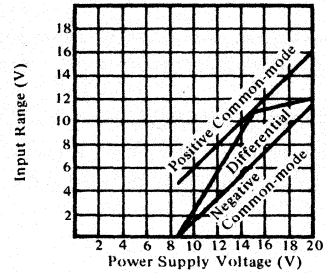


FIGURE 4. Input Range for Linear Response.

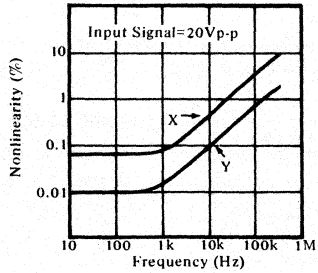


FIGURE 5. Nonlinearity vs. Frequency.

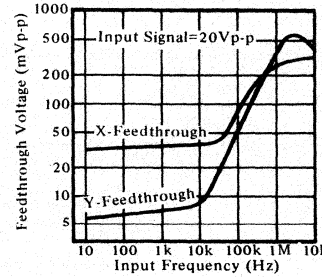


FIGURE 6.Feedthrough vs. Frequency.

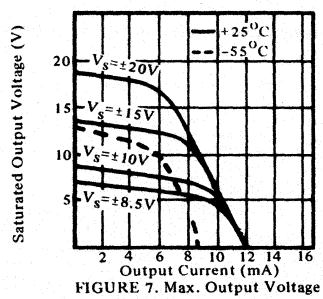


FIGURE 7. Max. Output Voltage vs. Output Current.

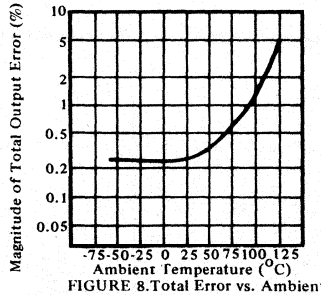


FIGURE 8.Total Error vs. Ambient Temperature.

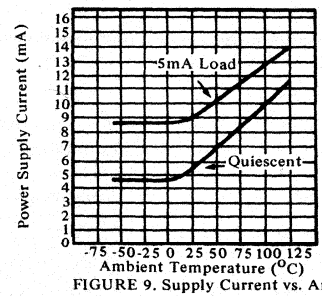


FIGURE 9. Supply Current vs. Ambient Temperature.

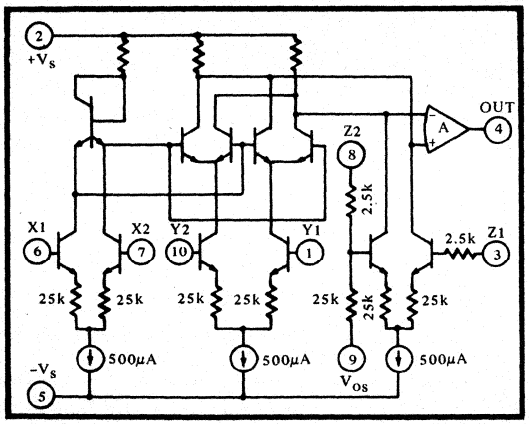


FIGURE 10. Simplified Equivalent Circuit.

OPERATING MODES MULTIPLICATION

The 4213 is a general purpose multiplier/divider with three sets of differential inputs viz. X, Y, and Z. Its open-loop transfer function is

$$e_O = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} - (Z_1 - Z_2)\right]$$

where, A is the open-loop gain of the internal output amplifier (see the simplified equivalent circuit, Figure 10). Due to very high gain ($A \rightarrow \infty$) of the output amplifier the feedback from the output to any of the inputs will establish the relationship

$$Z_1 - Z_2 = (X_1 - X_2)(Y_1 - Y_2)/10$$

Taking output at Z_1 the multiplication mode transfer function is obtained and is expressed as

$$e_O = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2.$$

This connection of 4213 is fully specified and shown on the previous page.

DIVISION

The 4213 may be used as a two quadrant divider, without the need for an external op amp. Note that the output error in the divide mode is approximately given by,

$$\text{Divider error} \simeq \frac{10 \in m}{X_1 - X_2}, \text{ where } \in m \text{ is}$$

the total error specified for the multiply mode. The divider error, as shown above, becomes excessively large for small values of $(X_1 - X_2)$. A 10:1 denominator range is usually the practical limit. This is true for all such units, where a multiplier is used in voltage feedback mode to generate "divide" function.

If more accurate division is required over wide range of denominator voltages, the Burr-Brown model 4291 is recommended (0.25% max error over 100; 1 range).

For optimum performance, the Z offset should be nulled by letting the input be zero and adjusting R_1 for zero output. This offset adjustment will improve the divider error to about $\frac{3 \in m}{(X_1 - X_2)}$ for $(X_1 - X_2)$ much less than 10V.

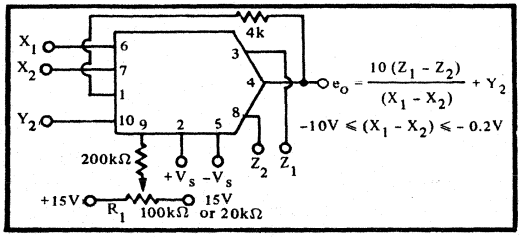


FIGURE 11. Divide Mode Connections - 4213.

SQUARE ROOT

By applying feedback from the output to both the X and Y inputs, the square root function can be obtained. The errors in the square root mode become large for small values of Z input. The actual output is approximately

$$\text{Square root output } e_o = \sqrt{10(Z_1 - Z_2) + 10 \in m}$$

where $\in m$ is the total error for the multiply mode.

Burr-Brown's multifunction converter model 4302 is recommended for applications requiring more accuracy over wider dynamic range.

The output offset should be nulled for optimum performance by allowing the input to be its smallest expected value and adjusting R_1 for the proper output voltage.

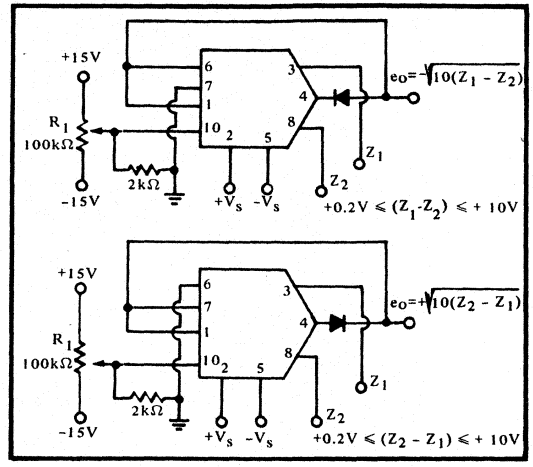


FIGURE 12. Square Root Mode Connections - 4213.

SINE FUNCTION GENERATOR

Two 4213's can be connected with implicit feedback as shown in Figure 13 to implement the following sine function approximation.

$$e_o = \frac{1.5715\, e_i - 0.004317\, e_i^3}{1 + 0.001398\, e_i^2} = 10 \text{ Sin } 9\, e_i$$

The theory and procedures for developing virtually any function generator or linearization circuit can be found in the new Burr-Brown/McGraw Hill book "FUNCTION CIRCUIT - Design and Applications."

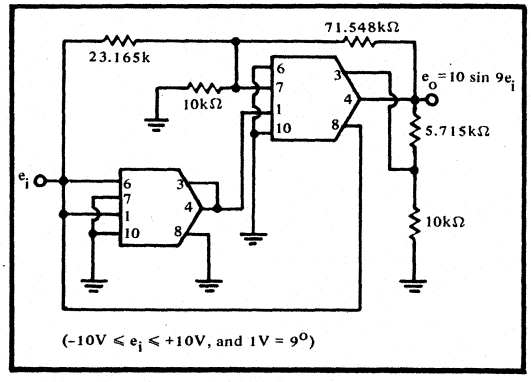
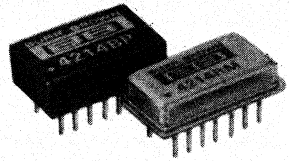


FIGURE 13. Sine Function Connections - 4213.

BURR-BROWN

4214



MULTIPLIER - DIVIDER

FEATURES

- DIFFERENTIAL INPUTS
- LASER-TRIMMED
- GUARANTEED ACCURACY
  0.5% and 1%
- SELF-CONTAINED
  No additional parts required
- LOW NOISE
  120μV rms, 10Hz - 10kHz
- DIP PACKAGES

APPLICATIONS

- MULTIPLICATION
- DIVISION
- SQUARING
- SQUARE ROOTING
- ADAPTIVE CONTROL
- ALGEBRAIC COMPUTATION
- POWER COMPUTATION

DESCRIPTION

The 4214 family of multipliers are low cost integrated circuit multiplier/dividers designed for general purpose usage. In addition to four quadrant multiplication, they also perform division and square rooting of analog signals. They do not require use of additional amplifiers to perform these functions. The 4214 is laser-trimmed prior to final packaging and is guaranteed to its rated accuracy with no external components - a distinct advantage from standpoints of cost and reliability.

4214 contains its own zener regulated references and, as a result is much less sensitive to supply voltage variation than were earlier IC multipliers. The multipliers' output noise is only 120μV rms in a 10Hz to 10kHz bandwidth.

The unit is available in two 14 pin DIP packages. The plastic version ("P" package) is offered for minimum cost and is specified over the -25°C to +85°C range. The hermetic metal package ("M" package option) provides operation over the full -55°C to +125°C temperature range.

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PDS-395

Printed in U.S.A. July, 1978

ELECTRICAL SPECIFICATIONS

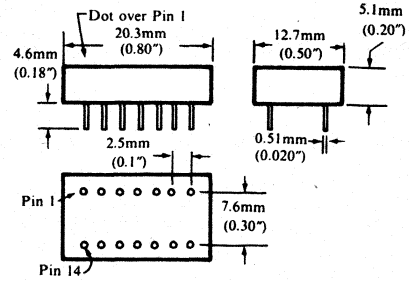
Typical performance at +25°C with rated power supplies unless otherwise noted.

MODEL	4214AP/RM	4214BP/SM
OUTPUT FUNCTION	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$	
TOTAL ERROR[1]		
Without Trimming	1% max	0.5% max
Error vs Temperature (-25°C to +85°C), (AP and BP)	0.008%/°C typ., 0.02%/°C max	
(-55°C to +125°C), (RM and SM)	0.025%/°C typ., 0.05%/°C max	
Error vs Supply	0.05%/%	
INDIVIDUAL ERRORS		
Output Offset	10mV typ	7mV typ
	50mV max	25mV max
vs Temperature	0.7mV/°C typ	0.3mV/°C typ
	2mV/°C max	0.7mV/°C max
vs Supply	0.25mV/%	
Scale Factor Error	0.12%	
vs Temperature	0.008%/°C	
vs Supply	0.05%/%	
Nonlinearity		
X(X = 20V p-p, Y = ±10VDC)	±0.08%	
Y(Y = 20V p-p, X = ±10VDC)	±0.01%	
Feedthrough at 50 Hz		
X = 20V p-p, Y = 0	30mV p-p	
Y = 20V p-p, X = 0	6mV p-p	
vs Temperature	0.1mV p-p/°C	
vs Supply	0.15mV p-p/%	
AC PERFORMANCE		
Small Signal ±3dB Flatness	610 kHz	
Small Signal ±1% Flatness	90 kHz	
Small Signal ±1% Vector Error (0.57° Phase Shift)	7.5 kHz	
Full Power Bandwidth	330 kHz	
Slew Rate	23V/μs	
Settling Time to 1% (20V step)	1.7μs	
OUTPUT NOISE (X = Y = 0)		
10 Hz to 10 kHz	120μV rms	
10 Hz to 10 MHz	700μV rms	
INPUT CHARACTERISTICS		
Input Voltage Range		
Rated Operation, min.	±10V	
Absolute max	±V_s	
Input Impedance, X, Y, Z[2]	10 MΩ	
Input Bias Current, X, Y, Z	1.4μA	
OUTPUT CHARACTERISTICS		
Rated Output	±10V at ±5mA min	
Output Impedance	1.5Ω	
POWER SUPPLY REQUIREMENTS		
Rated Voltage	±15V	
Operating Range	±8.5VDC to ±20VDC	
Quiescent Current	±5.5mA	
TEMPERATURE RANGE	AP and BP	-25°C to +85°C
Rated Performance (specification)	RM and SM	-55°C to +125°C
Operation		-55°C to +125°C
Storage		-65°C to +150°C

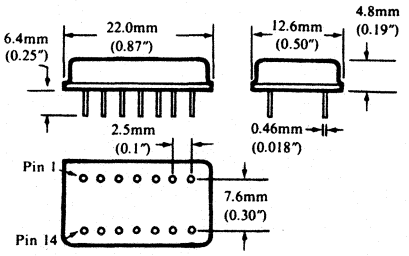
1. Total error is the maximum allowed value of the sum of the individual errors.
2. Z_2 input impedance is 10 MΩ typ with Pin 11 open circuit. If Pin 11 is grounded or used for optional offset adjustment the Z_2 input impedance may become as low as 25kΩ.

MECHANICAL

4214AP, 4214BP
Weight: 2.9 grams (0.10 oz.)

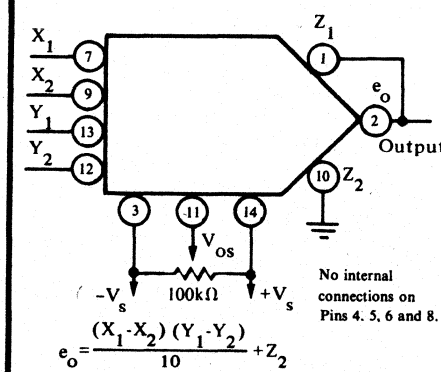


4214RM, 4214SM
Weight: 3.9 grams (0.13 oz.)



Connector: 0145MC (14-pin DIP)
Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)

CONNECTION DIAGRAM



No internal connections on Pins 4, 5, 6 and 8.

$$e_o = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$$

NOTE: V_{OS} adjustment optional, not normally recommended. Pin 11 may be left open or grounded.

TYPICAL PERFORMANCE CURVES

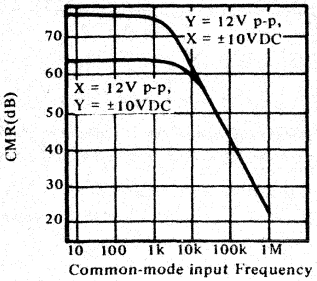


FIGURE 1. Common-mode Rejection vs. Frequency.

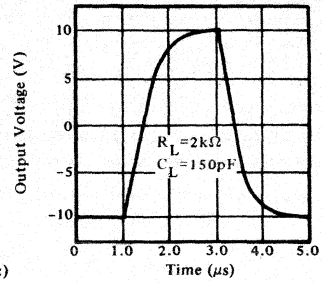


FIGURE 2. Step Response.

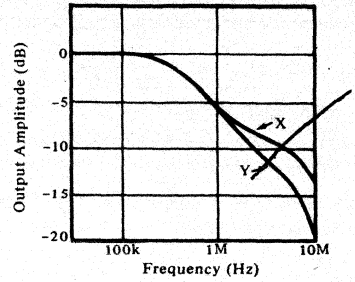


FIGURE 3. Small-signal Frequency Response.

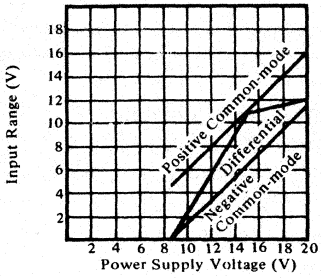


FIGURE 4. Input Range for Linear Response.

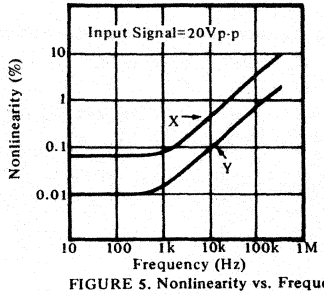


FIGURE 5. Nonlinearity vs. Frequency.

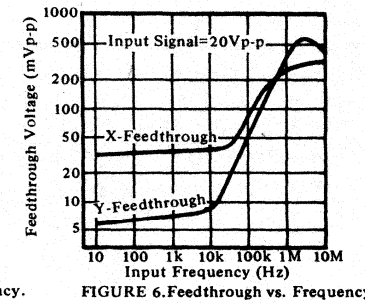


FIGURE 6.Feedthrough vs. Frequency.

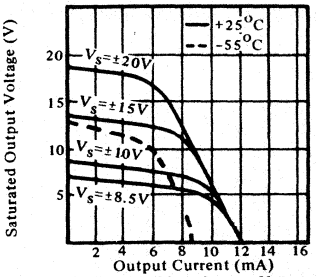


FIGURE 7. Max. Output Voltage vs. Output Current.

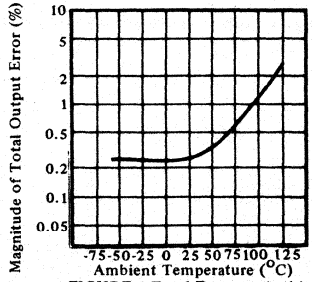


FIGURE 8.Total Error vs. Ambient Temperature.

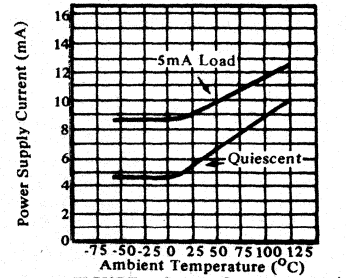


FIGURE 9. Supply Current vs. Ambient Temperature.

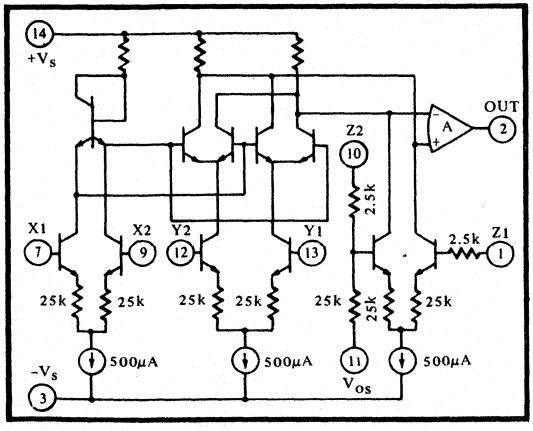


FIGURE 10. Simplified Equivalent Circuit.

OPERATING MODES MULTIPLICATION

The 4214 is a general purpose multiplier/divider with three sets of differential inputs viz. X, Y, and Z. Its open-loop transfer function is

$$e_o = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} - (Z_1 - Z_2)\right]$$

where, A is the open-loop gain of the internal output amplifier (see the simplified equivalent circuit, Figure 10). Due to very high gain ($A \rightarrow \infty$) of the output amplifier the feedback from the output to any of the inputs will establish the relationship

$$Z_1 - Z_2 = (X_1 - X_2)(Y_1 - Y_2)/10$$

Taking output at Z_1 the multiplication mode transfer function is obtained and is expressed as

$$e_o = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2.$$

This connection of 4214 is shown on the previous page.

DIVISION

The 4214 may be used as a two quadrant divider, without the need for an external op amp. Note that the maximum output error in the divide mode is given approximately by,

$$\text{Divider error} \simeq \frac{10 \in m}{X_1 - X_2}, \text{ where } \in m \text{ is}$$

the total error specified for the multiply mode. The divider error, as shown above, becomes excessively large for small values of $(X_1 - X_2)$. A 10:1 denominator range is usually the practical limit. This is true for all such units, where a multiplier is used in voltage feedback mode to generate "divide" function.

If more accurate division is required over wide range of denominator voltages, the Burr-Brown model 4291 is recommended (0.25% max error over 100:1 range).

For optimum performance, the Z offset should be nulled by letting the input be zero and adjusting R_1 for zero output. This offset adjustment will improve the divider error to about $\frac{3 \in m}{(X_1 - X_2)}$ for $(X_1 - X_2)$ much less than 10V.

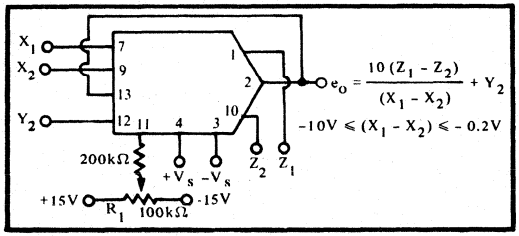


FIGURE 11. Divide Mode Connections - 4214.

SQUARE ROOT

By applying feedback from the output to both the X and Y inputs, the square root function can be obtained. The errors in the square root mode become large for small values of Z input. The actual output is approximately

$$\text{Square root output } e_O = \sqrt{10 (Z_1 - Z_2) + 10 \in m}$$

where $\in m$ is the total error for the multiply mode.

Burr-Brown's multifunction converter model 4302 is recommended for applications requiring more accuracy over wider dynamic range.

The output offset should be nulled for optimum performance by allowing the input to be its smallest expected value and adjusting R_1 for the proper output voltage.

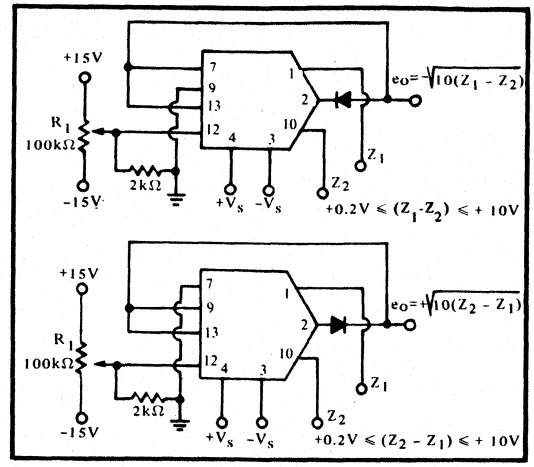


FIGURE 12. Square Root Mode Connections - 4214.

SINE FUNCTION GENERATOR

Two 4214's can be connected with implicit feedback as shown in Figure 13 to implement the following sine function approximation.

$$e_O = \frac{1.5715\, e_i - 0.004317\, e_i^3}{1 + 0.001398\, e_i^2} = 10 \text{ Sin } 9\, e_i$$

The theory and procedures for developing virtually any function generator or linearization circuit can be found in the new Burr-Brown/McGraw Hill book "FUNCTION CIRCUIT - Design and Applications."

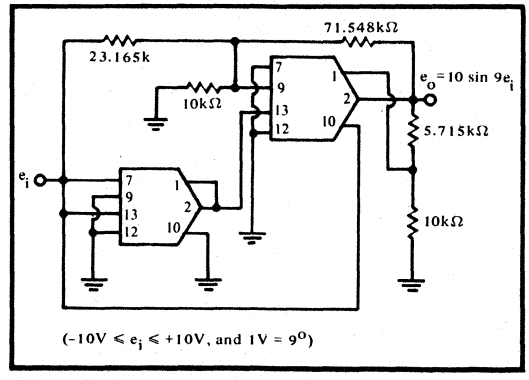


FIGURE 13. Sine Function Connections - 4214.

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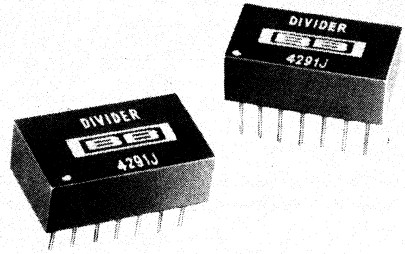

4291

ANALOG DIVIDER

FEATURES

- **HIGH ACCURACY**
  0.25% max for D ⩾ 100mV
- **EASY TO USE**
  No external components required
- **WIDE DYNAMIC RANGE**
  10mV < D < 10V
- **SMALL SIZE**
  14 pin dual-in-line package

DESCRIPTION

The 4291 hybrid IC divider offers high accuracy over a 100 to 1 dynamic range with no external components required, and the specified accuracy can be achieved with denominator voltages as low as 100mV.

The unique circuit approach produces a two-quadrant divider with performance that exceeds that of conventional multiplier/dividers. With the addition of several external resistors to null the offset and gain errors, an accuracy of 0.1% can be achieved with denominator voltages down to 10mV.

Manufacturers of industrial control systems and analytical instruments will find the 4291 to be a low cost, accurate solution to many of their signal processing problems.

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PDS-336A

Printed in U.S.A. July, 1978

DEFINITION OF SPECIFICATIONS

ACCURACY: The accuracy of the divider is specified as a percent of full scale (10V) and is derived from the total error specification.

TOTAL ERROR: The total error specification means that at +25°C with ±15V supplies, the divider output will always be within the specified percentage (of full scale) of the ideal transfer function, $E_O = 10\frac{N}{D}$ for D greater than the specified voltages and for $N \leq D$.

Beware of analog dividers which only specify total error for D = 10V or do not specify error drift for D < 10V. In some cases the errors for D = 0.1V may be 100 times the error at D = 10V.

SCALE FACTOR ERROR: With N = D = 10V and the output offset zeroed, scale factor error represents the difference between the actual voltage and 10.000V.

NON-LINEARITY: With D = 10V, non-linearity is defined as the departure of $\frac{E_O}{E_i}$ from a straight line when N varies between 5 mV and 10V. Non-linearity is best observed on an oscilloscope or x-y plotter. (See Figure 6.)

DYNAMIC PERFORMANCE: The frequency response specifications are generally self-explanatory. Small signal -3dB bandwidth is typically 400 kHz.

OVERLOAD RECOVERY: Overload recovery is the time required for E_O to settle within 50 mV of final value if N or D are first driven negative or if the output saturates (N > D). In contrast, overload recovery may require as much as 1 sec. if a "chopper" (modulation) type multiplier is used for division.

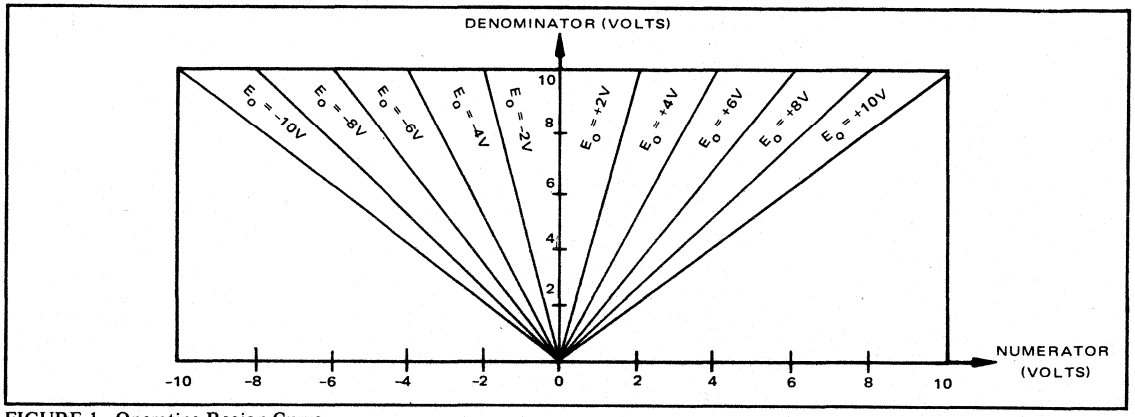


FIGURE 1. Operating Region Curve

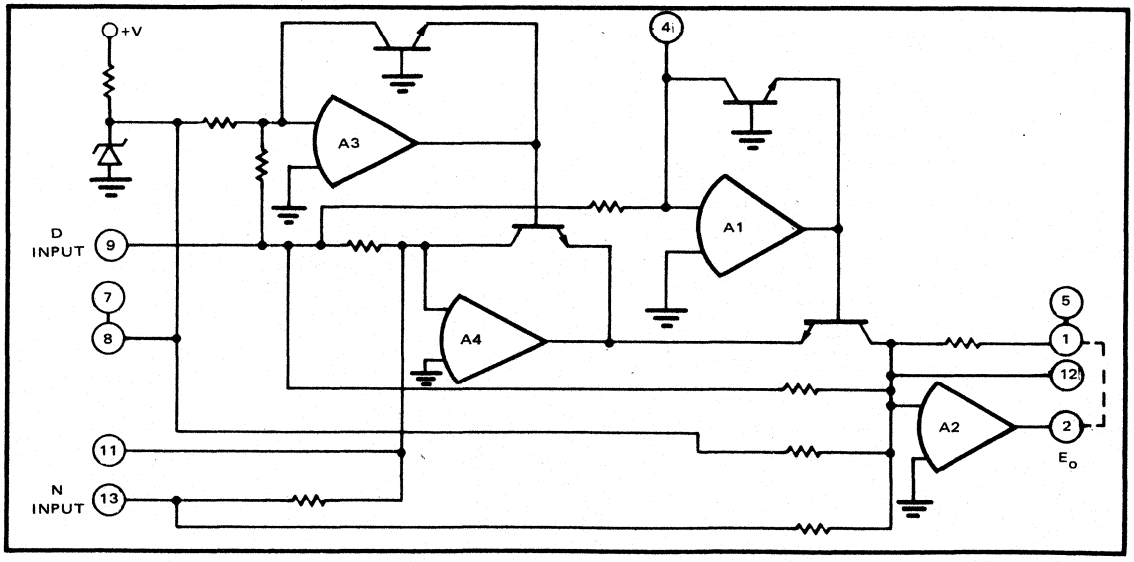


FIGURE 2. Simplified Schematic.

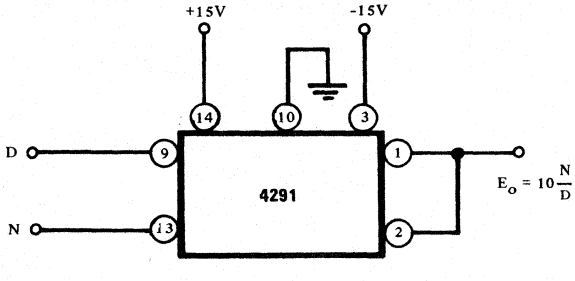
SPECIFICATIONS

Typical performance at +25°C with rated power supplies unless otherwise noted.

Percent specifications refer to % of full scale (10V)

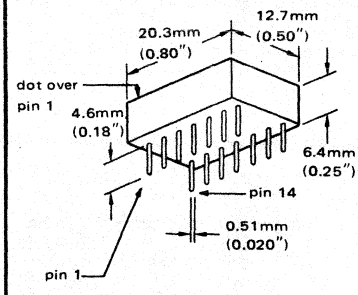
ELECTRICAL

MODEL	4291 H	4291 J	4291 K
Transfer Function	$E_o = 10\frac{N}{D}$		
ACCURACY			
Total Error			
No external trims, (max), D > 100 mV	1%	0.5%	0.25%
With external trims, D > 10 mV	0.25%	0.1%	0.1%
Error vs. Temperature	0.03%/°C		
Error vs. Supply	0.15%/%		
AC PERFORMANCE, D = +10V			
Small signal, -3dB	400 kHz		
Full Power Response	20 kHz		
0.5% amplitude error	15 kHz		
0.5% vector error	600 Hz		
Slew rate	1.25 V/μsec		
INPUT CHARACTERISTICS			
Rated Input voltages	-10V ≤ N ≤ +10V +10mV ≤ D ≤ +10V and |N| ≤ D		
Maximum safe level, N,D	± supply		
Input Impedance N,D	25 kΩ		
OUTPUT CHARACTERISTICS			
Rated output voltage, min	±10V		
Rated output current, min	±5mA		
Output Impedance	0.1Ω		
Output Noise, 10 Hz to 10 kHz	See Figure 4		
TEMPERATURE RANGE			
Specified Performance	0°C to +70°C		
Operating	-25°C to +85°C		
Storage	-55°C to +125°C		
POWER SUPPLY REQUIREMENTS			
Rated supply	±15VDC		
Operating range	±14 to ±16VDC		
Quiescent current	+15mA, -8.5mA		



DIVIDE MODE CONNECTION

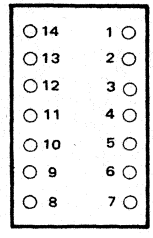
MECHANICAL



Row Spacing: 7.6mm (0.300")
Weight: 3.4 grams (0.12 oz.)
Connector: 14 pin DIP

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std 202.

PIN CONNECTIONS



(BOTTOM VIEW)

1 Gain Error Adjust
2 Output
3 -15VDC
4 D Input Offset Adj.
5 Internally connected to Pin 1
6 Internally connected to Pin 14
7 Internally connected to Pin 8
8 Reference Voltage
9 D Input
10 Common
11 N Input Offset Adjust
12 Output Offset Adjust
13 N Input
14 +15VDC

TYPICAL PERFORMANCE CURVES

Typical Performance @ 25°C and Rated Supplies

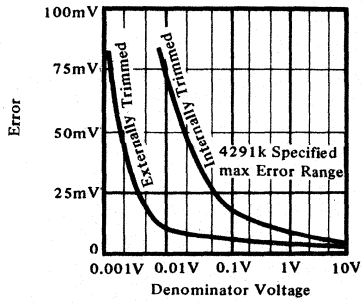


FIGURE 3. Output Error vs. Denominator Voltage

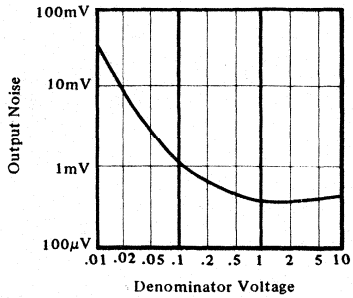


FIGURE 4. Output Noise vs. Denominator Voltage

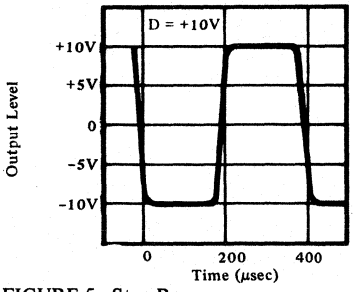


FIGURE 5. Step Response

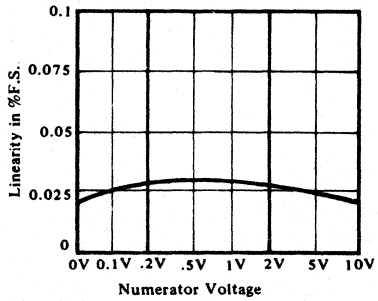
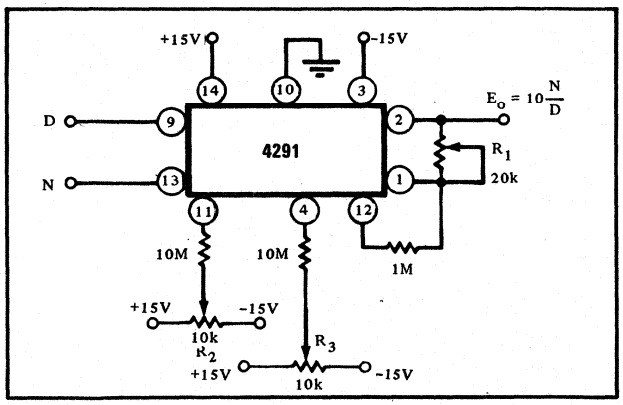


FIGURE 6. Linearity vs. Numerator Voltage

OPTIONAL ADJUSTMENT PROCEDURES



By following this adjustment procedure, the accuracy and dynamic range of the 4291 can be improved, as indicated in the Electrical Specification table. Note that the numerator gain is 1,000 when D = 10 mV, so the accuracy drift will normally be somewhat worse than 0.03%/°C which applies for D ≥ 100 mV.

1. With N = D = 10.000 V ±1 mV, adjust R_1 such that E_o = +10.000 V ±1 mV.
2. Set D at the minimum expected denominator voltage. With N = -D adjust R_2 such that E_o = -10.000 V.
3. Set D at the minimum expected denominator voltage. With N = D adjust R_3 such that E_o +10.000 V.
4. Repeat steps 2 and 3 until no more trimming is required. Check step 1. If adjustment is required, repeat procedure until desired accuracy is attained.

BURR-BROWN

4301

Low Cost MULTIFUNCTION CONVERTER

FEATURES

- LOW COST
- SMALL PACKAGE - Dual-in-line
- HERMETIC, SHIELDED PACKAGE
- UNIVERSAL CONVERTER

FUNCTIONS	ACCURACY
MULTIPLY	±0.25%
DIVIDE	±0.25%
SQUARE	±0.03%
SQUARE ROOT	±0.07%
EXPONENTIATE	±0.15% (m = 5)
ROOTS	±0.2% (m = .2)
SINE θ	±0.5%
COSINE θ	±0.8%
TAN $^{-1}$ (Y/X)	±0.6%
$\sqrt{X^2 + Y^2}$	±0.07%

Typical accuracies expressed as a % of output full scale (+10VDC) at 25°C.

DESCRIPTION

Burr-Brown's multifunction converter model 4301 is a low cost solution to many analog conversion needs. Much more than just another multiplier/divider, the 4301 out performs many analog circuit functions with a very high degree of accuracy at a very low total cost to the user.

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PDS-307E

Printed in U.S.A. July, 1978

MULTIFUNCTION CONVERTER

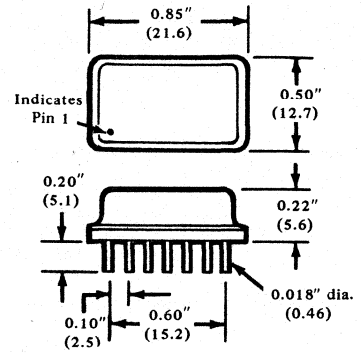
MODEL 4301
GENERAL SPECIFICATIONS

Performance typical at 25°C and with rated supply unless otherwise noted.

MODEL	4301
TRANSFER FUNCTION	$E_O = V_Y \left(\frac{V_Z}{V_X}\right)^m$
RATED OUTPUT	
Voltage	+10.0 V
Current	5 mA
INPUT	
Signal Range	$0 \leq (V_X, V_Y, V_Z) \leq +10$ V
Absolute Maximum	$(V_X, V_Y, V_Z) \leq \pm 18$ V
Impedance (X/Y/Z)	100 kΩ/90 kΩ/100 kΩ
EXPONENT RANGE	
Roots ($0.2 \leq m < 1$)	$m = \frac{R_2}{R_1 + R_2}$ Refer to Functional Diagram below
Powers ($1 < m \leq 5$)	$m = \frac{R_1 + R_2}{R_2}$
($m = 1$)	$R_1 = 0\ \Omega$, R_2 not used
POWER REQUIREMENTS	
Rated Supply	±15 Vdc
Range	±12 to ±18 Vdc
Quiescent Current	±10 mA
TEMPERATURE RANGE	
Operating	-25°C to +85°C
Storage	-25°C to +85°C

MECHANICAL

Dimensions in millimeters are shown in parentheses.

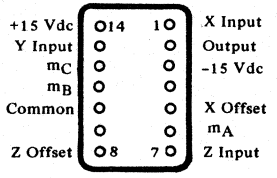


PIN SPACING: 0.30" (7.6)
CASE - Kovar or equiv.
WEIGHT - .15 oz (3.4 grams)
CONNECTOR - 14 pin DIP connector
(Burr-Brown Model No. 0145MC)

ROW SPACING: 0.30" (7.6)

Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]

PIN CONNECTIONS



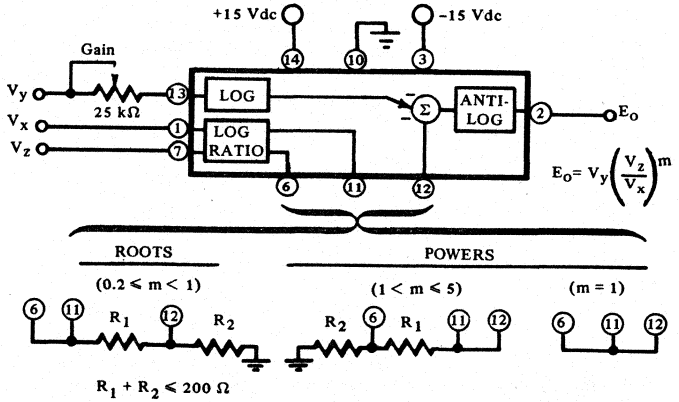
(BOTTOM VIEW)

General specifications for the Model 4301 Multifunction Converter are presented on this page. These specifications characterize the 4301 as a versatile three input multifunction converter.

The following pages are applications oriented to help you apply the 4301 to your particular circuit function need. These pages contain dedicated circuit configurations in order to produce the functions of: multiplication, division, exponentiation, square rooting, squaring, sine, cosine, arctangent, and vector algebra.

It is the purpose of this product data sheet to enable you to apply the 4301 to your analog conversion needs quickly and efficiently.

4301 FUNCTIONAL DIAGRAM

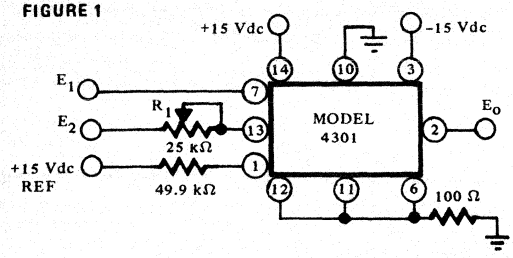


MULTIPLIER/DIVIDER FUNCTIONS

MULTIPLIER

In multiplier applications the 4301 will provide high accuracy at a low cost. The 4301 will accept inputs from 0 to +10 Vdc and provide a typical accuracy of ±0.25% of full scale.

FIGURE 1



NOTE:
(1) Set R_1 so that with $E_1 = E_2 = +10.00$ Vdc, $E_o = +10.00$ Vdc.

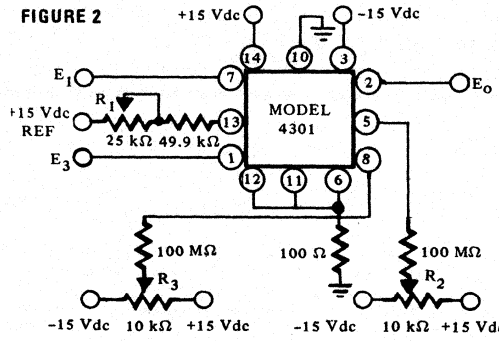
Transfer Function	$E_o = + \frac{E_1 E_2}{10}$
ACCURACY	
Total Errors	
Typical at +25°C	±25 mV
Maximum at +25°C	±50 mV
(for input range)	0.01 V ≤ E_1 ≤ 10 V 0.01 V ≤ E_2 ≤ 10 V
vs. Temperature	±1 mV/°C
Offset Errors ($E_1 = E_2 = 0$)	
Output Offset (at 25°C)	±10 mV
vs. Temperature	±0.2 mV/°C
NOISE (10 Hz to 1 kHz)	100 μV rms
BANDWIDTH (E_1, E_2)	
Small Signal (-3 dB)	500 kHz
Full Output	60 kHz

DIVIDER

As a divider, the 4301 will out-perform many of the multiplier/dividers on the market at a much lower cost. In the divider configuration the 4301 boasts a typical conversion accuracy of ±0.25% of full scale for input from 0 to +10 Vdc.

Transfer Function	$E_o = +10 (E_1/E_3)$
ACCURACY	
Total Errors	
Typical at +25°C	±25 mV
Maximum at +25°C	±50 mV
(for $E_1 \leq E_3$ and input range)	0.01 V ≤ E_1 ≤ 10 V 0.1 V ≤ E_3 ≤ 10 V
vs. Temperature	±1 mV/°C
Offset Errors ($E_1 = 0$, $E_3 = +10$ V)	
Output Offset (at 25°C)	±10 mV
vs. Temperature	±1 mV/°C
NOISE (10 Hz to 1 kHz)	
$E_3 = +10$ V	100 μV rms
$E_3 = +0.1$ V	300 μV rms
BANDWIDTH (E_1, E_3)	
Small Signal (-3 dB)	500 kHz
Full Output	
($E_3 = +10$ V)	60 kHz

FIGURE 2

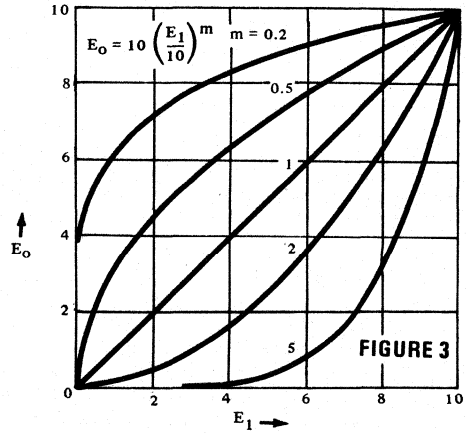


NOTES:
(1) Set R_1 so that with $E_1 = E_3 = +10.00$ Vdc, $E_o = +10.00$ Vdc.
(2) Set R_2 so that with $E_1 = E_3 = +0.10$ Vdc, $E_o = +10.00$ Vdc.
(3) Set R_3 so that with $E_1 = +0.01$ Vdc and with $E_3 = +0.10$ Vdc, $E_o = +1.00$ Vdc.
(4) Repeat steps 1 through 3 as necessary to achieve the specified output voltages.

EXPONENTIAL FUNCTIONS

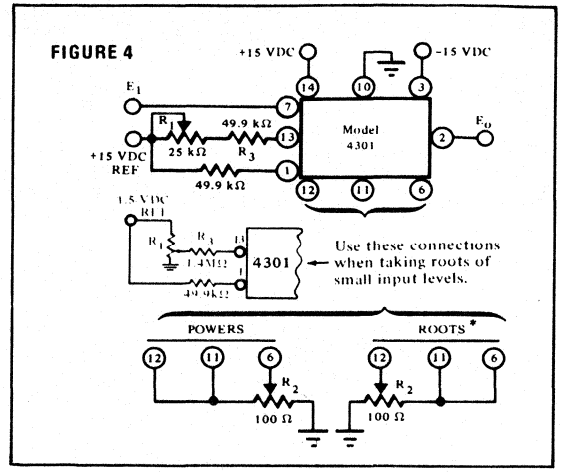
Model 4301 may be used as exponentiator over a range of exponents from 0.2 to 5. The exponents .5 and 2, square rooting and squaring respectively are often used functions and are treated below. Other values of exponents (m) may be useful in terms of linearization of nonlinear functions or simply for producing the mathematical conversions. Characteristics of m = .2 and m = 5 are presented on the right. For other values of m the curves presented in Figure 3 may be used to interpolate the error for a nonspecified value of m.

Transfer Function	$E_o = 10 \left(\frac{E_1}{10}\right)^m$
Total Conversion Error (typical)	
m = 0.2	
0.5 Vdc < E_1 ≤ 10 Vdc	±2 m Vdc
0.1 Vdc < E_1 ≤ 0.5 Vdc	±25 m Vdc
m = 5	
1.0 Vdc < E_1 ≤ 10 Vdc	±15 m Vdc
Exponent Range (continuous)	0.2 ≤ m ≤ 5
Input Voltage Range	0 to +10 Vdc
Output Voltage Range	0 to +10 Vdc



Exponentiator Transfer Characteristics

NOTES:
(1) Connect a 100 Ω potentiometer as shown in Figure 4 for either roots ($0.2 \leq m < 1$) or powers ($1 < m \leq 5$).
(2) Set R_1 so that with E_1 = +10.00 Vdc, E_o = +10.00 Vdc.
(3) Select a + dc voltage level (E_1) such that the output voltage (E_o), as acted upon by the desired exponent, will not exceed +10.00 Vdc. A level which is mid-range for input values of interest is an appropriate one to use. Set R_2 so that the output voltage (E_o) is the value expected for the chosen values of input (E_1) and exponent (m).



(4) Repeat steps (2) through (4) as necessary.

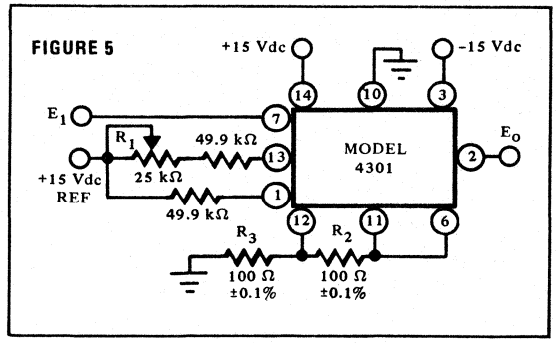
* When taking roots of smaller input levels, a modified transfer equation [$E_o = (10E_1)^m$] will provide improved conversion accuracy. To achieve this transfer function: 1) apply a +1.5 Vdc REF in place of the +15 Vdc REF shown in Figure 4., 2) make R_3 a 1.40 MΩ resistor, and 3) follow all notes except in note (2) apply +0.10 Vdc to pin 7 to set R_1 for E_o = +1.00 Vdc.

SQUARE ROOT

As a Square Rooter (m = 0.5), the 4301 provides a typical total conversion accuracy of ±0.07%. Refer to Figure 5 and notes for connections and adjustments respectively.

Transfer Function	$E_o = 10\sqrt{\frac{E_1}{10}}$
Total Conversion Error (Typical)	
0.5 Vdc < E_1 ≤ 10 Vdc	±7 mV
.02 Vdc < E_1 ≤ 0.5 Vdc	±55 mV
Input Voltage Range	0 to +10 Vdc
Output Voltage Range	0 to +10 Vdc

NOTES:
(1) Connect pins 12, 11, and 6 together. Set R_1 such that with E_1 = +10.00 Vdc; E_o = +10.00 Vdc.
(2) Connect 100 Ω resistors as shown in Figure 5.
(3) For greater conversion accuracy, R_2 & R_3 may be replaced by a potentiometer as shown in Figure 4.

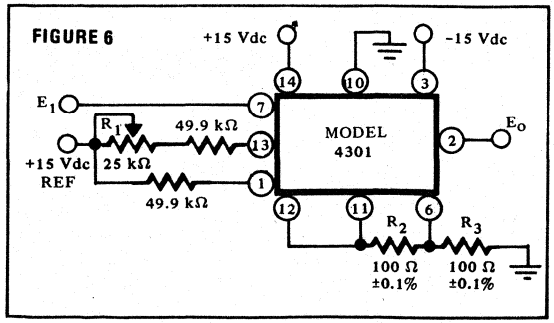


SQUARE

Configured as a Square Function Converter (m = 2), the 4301 will produce high conversion accuracies of typically 0.03%. Please refer to Figure 6 and accompanying notes.

Transfer Function	$E_o = 10\left(\frac{E_1}{10}\right)^2$
Total Conversion Error (typical)	
0.1 Vdc ≤ E_1 ≤ 10 Vdc	±3 mV
Input Voltage Range	0 to +10 Vdc
Output Voltage Range	0 to +10 Vdc

NOTES:
(1) Set R_1 such that with E_1 = +10.00 Vdc, E_o = +10.00 Vdc.
(2) Connect 100 Ω resistors as shown in Figure 6.
(3) For greater conversion accuracy R_2 & R_3 may be replaced by a potentiometer as shown in Figure 4.



TRIGONOMETRIC FUNCTIONS

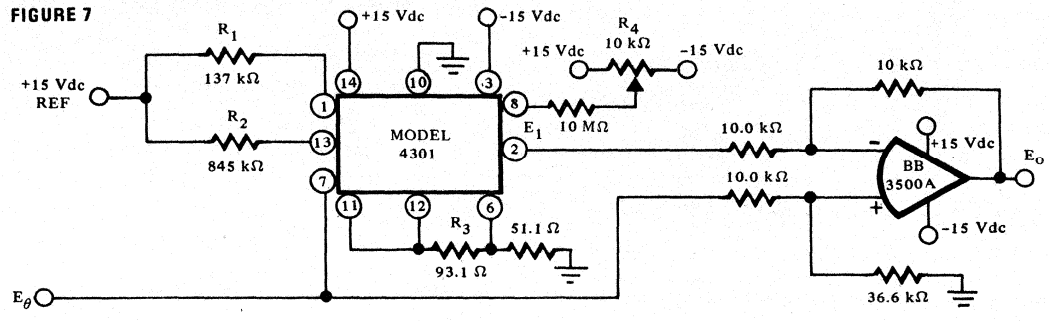
SINE

Sine functions can be accurately generated from input voltage levels representing angular displacement from 0 to 90°. Model 4301 configured as in Figure 7 will produce the sine power series approximations with modified coefficients to typically better than ±0.5% of full scale. In this circuit, the 4301 is scaled so that when $\theta = 0$, $E_O = 0$ Vdc, and when $\theta = 90$, $E_O = 10$ Vdc.

NOTES:
(1) Adjust R_4 if needed so that $E_1 < 1$ m Vdc when $E_\theta = 0$.
(2) Adjust R_2 so that $E_1 = +0.8045$ Vdc when $E_\theta = +5.00$ Vdc.
(3) Adjust R_3 so that $E_1 = +5.709$ Vdc when $E_\theta = +10.00$ Vdc.
(4) Repeat steps (2) and (3) as necessary.

Transfer Function	$E_O = 10 \text{ Sin } 9E_\theta$
Power Series Approximation $E_O = 1.5708E_\theta - 1.5924\left(\frac{E_\theta}{6.366}\right)^{2.827}$	
Total Conversion Error (typical)	±50 mV
Input Voltage Range ($0 \leq \theta \leq 90^o$)	0 to +10 Vdc
Output Voltage Range ($0 \leq \sin\theta \leq 1$)	0 to +10 Vdc

FIGURE 7



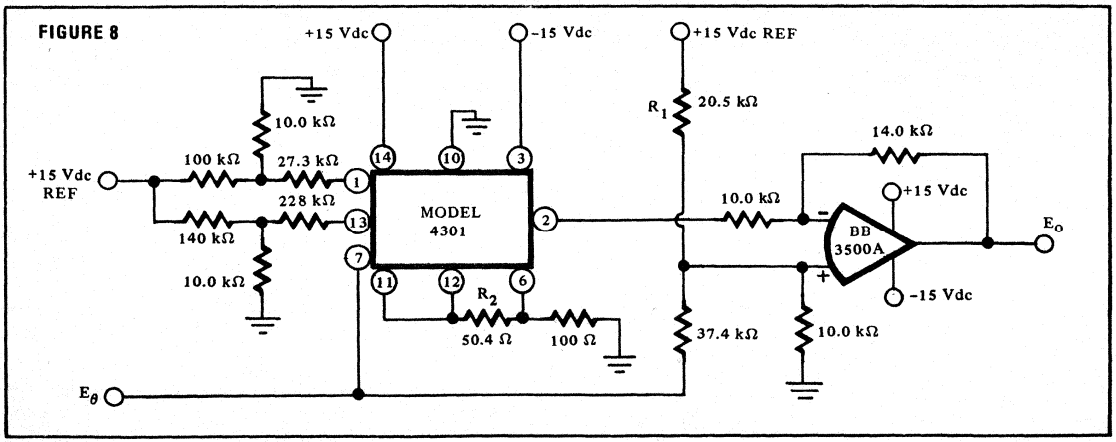
COSINE

Connected as in Figure 2, the Model 4301 will generate a cosine function of the input voltage. Typical accuracies of ±0.8% can be expected from this configuration.

NOTES:
(1) Adjust R_1 so that $E_O = +10.00$ Vdc when $E_\theta = 0$.
(2) Adjust R_2 so that $E_O = 0$ when $E_\theta = +10.00$ Vdc.

Transfer Function	$E_O = 10 \cos 9E_\theta$
Power Series Approximation $E_O = 10 + 0.3652\ E_\theta - 0.4276E^{1.504}$	
Total Conversion Error (typical)	±80 mV
Input Voltage Range ($0 \leq \theta \leq 90^o$)	0 Vdc to +10 Vdc
Output Voltage Range ($1 \leq \cos\theta \leq 0$)	+10 Vdc to 0 Vdc

FIGURE 8



ARCTANGENT

Model 4301 and the associated circuitry shown below will produce the inverse tangent of a ratio. This application is particularly well suited to conversion from rectangular coordinates to polar coordinates where

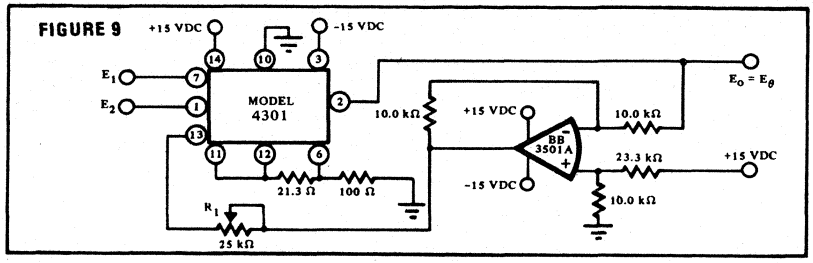
$$E_\theta = \tan^{-1}\frac{E_y}{E_x}$$

The accuracy of conversion depends upon the levels of the input signals. Please refer to table at right.

Transfer Function	$E_o = \tan^{-1}\left(\frac{\lvert E_1\rvert}{\lvert E_2\rvert}\right)$
Power Series Approximation	$E_o = \frac{\left(\frac{\lvert E_1\rvert}{\lvert E_2\rvert}\right)^{1.2125}}{1+\left(\frac{\lvert E_1\rvert}{\lvert E_2\rvert}\right)^{1.2125}}(90^o)$
Total Conversion Error $2 < E_1, E_2 \leq 10$ VDC $0.1 < E_1, E_2 \leq 2$ VDC $0.03 < E_1, E_2 \leq 0.1$ VDC Input Voltage Range (E_1, E_2) Output Voltage Range $0 \leq E_\theta \leq 90^o$	 ±55 m VDC ±65 m VDC ±340 m VDC +0.01 VDC to +10 VDC 0 VDC to +9 VDC

NOTE:
(1) Set R_1 so that with $E_1 = E_2 = +10.000$ VDC, $E_o = +4.500$ VDC ±1 mVDC.

FIGURE 9



VECTOR MAGNITUDE FUNCTION

The model 4301 will produce the square root of the sum of the squares of two inputs. This function is companion to the arctangent of a ratio for the conversion of rectangular to polar coordinates.

Transfer Function	$E_o = \sqrt{E_1^2 + E_2^2}$
Input Voltage Range E_1 E_2	0 to +10VDC -10VDC to +10VDC
(refer to notes 1 and 2)	
Output Voltage Range	0 to +10VDC
Conversion Error	±7m VDC

NOTES:

1. Figure 10 shows one practical way to implement the transfer function $E_o = \sqrt{E_1^2 + E_2^2}$ using 4301. It shows use of model 3501A op amp. Model 3501's rated output is ±10V. This limits the range of E_1 and E_2, such that the conditions $E_1 \leq \sqrt{100 - E_2}$ and $|E_2| \leq (5 - E_1^2/20)$ and $\sqrt{E_1^2 + E_2^2} \leq 10$ are always satisfied.
   (a) The above conditions imply, $0V \leq E_1 \leq 10V$ and $-5V \leq E_2 \leq 5V$.
   (b) The above conditions also imply that for applications where $E_1 = |E_2|$ the range would be limited to 4.142V max.
2. Use of model 3627 as shown in Figure 11 would directly substitute the eight 10kΩ resistors and the two model 3501A op amps. This would reduce the number of components needed to implement vector magnitude function and reduce overall cost.

FIGURE 10

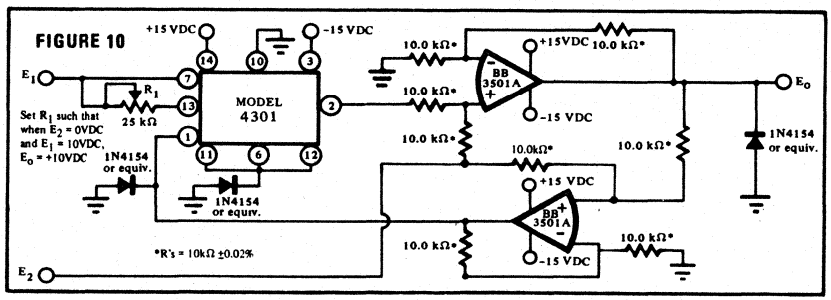
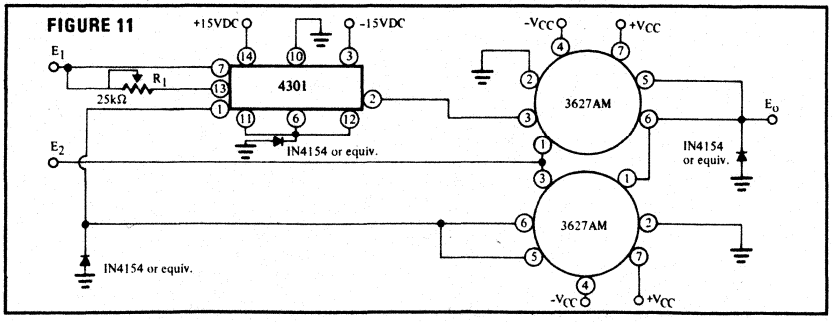
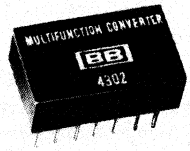


FIGURE 11



BURR-BROWN

4302



Low Cost MULTIFUNCTION CONVERTER

FEATURES

- LOW COST
- SMALL PACKAGE - Dual-in-line
- RELIABLE HYBRID CONSTRUCTION
- VERSATILE

FUNCTIONS	ACCURACY
MULTIPLY	±0.25%
DIVIDE	±0.25%
SQUARE	±0.03%
SQUARE ROOT	±0.07%
EXPONENTIATE	±0.15% (m = 5)
ROOTS	±0.2% (m = .2)
SINE θ	±0.5%
COSINE θ	±0.8%
TAN $^{-1}$ (Y/X)	±0.6%
$\sqrt{X^2 + Y^2}$	±0.07%

Typical accuracies expressed as a % of output full scale (+10VDC) at 25°C.

DESCRIPTION

Burr-Brown's multifunction converter model 4302 is a low cost solution to many analog conversion needs. Much more than just another multiplier/divider, the 4302 out performs many analog circuit functions with a very high degree of accuracy at a very low total cost to the user.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-326C

Printed in U.S.A. July, 1978

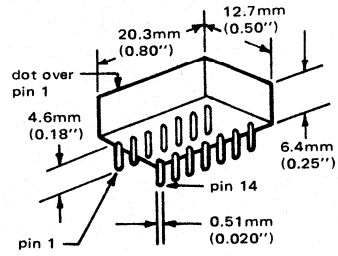
SPECIFICATIONS

Performance typical at 25°C and with rated supply unless otherwise noted.

ELECTRICAL

MODEL	4302
TRANSFER FUNCTION	$E_O = V_Y \left(\frac{V_Z}{V_X}\right)^m$
RATED OUTPUT	
Voltage	+10.0 V
Current	5 mA
INPUT	
Signal Range	$0 \leq (V_X, V_Y, V_Z) \leq +10$ V
Absolute Maximum	$(V_X, V_Y, V_Z) \leq \pm 18$ V
Impedance (X/Y/Z)	100 kΩ/90 kΩ/100 kΩ
EXPONENT RANGE	
Roots ($0.2 \leq m < 1$)	$m = \frac{R_2}{R_1 + R_2}$ Refer to Functional Diagram below
Powers ($1 < m \leq 5$)	$m = \frac{R_1 + R_2}{R_2}$
($m = 1$)	$R_1 = 0\ \Omega$, R_2 not used
POWER REQUIREMENTS	
Rated Supply	±15 VDC
Range	±12 to ±18 VDC
Quiescent Current	±10 mA
TEMPERATURE RANGE	
Operating	-25°C to +85°C
Storage	-55°C to +125°C

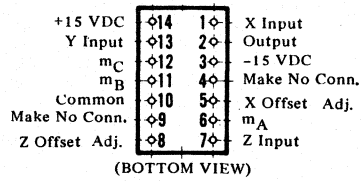
MECHANICAL



Row Spacing: 7.6mm (0.300")
Weight: 3.4 grams (0.12 oz.)
Connector: 14-pin DIP
0145MC

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std-202.

PIN CONNECTIONS



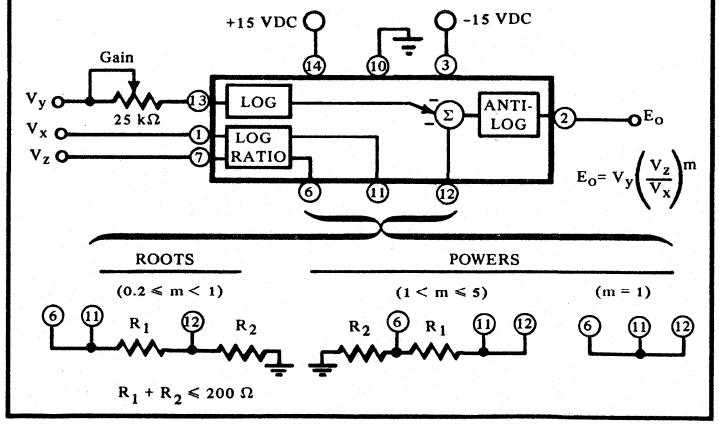
(BOTTOM VIEW)

General specifications for the Model 4302 Multifunction Converter are presented on this page. These specifications characterize the 4302 as a versatile three input multifunction converter.

The following pages are applications oriented to help you apply the 4302 to your particular circuit function need. These pages contain dedicated circuit configurations in order to produce the functions of: multiplication, division, exponentiation, square rooting, squaring, sine, cosine, arctangent, and vector algebra.

It is the purpose of this product data sheet to enable you to apply the 4302 to your analog conversion needs quickly and efficiently.

4302 FUNCTIONAL DIAGRAM



Many of the following circuit configurations using the 4302 require a reference voltage for scaling purposes. The reference voltage is shown to be +15 VDC (+15 VDC REF.) since in most cases the +15 VDC power source for the 4302 has sufficient time and temperature related stability to achieve the specified typical accuracies.

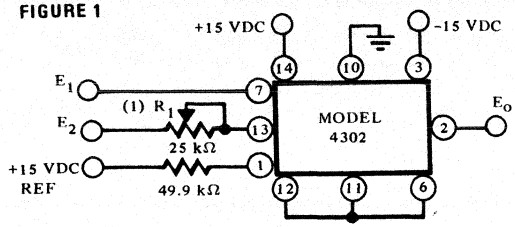
If the particular supplies which are available for powering the 4302 do not have the necessary stability for the required conversion accuracy, an additional +15 VDC precision supply may be required.

MULTIPLIER/DIVIDER FUNCTIONS

MULTIPLIER

In multiplier applications the 4302 provides high accuracy at a low cost. The 4302 accepts inputs up to +10 VDC and provides a typical accuracy of ±0.25% of full scale.

FIGURE 1



(1) Set R_1 so that with $E_1 = E_2 = +10.00$ VDC, $E_o = +10.00$ VDC.

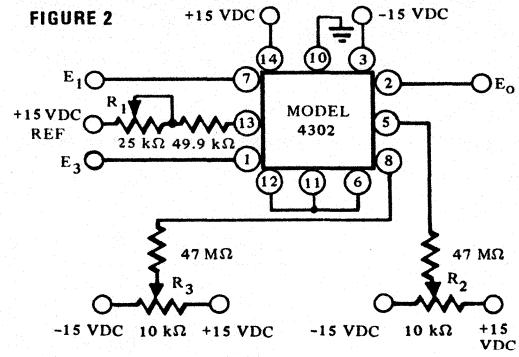
Transfer Function	$E_o = +\frac{E_1 E_2}{10}$
ACCURACY	
Total Errors	
Typical at +25°C	±25 mV
Maximum at +25°C	±50 mV
(for input range)	0.03V ≤ E_1* ≤ 10 V 0.01 V ≤ E_2 ≤ 10 V
vs. Temperature	±1 mV/°C
Offset Errors ($E_1 = E_2 = 0$)	
Output Offset (at 25°C)	±10 mV
vs. Temperature	±0.2 mV/°C
NOISE (10 Hz to 1 kHz)	100 μV rms
BANDWIDTH (E_1, E_2)	
Small Signal (-3 dB)	500 kHz
Full Output	60 kHz

DIVIDER

As a divider, the 4302 outperforms many of the multiplier/dividers on the market at a much lower cost. In the divider configuration the 4302 boasts a typical conversion accuracy of ±0.25% of full scale.

Transfer Function	$E_o = +10\ (E_1/E_3)$
ACCURACY	
Total Errors	
Typical at +25°C	±25 mV
Maximum at +25°C	±50 mV
(for $E_1 \leq E_3$ and input range)	0.03V ≤ E_1* ≤ 10 V 0.1 V ≤ E_3 ≤ 10 V
vs. Temperature	±1 mV/°C
Offset Errors ($E_1 = 0$, $E_3 = +10$ V)	
Output Offset (at 25°C)	±10 mV
vs. Temperature	±1 mV/°C
NOISE (10 Hz to 1 kHz)	
$E_3 = +10$ V	100 μV rms
$E_3 = +0.1$ V	300 μV rms
BANDWIDTH (E_1, E_3)	
Small Signal (-3 dB)	500 kHz
Full Output ($E_3 = +10$ V)	60 kHz

FIGURE 2



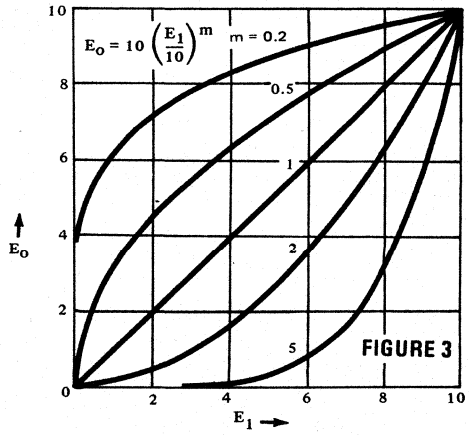
NOTES:
(1) Set R_1 so that with $E_1 = E_3 = +10.00$ VDC, $E_o = +10.00$ VDC.
(2) Set R_2 so that with $E_1 = E_3 = +0.10$ VDC, $E_o = +10.00$ VDC.
(3) Set R_3 so that with $E_1 = +0.01$ VDC and with $E_3 = +0.10$ VDC, $E_o = +1.00$ VDC.
(4) Repeat steps 1 through 3 as necessary to achieve the specified output voltages.

* The input voltage may be extended below 0.03V by connecting a 0.047 μF capacitor between pins 11 and 5, causing a slight reduction in bandwidth. (Multiply and Divide Modes).

EXPONENTIAL FUNCTIONS

Model 4302 may be used as exponentiator over a range of exponents from 0.2 to 5. The exponents 0.5 and 2, square rooting and squaring respectively, are often used functions and are treated below. Other values of exponents (m) may be useful in terms of linearization of nonlinear functions or simply for producing the mathematical conversions. Characteristics of m = 0.2 and m = 5 are presented on the right. For other values of m the curves presented in Figure 3 may be used to interpolate the error for a nonspecified value of m.

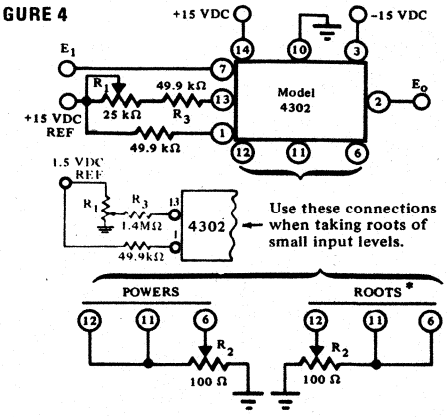
Transfer Function	$E_o = 10\left(\frac{E_1}{10}\right)^m$
Total Conversion Error (typical)	
m = 0.2	
0.5 VDC < E_1 ≤ 10 VDC	±2 m VDC
0.1 VDC < E_1 ≤ 0.5 VDC	±25 m VDC
m = 5	
1.0 VDC < E_1 ≤ 10 VDC	±15 m VDC
Exponent Range (continuous)	0.2 ≤ m ≤ 5
Input Voltage Range	0 to +10 VDC
Output Voltage Range	0 to +10 VDC



Exponentiator Transfer Characteristics

NOTES:
(1) Connect a 100 Ω potentiometer as shown in Figure 4 for either roots ($0.2 \leq m < 1$) or powers ($1 < m \leq 5$).
(2) Set R_1 so that with E_1 = +10.00 VDC, E_o = +10.00 VDC.
(3) Select a + DC voltage level (E_1) such that the output voltage (E_o), as acted upon by the desired exponent, will not exceed +10.00 VDC. A level which is mid-range for input values of interest is an appropriate one to use. Set R_2 so that the output voltage (E_o) is the value expected for the chosen values of input (E_1) and exponent (m).

FIGURE 4



(4) Repeat steps (2) through (4) as necessary.

* When taking roots of smaller input levels, a modified transfer equation [$E_o = (10E_1)^m$] will provide improved conversion accuracy. To achieve this transfer function: 1) apply a +1.5 VDC REF in place of the +15 VDC REF shown in Figure 4., 2) make R_3 a 1.40 MΩ resistor, and rearrange R_1 and R_3 as 1.5VDC REF and 3) follow all notes except in note (2) apply +0.10VDC to pin 7 to set R_1 to E_o = +1.00VDC.

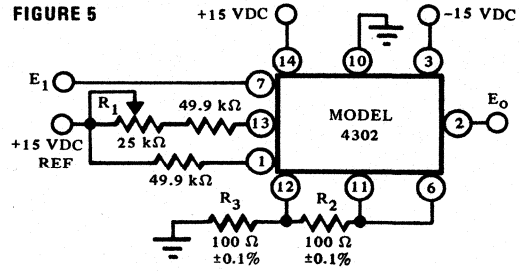
SQUARE ROOT

As a Square Rooter (m = 0.5), the 4302 provides a typical total conversion accuracy of ±0.07%. Refer to Figure 5 and notes for connections and adjustments respectively.

Transfer Function	$E_o = 10\sqrt{\frac{E_1}{10}}$
Total Conversion Error (Typical)	
0.5 VDC < E_1 ≤ 10 VDC	±7 mV
0.02 VDC < E_1 ≤ 0.5 VDC	±55 mV
Input Voltage Range	0 to +10 VDC
Output Voltage Range	0 to +10 VDC

NOTES:
(1) Connect pins 12, 11, and 6 together. Set R_1 such that with E_1 = +10.00 VDC; E_o = +10.00 VDC.
(2) Connect 100 Ω resistors as shown in Figure 5.
(3) For greater conversion accuracy, R_2 & R_3 may be replaced by a potentiometer as shown in Figure 4.

FIGURE 5



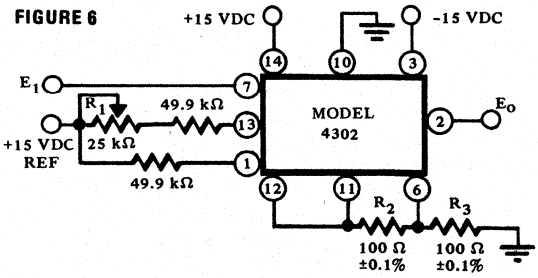
SQUARE

Configured as a Square Function Converter (m = 2), the 4302 produces high conversion accuracies of typically 0.03%. Please refer to Figure 6 and accompanying notes.

Transfer Function	$E_o = 10\left(\frac{E_1}{10}\right)^2$
Total Conversion Error (typical)	
0.1 VDC ≤ E_1 ≤ 10 VDC	±3 mV
Input Voltage Range	0 to +10 VDC
Output Voltage Range	0 to +10 VDC

NOTES:
(1) Set R_1 such that with E_1 = +10.00 VDC, E_o = +10.00 VDC.
(2) Connect 100 Ω resistors as shown in Figure 6.
(3) For greater conversion accuracy R_2 & R_3 may be replaced by a potentiometer as shown in Figure 4.

FIGURE 6



TRIGONOMETRIC FUNCTIONS

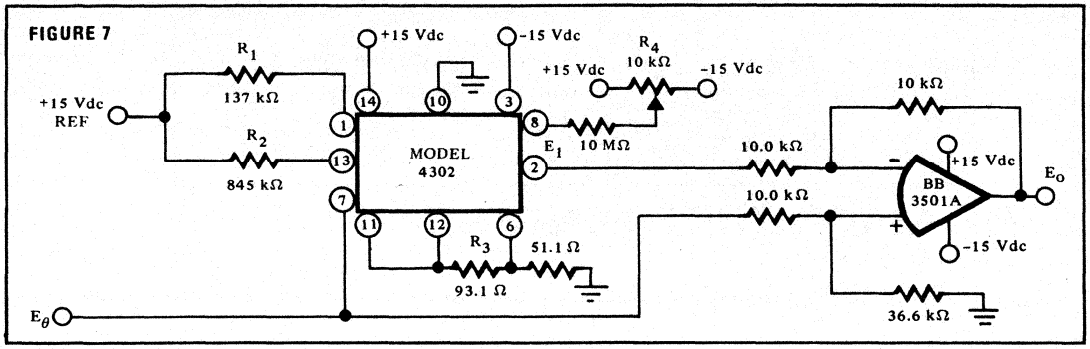
SINE

Sine functions can be accurately generated from input voltage levels representing angular displacement from 0 to 90°. Model 4302 configured as in Figure 7 will produce the sine power series approximations with modified coefficients to typically better than ±0.5% of full scale. In this circuit, the 4302 is scaled so that when $\theta = 0$, $E_O = 0$ VDC, and when $\theta = 90$, $E_O = 10$ VDC.

NOTES:
(1) Adjust R_4 if needed so that $E_1 < 1$ m VDC when $E_\theta = 0$.
(2) Adjust R_2 so that $E_1 = +0.8045$ VDC when $E_\theta = +5.00$ VDC.
(3) Adjust R_3 so that $E_1 = +5.709$ VDC when $E_\theta = +10.00$ VDC.
(4) Repeat steps (2) and (3) as necessary.

Transfer Function	$E_O = 10 \text{ Sin } 9E_\theta$
Power Series Approximation $E_O = 1.5708E_\theta - 1.5924\left(\frac{E_\theta}{6.366}\right)^{2.827}$	
Total Conversion Error (typical)	±50 mV
Input Voltage Range ($0 \leq \theta \leq 90^o$)	0 to +10 VDC
Output Voltage Range ($0 \leq \sin\theta \leq 1$)	0 to +10 VDC

FIGURE 7



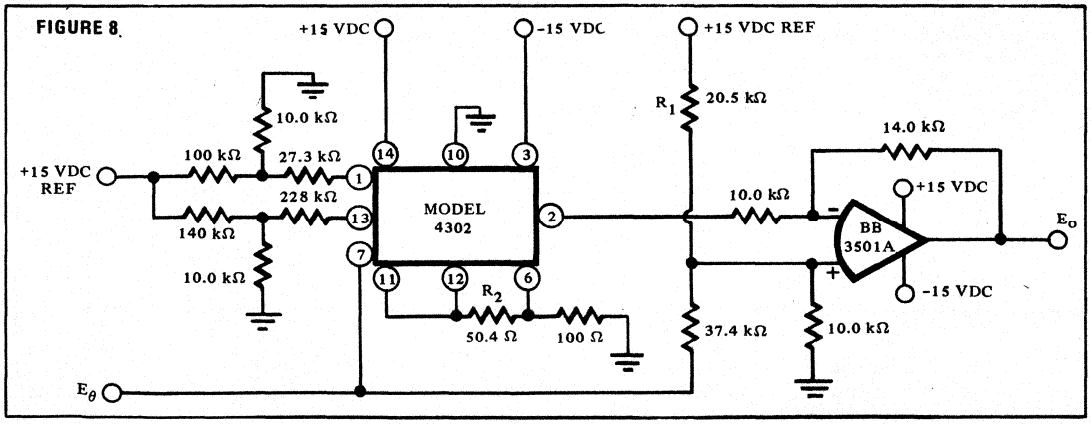
COSINE

Connected as in Figure 2, the Model 4302 will generate a cosine function of the input voltage. Typical accuracies of ±0.8% can be expected from this configuration.

NOTES:
(1) Adjust R_1 so that $E_O = +10.00$ VDC when $E_\theta = 0$.
(2) Adjust R_2 so that $E_O = 0$ when $E_\theta = +10.00$ VDC.

Transfer Function	$E_O = 10 \cos 9E_\theta$
Power Series Approximation $E_O = 10 + 0.3652\,E_\theta - 0.4276E^{1.504}$	
Total Conversion Error (typical)	±80 mV
Input Voltage Range ($0 \leq \theta \leq 90^o$)	0 VDC to +10 VDC
Output Voltage Range ($1 \leq \cos\theta \leq 0$)	+10 VDC to 0 VDC

FIGURE 8



MULTI. CONV. 4302

ARCTANGENT

Model 4302 and the associated circuitry shown below will produce the inverse tangent of a ratio. This application is particularly well suited to conversion from rectangular coordinates to polar coordinates where

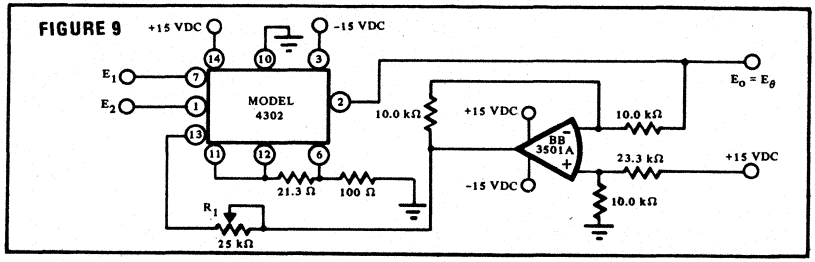
$$E_\theta = \tan^{-1}\frac{E_Y}{E_X}$$

The accuracy of conversion depends upon the levels of the input signals. Please refer to table at right.

Transfer Function	$E_O = \tan^{-1}\left(\frac{[E_1]}{[E_2]}\right)$
Power Series Approximation	$E_O = \frac{\left(\frac{[E_1]}{[E_2]}\right)^{1.2125}}{1+\left(\frac{[E_1]}{[E_2]}\right)^{1.2125}}(90^o)$
Total Conversion Error $2 < E_1, E_2 \leq 10$ VDC $0.1 < E_1, E_2 \leq 2$ VDC $0.03 < E_1, E_2 \leq 0.1$ VDC Input Voltage Range (E_1, E_2) Output Voltage Range $0 \leq E_\theta \leq 90^o$	 ±55 m VDC ±65 m VDC ±340 m VDC +0.01 VDC to +10 VDC 0 VDC to +9 VDC

NOTE:
(1) Set R_1 so that with $E_1 = E_2 = +10.00$ VDC, $E_O = +4.500$ VDC ±1 mVDC.

FIGURE 9



VECTOR MAGNITUDE FUNCTION

The model 4302 will produce the square root of the sum of the squares of two inputs. This function is companion to the arctangent of a ratio for the conversion of rectangular to polar coordinates.

Transfer Function	$E_O = \sqrt{E_1^2 + E_2^2}$
Input Voltage Range E_1 E_2	0 to +10VDC -10VDC to +10VDC
(refer to notes 1 and 2)	
Output Voltage Range	0 to +10VDC
Conversion Error	±7m VDC

NOTES:

1. Figure 10 shows one practical way to implement the transfer function $E_o = \sqrt{E_1^2 + E_2^2}$ using 4302. It shows use of model 3501A op amp. Model 3501's rated output is ±10V. This limits the range of E_1 and E_2, such that the conditions $E_1 \leq \sqrt{100 - E_2}$ and $|E_2| \leq (5 - E_1^2/20)$ and $\sqrt{E_1^2 + E_2^2} \leq 10$ are always satisfied.
   (a) The above conditions imply, $0V \leq E_1 \leq 10V$ and $-5V \leq E_2 \leq 5V$.
   (b) The above conditions also imply that for applications where $E_1 = |E_2|$ the range would be limited to 4.142V max.
2. Use of model 3627 as shown in Figure 11 would directly substitute the eight 10kΩ resistors and the two model 3501A op amps. This would reduce the number of components needed to implement vector magnitude function and reduce overall cost.

FIGURE 10

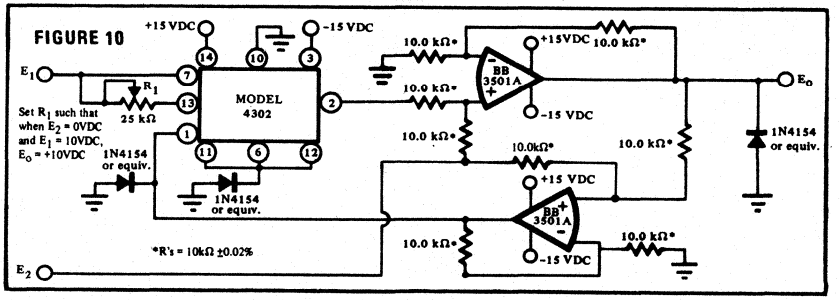
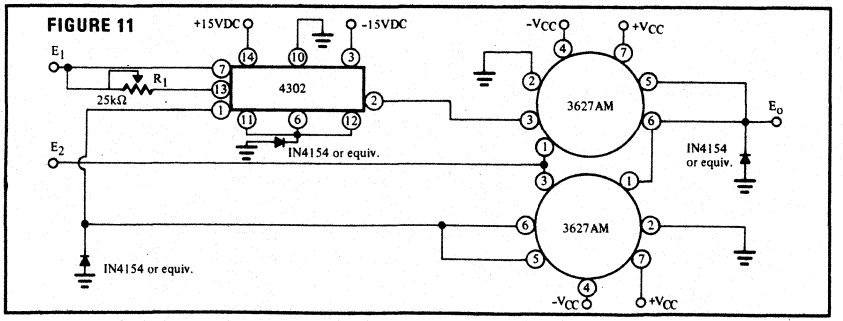
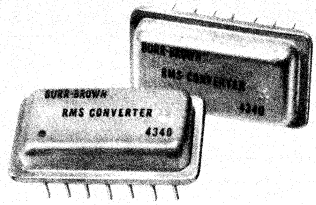


FIGURE 11



BURR-BROWN

4340



TRUE RMS-TO-DC CONVERTER

FEATURES

- LOW COST
- HIGH ACCURACY
  ±0.3mV ±0.1% Rdg.
- HIGH INPUT IMPEDANCE - 5kΩ
- HERMETIC METAL PACKAGE

DESCRIPTION

The Burr-Brown Model 4340 is a True RMS-to-DC Converter featuring high performance, low cost, and a small hermetic package. The 4340 will compute the True RMS value of a variety of signals applied to the input. The input signal may consist of complex AC waveforms as well as a DC voltage level. The output of the 4340 is a DC voltage, the amplitude of which is equal to the RMS value of the input voltage.

The 4340 will accept input voltages from 0 to ±10V over a wide input frequency range. The conversion accuracy of the 4340 is specified in terms of error in millivolts (mV) plus a percent of reading, as a function of input signal level over an input frequency range.

The 4340 has an input impedance of 5kΩ and an output impedance of 1Ω. This product will supply up to 5mA of output current at a voltage of +10VDC. The input is fully protected for conditions of overvoltage up to the supply voltage. The output will withstand short-circuit to power supply common for an indefinte period of time.

The specified unadjusted performance characteristics of the 4340 are shown in the ELECTRICAL SPECIFICATIONS. Provision for the external adjustment of: gain, voltage offset, DC reversal error, and frequency response performance allow the user to improve upon the specified conversion accuracies to the degree required by the user's application.

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PDS-304D
Printed in U.S.A. July, 1978

SPECIFICATIONS

ELECTRICAL

(Typical at 25°C with rated power supplies unless otherwise noted).

MODEL	4340
TRANSFER FUNCTION	E_o (d.c.) = $\sqrt{\overline{E_{IN}^2}}$
INPUT	
Peak Voltage	±10 Vdc
Absolute Maximum Voltage	± Supply
Impedance	5 kΩ
OUTPUT	
Voltage	0 to +10 Vdc
Current (min)	+5 mA
Impedance	1 Ω
CONVERSION ACCURACY	
Total Unadjusted Error (max)	
Input: 10 mV rms to 7.0 rms 100 Hz to 10 kHz sine wave*	±2 mV ±0.2% Reading
Total Adjusted Error**	
Input: 10 mV rms to 7 V rms 50 Hz to 20 kHz*	±0.3 mV ±0.1% Reading
STABILITY	
Accuracy vs Temperature	±0.001% of FS plus ±0.01% of reading per °C
Accuracy vs Supply	±0.001% of FS plus ±0.01% of reading per %ΔV
TEMPERATURE RANGE	
Operating	-25°C to +85°C
Storage	-55°C to +125°C
POWER REQUIREMENTS	
Rated Voltage	±15 Vdc
Voltage Range	±14 Vdc to ±16 Vdc
Quiescent Current	±12 mA

* Model 4340 will convert d.c. inputs. Lower frequency a.c. input signals will require the addition of external capacitors to preserve the accuracy. (Refer to page 4-74)

** Performance with external trims and $C_L \geq 3\ \mu F$ and $20\ pF \leq C_H \leq 100\ pF$. (Refer to page 4-74)

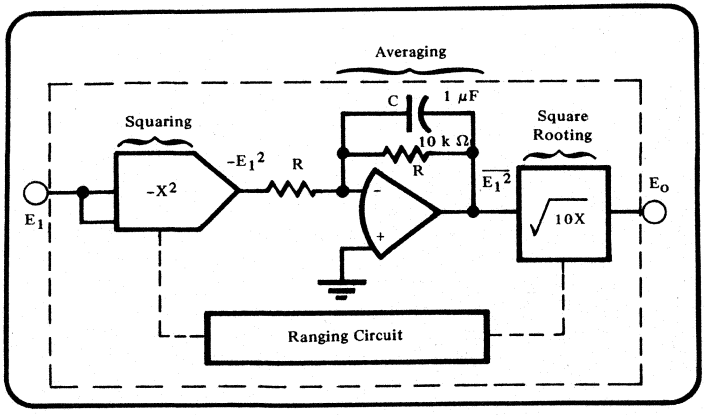
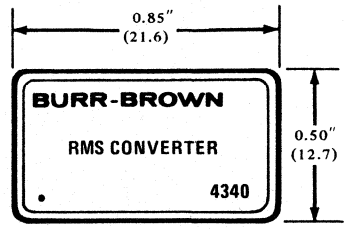


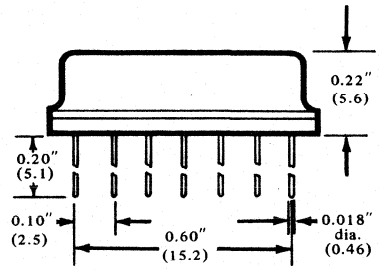
FIGURE 1. Functional Block Diagram of Model 4340.

MECHANICAL



(TOP VIEW)

Dimensions in millimeters are shown in parentheses.

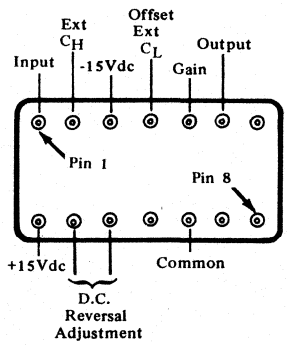


(SIDE VIEW)

Row Spacing: 0.30" (7.6)

Pin material and plating composition meet Method 2003 (solderability) of Mil-Std-883 [except for paragraph 3.2.]

PIN CONNECTIONS



(BOTTOM VIEW)

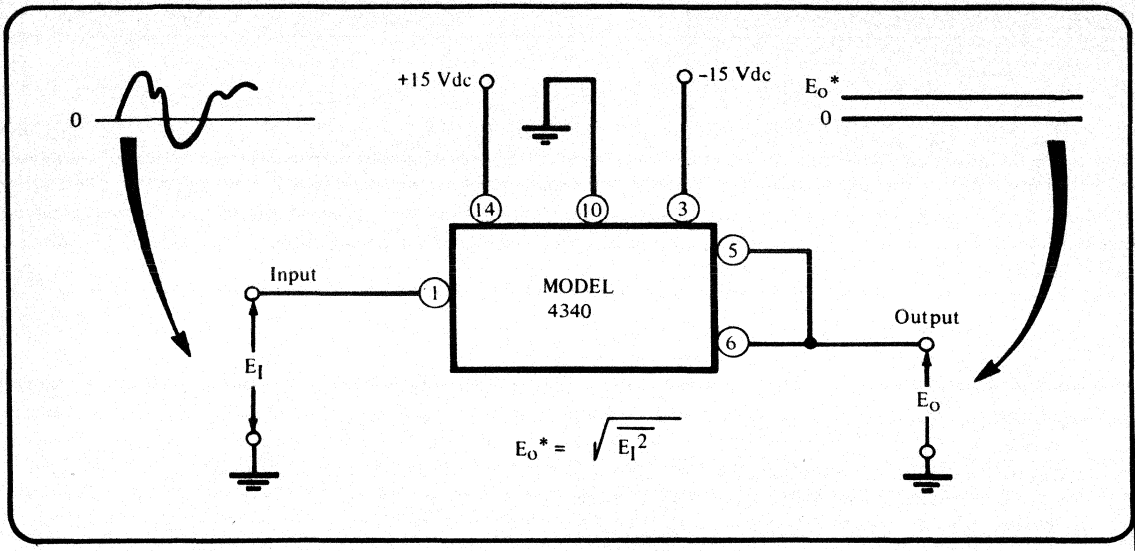


FIGURE 2. Model 4340 RMS Converter – Connected to produce specified unadjusted accuracy.

OPTIONAL EXTERNAL ADJUSTMENTS

Although the unadjusted performance of the 4340 is quite high for most applications, optimized performance can be achieved with external adjustments. The following paragraphs and figures will demonstrate the techniques for external adjustments of gain, voltage offset, d.c. reversal error, and frequency response. The unity gain adjustment should be made first, then the offset voltage adjustment. The unity gain adjustment should then be repeated for best results.

UNITY GAIN

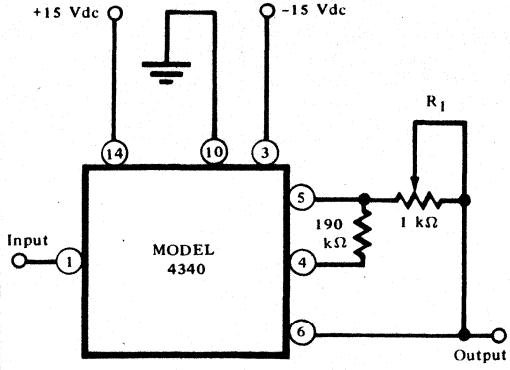


FIGURE 3. Unity Gain Adjustment – Apply +5 V rms Sine Wave to Input. Adjust R_1 for +5 Vdc at Output.

OFFSET VOLTAGE

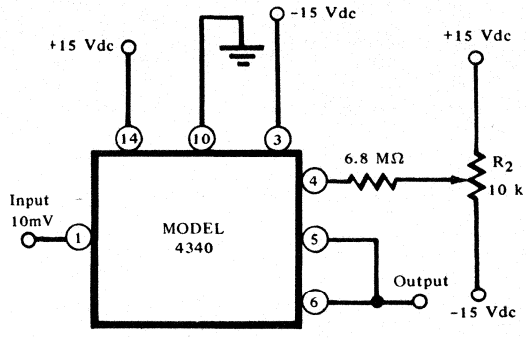


FIGURE 4. Offset Voltage Adjustment – Adjust R_2 for 10mVdc at Output.

FREQUENCY RESPONSE

The conversion accuracy of the 4340 over a broad range of input frequencies can be enhanced by the addition of one or more externally connected capacitors. Refering to Figure 5, C_H will improve the high frequency performance and C_L will extend the low frequency response.

HIGH FREQUENCY RESPONSE COMPENSATION

The upper limit of frequency response of the 4340 may be extended to meet the adjusted conversion accuracy specification by the proper selection of C_H.

Sweep a 1.0 V rms signal from 10 kHz to 20 kHz, measure the output voltage change from 1.0 Vdc. Select a value for C_H that minimizes the change in output voltage over 10 kHz to 20 kHz frequency range.

* C_H may be selected from 22 pF, 33 pF, 47 pF, or 100 pF.

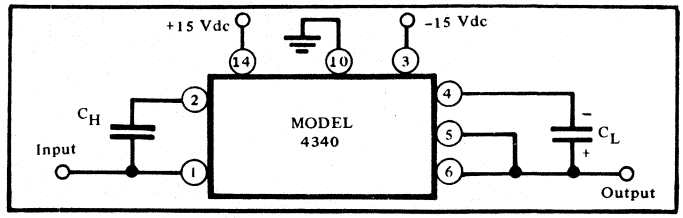


FIGURE 5. Frequency Response Adjustments – C_H* = 22 pF to 100 pF and C_L > 3.0 μF for "adjusted" frequency response range.

LOW FREQUENCY RESPONSE EXTENSION

In the 4340, a single-pole, low pass filter provides the averaging function. The time constant of this filter (To) is selected to be 0.005 seconds. Larger time constants should be selected in order to achieve the Conversion Accuracy at frequencies lower than 100 Hz.

The external capacitor can be 100's of microfarads, but the shunt resistance of the capacitor must be very large in order to maintain gain accuracy. The best value of C_L is inherently a compromise – the larger the capacitor the lower the ripple, but the response time is increased. Calculating the proper C_L for a given waveform can be done, but is tedious. The fastest method of choosing C_L is to apply a representative input signal, and observe the ripple at the output. Select various values of C_L until the ripple is attenuated sufficiently. The amount of allowable output ripple depends upon the application. For example, if the output is being read by an integrating DVM, then output ripple won't be critical.

ADDITIONAL ADJUSTMENTS

NON-UNITY GAIN

The 4340 may be adjusted to achieve a non-unity gain transfer function: $E_O = A\sqrt{E_{IN}^2}$ for $1 < A \leq 10$. Figure 6 illustrates the technique to achieve this gain change.

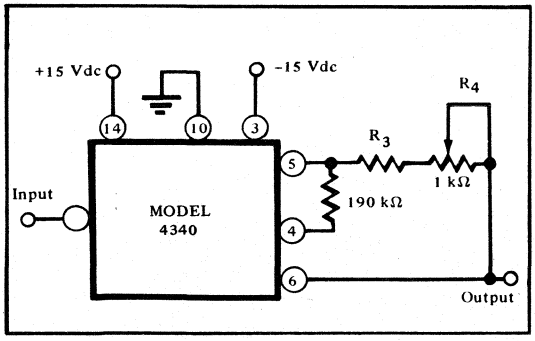


FIGURE 6. Non-Unity Gain Adjustment – Set desired gain by selecting R_3 such that $R_3 = (A^2 - 1) \times 10k\Omega$. Apply appropriate mid-scale d.c. level to Input and adjust R_4 for output equal to A x V_{Input} (Vdc).

D.C. REVERSAL ERROR

When the 4340 is utilized with D.C. inputs and a high degree of conversion accuracy is required, a correction for d.c. reversal error may be required. Figure 7 illustrates the method to accomplish this adjustment.

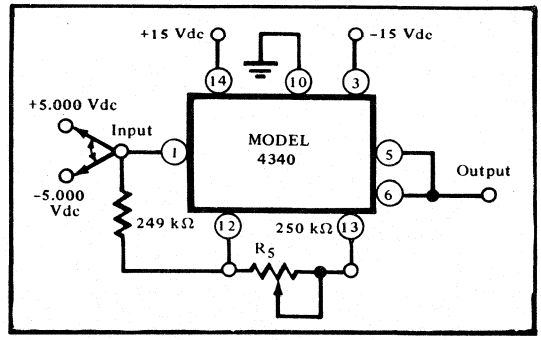
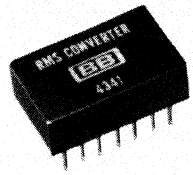


FIGURE 7. D.C. Reversal Error Adjustment – Alternately switch the input between +5.000 Vdc and -5.000 Vdc, adjust R_5 so that the output error voltage from +5.000 Vdc is the same for both input polarities.

NOTE: Some minor interaction may be experienced between the various adjustments requiring repeating of these adjustments for lowest total error.

BURR-BROWN

4341



Low Cost
TRUE RMS-TO-DC CONVERTER

FEATURES

- **LOW COST**
- **HIGH ACCURACY**
  ±0.2% ±2mV
- **HIGH RELIABILITY**
  Hybrid construction

DESCRIPTION

The Burr-Brown Model 4341 RMS-to-DC Converter features low cost without sacrificing performance. The 4341 computes a DC voltage proportional to the true rms value of signals which may be complex waveforms, DC levels, or a combination of both.

The input and output are fully protected against overvoltages and short circuits. Provisions for the external adjustment of gain, offset voltage, DC-reversal error, and frequency response make the 4341 versatile enough to fill the majority of your applications.

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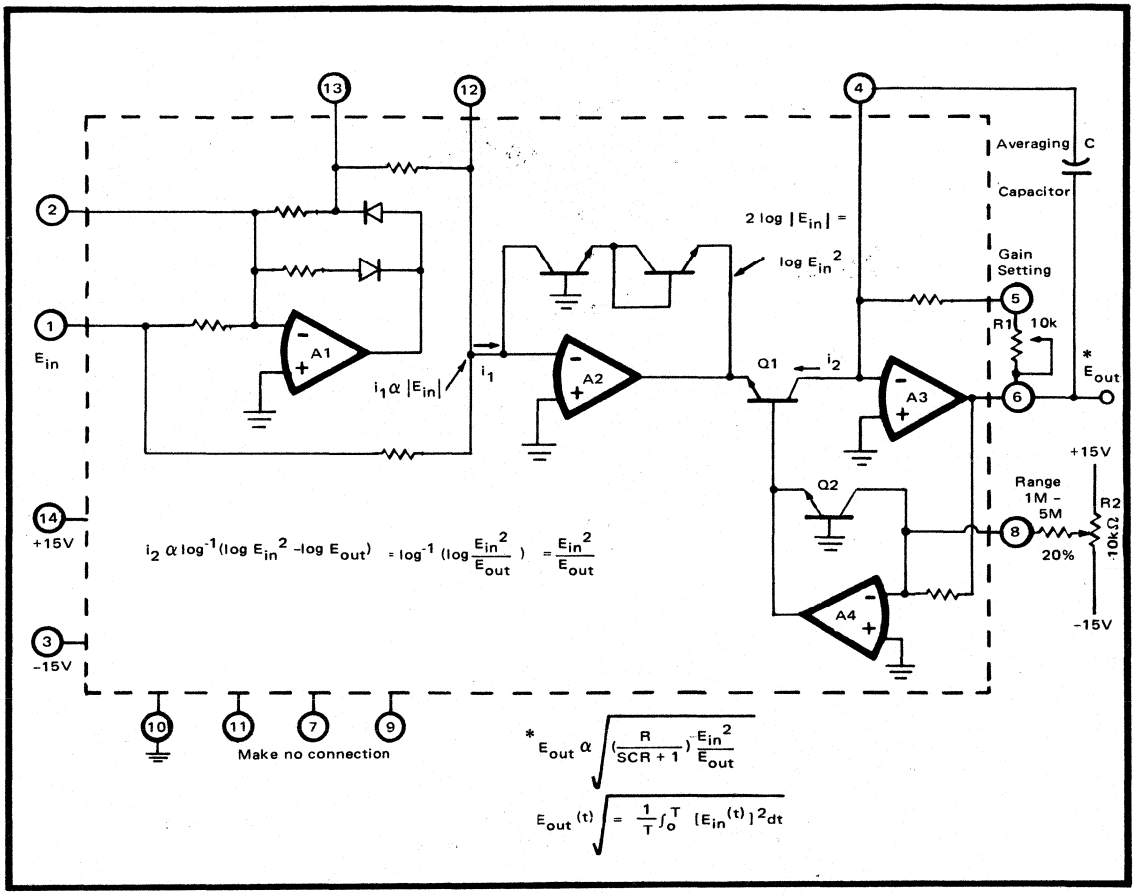


FIGURE 1. Simplified Schematic.

THEORY OF OPERATION

The true RMS value of a time-varying signal E (t) over a time period T is

$$E_{RMS} = \sqrt{\frac{1}{T} \int_0^T [E(t)]^2 \, dt}$$

The required operations are squaring, averaging and square rooting. A simplified schematic diagram of the 4341 is shown in Figure 1. The A1 circuit produces a current i_1 which is proportional to the rectified input voltage. The A2 circuit is a logarithmic amplifier which produces a voltage proportional to 2 log E_{in} or log E_{in}^2. The logarithmic gain of the A2 circuit is derived from the inherent exponential characteristics of transistor junctions. By using proprietary monolithic components, the circuit provides an accurate log function over many decades which is relatively insensitive to temperature variations. Amplifier A4 uses the same techniques as A2 to generate log E_{out}.

Transistor Q1 produces a collector current i_2 proportional to the antilog of its base-emitter voltage, such that

$$i_2 \alpha \log^{-1} (\log E_{in}^2 - \log E_{out})$$

$$= \log^{-1} \left(\log \frac{E_{in}^2}{E_{out}}\right) = \frac{E_{in}^2}{E_{out}}$$

The A3 circuit which contains the external capacitor takes the time average of the i_2 signal and produces E_{out} which is directly proportional to the RMS value of E_{in}.

Figures 2 and 3 show the effects of the external filter capacitor on ripple magnitude and response time. As the frequency of the input approaches DC, the 4341 begins to act like a full wave rectifier such that the output is the absolute value of the input. While the 4341 will accurately convert dc input voltages, the averaging capacitor must be made very large to minimize ripple at low frequencies.

SPECIFICATIONS

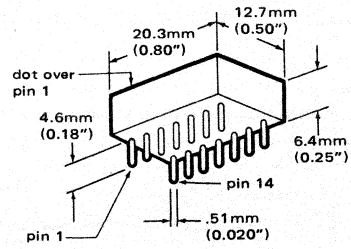
(Typical at 25°C with rated supply voltages, unless otherwise noted.)

ELECTRICAL

MODEL	4341
TRANSFER FUNCTION	$E_{out}(DC) = \sqrt{\frac{1}{T}\int_o^T E_{in}^2(t)\,dt}$
INPUT	
Peak Operating Voltage	±10V
Absolute Maximum Voltage	±Supply
Impedance	5 kΩ
OUTPUT	
Voltage	0 to +10V
Current	+5mA, min
Resistance	1 Ω, max
BANDWIDTH	
±1% of Theoretical Output	80 kHz
-3 dB	450 kHz
CONVERSION ACCURACY(2)	
Input: 500 mV RMS to 5.0 V RMS DC to 10 kHz Sine Wave	±0.5% of Reading, max(1)
Input: 10 mV RMS to 7 V RMS DC to 20 kHz	±2 mV ±0.2% Reading
STABILITY	
Accuracy vs. Temperature	±0.1 mV ±0.01% of Reading/°C
Accuracy vs. Supply Voltage	±0.1 mV ±0.01% of Reading/% of Supply Voltage Change
TEMPERATURE RANGE	
Operating	-25°C to +85°C
Storage	-55°C to +125°C
POWER REQUIREMENTS	
Rated Voltage	±15 VDC
Voltage Range	±14 VDC to ±16 VDC
Quiescent Current	±12 mA, typ./±24 mA, max

(1) After standard trim procedure (see below).
(2) Model 4341 will convert DC inputs. Lower frequency AC inputs require a large value of averaging capacitor to minimize ripple at output. (See Figure 2)

MECHANICAL



Row Spacing: 7.6mm (0.300")
Weight: 3.4 grams (0.12 oz.)
Connector: 14-Pin DIP
0145MC

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std-202.

RMS/DC CONV.

STANDARD TRIM PROCEDURE

If the 4341 is used to measure sine waves or distorted sine waves, only two trims are needed to achieve an accuracy of ±0.5% of reading from 500 mV RMS to 5 V RMS up to 10 kHz. Refer to Figure 1.

1. Set E_{in} = 5.000 V RMS ±0.02% and adjust R1 such that E_o = 5.000 VDC ±2 mV.
2. Set E_{in} = 500 mV RMS ±0.02% and adjust R2 such that E_o = 500 mVDC ±0.2 mV.
3. Repeat Step 1.

CHOOSING THE AVERAGING CAPACITOR

A single-pole low pass RC filter provides the averaging function. The time constant is 1/2 RC where R is 10 k when the 4341 is adjusted for unity gain. To select the best value of C, make a tradeoff between output ripple and response time. Figure 2 shows the ripple magnitude vs. frequency for several typical values of capacitor. Response time vs. capacitor value is shown in Figure 3. (Note that rise times and fall times are different for the same value of capacitor).

While the ripple magnitude for signals other than sine waves can be analytically determined, it is tedious. The fastest method of choosing C is to apply a representative input signal and observe the output for various values of C. C can be 100's of microfarads, but should have a leakage current less than 0.1μA to minimize gain errors. With very large values of C, the input signals with frequencies approaching DC level could be averaged. Since the output is always a positive voltage, C can be a polar capacitor.

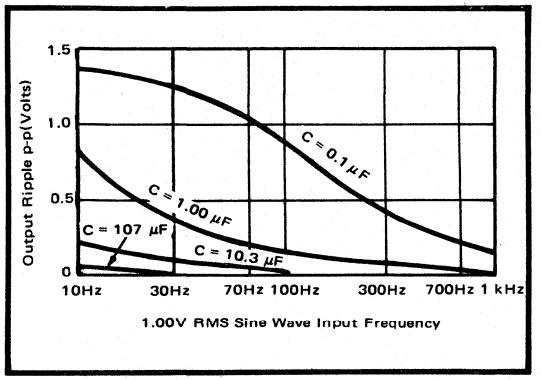


FIGURE 2. Output Ripple Magnitude vs. Input Signal Frequency.

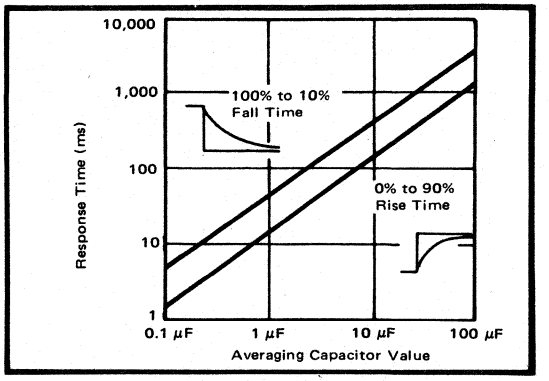


FIGURE 3. Response Time vs. Value of Averaging Capacitor.

EXPANDED TRIM PROCEDURE FOR GREATER ACCURACY

If the 4341 is used in applications to measure complex waveforms, the following expanded trim procedure is recommended. (Refer to Figure 4).

First set all potentiometers at mid turn position

1. DC Reversal Error - Apply +10.000V ±1 mV and -10.000V ±1 mV to E_{in} alternatively, adjust R5 such that E_o readings are the same ±2 mV.
2. Gain Adjustment - Apply E_{in} = +10.000 VDC ±1 mV, adjust R1 such that E_o = +10.000 VDC ±1 mV.
3. Input Offset - Apply +10.0 mV ±0.1 mV and -10.0 mV ±0.1 mV to E_{in}, adjust R4 such that E_o readings are the same ±0.1 mV.
4. Offset - Ground E_{in}, adjust R3 such that E_o = 0 ±0.1 mV. Repeat Step (3).
5. Low Level Accuracy - Apply E_{in} = +10.0 mV ±0.1 mV, adjust R2 such that E_o = +10.0 mV ±0.1 mV.

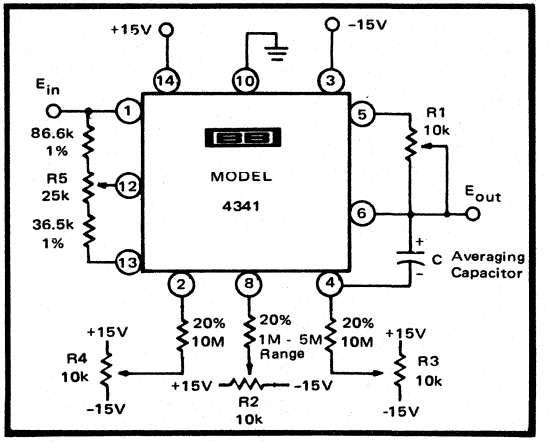


FIGURE 4. Expanded Trim Procedure (High Accuracy Applications).

NONUNITY GAINS

Gain values greater than unity can be achieved by inserting resistor R_X between pin 5 and pin 6. $R_X \simeq (A^2 - 1) \times 10k + 2k$ where A is the desired value of gain ($1 < A \leq 10$). (R_X is in ohms).

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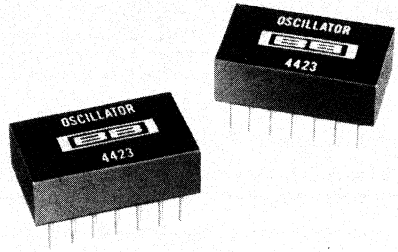


4423

PRECISION QUADRATURE OSCILLATOR

FEATURES

- SINE AND COSINE OUTPUTS
- RESISTOR PROGRAMMABLE FREQUENCY
- WIDE FREQUENCY RANGE
  0.002Hz to 20kHz
- LOW DISTORTION
  0.2% max up to 5kHz
- EASY ADJUSTMENTS
- SMALL SIZE
- LOW COST

DESCRIPTION

The Model 4423 is a precision quadrature oscillator. It has two outputs 90 degrees out of phase with each other, thus providing sine and cosine wave outputs available at the same time. The 4423 is resistor programmable and is easy to use. It has low distortion (0.2% max up to 5 kHz) and excellent frequency and amplitude stability.

The Model 4423 also includes an uncommitted operational amplifier which may be used as a buffer, a level shifter or as an independent operational amplifier. The 4423 is packaged in a versatile, small, low cost DIP package.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-365A Printed in U.S.A. July, 1978

SPECIFICATIONS

Specifications typical at 25°C and ±15VDC
Power Supply Unless Otherwise Noted.

ELECTRICAL

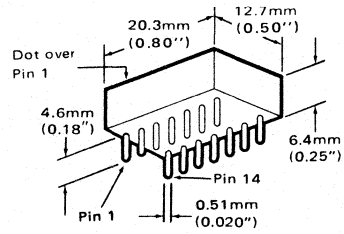
	MIN	TYP	MAX	UNITS
FREQUENCY				
Initial Frequency (no adjustments)	20.0k	20.5k	21.0k	Hz
Frequency Range (using 2 R's only)	2k		20k	Hz
Frequency Range (using 2 R's and 2 C's)	0.002		20k	Hz
Accuracy of Frequency Equation*		±1	±5	%
Stability vs Temperature		±50	±100	ppm/°C
Quadrature Phase Error		±0.1		degree
DISTORTION				
Sine Output (pin 1)				
0.002Hz to 5kHz			0.2	%
5kHz to 20kHz			0.5	%
Cosine Output (pin 7)				
0.002Hz to 5kHz		0.2		%
5kHz to 20kHz		0.8		%
Distortion vs Temperature		0.015		%/°C
OUTPUT				
Amplitude (Sine)				
At 20 kHz	6.5	7	7.5	V rms
vs Temperature		0.05		%/°C
vs Supply		0.4		V/V
Output Current	1.5	5		mA
Output impedance			1	Ω
UNCOMMITTED OP AMP				
Input Offset Voltage		1.5		mV
Input Bias Current		275		nA
Input Impedance		1		MΩ
Open Loop Gain		90		dB
Output Current	5			mA
POWER SUPPLY				
Rated Supply Voltage		±15		VDC
Supply Voltage Range	±12		±18	VDC
Quiescent Current		±9	±18	mA
TEMPERATURE RANGE				
Specifications	0		+70	°C
Operation	-25		+85	°C
Storage	-55		+125	°C

* May be trimmed for better accuracy.

PIN CONNECTIONS

1. E_1, Sine Output
2. Frequency Adjustment
3. Frequency Adjustment
4. +In, Uncommitted Op Amp
5. -In, Uncommitted Op Amp
6. Output, Uncommitted Op Amp
7. E_2, Cosine Output
8. Frequency Adjustment
9. $-V_{CC}$, -15VDC
10. $+V_{CC}$, +15VDC
11. Common
12. Frequency Adjustment
13. Frequency Adjustment
14. Frequency Adjustment

MECHANICAL



ROW SPACING - 7.6 (0.300")
WEIGHT - 3.4 gms (0.12 oz)
CONNECTOR - 14 pin DIP connector
(145 MC)

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

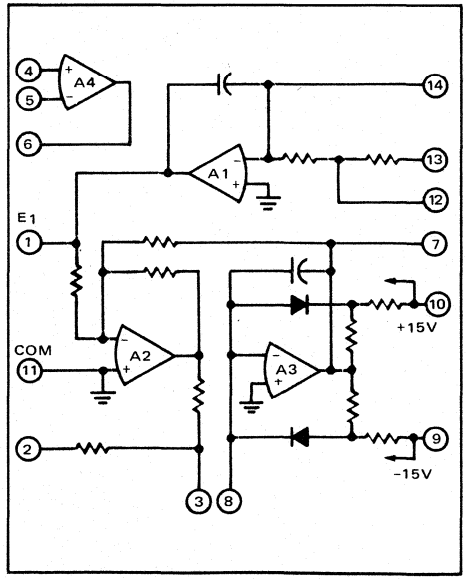


FIGURE 1. Equivalent Circuit.

TYPICAL PERFORMANCE CURVES

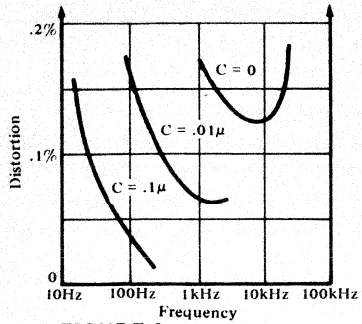


FIGURE 2.

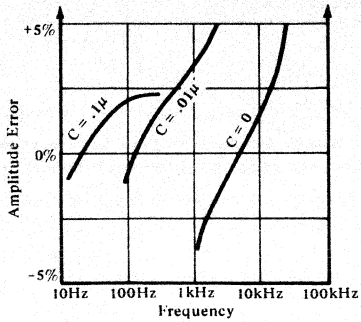


FIGURE 3.

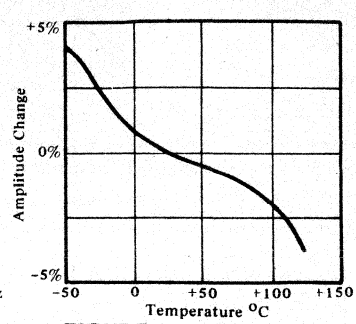


FIGURE 4.

EXTERNAL CONNECTIONS

1. 20 kHz Quadrature Oscillator

The 4423 does not require any external component to obtain a 20 kHz quadrature oscillator. The connection diagram is as shown in Figure 5.

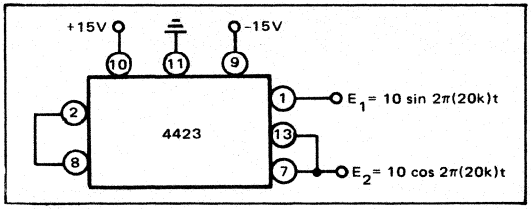


FIGURE 5.

2. Resistor Programmable Quadrature Oscillator

For resistor programmable frequencies in the 2 kHz to 20 kHz frequency range, the connection diagram is shown in Figure 6. Note that only two resistors of equal value are required. The resistor R can be expressed by,

$$R = \frac{3.785f}{42.05 - 2f}$$, R in kΩ, f in kHz

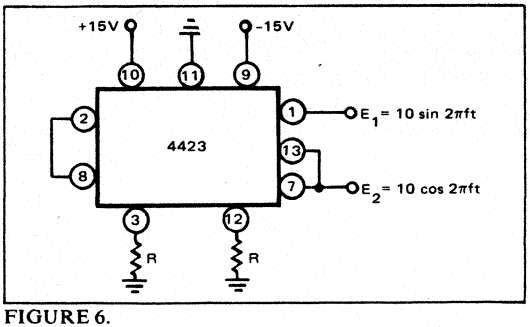


FIGURE 6.

3. Quadrature Oscillator Programmable to 0.002 Hz

For oscillator frequencies below 2000 Hz, use of two capacitors of equal value and two resistors of equal value as shown in Figure 7 is recommended. Connections shown in Figure 7 can be used to get oscillator frequency in the 0.002 Hz to 20 kHz range.

The frequency f can be expressed by:

$$f = \frac{42.05\ R}{(C + 0.001)\ (3.785 + 2R)}$$

where, f is in Hz
C is in μF
and R is in kΩ

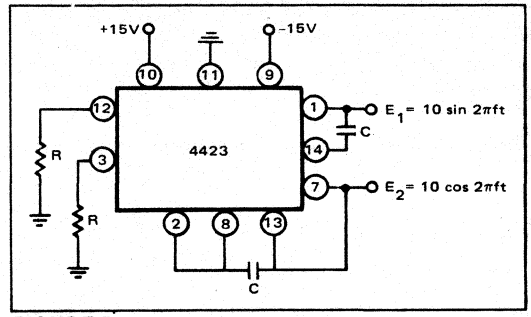


FIGURE 7.

For best results, the capacitor values shown in Table I should be selected with respect to their frequency ranges.

	f	20 kHz to 2 kHz	2 kHz to 200 Hz	200 Hz to 20 Hz
	C	0	0.01μF	0.1μF
f	20 Hz to 2 Hz	2 Hz to 0.2 Hz	0.2 Hz to 0.02 Hz	0.02 Hz to 0.002 Hz
C	1μF	10μF	100μF	1000μF

TABLE I.

After selecting the capacitor for a particular frequency the value of the required resistor can be obtained by using the resistor selection curve shown in Figure 8 or by the expression:

$$R = \frac{3.785f\ (C + 0.001)}{42.05 - 2f\ (C + 0.001)}$$

where,
R is in kΩ
f is in Hz
and C is in μF

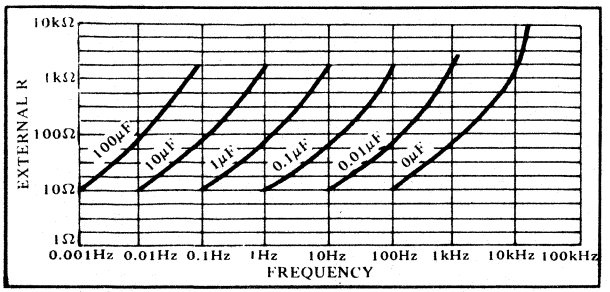


FIGURE 8.

The curves shown in Figure 8 are provided only as a nomographic design aid. The selection of capacitor values is not limited to the values shown in Figure 8. Any suitable combination of R and C values which satisfies the expression relating R, F and C as shown above, would work satisfactorily with the 4423.

NOTES ON TYPES OF CAPACITORS TO USE:

There are various kinds of capacitors available for use. There are polarized, also known as DC capacitors and non-polarized, also known as AC capacitors available. Of these two types, the polarized capacitors cannot be used with 4423 to set the frequencies.

Commonly available non-polarized capacitors include NPO ceramic, silver mica, teflon, polystyrene, polycarbonate, mylar, ceramic disc etc. A comparison is shown in Table II.

	Capacitance Range (μF)	Temperature Coefficients ppm/°C	Dissipation Factor (%)
NPO Ceramic	5pF - 0.1 μF	30	0.05
Silver Mica	5pF - 0.047 μF	60	0.05
Teflon	0.001 - 100 μF	200	0.01
Polystyrene	0.001 - 500 μF	100	0.03
Polycarbonate	0.001 - 1000 μF	90	0.08
Metalized Teflon	0.001 - 100 μF	60	0.1
Metalized Polycarbonate	0.001 - 1000 μF	10	0.4
Mylar	0.001 - 1000 μF	700	0.7
Metalized Mylar	0.001 - 2000 μF	700	1
Ceramic Disc	5pF - 0.5 μF	10,000	3

TABLE II.

For use with the 4423 oscillator, the choice of capacitors depends mainly on the user's application, error budget and cost budget. Note that the specifications of 4423 do not include the error contribution of the external components. The errors sourced by external components normally have to be added to the 4423 specifications.

As a general selection criteria we recommend the use of the above table. Start from the top of the list in the above table. If the capacitor is found unsuitable due to it being too large in size, too expensive, or is not easily available, then move down in the list for the next best selection. In any case do not choose or use any capacitors with dissipation factors greater than 1%. Such a capacitor would stop 4423 oscillation.

DISSIPATION FACTOR (DF)

A capacitor can be modeled by an ideal capacitor in parallel with an internal resistor whose value depends on its dissipation factor (DF). Mathematically, the internal resistor R is given by,

$$R = \frac{1}{2\pi f\, C(DF)}$$

where R is in Ω, f is the Hz, and C is in farads.

For example, the DF of ceramic disc capacitors is of the order of 3%, which for a 0.01 μF capacitor would look like having an internal resistor of 530kΩ at 1 kHz. The 530 kΩ value resistor is small enough to stop the 4423 oscillator from oscillating.

Some capacitor manufacturers use the terms "Power Factor" (PF) or "Q Factor" (Q) instead of the term "Dissipation Factor". These terms are similar in meaning and are mathematically related by,

$$(PF) = \frac{(DF)}{\sqrt{1 + (DF)^2}} \quad ; \quad Q = \frac{1}{(DF)}$$

OSCILLATION AMPLITUDE

It takes a finite time to build up the amplitude of the oscillation to its final full scale value. There is a relationship between the amplitude build-up time and the frequency. The lower the frequency, the longer the amplitude build-up time. For example, typically it takes 250 seconds at 1 Hz, 30 seconds at 10 Hz, 4 seconds at 100 Hz, 400 milliseconds at 1 kHz, and 40 milliseconds at 10 kHz oscillator frequencies.

There are two methods available to shorten this normal amplitude build-up time. But there is also a relationship between the amplitude build-up time and distortion at final amplitude value. When the amplitude build-up time is shortened, the distortion can get worse.

One method to shorten the amplitude build-up time is to connect a resistor between pin 3 and pin 14. The lower this resistor is the shorter will be the time to build up amplitude of the oscillation, and worse will be the distortion of the output waveform. For example, a 100kΩ resistor would shorten the amplitude build up time from 15 seconds to 1 second at 20 Hz frequency, but the distortion could be degraded from tpically 0.05% to 0.5%.

The other method is to momentarily insert a 1kΩ resistor via a reset switch betwen pin 3 and pin 14. The amplitude of oscillation is built up instantaneously when the reset switch is pushed. There will be no degradation of distortion with this method since the 1kΩ resistor does not remain in the circuit continuously.

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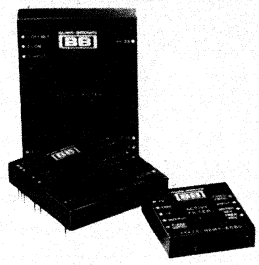

ATF76

ACTIVE FILTERS

FEATURES

- LOW PROFILE PACKAGE
- FACTORY TUNED
- NO EXTERNAL COMPONENTS REQUIRED
- WIDE TEMPERATURE RANGE

DESCRIPTION

Burr-Brown's standard series of fixed-frequency active filters is available with a wide range of transfer characteristics and resonant frequencies. These modular units are pre-tuned at Burr-Brown to the response you specify and they require no external components or adjustments. The ATF76 series includes Bessel, Butterworth, Chebyschev, band pass and band reject filters with up to eight poles. You can save hours of design and analysis, especially when your application requires a complex transfer function.

These units have applications in communications equipment, servo systems, and process controllers as well as test equipment. All filters are completely tested at the factory, and all give you the reliability you expect from Burr-Brown.

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PDS-345A

Printed in U.S.A. July, 1978

FIXED FREQUENCY ACTIVE FILTERS

Burr-Brown's standard catalog active filters, the ATF76 series, are available with low pass, band pass, and band reject characteristics. The filters in this series are packaged in space-saving 0.4" high modules ranging in size from 1.5" x 1.5" for 2 pole low pass and notch models to only 2.1" x 3.0" for 8 pole low pass models. All filters are complete units that are factory tuned with no external components required. All standard active filters operate from ±15 VDC power over a -25°C to +85°C temperature range.

Specifications typical at 25°C and rated supply voltage unless otherwise noted.

MODEL(1)	BAND PASS SINGLE TUNED				
	ATF76-B1*M	ATF76-B1*N	ATF76-B1*P	ATF76-B1*Q	ATF76-B1*R
FILTER ORDER No. of Poles	2				
INPUT					
Voltage Range	±10 V, min				
Impedance	100 kΩ, min				
FREQUENCY (f_c)					
Range	1 to 20kHz				
Accuracy	±1%				
Temp. Coeff.	±0.03%/°C				
Adj. Range	±3%				
GAIN	(inverting)				
Pass Band	0 ±0.5 dB				
SELECTIVITY (Q)					
Value	2	5	10	20	50
Tolerance	±10%				
OUTPUT					
Noise(2)	100 µV				
Impedance	10 Ω				
Current	±5 mA				
POWER SUPPLY CURRENT					
±15 VDC @ Quiescent(6)	±10 mA				
PACKAGE DWG. (See page 7)	#23	2" x 2" x 0.4"			

Specifications typical at 25°C and rated supply voltage unless otherwise noted.

MODEL(1)	LOW PASS BUTTERWORTH				LOW PASS BESSEL (Linear Phase)			
	ATF76-L2*B	ATF76-L4*B	ATF76-L6*B	ATF76-L8*B	ATF76-L2*L	ATF76-L4*L	ATF76-L6*L	ATF76-L8*L
FILTER ORDER No. of Poles	2	4	6	8	2	4	6	8
INPUT								
Voltage Range	±10 V min				±10 V min			
Impedance(5)	30 kΩ, min				30 kΩ, min			
FREQUENCY								
Range	1 to 20kHz				1 to 20kHz			
Accuracy	±2%				±2%			
Temp. Coeff.	±0.05%/°C				±0.05%/°C			
GAIN(9)	(non-inverting)				(non-inverting)			
Pass Band	0 dB, nom				0 dB, nom			
DC Accuracy	±0.05 dB, max				±0.05 dB, max			
Q-FACTOR	N/A				N/A			
OUTPUT								
Noise(2)	50 µV, RMS				50 µV, RMS			
Output Impedance	1Ω				1Ω			
Rated Current	±5 mA				±5 mA			
Offset at 25°C(8)	±2 mV				±2 mV			
Offset Drift -25°C to +85°C	±25 µV/°C		±50 µV/°C		±25 µV/°C		±50 µV/°C	
POWER SUPPLY CURRENT ±15 VDC @ Quiescent (7)	±6 mA	±10 mA	±14 mA	±18 mA	±6 mA	±10 mA	±14 mA	±18 mA
PACKAGE DWG. (See page 7)	#14 1.5" x 1.5" x 0.4"	#23 2" x 2" x 0.4"	#33 3" x 2.1" x 0.4"		#14 1.5" x 1.5" x 0.4"	#23 2" x 2" x 0.4"	#33 3" x 2.1" x 0.4"	

*Insert L or M, depending on frequency required.
(1) See below for ordering information.
(2) 10 Hz to 50 kHz with input grounded.
(3) -40 dB notch attenuation, minimum.
(4) ±3% f_c adjustment and notch depth adjustment.

ORDERING INFORMATION

ATF76 - B 2 M

- **ATF76** — (Designates Series)
- **DEFINES FILTER TYPE** — L = Low Pass; B = Band Pass; N = Notch
- **DESIGNATES NO. OF POLES OR POLE PAIRS OR ZERO PAIRS** — Low Pass: 2 = 2 poles, 4 = 4 poles, 6 = 6 poles, 8 = 8 poles; Band Pass: 1 = 1 pole pair, 2 = 2 pole pairs; Notch: 1 = zero pair
- **GROSS FREQUENCY RANGE** — L < 10 Hz; M ≥ 10 Hz

BAND PASS STAGGER TUNED				
ATF76-B2 *K	ATF76-B2 *M	ATF76-B2 *N	ATF76-B2 *P	ATF76-B2 *Q
4				
±10 V, min 100 kΩ, min				
1 to 20kHz ±1% ±0.03%/°C				
(non-inverting) 0 ±0.5 dB				
1	2	5 ±10%	10	20
100 μV 10 Ω ±5 mA				
±20 mA				
#33	3" x 2.1" x 0.4"			

Prices and specifications are subject to change without notice.

LOW PASS CHEBYSCHEV (±0.4 dB Ripple)				LOW PASS CHEBYSCHEV (±1.6 dB Ripple)				BAND-REJECT (NOTCH)		
ATF76-L2 *C	ATF76-L4 *C	ATF76-L6 *C	ATF76-L8 *C	ATF76-L2 *D	ATF76-L4 *D	ATF76-L6 *D	ATF76-L8 *D	ATF76-N1 *M	ATF76-N1 *N	ATF76-N1 *P
2	4	6	8	2	4	6	8	2	2	2
±10V 30 kΩ, min				±10V 30 kΩ, min				±10V 30 kΩ, min		
1 to 20kHz ±2% ±0.05%/°C				1 to 20kHz ±2% ±0.05%/°C				1 to 20kHz ±2%(4) ±0.03%/°C		
(non-inverting) 0 dB, nom -0.4 dB, max				(non-inverting) 0 dB, nom -1.6 dB, max				(inverting) 0 dB, nom(3) ±0.05 dB, max		
N/A				N/A				2 ± 10%	5 ± 10%	10 ± 10%
50 μV, RMS 1 Ω ±5 mA ±2 mV				50 μV, RMS 1 Ω ±5 mA ±2 mV				200 μV, RMS 1 Ω ±5 mA ±2 mV		
±25 μV/°C		±50 μV/°C		±25 μV/°C		±50 μV/°C		±25 μV/°C		
±6 mA	±10 mA	±14 mA	±18 mA	±6 mA	±10 mA	±14 mA	±18 mA	±10 mA		
#14 1.5" x 1.5" x 0.4"	#23 2" x 2" x 0.4"	#33 3" x 2.1" x 0.4"		#14 1.5" x 1.5" x 0.4"	#23 2" x 2" x 0.4"	#33 3" x 2.1" x 0.4"		#14 1.5" x 1.5" x 0.4"		

(5) For models with higher input impedance contact Burr-Brown or your local representative.
(6) +9 to +18 VDC power may be used.
(7) ±12 to ±18 VDC power may be used.
(8) The offset may be trimmed to zero, see pg. 7.
(9) All filters have noninverting outputs except the single tuned band pass and band reject filter which have inverting outputs.

M – 58RO

TYPE OF FILTER RESPONSE

Low Pass	Band Pass		Notch
B = Butterworth	K for Q = 1(2 pole pairs only)	S - Special Order **	M for Q = 2
C = Chebyschev 0.4 dB nom ripple	M for Q = 2	indicate Q on order for 2 pole pairs 1 ⩽ Q ⩽ 20	N for Q = 5
D = Chebyschev - 1.6 dB nom ripple	N for Q = 5	1 pole pair 2 ⩽ Q ⩽ 50	P for Q = 10
L = Bessel	P for Q = 10	** Add $25 to order for each special Q value.	S for Q = Special ** (indicate Q on order, 2 ⩽ Q ⩽ 10)
	Q for Q = 20		
	R for Q = 50 (1 pole pair only)		

CUTOFF OR CENTER FREQUENCY

For frequencies less than 100 Hz, use "R" to indicate decimal point. For frequencies greater than 100 Hz, the last digit indicates number of zeros following first 3 digits of frequency. For example: 58 Hz = 58RO, 580 Hz = 5800, 5800 Hz = 5801

Definition of Filter Responses

LOW PASS FILTERS

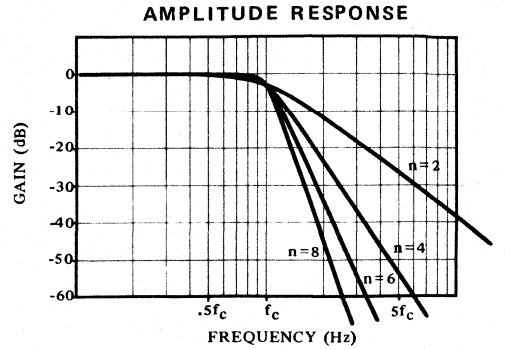
BUTTERWORTH

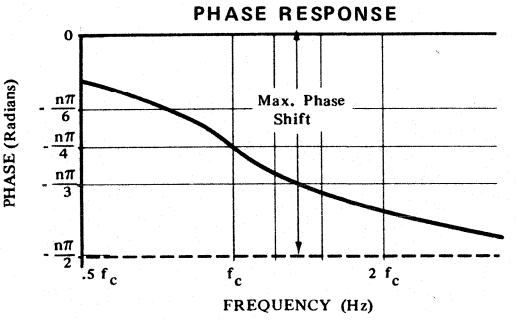
The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.

The cutoff frequency, f_c, is the frequency at which the amplitude response is down 3 dB. The attenuation rate beyond the cutoff frequency is -n6 dB per octave of frequency where n is the order (number of poles) of the filter.

Other characteristics:

- Flattest possible amplitude response
- Excellent gain accuracy at low frequency end of passband.





BESSEL

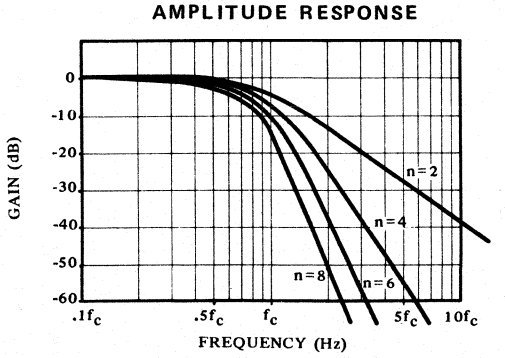
The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

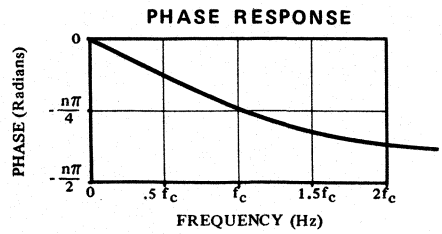
The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, f_c, is defined as the frequency at which the phase shift is one half of this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the -3 dB frequency of the filter.

	2 pole	4 pole	6 pole	8 pole
3 dB Frequency	.77 f_c	.67 f_c	.57 f_c	.50 f_c

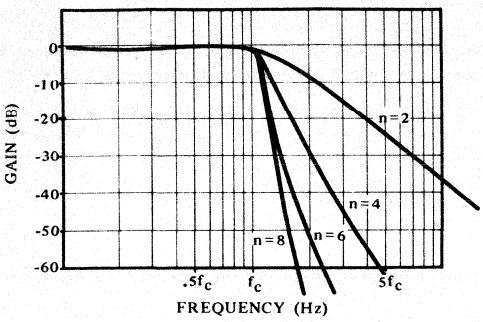
Other characteristics:

- Selectivity not as great as Chebyschev or Butterworth
- Very little overshoot response to step inputs
- Fast rise time

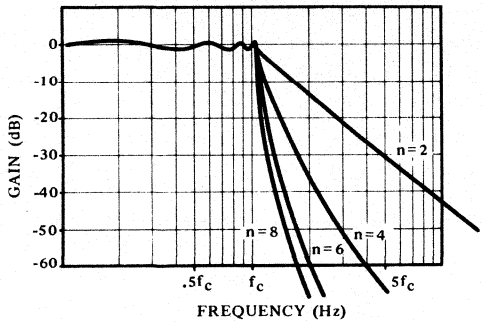




C MODEL AMPLITUDE RESPONSE
(± 0.4 dB Ripple)



D MODEL AMPLITUDE RESPONSE
(± 1.6 dB Ripple)



CHEBYSCHEV

Chebyschev filters have greater selectivity than either the Bessel or Butterworth at the expense of ripple in the passband.

Burr-Brown offers Chebyschev filters with peak to peak ripple design values of ±0.25 dB and ±1.0 dB in the passband. Due to parameter tolerances the actual ripple is allowed to go to ±0.4 and ±1.6 dB; however the rolloff in the stopband will closely approximate the design response. Increased ripple in the passband allows increased attenuation past the cutoff frequency. The filter is designed so that the passband ripples equally about 0 dB.

The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.

Other characteristics:

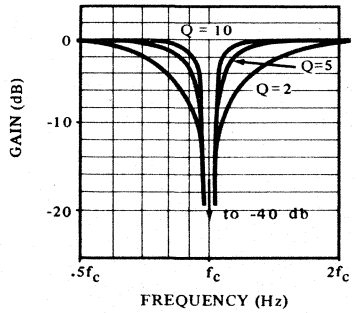
- Greatest selectivity
- Very nonlinear phase response
- High overshoot response to step inputs

The table below shows the typical overshoot and settling time response of the low pass filters to a step input.

	NUMBER OF POLES	PEAK OVERSHOOT	SETTLING TIME (% of final value)		
		% Overshoot	±1%	±0.1%	±0.01%
BUTTERWORTH	2	4	$1.1/f_c$ sec.	$1.7/f_c$ sec.	$1.9/f_c$ sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
BESSEL	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
CHEBYSCHEV (C Model)	2	11	$1.1/f_c$	$1.6/f_c$	-
	4	18	$3.0/f_c$	$5.4/f_c$	-
	6	21	$5.9/f_c$	$10.4/f_c$	-
	8	23	$8.4/f_c$	$16.4/f_c$	-
CHEBYSCHEV (D Model)	2	21	$1.6/f_c$	$2.7/f_c$	-
	4	28	$4.8/f_c$	$8.4/f_c$	-
	6	32	$8.2/f_c$	$16.3/f_c$	-
	8	34	$11.6/f_c$	$24.8/f_c$	-

BAND REJECT FILTERS

AMPLITUDE RESPONSE



Burr-Brown's band reject filters have steep attenuation skirts and a minimum of 40 dB attenuation at f_c. Although f_c is factory adjusted to ±1%, an external trim potentiometer allows adjustment of f_c within a ±3% range allowing the user to obtain the exact frequency desired. A notch adjustment trimmer may also be used to provide a minimum of 40 dB attenuation at any point within the ±3% f_c adjustment range.

The frequencies below and above f_c where the amplitude response is down by 3 dB are referred to as f_1 and f_2 respectively. The selectivity of the filter is defined as: $Q = f_c / (f_2 - f_1)$.

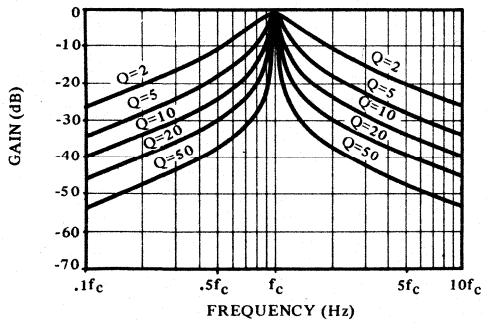
BAND PASS FILTERS

Burr-Brown makes both single-tuned (2 pole) and stagger-tuned (4 pole) bandpass filters. The center frequency, f_c, of single tuned filters can be user adjusted over a ±3% range. Stagger tuned filters are maximally flat in the passband and have steeper attenuation rolloffs than single tuned filters of comparable Q.

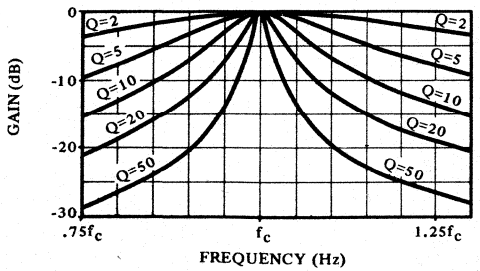
The 3 dB frequencies below and above f_c are f_1 and f_2. The selectivity, Q, is defined as: $Q = f_c / (f_2 - f_1)$. f_c itself is defined as: $f_c = \sqrt{f_1 f_2}$.

SINGLE-TUNED

AMPLITUDE RESPONSE

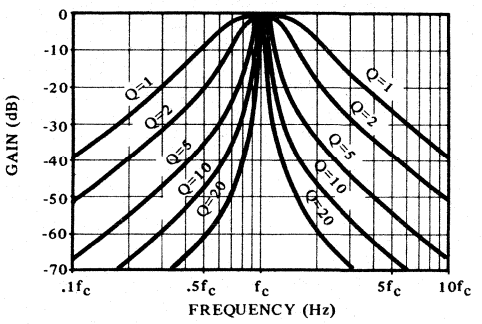


AMPLITUDE RESPONSE EXPANDED SCALE

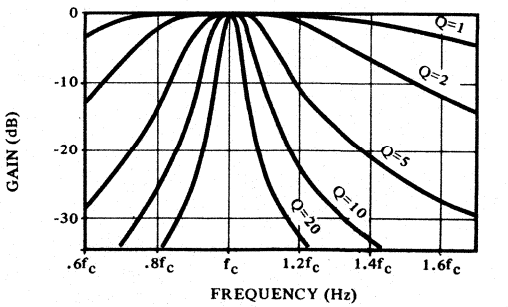


STAGGER-TUNED

AMPLITUDE RESPONSE

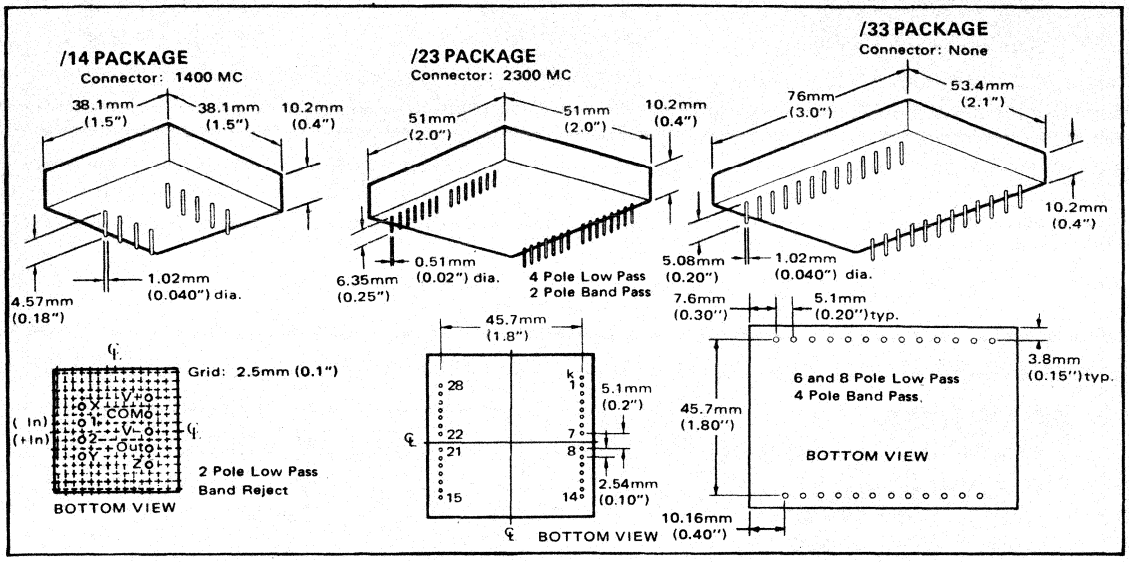


AMPLITUDE RESPONSE EXPANDED SCALE



Mechanical Specifications

Dimensions in millimeters are shown in parentheses.

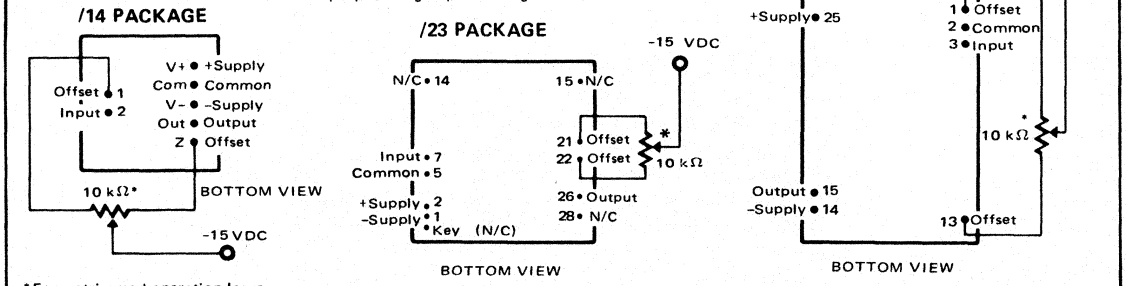


FILTER

Pin Connections

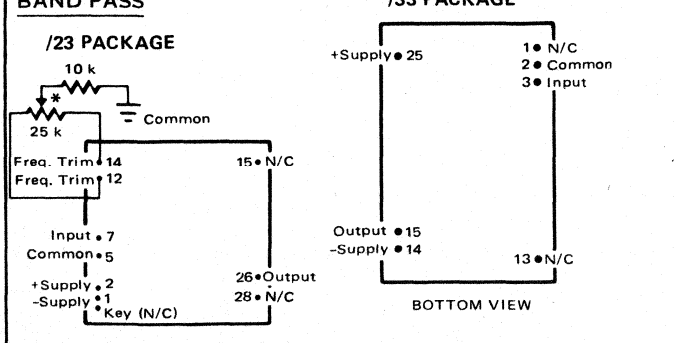
LOW PASS

NOTE: Only the pins shown below are present on actual product package. In the above more pins are shown for purpose of grid positioning.



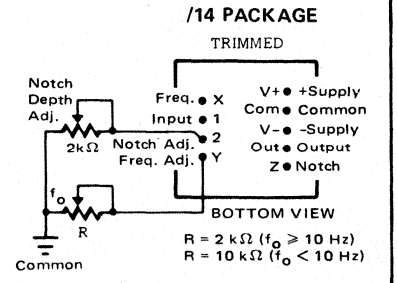
*For untrimmed operation leave adjustment pins open.

BAND PASS



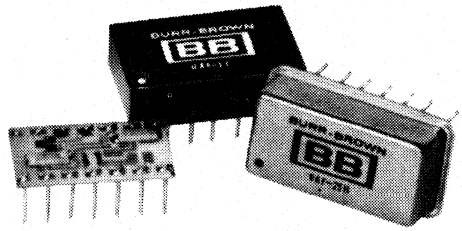
*For untrimmed operation leave adjustment pins open.

BAND REJECT



For untrimmed operation, leave pin 2 and pin Y open while tying pin X and pin Z to ground. When using trimpots leave pins X and Z open.

BURR-BROWN

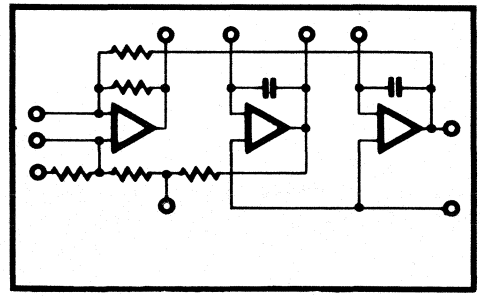


UAF11
UAF21

UNIVERSAL ACTIVE FILTERS

FEATURES

- USER TUNEABLE FREQUENCY, Q-FACTOR, and GAIN
- WIDE FREQUENCY RANGES
  UAF11 - 0.001Hz to 20kHz
  UAF21 - 0.001Hz to 200kHz
- Q-FACTOR RANGE - 0.5 to 500
- EPOXY or HERMETIC DUAL-IN-LINE PACKAGE
- -55°C to +125°C TEMPERATURE RANGE



DESCRIPTION

Burr-Brown's new universal active filters (UAF's) are low cost, versatile units that the user can easily tailor to any active filtering application using the extensive information provided in this data sheet. These UAF's are excellent choices for use in communications equipment, test equipment (engine analyzers, aircraft and automotive test, medical test, etc.), servo systems, process control equipment, sonar and many others.

These UAF's are complete 2-pole active filters with the addition of four external resistors that provide the user easy control of the Q-factor, resonant frequency and gain. Any complex filter response can be obtained by cascading these units. Three separate outputs provide low pass, high pass, and band pass transfer functions. A band reject (notch) transfer function may be realized simply by summing the high pass and low pass outputs.

Since these UAF's are so versatile and flexible, they can be stocked by the user in quantity for use as building blocks whenever the requirement arises. This means instant availability and that UAF purchases may be made in volume to take advantage of quantity price discounts.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-295D

Printed in U.S.A. July, 1978

SPECIFICATIONS

ELECTRICAL

Typical at 25°C and with rated supply unless otherwise noted.

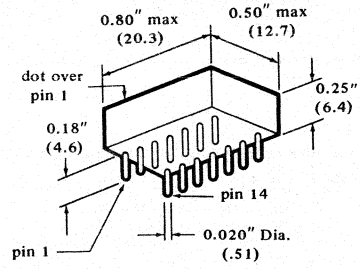
MODEL	UAF11	UAF21(1)	UNITS
INPUT			
Input Bias Current	±100	±15	nA
Input Voltage Range	±10	±10	V
Input Resistance	100 k	100 k	Ω
TRANSFER CHARACTERISTICS			
Frequency Range (f_o)	0.001 to 20 k	0.001 to 200 k	Hz
f_o Accuracy(2)	±1	±1	%
f_o Stability(3) (over temp.range)	±0.005	±0.005	%/°C
Q Range(4)	0.5 −500	0.5 −500	− −
Q Stability(5)			
@ f_o $Q \leq 10^4$	±0.025	±0.01	%/°C
@ f_o $Q \leq 10^5$	±0.1	±0.025	%/°C
Gain Range	0.1 to 50	0.1 to 50	− −
OUTPUT			
Slew Rate	0.6	6.0	V/μsec
Peak to Peak Output Swing(6)			
$f_o \leq 10$ kHz	20	20	V
$f_o \leq 20$ kHz	10	20	V
$f_o \leq 100$ kHz	2	20	V
Output Offset			
(at L.P. output with unity gain)	±10	±10	mV
Output Impedance	2	10	Ω
Noise(7)	200	200	μV (rms)
Output Current(8)	10	10	mA
POWER SUPPLIES			
Rated Power Supplies	±15	±15	V
Power Supply Range(9)	±5 to ±18	±5 to ±18	V
Supply Current @ ±15 V (Quiescent)	±12 max	±12 max	mA
TEMPERATURE RANGE			
Specification Temperature Range			
Epoxy	-25 to +85	-25 to +85	°C
Hermetic	-55 to +125	-55 to +125	°C
Storage Temperature Range	-55 to +125	-55 to +125	°C

(1) The UAF21 includes two internal 0.002μf power supply bypass capacitors.
(2) Repeatability of f_o using 0.1% frequency determining resistors.
(3) T.C.R. of external frequency determining resistors must be added to this figure.
(4) Derated 50% from maximum - see figure 2 for Q vs. F curve.
(5) Q stability varies with both the value of Q and the resonant frequency f_o.
(6) Low pass output - see figure 1 for full power response curve.
(7) Measured at the band pass output with Q = 50 over DC to 50 kHz.
(8) The current required to drive R_7 and R_8 (external) as well as C_7 and C_8 must come from this current.
(9) For supplies below ±10 V, Q max will decrease slightly; filters will operate below ±5 V.

MECHANICAL

Dimensions in millimeters are shown in parentheses.

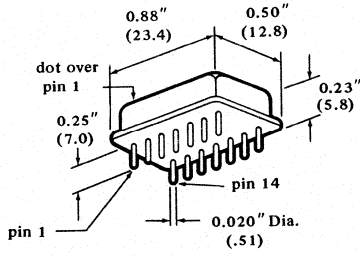
UAF11 UAF21
Epoxy Package



Case - Epoxy
Weight - .12 oz. (3.4)
Connector - 14 pin DIP Connector

"Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)."

UAF11H UAF21H
Hermetic Package



Case - Hermetic Kovar
Weight - .15 oz. (3.4)
Connector - 14 pin DIP Connector

PIN CONNECTIONS

Pin 1 – High Pass Output
Pin 2 – N/C
Pin 3 – Band Pass Output
Pin 4 – Q Adj. Point
Pin 5 – Common
Pin 6 – + Supply
Pin 7 – Low Pass Output
Pin 8 – Frequency Adj.
Pin 9 – – Supply
Pin 10 – Frequency Adj.
Pin 11 – N/C
Pin 12 – Input 1
Pin 13 – Input 2
Pin 14 – Input 3

TYPICAL PERFORMANCE CURVES

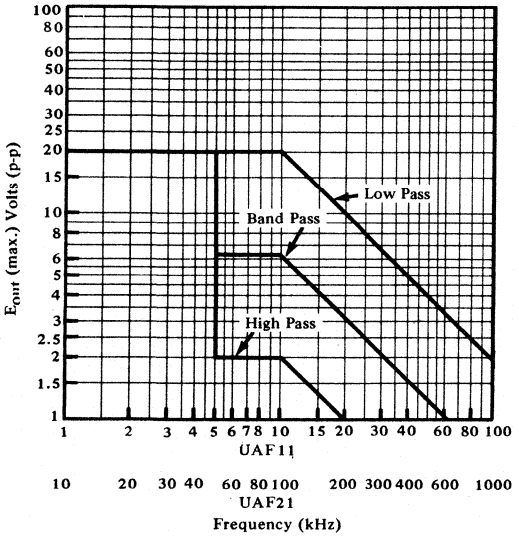


FIGURE 1. Full Power Response.

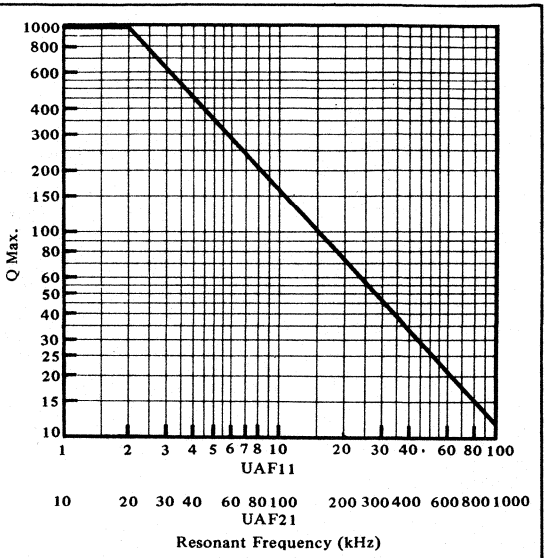


FIGURE 2. Q max. vs. Resonant Frequency.

ACTIVE FILTER DESIGN
USING UNIVERSAL ACTIVE FILTERS

The UAF as shown in Figure 3 can be connected in a variety of configurations. Figures 5, 6, 7 and 8 illustrate four useful circuits. These circuits and the simplified design equations needed to calculate their four external resistors are shown. Detailed design formulas are also shown to allow the user more design flexibility.

One UAF is required for every two poles of low pass or high pass filters. One UAF is required for each pole-pair of band pass or band reject filters.

The three basic second order transfer function forms are:

$$T(\text{Low Pass}) = \frac{A_{LP}\,\omega_o^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2} \qquad T(\text{Band Pass}) = \frac{A_{BP}\,(\omega_o/Q)s}{s^2 + (\omega_o/Q)\,s + \omega_o^2} \qquad T(\text{High Pass}) = \frac{A_{HP}\,s^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

where $\omega_o = 2\pi f_o$.

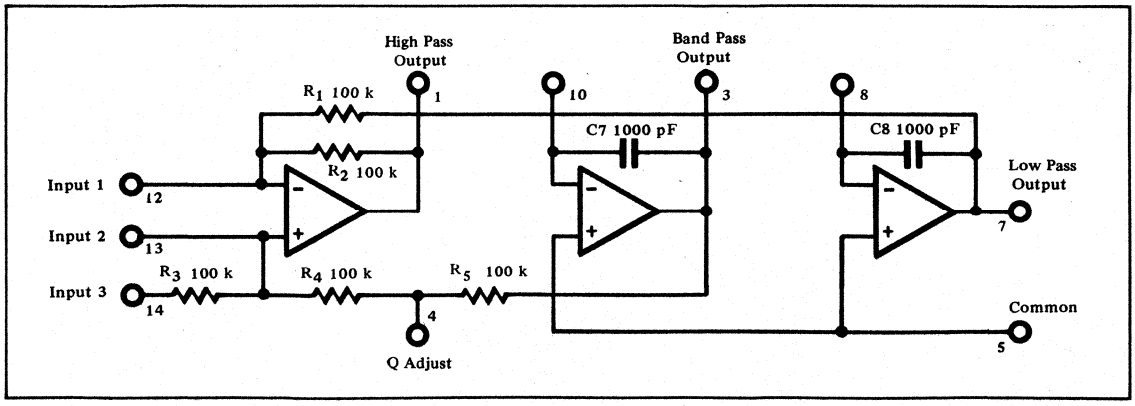


FIGURE 3. Universal Active Filter Simplified Schematic.

To use the four UAF circuits in Figures 5, 6, 7 and 8, the following information should be known about each 2-pole filter section:

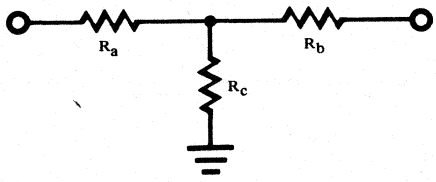
1. f_o – the undamped natural frequency of the complex pole-pair.

   f_o values for many low pass and high pass filters are given in the filter parameter table on page 4-96.

   f_o for each one pole-pair band pass filter is the center frequency (f_c). f_c is defined as $f_c = \sqrt{f_1 f_2}$ when f_1 is the upper 3 dB point and f_2 is the lower 3 dB point of the filter.

   To use these UAF's with f_o above 5kHz for the UAF11 or above 50kHz for the UAF21 an 11kΩ resistor must be placed in parallel with R_2 (between pins 12 and 1). For the higher frequencies where an 11kΩ resistor is required, use simplified design equations "B". For operation below these frequencies, use simplified design equations "A".

   To obtain f_o below 100 Hz using practical resistor values, T-networks may be used for the frequency determining resistors (R_7 and R_8).



   The equivalent resistance if inserted between pins 1 and 10 or pins 3 and 8 is

$$R = \frac{R_a R_b}{R_c} + R_a + R_b$$

   Capacitors may also be paralleled with C_7 and C_8 to reduce f_o. If capacitors are added in parallel, use the detailed frequency determination equations given with each circuit.

   If the ratio $\frac{R_2}{R_1}$ is decreased, f_o is reduced by the factor $\sqrt{R_2/R_1}$. If the R_2/R_1 ratio is changed, the detailed transfer function equations should be used.

2. A – The gain (V/V) required of the filter section:
   A_{LP} - for low pass output - gain at d.c.
   A_{BP} - for band pass output - gain at f_o
   A_{HP} - for high pass output - gain at high frequencies

3. Q factor
   For band pass filters $Q = \frac{f_o}{3\text{ dB bandwidth}}$

Q values for many low pass and high pass filters are given in Table I.

Table III shows a FORTRAN computer program to transform positions to band pass pole positions.

When designing low pass filters of more than two poles, best results will be obtained if the two pole sections with lower Q are followed by the sections with higher Q. This will eliminate any possibility of clipping due to high gain ripple in high Q sections.

Calculate the f_o times Q product of the filter. If the product is above 10^4Hz for the UAF11 (or 10^5Hz for the UAF21) locate the corresponding f_o Q_p product in Figure 4. Divide f_o Q_p by f_o to obtain Q_p. Use Q_p as indicated in the following equations to correct for amplifier phase shift errors. For f_o Q products below 10^4 (or 10^5)Hz, simply use Q.

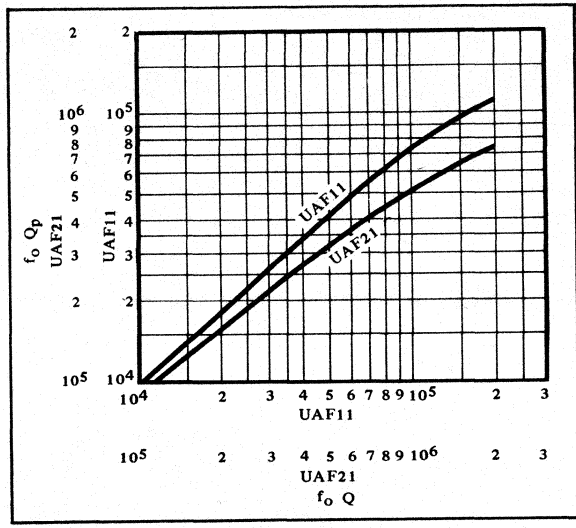
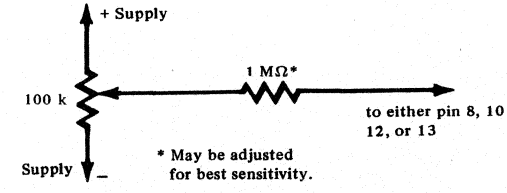


FIGURE 4. Q_p Determination

OFFSET ERROR ADJUSTMENT

- DC offset errors will be minimized by grounding pin 5 through a resistor equal to 1/2 the value of R_7 or R_8.
- The DC offset adjustment shown below may be used if required. It is particularly useful when large values of resistance are used for R_7 and R_8.



BI-QUAD CONFIGURATION

The connection of the UAF shown in Figure 5 is known as the Bi-Quad configuration. The low pass and band pass outputs only are available. The design equations are very straight forward but variations in R_7 affect Q as well as frequency. This results in a constant bandwidth filter at the band pass output as resonant frequency is varied. Note: The two other circuits shown (figures 6 and 7) maintain constant Q with resonant frequency variations.

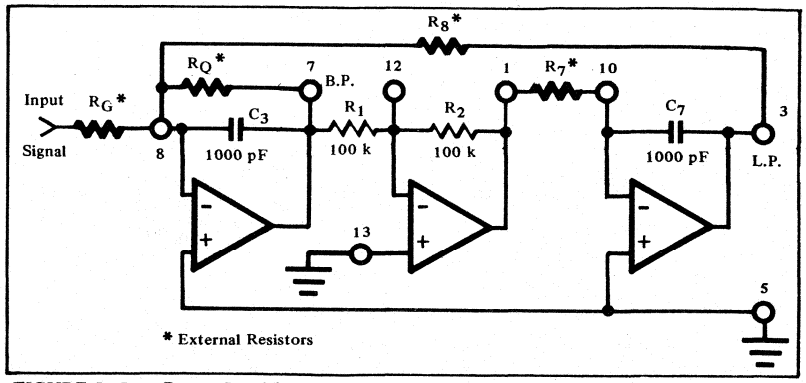


FIGURE 5. Low Pass & Band Pass Active Filter Circuit.

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 5$ kHz (UAF11) or 50 kHz (UAF21)

1. $R_7 = R_8 = 10^9/\omega_o = 1.59 \times 10^8/f_o$
2. $Q\,A_{LP} = A_{BP}$
3. $R_Q = Q_p R_7$
4. $R_G = R_Q/A_{BP}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o > 5$ kHz (UAF11) or 50 kHz (UAF21)

1. $R_7 = R_8 = 3.16 \times 10^8/\omega_o = 5.03 \times 10^7/f_o$
2. $Q\,A_{LP} = A_{BP}$
3. $R_Q = 3.16\,Q_p R_7$
4. $R_G = R_Q/A_{BP}$

DETAILED TRANSFER FUNCTION EQUATIONS

1. $\omega_o^2 = R_2/(R_1 R_7 C_7 R_8 C_8)$
2. $Q = R_Q C_8 \omega_o$
3. $Q\,A_{LP}/(\omega_o R_8 C_8) = A_{BP} = R_Q/R_G$

LOW PASS and HIGH PASS

The UAF configuration shown in Figure 6 is best suited for low pass and high pass responses (they are inverted while the band pass output is not inverted).

NOTE: To obtain a positive value for R_Q (equation 4)

$A_{BP}\,(2\,R_G \times 10^{-5} + 1) > 1$

$[A_{BP}\,(L1\,R_G \times 10^{-4} + 1) > 1]$

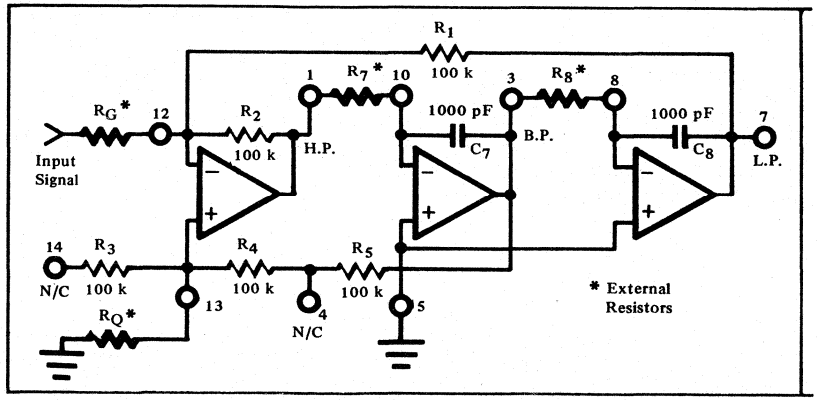


FIGURE 6. High Pass and Low Pass Active Filter Circuit.

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 5$ kHz (UAF11) or 50 kHz (UAF21)

1. $R_7 = R_8 = 10^9/\omega_o = 1.59 \times 10^8/f_o$
2. $Q\,A_{LP} = Q\,A_{HP} = A_{BP}$
3. $R_G = 10^5\,Q_p/A_{BP}$
4. $R_Q = 2 \times 10^5/(2\,A_{BP}\,R_G \times 10^{-5} + A_{BP} - 1)$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o > 5$ kHz (UAF11) or 50 kHz (UAF21)

1. $R_7 = R_8 = 3.16 \times 10^8/\omega_o = 5.03 \times 10^7/f_o$
2. $Q\,A_{LP} = 10\,Q\,A_{HP} = 3.16\,A_{BP}$
3. $R_G = 3.16 \times 10^4\,Q_p/A_{BP}$
4. $R_Q = 2 \times 10^5/(1.1\,A_{BP}\,R_G \times 10^{-4} + A_{BP} - 1)$

DETAILED TRANSFER FUNCTION EQUATIONS

1. $\omega_o^2 = R_2/(R_1 R_7 C_7 R_8 C_8)$
2. $Q = R_p\,(1 + 2 \times 10^5/R_Q)\sqrt{R_7 C_7/(R_1 R_2 R_8 C_8)}$
3. $Q\,A_{LP} = Q\,R_1\,A_{HP}/R_2 = A_{BP}\sqrt{R_1 R_7 C_7/(R_2 R_8 C_8)}$
4. $A_{BP} = \sqrt{R_1 R_2 R_8 C_8/(R_7 C_7)}\;Q/R_G$
5. $1/R_p = 1/R_1 + 1/R_2 + 1/R_G$

BAND PASS

The circuit shown in Figure 7 is an excellent one for use with band pass filters. Since the signal input is fed to the noninverting input, the high pass and low pass outputs are not inverted while the band pass output is inverted.

NOTE: To obtain a positive value for R_Q (equation 3), $2\ Q_p > A_{BP} + 1$ (or $3.48\ Q_p > A_{BP} + 1$).

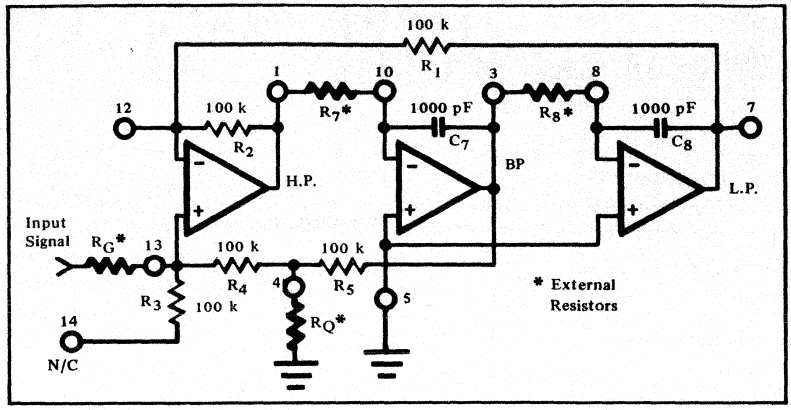


FIGURE 7. Band Pass Active Filter Circuit.

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 5$ kHz (UAF11) or 50 kHz (UAF21)

1. $R_7 = R_8 = 10^9/\omega_o = 1.59 \times 10^8/f_o$
2. $Q\,A_{LP} = Q\,A_{HP} = A_{BP}$
3. $R_Q = 10^5/(2Q_p - A_{BP} - 1)$
4. $R_G = (2\,Q_p - A_{BP} + 1)\ 10^5/A_{BP}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o > 5$ kHz (UAF11) or 50 kHz (UAF21)

1. $R_7 = R_8 = 3.16 \times 10^8/\omega_o = 5.03 \times 10^7/f_o$
2. $Q\,A_{LP} = 10\,Q\,A_{HP} = 3.16\,A_{BP}$
3. $R_Q = 10^5/(3.48\,Q_p - A_{BP} - 1)$
4. $R_G = (3.48\ Q_p - A_{BP} + 1)\ 10^5/A_{BP}$

DETAILED TRANSFER FUNCTION EQUATIONS

1. $\omega_o^2 = R_2/(R_1R_7C_7R_8C_8)$
2. $Q = \left(1 + \frac{R_E}{R_G}\right)\left(\frac{R_1}{R_1 + R_2}\right)\ (1 + 10^5/R_Q)\ \sqrt{\frac{R_2R_7C_7}{R_1R_8C_8}}$
3. $R_E = 10^5 + 10^5\,R_Q/(10^5 + R_Q)$
4. $Q\,A_{LP} = Q\,A_{HP}\,R_1/R_2 = A_{BP}\sqrt{R_1R_7C_7/(R_2R_8C_8)}$
5. $A_{BP} = 10^5\,(2 + 10^5/R_Q)/R_G$

BAND REJECT

The band reject configuration is achieved by summing the high pass and low pass UAF outputs. The circuits shown in Figures 6 and 7 can be used to provide the band reject function if they are connected as shown in Figure 8. The Figure 8 circuit is applicable when using simplified design equations "A" ($A_{LP} = A_{HP}$), but when operating with an 11 k resistor between pins 12 and 1 ($A_{LP} = 10\ A_{HP}$), the resistor at pin 7 must be 10 times the resistor at pin 1 to obtain equal passband gains above and below f_o.

In either case, the four external UAF resistors (R_G, R_Q, R_7 and R_8) should be calculated for f_o and Q of the band reject filter desired and for A_{LP} to equal the desired passband gain. An input constraint: the input voltage times A_{BP} must not exceed the rated peak-peak output voltage of the band pass output or clipping and distortion will result.

NOTE: The band reject output may simply be taken at point A if 5 kΩ output impedance is acceptable.

$Q = f_o/(3\text{ dB bandwidth})$

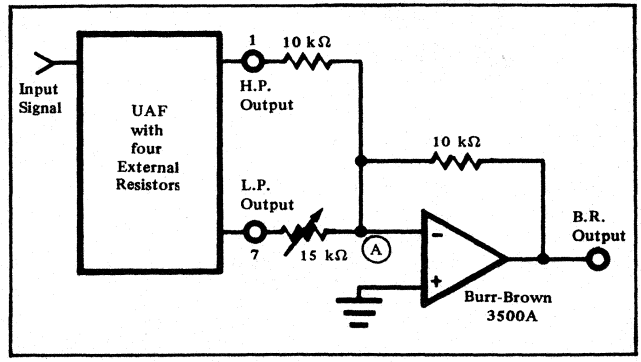


FIGURE 8. Band Reject Output.

FILTER PARAMETERS

LOW PASS and HIGH PASS

Table I shows filter parameters for many 2-8 pole low pass filters. The Q and the normalized undamped natural frequency, f_n, for each two-pole section are shown. The Q values should be used with Figure 3 and in the design formulas. f_n must be multiplied by the desired cutoff frequency of the overall filter to obtain the required frequency, f_o, for the design formulas. As an example, consider a 4-pole low pass Bessel filter with a cutoff frequency of 1000 Hz. The first stage would be designed to an f_o of 1432.41 Hz and a Q of 0.52193 while the second stage would have an f_o of 1605.94 Hz and a Q of 0.80554. The low pass output of the first stage (pin 7) should be connected to the input resistor (R_G) of the second stage.

Filters with an odd number of poles show one f_n with no corresponding Q value. This represents the simple RC network that is required for odd pole filters. This RC network with a cutoff frequency equal to f_n times the overall filter cutoff frequency should be placed in series with the first UAF two-pole section. A buffer amplifier between the RC network and the UAF input will isolate the RC network so that the UAF input resistor will not affect the cutoff frequency of the RC network.

The cutoff frequency determined by the Table I filter parameters is (1) the 3 dB frequency of the Butterworth response and of the Bessel response and (2) the frequency at which the amplitude response of the Chebyshev filters passes through the maximum ripple band and enters the stop band.

To obtain high pass pole positions, the low pass to high pass transformation may be used: $f_n\,(\text{high pass}) = \dfrac{1}{f_n\,(\text{low pass})}$

$Q\,(\text{high pass}) = Q\,(\text{low pass})$

The low pass to band pass transformation is much more complicated, but it can be done using the low pass to band pass conversion program (Table III).

Number of Poles	Butterworth		Bessel		CHEBYSHEV 0.5 dB Ripple		CHEBYSHEV 2 dB Ripple	
	f_n	Q	f_n	Q	f_n	Q	f_n	Q
2	1.0	0.70711	1.2742	0.57735	1.23134	0.86372	0.907227	1.1286
3	1.0	-------	1.32475	------	0.626456	-----	0.368911	-----
	1.0	1.0	1.44993	0.69104	1.068853	1.7062	0.941326	2.5516
4	1.0	0.54118	1.43241	0.52193	0.597002	0.70511	0.470711	0.9294
	1.0	1.3065	1.60594	0.80554	1.031270	2.9406	0.963678	4.59388
5	1.0	-------	1.50470	------	0.362320	-----	0.218308	-----
	1.0	0.61805	1.55876	0.56354	0.690483	1.1778	0.627017	1.77509
	1.0	1.61812	1.75812	0.91652	1.017735	4.5450	0.97579	7.23228
6	1.0	0.51763	1.60653	0.51032	0.396229	0.68364	0.31611	0.9016
	1.0	0.70711	1.69186	0.61120	0.768121	1.8104	0.730027	2.84426
	1.0	1.93349	1.90782	1.0233	1.011446	6.5128	0.982828	10.4616
7	1.0	-------	1.68713	-----	0.256170	-----	0.155410	-----
	1.0	0.55497	1.71911	0.53235	0.503863	1.0916	0.460853	1.64642
	1.0	0.80192	1.82539	0.66083	0.822729	2.5755	0.797114	4.11507
	1.0	2.2472	2.05279	1.1263	1.008022	8.8418	0.987226	14.2802
8	1.0	0.50980	1.78143	0.50599	0.296736	0.6765S	0.237699	0.89236
	1.0	0.60134	1.83514	0.55961	0.598874	1.6107	0.571925	2.5327
	1.0	0.89998	1.95645	0.71085	0.861007	3.4657	0.842486	5.58354
	1.0	2.5629	2.19237	1.2257	1.005984	11.530S	0.990142	18.6873

TABLE I. Low Pass Filter Parameters.

LOW PASS CHEBYSHEV

Table II details a FORTRAN program to determine f_n and Q for a Chebyshev low pass filter. The only inputs required are the number of poles and the peak to peak ripple (dB) of the desired filter. The program outputs are treated exactly as the values on the pole position table (Table I).

```
      PI=3.1415926536
      COMPLEX P(10)
      READ 5,N,R
    5 FORMAT(I2,F8.6)
      A=SQRT(EXP(R/4.3429448)-1.)
      B=1./A
      AN=ALOG(B+SQRT(B**2+1.))
      AN=AN/FLOAT(N)
      J=MOD(N,2)+N/2
      DO 10 K=1,J
      RP=-SINH(AN)*SIN(PI*FLOAT(2*K-1)/FLOAT(2*N))
      XIP=COSH(AN)*COS(PI*FLOAT(2*K-1)/FLOAT(2*N))
      WN=SQRT(RP**2+XIP**2)
      Q=-WN/(2.*RP)
      P(K)=CMPLX(WN,Q)
      IF(MOD(N,2).NE.O.AND.K.EQ.J) GO TO 15
      PRINT 20,P(K)
      GO TO 10
   15 F=REAL(P(K))
      PRINT 30,F
   10 CONTINUE
   20 FORMAT(2X"FN = "E20.8" Q = "E20.8)
   30 FORMAT (2X"FN = "E20.8)
      STOP
      END
```

TABLE II. Low Pass Chebyshev Program.

BAND PASS

Table III details a FORTRAN program that may be used to transform low pass pole positions into the equivalent band pass pole positions.

Program Inputs:

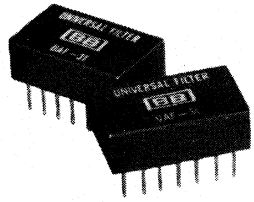
1. f_o - From Table I for the low pass filter of interest.
2. Q from Table I.
3. Q_{BP} - Desired Q of the band pass filter.

For filters with an odd number of poles a Q of .5 should be used where Q is not given in Table I. The program transforms each low pass pole into a band pass pole pair. That is, using the two-pole low pass pole positions would result in the pole positions for a two pole pair, band pass filter, requiring two UAF stages. Enter 10^6 for Q when transforming zeros on the imaginary axis. This program automates the transformation $s = p/2 \pm \sqrt{(p/2)^2 - 1}$.

```
      COMPLEX P,S,U
      READ 5, FN, Q, QBP
    5 FORMAT (3F12.5)
      Y=FN*SQRT(1.-(1./(Q*2.))**2)
      X=-FN/(Q*2.)
      P=CMPLX(X,Y)
      U=CONJG(P)
      DO 30 I=1,2
      S=P/(2.*QBP)
      P=S**2-1.
      T=ATAN2(AIMAG(P),REAL(P))
      IF(T.GE.O.) GO TO 10
      T=2.*3.14159+T
   10 T=T/2.
      A=SQRT(CABS(P))*COS(T)
      B=SQRT(CABS(P))* SIN(T)
      S=S+CMPLX(A,B)
      FN=CABS(S)
      Q=-FN/(2.*REAL(S))
      PRINT 20,FN,Q
   20 FORMAT (2X"FN = "F12.5" Q = "F12.5)
      IF(AIMAG(U).EQ.O.) GO TO 40
   30 P=U
   40 STOP
      END
```

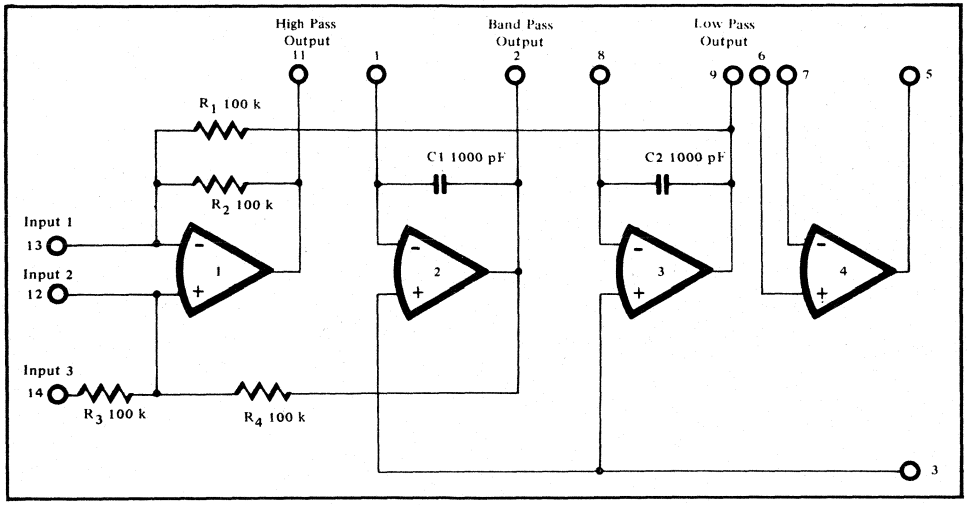
TABLE III. Low Pass to Band Pass Transformation Program.

BURR-BROWN



UAF31

UNIVERSAL ACTIVE FILTER



FEATURES

- **LOW COST**
- **SAVES DESIGN TIME**
  - **Calculate only three resistance values**
  - **Design directly from this data sheet**
  - **Completely characterized parameters**
- **IMPROVED PERFORMANCE**
  - **1% frequency accuracy**
  - **Uncommitted op amp included**
  - **Q range of 0.5 to 500**
  - **Reliable hybrid construction**
  - **NPO capacitors and thin-film resistors**

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PDS-318B

Printed in U.S.A. July, 1978

DESCRIPTION

The UAF31 is a versatile 2-pole active filter which, with the addition of three or four external resistors, provides the user easy control of the Q-factor, resonant frequency and gain. Any complex filter response can be obtained by cascading units. The UAF31 is an ideal building block that can be purchased and stocked in quantity to be used whenever the requirement for a filter arises. In this way filters are available immediately and may be purchased in volume to take advantage of quantity price discounts.

Three separate outputs provide low pass, high pass, and band pass transfer functions. A band reject (notch) transfer function may be realized simply by summing the high pass and low pass outputs. The UAF31 also includes an uncommitted op amp that may be used as an input or output buffer or to add an additional one-pole response to the filter.

TRANSFER FUNCTION

The UAF31 uses the state variable technique to produce a basic second order transfer function. The equations describing the three outputs available are:

$$T(\text{Low Pass}) = \frac{A_{LP}\omega_o^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{Band Pass}) = \frac{A_{BP}(\omega_o/Q)s}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{High Pass}) = \frac{A_{HP}\,s^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

To obtain band reject characteristics the low pass and high pass outputs are summed to form a pair of $j\omega$ axis zeros:

$$T(\text{Band Reject}) = \frac{A\,(s^2 + \omega_o^2)}{s^2+(\omega_o/Q)\,s + \omega_o^2} \text{ where } A_{LP}=A_{HP}=A.$$

The state variable approach uses two op amp integrators (#2 and #3 in the simplified schematic below) and a summing amplifier (#1) to provide simultaneous low pass, band pass and high pass responses. One UAF31 is required for each two poles of low pass or high pass filters and for each pole-pair of band pass or band reject filters.

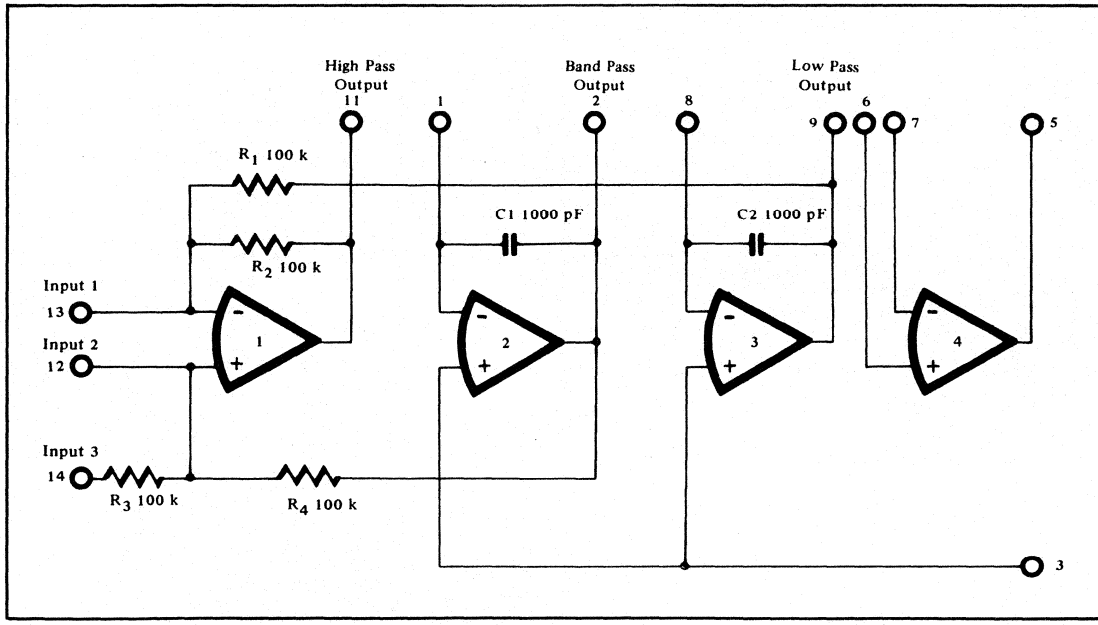


FIGURE 1. UAF31 Schematic.

SPECIFICATIONS

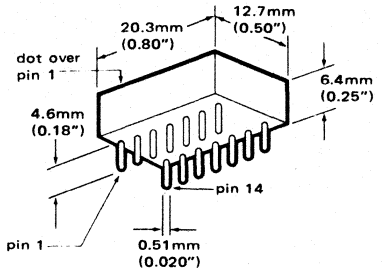
ELECTRICAL

Typical at 25°C and with rated supply unless otherwise noted.

MODEL	UAF31
INPUT	
Input Bias Current	±40 nA
Input Voltage Range	±10 V
Input Resistance	100 kΩ
TRANSFER CHARACTERISTICS	
Frequency Range (f_o)	0.001 to 25 kHz
f_o Accuracy(1), max	±1%
f_o Stability(2)	±0.002%/°C
Q Range(3)	0.5-500
Q Stability(4)	
@f_o Q ≤ 10^4	±0.01%/°C
@f_o Q ≤ 10^5	±0.025%/°C
Q Repeatability	±10%
Gain Range	0.1 to 50V/V
OUTPUT	
Peak to Peak Output Swing(5)	20 V
Output Offset (at L.P. output with unity gain)	±20 mV
Output Impedance	1 Ω
Noise(6)	200 μV (rms)
Output Current(7)	5 mA
UNCOMMITTED AMP CHARACTERISTICS	
Input Offset Voltage	5 mV
Input Bias Current	40 nA
Input Impedance	1 MΩ
Large Signal Voltage Gain	85 dB
Output Current	5 mA
POWER SUPPLIES	
Rated Power Supplies	±15 V
Power Supply Range(8)	±5 to ±18 V
Supply Current @ ±15 V(Quiescent), max	12 mA
TEMPERATURE RANGE	
Specification Temperature Range	-25 to +85°C
Storage Temperature Range	-25 to +85°C

(1) The tolerance of external frequency determining resistors must be added to this figure.
(2) T.C.R. of external frequency determining resistors must be added to this figure.
(3) See figure 3 for Q vs. F curve.
(4) Q stability varies with both the value of Q and the resonant frequency f_o.
(5) See figure 2 for full power response curve.
(6) Measured at the band pass output with Q @ 50 over DC to 50 kHz.
(7) The current required to drive R_{F1} and C_1 and C_2 must come from this current.
(8) For supplies below ±10 V, Q max will decrease slightly; filters will operate below ±5 V.

MECHANICAL



ROW SPACING—7.6 (0.300")
WEIGHT—.12 oz. (3.4)
CONNECTOR—14 pin DIP connector

Pin material and plating composition conform to method 208 (solderability) of MIL-STD-202.

PIN CONNECTIONS

Pin 1—Frequency Adjust
Pin 2—Band pass Output
Pin 3—Common
Pin 4—Positive Supply
Pin 5—Auxiliary Amp. Output
Pin 6—Auxiliary Amp + Input
Pin 7—Auxiliary Amp - Input
Pin 8—Frequency Adjust
Pin 9—Low Pass Output
Pin 10—Negative Supply
Pin 11—High Pass Output
Pin 12—Filter Input 2
Pin 13—Filter Input 1
Pin 14—Filter Input 3

TYPICAL PERFORMANCE CURVES

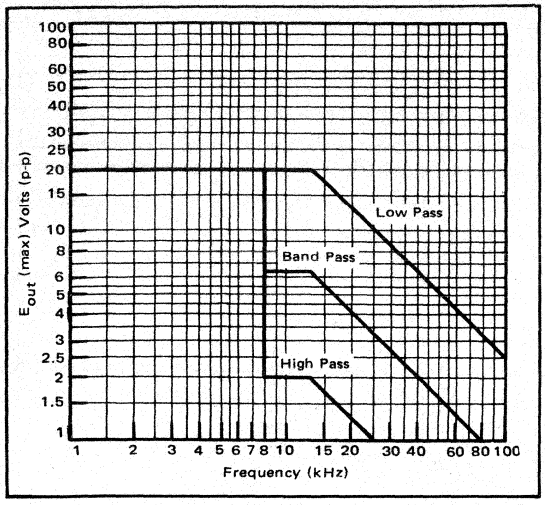


FIGURE 2. Full Power Response

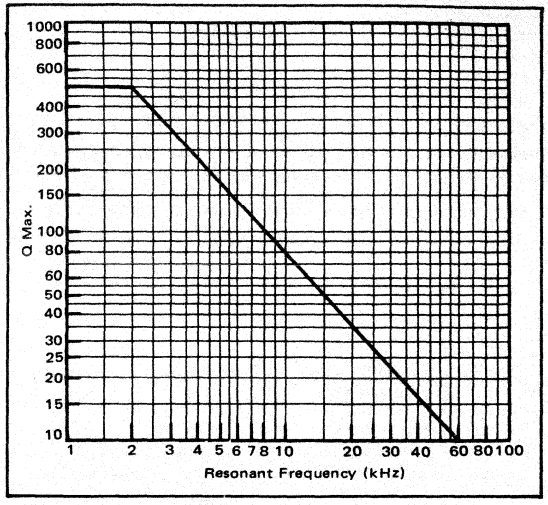


FIGURE 3. Q Max. vs. Resonant Frequency

ACTIVE FILTER DESIGN PROCEDURE

To design filters using the circuits shown on the following pages, these six design steps should be followed:

1. Determine f_o, the natural frequency of the pole pair.
2. Determine A, the gain of the filter section (V/V).
3. Determine the Q factor.
4. Calculate Q_p as shown in the Q factor design notes to compensate for amplifier phase shift errors.
5. Determine the filter configuration that will be used (see configuration selection guide on the opposite page for recommendations).
6. Calculate the resistance values required using the design equations for the filter configuration selected.

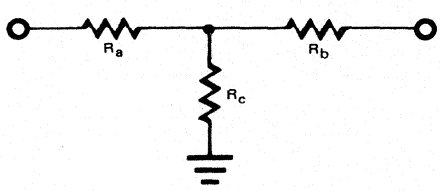
NATURAL FREQUENCY (f_o) DESIGN NOTES

f_o values for many low pass and high pass filters are given in the filter parameter table on page 4-104.

f_o for each one pole-pair band pass filter is the center frequency (f_c). f_c is defined as $f_c = \sqrt{f_1 f_2}$ when f_1 is the lower 3 dB point and f_2 is the upper 3 dB point of the filter.

To use the UAF31 with f_o above 8 kHz, an 11 kΩ resistor must be placed in parallel with R_2 (between pins 13 and 11). For the higher frequencies where an 11 kΩ resistor is required, use simplified design equations "B". For operation below these frequencies; use simplified design equations "A" or "B".

To obtain f_o below 100 Hz using practical resistor values, T-networks may be used for the frequency determining resistors (R_{F1} and R_{F2}).



The equivalent resistance if inserted between pins 1 and 11 or pins 2 and 8 is

$$R = \frac{R_a R_b}{R_c} + R_a + R_b$$

Capacitors may also be paralleled with C_1 and C_2 to reduce the size of R_{F1} and R_{F2}. If capacitors are added in parallel,

$$R_{F1}(\text{new}) = R_{F2}(\text{new}) = R_{F1}(\text{old}) \frac{1000\ \text{pF}}{C + 1000\ \text{pF}}$$

where R_F(new) are the new lower value frequency resistors, C is the value of the two external capacitors placed across C_1 and C_2 (between pins 1 and 2 and pins 8 and 9), R_{F1} (old) is the value calculated in the simplified design equations.

GAIN (A) DESIGN NOTES

The gain (V/V) of the filter section is:

A_{LP} - for low pass output - gain at DC.

A_{BP} - for band pass output - gain at f_o.

A_{HP} - for high pass output - gain at high frequencies.

Q FACTOR DESIGN NOTES

For band pass filters $Q = \frac{f_o}{3\text{ dB bandwidth}}$

Q values for many low pass and high pass filters are given in the pole position table on page 4-104.

A FORTRAN computer program to transform low pass pole positions to band pass pole positions is given on page 4-105.

When designing low pass filters of more than two poles, best results will be obtained if the two pole sections with lower Q are followed by the sections with higher Q. This will eliminate any possibility of clipping due to high gain ripple in high Q sections.

Q repeatability (Q change from unit-to-unit) is typically ±5% at f_oQ products less than 10^4. The Q repeatability error increases as the f_oQ product increases, to approximately ±20% for f_oQ products near 10^6.

Calculate the f_o times Q product of the filter. If the product is above 10^4 Hz, locate the corresponding f_oQ_p product in Figure 4. Divide f_oQ_p by f_o to obtain Q_p. Use Q_p as indicated in the equations on page 6 to correct for amplifier phase shift errors. For f_oQ products below 10^4 Hz, simply use Q. As can be seen in Figure 4, the amplifier phase shift errors cause Q to rise with increasing f_oQ products.

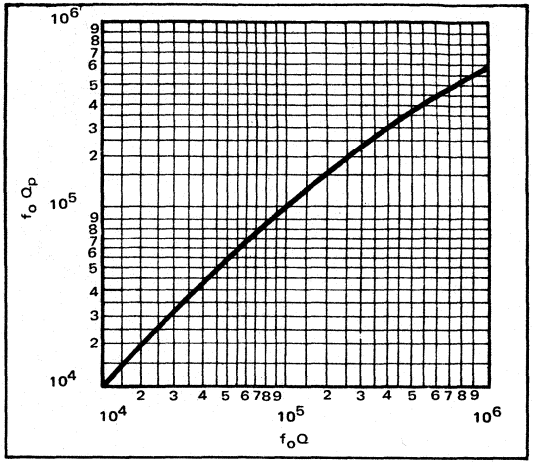


FIGURE 4. Qp Determination

NOTE: For more comprehensive detailed design procedure and illustrated examples of filter design using the Universal Active Filters, please refer to PDS-359, product data sheet for Burr-Brown model No. UAF41.

CONFIGURATION SELECTION GUIDE

	NONINVERTING INPUT	INVERTING INPUT	BI-QUAD
Outputs Available	BP, LP and HP	BP, LP and HP	BP and LP
Inverted Outputs	BP	HP and LP	BP and LP
Q & Gain Independent of Frequency Resistors?	Yes	Yes	No
Type of Q Variation With Changes in R_F	Constant Q	Constant Q	Constant bandwidth
Other Advantages	May be used with only three external resistors (use internal R_3 as R_G)		R_G and R_Q are small at high frequencies
Parameter Limitations	$2Q_p - A_{BP} > 1$ ($f_o < 8$ kHz) $3.48Q_p - A_{BP} > 1$ ($f_o > 8$ kHz)	$2Q_p + A_{BP} > 1$ ($f_o < 8$ kHz) $3.48Q_p + A_{BP} > 1$ ($f_o > 8$ kHz)	NONE
Summary:	The Bi-Quad filter is particularly useful as a bandpass filter if the filter bandwidth must be kept constant as the center frequency is varied. If Q must be kept constant (i.e., constant Q of a band pass or maintaining a constant response of a lowpass or highpass) one of the other two configurations should be used. The Bi-Quad also has the advantage that R_G and R_Q are smaller than R_G and R_Q of the other two configurations (this is especially useful at high frequencies). The noninverting input configuration has the advantage that for $A_{BP} = 1$, $R_G = 100$ k therefore R_3 (internal) may be used so that only three external resistors are needed (R_{F1}, R_{F2}, R_Q).		

NONINVERTING INPUT CONFIGURATION

For applications requiring a band pass gain of 1 (V/V), the internal resistor R_3 may be used (input at pin 14) as the gain resistor R_G. Thus only three external resistors are needed to configure the filter.

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 8$ kHz

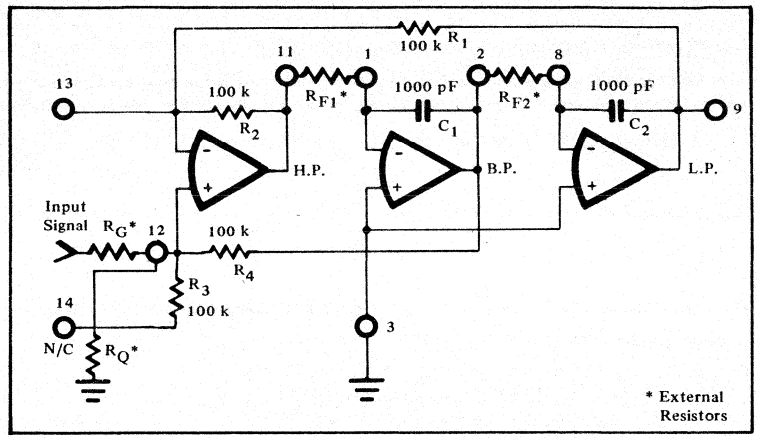
1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$
2. $A_{BP} = Q\,A_{LP} = Q\,A_{HP}$
3. $R_G = \frac{10^5\ Q}{A_{BP}\ Q_P}$
4. $R_Q = \frac{10^5}{2Q_P - \frac{A_{BP}\,Q_P}{Q} - 1}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o \geq 8$ kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$
2. $A_{BP} = \frac{Q}{3.16}\,A_{LP} = 3.16\,Q\,A_{HP}$
3. $R_G = \frac{10^5\ Q}{A_{BP}\ Q_P}$
4. $R_Q = \frac{10^5}{3.48\,Q_P - A_{BP}\,Q_P/Q - 1}$

* To use equations "B" connect an 11 k resistor between pins 11 and 13. Equations "B" are also valid for frequencies below 8 kHz.



INVERTING INPUT CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

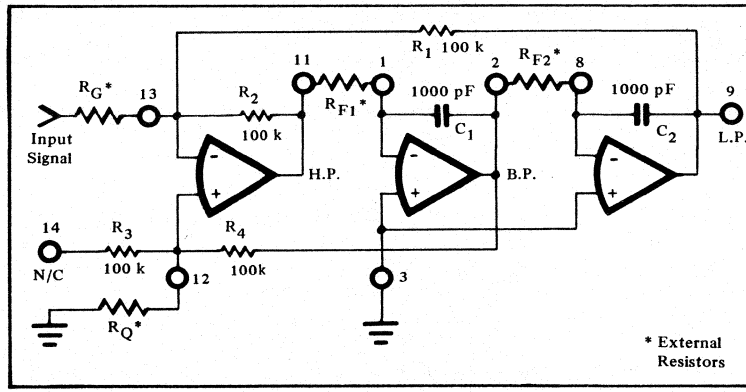
$f_o < 8$ kHz

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$
2. $A_{BP} = Q_P\,A_{LP} = Q_P\,A_{HP}$
3. $R_G = \frac{10^5\,Q_P}{A_{BP}}$
4. $R_Q = \frac{10^5}{2Q_P + A_{BP} - 1}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o \geq 8$ kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$
2. $A_{BP} = \frac{Q_P}{3.16}\,A_{LP} = 3.16\,Q_P\,A_{HP}$
3. $R_G = \frac{3.16 \times 10^4\,Q_P}{A_{BP}}$
4. $R_Q = \frac{10^5}{3.48\,Q_P + A_{BP} - 1}$



BI-QUAD CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

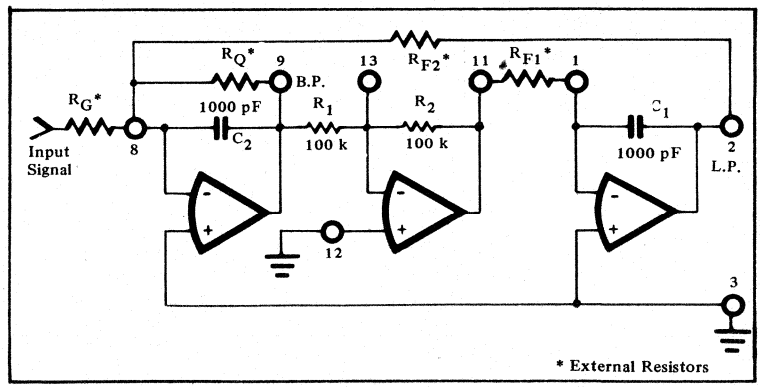
$f_o < 8$ kHz

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$
2. $A_{BP} = Q\,A_{LP}$
3. $R_Q = Q_P\,R_{F1}$
4. $R_G = \frac{R_Q}{A_{BP}}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o \geq 8$ kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$
2. $A_{BP} = 3.16\,Q\,A_{LP}$
3. $R_Q = 3.16\,Q_P\,R_{F1}$
4. $R_G = \frac{R_Q}{A_{BP}}$



FILTER

BAND REJECT

The band reject configuration is achieved by summing the high pass and low pass UAF outputs. The circuits shown in Figures 5 and 6 can be used to provide the band reject function if they are connected as shown in Figure 8. The Figure 8 circuit is applicable when using simplified design equations "A" ($A_{LP} = A_{HP}$), but when operating with an 11 kΩ resistor between pins 13 and 11 ($A_{LP} = 10\ A_{HP}$), the resistor at pin 9 must be 10 times the resistor at pin 11 to obtain equal passband gains above and below f_o.

In either case, the four external UAF resistors (R_G, R_Q, R_{F1} and R_{F2}) should be calculated for f_o and Q of the band reject filter desired and for A_{LP} to equal the desired passband gain. An input constraint: the input voltage times A_{BP} must not exceed the rated peak-to-peak output voltage of the band pass output, or clipping and distortion will result.

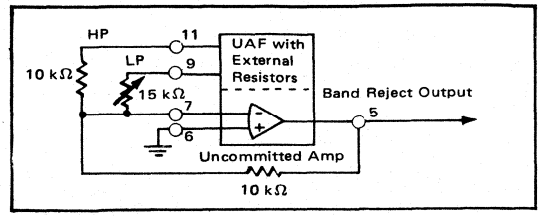


FIGURE 8. Band Reject Output

FILTER PARAMETERS

LOW PASS AND HIGH PASS

Table 1 shows filter parameters for many 2 to 8 pole low pass filters. The Q and the normalized undamped natural frequency, f_n, for each two-pole section are shown. The Q values should be used with Figure 4 and in the design formulas on page 6 and f_n must be multiplied by the desired cutoff frequency of the overall filter to obtain the required frequency, f_o, for the design formulas. As an example, consider a 4-pole low pass Bessel filter with a cutoff frequency of 1000 Hz. The first stage would be designed to an f_o of 1432.41 Hz and a Q of 0.52193 while the second stage would have an f_o of 1605.94 Hz and a Q of 0.80554. The low pass output of the first stage (pin 9) should be connected to the input resistor (R_G) of the second stage.

Filters with an odd number of poles show one f_n with no corresponding Q value. This represents the simple RC network that is required for odd pole filters. This RC network with a cutoff frequency equal to f_n times the overall filter cutoff frequency should be placed in series with the first UAF two-pole section. The uncommitted internal op amp should be used as a buffer to isolate the RC network so that the UAF input resistor will not affect the cutoff frequency of the RC network.

The cutoff frequency determined by the Table 1 filter parameters is (1) the 3 dB frequency of the Butterworth response and of the Bessel response and (2) the frequency at which the amplitude response of the Chebyschev filters passes through the maximum ripple band and enters the stop band.

To obtain high pass pole positions, the low pass to high pass transformation may be used:

$$f_n\ (\text{high pass}) = \frac{1}{f_n\ (\text{low pass})}$$

$$Q\ (\text{high pass}) = Q\ (\text{low pass})$$

The low pass to band pass transformation is much more complicated, but it can be done using the low pass to band pass conversion program (Table III).

NUMBER OF POLES	BUTTERWORTH		BESSEL		CHEBYSCHEV 0.5 dB RIPPLE		CHEBYSCHEV 2 dB RIPPLE	
	f_n	Q	f_n	Q	f_n	Q	f_n	Q
2	1.0	0.70711	1.2742	0.57735	1.23134	0.86372	0.907227	1.1286
3	1.0	----------	1.32475	----------	0.626456	----------	0.368911	----------
	1.0	1.0	1.44993	0.69104	1.068853	1.7062	0.941326	2.5516
4	1.0	0.54118	1.43241	0.52193	0.597002	0.70511	0.470711	0.9294
	1.0	1.3065	1.60594	0.80554	1.031270	2.9406	0.963678	4.59388
5	1.0	----------	1.50470	----------	0.362320	----------	0.218308	----------
	1.0	0.61805	1.55876	0.56354	0.690483	1.1778	0.627017	1.77509
	1.0	1.61812	1.75812	0.91652	1.017735	4.5450	0.97579	7.23228
6	1.0	0.51763	1.60653	0.51032	0.396229	0.68364	0.31611	0.9016
	1.0	0.70711	1.69186	0.61120	0.768121	1.8104	0.730027	2.84426
	1.0	1.93349	1.90782	1.0233	1.011446	6.5128	0.982828	10.4616
7	1.0	----------	1.68713	----------	0.256170	----------	0.155410	----------
	1.0	0.55497	1.71911	0.53235	0.503863	1.0916	0.460853	1.64642
	1.0	0.80192	1.82539	0.66083	0.822729	2.5755	0.797114	4.11507
	1.0	2.2472	2.05279	1.1263	1.008022	8.8418	0.987226	14.2802
8	1.0	0.50980	1.78143	0.50599	0.296736	0.67657	0.237699	0.89236
	1.0	0.60134	1.83514	0.55961	0.598874	1.6107	0.571925	2.5327
	1.0	0.89998	1.95645	0.71085	0.861007	3.4657	0.842486	5.58354
	1.0	2.5629	2.19237	1.2257	1.005984	11.5305	0.990142	18.6873

TABLE 1. Low Pass Filter Parameters

LOW PASS CHEBYSCHEV

Table II details a FORTRAN program to determine f_n and Q for a Chebyschev low pass filter. The only inputs required are the number of poles and the peak to peak ripple (dB) of the desired filter. The program outputs are treated exactly as the values on the pole position table (Table 1).

BAND PASS

Table III details a FORTRAN program that may be used to transform low pass pole positions into the equivalent band pass pole positions.

Program Inputs:

1. f_n—From Table I for the low pass filter of interest.
2. Q From Table I.
3. Q_{BP}—Desired Q of the band pass filter.

For filters with an odd number of poles a Q of .5 should be used where Q is not given in Table I. The program transforms each low pass pole into a band pass pole pair. That is, using the two-pole low pass pole positions would result in the pole positions for a two pole pair, band pass filter, requiring two UAF stages. Enter 10^6 for Q when transforming zeros on the imaginary axis. This program automates the transformation $s = p/2 \pm (p/2)^2 - 1$.

```
   PI=3.1415926536
   COMPLEX P(10)
   READ 5,N,R
5 FORMAT(I2,F8.6)
   A=SQRT(EXP(R/4.3429448)-1.)
   B=1./A
   AN=ALOG(B+SQRT(B**2+1.))
   AN=AN/FLOAT(N)
   J=MOD(N,2)+N/2
   DO 10 K=1,J
   RP=SINH(AN)*SIN(PI*FLOAT(2*K-1)/FLOAT(2*N))
   XIP=COSH(AN)*COS(PI*FLOAT(2*K-1)/FLOAT(2*N))
   WN=SQRT(RP**2+XIP**2)
   Q=-WN/(2.*RP)
   P(K)=CMPLX(WN,Q)
   IF(MOD(N,2).NE.0.AND.K.EQ.J) GO TO 15
   PRINT 20,P(K)
   GO TO 10
15 F=REAL(P(K))
   PRINT 30,F
10 CONTINUE
20 FORMAT(2X"FN="E20.8" Q = "E20.8)
30 FORMAT(2X"FN="E20.8)
   STOP
   END
```

```
   COMPLEX P,S,U
   READ 5, FN, Q, QBP
5  FORMAT (3F12.5)
   Y=FN*SQRT(1.-(1./(Q*2.))**2)
   X=-FN/(Q*2.)
   P=CMPLX(X,Y)
   U=CONJG(P)
   DO 30 I=1,2
   S=P/(2.*QBP)
   P=S**2-1.
   T=ATAN2(AIMAG(P),REAL(P))
   IF(T.GE.0.) GO TO 10
   T=2.*3.14159+T
10 T=T/2.
   A=SQRT(CABS(P))*COS(T)
   B=SQRT(CABS(P))*SIN(T)
   S=S+CMPLX(A,B)
   FN=CABS(S)
   Q=-FN/(2.*REAL(S))
   PRINT 20,FN,Q
20 FORMAT (2X"FN = "F12.5" Q = "F12.5)
   IF(AIMAG(U).EQ.0.) GO TO 40
30 P=U
40 STOP
   END
```

TABLE III. Low Pass to Band Pass Transformation Program

DETAILED TRANSFER FUNCTION EQUATIONS

The following equations show the action of all the internal and external UAF31 filter components. They should be used if a detailed analysis, not covered in the simplified equations, is required.

NONINVERTING INPUT CONFIGURATION

1. $\omega_o^2 = \dfrac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = \dfrac{1 + \frac{R_4 (R_G + R_Q)}{R_G R_Q}}{1 + \frac{R_2}{R_1}} \left(\dfrac{R_2}{R_1} \dfrac{R_{F1} C_1}{R_{F2} C_2}\right)^{1/2}$

3. $Q\,A_{LP} = Q\,A_{HP} \left(\dfrac{R_1}{R_2}\right) = A_{BP} \left(\dfrac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$

4. $A_{LP} = \dfrac{1 + \frac{R_1}{R_2}}{R_G\left(\frac{1}{R_G} + \frac{1}{R_Q} + \frac{1}{R_4}\right)}$

5. $A_{HP} = \dfrac{R_2}{R_1} A_{LP} = \dfrac{1 + \frac{R_2}{R_1}}{R_G\left(\frac{1}{R_G} + \frac{1}{R_Q} + \frac{1}{R_4}\right)}$

6. $A_{BP} = \dfrac{R_4}{R_G}$

INVERTING INPUT CONFIGURATION

1. $\omega_o^2 = \dfrac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = \left(1 + \dfrac{R_4}{R_Q}\right) \left(\dfrac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_G}}\right) \left(\dfrac{R_{F1} C_1}{R_1 R_2 R_{F2} C_2}\right)^{1/2}$

3. $Q\,A_{LP} = Q\,A_{HP} \left(\dfrac{R_1}{R_2}\right) = A_{BP} \left(\dfrac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$

4. $A_{LP} = \dfrac{R_1}{R_G}$

5. $A_{HP} = \dfrac{R_2}{R_1} A_{LP} = \dfrac{R_2}{R_G}$

6. $A_{BP} = \left(1 + \dfrac{R_4}{R_Q}\right) \dfrac{1}{R_G\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_G}\right)}$

BI-QUAD CONFIGURATION

1. $\omega_o^2 = \dfrac{R_2}{R_1 R_{F1} C_1 R_{F2} C_2}$

2. $Q = R_Q C_2 \omega_o$

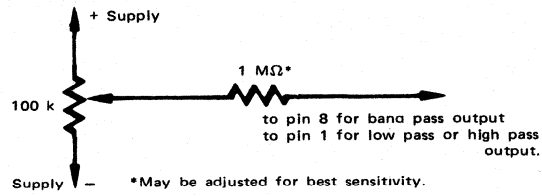
3. $A_{BP} = \dfrac{Q A_{LP}}{\omega_o R_{F2} C_2} = \dfrac{R_Q}{R_G}$

OFFSET ERROR ADJUSTMENT

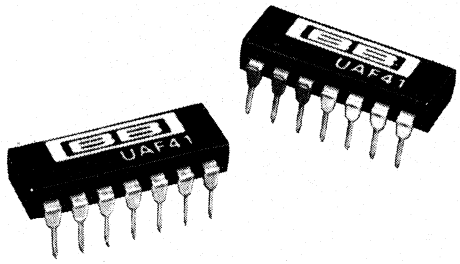
DC offset errors will be minimized by grounding pin 3 through a resistor equal to 1/2 the value of R_{F1} or R_{F2}.

The DC offset adjustment shown here may be used if required.

Offset errors will increase with increases in R_F.



BURR-BROWN



UAF41

UNIVERSAL ACTIVE FILTER

FEATURES

- LOW COST
- SMALL SIZE
  - Single wide DIP package
- FULLY CHARACTERIZED PARAMETERS
- HYBRID CONSTRUCTION
- IMPROVED PERFORMANCE
  - 1% frequency accuracy
  - Q range of 0.5 to 500
  - NPO capacitors and thin-film resistors
  - Uncommitted op amp included

BENEFITS

- SAVES PRINTED CIRCUIT BOARD SPACE
- SAVES DESIGN TIME
  - Calculate only four resistance values
  - Design directly from this data sheet
  - Versatile building block for filter design
- HIGH RELIABILITY
- HIGH STABILITY

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PDS-359

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DESCRIPTION

The UAF41 is a versatile 2-pole active filter. It uses a three operational amplifier double integrater feedback loop to generate a complex pole pair (two conjugate poles). The location of the poles in the complex plane (and thus the natural frequency and Q) are determined by external, user supplied resistors. Either 3 or 4 resistors are used depending on the particular configuration chosen.

The UAF41 produces three transfer functions simultaneously - low pass, high pass, and band pass - which are available at three separate outputs. The fourth basic transfer function - the band reject or notch - can be obtained simply by summing the high pass and low pass outputs using the uncommitted amplifier (A4) contained in the UAF41. The uncommitted op amp can also be used to add a single pole response for complex filters requiring an odd number of poles.

More complex higher order filters can readily be obtained by cascading UAF's. This is easily done with the UAF41 since the high input impedance and low output impedance associated with the operational amplifiers used prevents the series connected stages from interacting (e.g., no frequency pull due to following stage loading). This data sheet contains the design procedures for an easy selection of resistor values for the stagger tuning of cascaded stages.

The versatility of the UAF41 makes it a general purpose building block for a wide variety of active filter applications. Its universal nature, ease of use, small size and low cost allows the user the convenience of keeping units on hand for immediate use whenever a filter requirement arises.

TRANSFER FUNCTION

The UAF41 uses the state variable technique to produce a basic second order transfer function. The equations describing the three outputs available are:

$$T(\text{Low Pass}) = \frac{A_{LP}\omega_o^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{Band Pass}) = \frac{A_{BP}(\omega_o/Q)s}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{High Pass}) = \frac{A_{HP}\,s^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

To obtain band reject characteristics the low pass and high pass outputs are summed to form a pair of $j\omega$ axis zeros:

$$T(\text{Band Reject}) = \frac{A\,(s^2 + \omega_o^2)}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

where $A_{LP}=A_{HP}=A$.

The state variable approach uses two op amp integrators (A2 and A3 in the simplified schematic below) and a summing amplifier (A1) to provide simultaneous low pass, band pass and high pass responses. One UAF41 is required for each two poles of low pass or high pass filters and for each pole-pair of band pass or band reject filters.

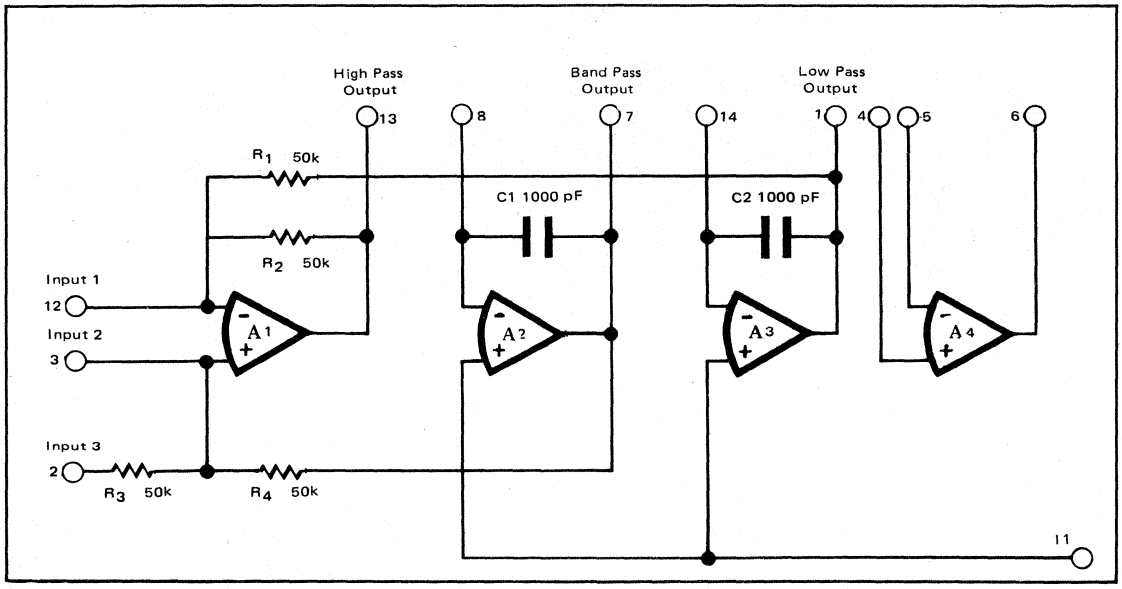


FIGURE 1. UAF41 Schematic.

SPECIFICATIONS

ELECTRICAL

Typical at 25°C and with rated supply unless otherwise noted.

MODEL	UAF41
INPUT	
Input Bias Current	±40 nA
Input Voltage Range	±10 V
Input Resistance (1)	50 kΩ
TRANSFER CHARACTERISTICS	
Frequency Range (f_o)	0.001 to 25 kHz
f_o Accuracy(2), max	±1%
f_o Stability(3)	±0.002%/°C
Q Range(4)	0.5-500
Q Stability(5)	
@f_o Q ≤ 10^4	±0.01%/°C
@f_o Q ≤ 10^5	±0.025%/°C
Q Repeatability at f_o Q ≤ 10^5	±10%
Gain Range	0.1 to 50V/V
OUTPUT	
Peak to Peak Output Swing(6)	20 V
Output Offset(7)	
(at L.P. output with unity gain)	±20 mV
Output Impedance	1 Ω
Noise(8)	200 μV (rms)
Output Current(9)	5 mA
UNCOMMITTED AMP CHARACTERISTICS	
Input Offset Voltage	5 mV
Input Bias Current	40 nA
Input Impedance	1 MΩ
Large Signal Voltage Gain	85 dB
Output Current	5 mA
POWER SUPPLIES	
Rated Power Supplies	±15 V
Power Supply Range(10)	±5 to ±18 V
Supply Current @ ±15 V(Quiescent), max	7 mA
TEMPERATURE RANGE	
Specification Temperature Range	-25 to +85°C
Storage Temperature Range	-25 to +85°C

(1) For noninverting input configuration with A_{BP} = 1.

(2) The tolerance of external frequency determining resistors must be added to this figure.

(3) T.C.R. of external frequency determining resistors must be added to this figure.

(4) See Figure 3 for Q_{max} vs F curve.

(5) Q stability varies with both the value of Q and the resonant frequency f_o.

(6) See Figure 2 for full power response curve.

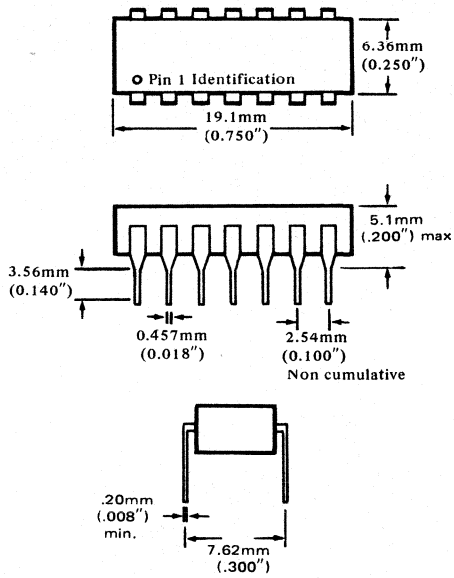
(7) $R_{F1} = R_{F2} < 100k\Omega$ at L.P. output with unity gain.

(8) Measured at the band pass output with Q @ 50 over DC to 50 kHz.

(9) The current required to drive R_{F1} and R_{F2} (external) as well as C_1 and C_2 must come from this current.

(10) For supplies below ±10V, Q_{max} will decrease slightly; filters will operate below ±5V.

MECHANICAL



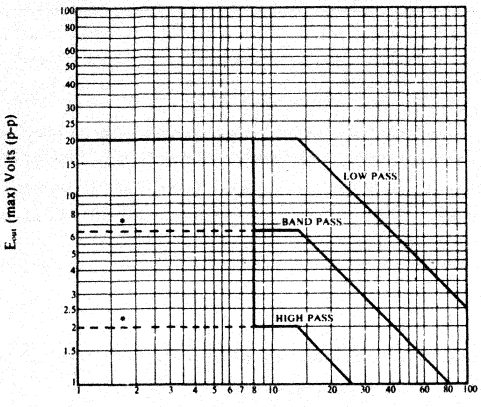
ROW SPACING - 7.63mm (0.300")
WEIGHT - 1.1gms max
CONNECTOR - 14 pin DIP connector

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

PIN CONNECTIONS

Pin 1 - Low Pass Output
Pin 2 - Filter Input 3
Pin 3 - Filter Input 2
Pin 4 - Auxiliary Amp + Input
Pin 5 - Auxiliary Amp - Input
Pin 6 - Auxiliary Amp Output
Pin 7 - Band Pass Output
Pin 8 - Frequency Adjust
Pin 9 - Negative Supply
Pin 10 - Positive Supply
Pin 11 - Common
Pin 12 - Filter Input 1
Pin 13 - High Pass Output
Pin 14 - Frequency Adjust

TYPICAL PERFORMANCE CURVES



*If Equations "B" used below 8 kHz.

FIGURE 2. Full Power Response.

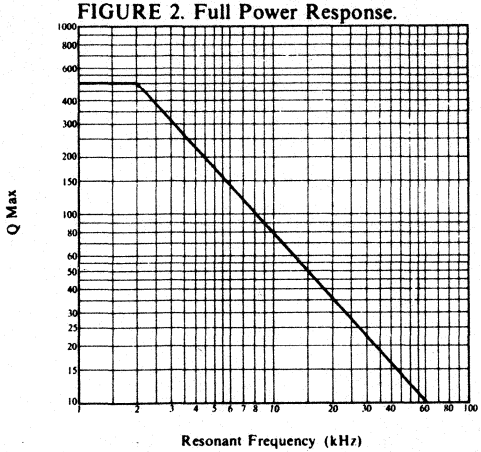


FIGURE 3. Q Max vs Resonant Frequency.

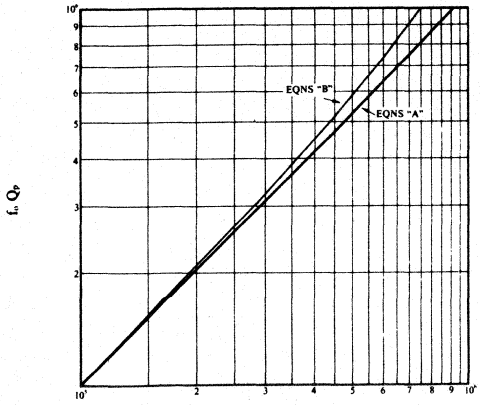


FIGURE 4. Q_p Determination

DESIGN PROCEDURE SUMMARY

This summary gives the design steps for the proper application of UAF41s and for the selection of the external components. More detailed information on filter theory pertinent to some of the steps can be found in the reference sources listed under USEFUL REFERENCES.

Burr-Brown also manufactures a line of completely self-contained active filters called the ATF76 series. These are available in most popular transfer functions with from 2 to 8 pole responses. They contain all necessary components and do not require any user design effort.

DESIGN STEPS:

1. Choose the type of transfer function (low pass, band pass, etc.), type of response (Butterworth, Bessel, etc.), number of poles, and cutoff frequency based on the particular application.

   If the transfer function is band reject see BAND REJECT TRANSFER FUNCTION, before proceeding to step 2.

2. Determine the normalized low pass filter parameters (f_n and Q) based on the type of response and number of poles selected in step 1. See NORMALIZED LOW PASS PARAMETERS.

3. If the actual response desired is low pass go to step 4. For other responses a transformation of variables must be made (low pass to band pass or low pass to high pass). See LOW PASS TRANSFORMATION.

4. Determine the actual (denormalized) cutoff frequency, f_o, by multiplying f_n by the actual desired cutoff frequency. See DENORMALIZATION OF PARAMETERS.

5. Pick the desired UAF configuration (noninverting, inverting or bi-quad) see CONFIGURATION SELECTION GUIDE, and UAF41 CONFIGURATIONS AND DESIGN EQUATIONS.

6. Decide whether to use design equations "A" or "B". See DESIGN EQUATIONS "A" AND "B".

7. Calculate R_{F1} and R_{F2}. See NATURAL FREQUENCY, and UAF CONFIGURATIONS AND DESIGN EQUATIONS.

8. Determine Q_P. See Q_P PROCEDURE.

9. Select the desired gain for each UAF and calculate the corresponding R_G and R_Q. See GAIN (A), and UAF41 CONFIGURATIONS AND DESIGN EQUATIONS.

NORMALIZED LOW PASS PARAMETERS

Usual active filter design procedure involves using normalized low pass parameters. Table I is provided to assist in this step for the more common filter responses. Table II is a FORTRAN program which allows f_n and Q to be calculated for any desired ripple and number of poles for the Chebyschev response. Consult the USEFUL REFERENCES for other information.

Note that for band pass and high pass filters complex conjugate pole pairs in the actual filter correspond to single poles in the normalized low pass model. Thus four poles in Table I would correspond to four pole pairs in a band pass or high pass filter.

Filters with an odd number of poles show one f_n with no corresponding Q value. This represents a simple RC network that is required for odd pole filters. This RC network with a cutoff frequency equal to f_n times the overall filter cutoff frequency should be placed in series with the first UAF two-pole section. The uncommitted internal op amp with an external RC network can be used for this purpose.

The cutoff frequency determined by the Table I filter parameters is (1) the -3dB frequency of the Butterworth response and of the Bessel response and (2) the frequency at which the amplitude response of the Chebyschev filters passes through the maximum ripple band (to enter the stop band).

NUMBER OF POLES	BUTTERWORTH		BESSEL		CHEBYSCHEV 0.5dB RIPPLE		CHEBYSCHEV 2dB RIPPLE	
	fn(1)	Q	fn(1)	Q	fn(2)	Q	fn(2)	Q
2	1.0	0.70711	1.2742	0.57735	1.23134	0.86372	0.907227	1.1286
3	1.0	- - - -	1.32475	- - - -	0.626456	- - - -	0.368911	- - - -
	1.0	1.0	1.44993	0.69104	1.068853	1.7062	0.941326	2.5516
4	1.0	0.54118	1.43241	0.52193	0.597002	0.70511	0.470711	0.9294
	1.0	1.3065	1.60594	0.80554	1.031270	2.9406	0.963678	4.59388
5	1.0	- - - -	1.50470	- - - -	0.362320	- - - -	0.218308	- - - -
	1.0	0.61805	1.55876	0.56354	0.690483	1.1778	0.627017	1.77509
	1.0	1.61812	1.75812	0.91652	1.017735	4.5450	0.97579	7.23228
6	1.0	0.51763	1.60653	0.51032	0.396229	0.68364	0.31611	0.9016
	1.0	0.70711	1.69186	0.61120	0.768121	1.8104	0.730027	2.84426
	1.0	1.93349	1.90782	1.0233	1.011446	6.5128	0.982828	10.4616
7	1.0	- - - -	1.68713	- - - -	0.256170	- - - -	0.155410	- - - -
	1.0	0.55497	1.71911	0.53235	0.503863	1.0916	0.460853	1.64642
	1.0	0.80192	1.82539	0.66083	0.822729	2.5755	0.797114	4.11507
	1.0	2.2472	2.05279	1.1263	1.008022	8.8418	0.987226	14.2802
8	1.0	0.50980	1.78143	0.50599	0.296736	0.67657	0.237699	0.89236
	1.0	0.60134	1.83514	0.55961	0.598874	1.6107	0.571925	2.5327
	1.0	0.89998	1.95645	0.71085	0.861007	3.4657	0.842486	5.58354
	1.0	2.5629	2.19237	1.2257	1.005984	11.5305	0.990142	18.6873

(1) -3 dB Frequency
(2) Frequency at which amplitude response passes through the ripple band.

TABLE I. Low Pass Filter Parameters.

NORMALIZED LOW PASS CHEBYSCHEV

Table II gives a FORTRAN program for the determination of f_n and Q for a general normalized Chebyschev low pass filter of any ripple and number of poles. Program inputs are the number of poles (N) and the peak-to-peak ripple (R). Program outputs are f_n and Q, which are used exactly as the values taken from Table I.

```
      PI=3.1415926536
      COMPLEX P(10)
      READ 5, N,R
    5 FORMAT (12, F8, 6)
      A=SQRT (EXP(R/4.3429448)-1)
      B=1./A
      AN=ALOG(B+SQRT(B**2+1.))
      AN=AN/FLOAT(N)
      J=MOD(N,2)+N/2
      DO 10 K=1, J
      RP=SINH(AN)*SIN(PI*FLOAT(2*K-1)/FLOAT(2*N))
      XIP=COSH(AN)*COS(PI*FLOAT(2*K-1)/FLOAT(2*N))
      WN=SQRT(RP**2+XIP**2)
      Q=-WN/(2.*RP)
      P(K)=CMPLX(WN,Q)
      IF(MOD(N,2).NE.0 AND.K.E Q.J)GO TO 15
      PRINT 20, P(K)
      GO TO 10
   15 F=REAL(P(K))
      PRINT 30, F
   10 CONTINUE
   20 FORMAT(2X"FN="E20.8"Q="E20.8)
   30 FORMAT(2X"FN="E20.8)
      STOP
      END
```

TABLE II. Low Pass Chebyschev Program

BAND REJECT TRANSFER FUNCTION

The band reject is achieved by summing the high pass and low pass UAF outputs. Either of the configurations in Figures 6 and 7 can be used to provide the band reject function if they are used as shown in Figure 5.

The 15kΩ resistor is adjusted for maximum rejection. The circuit in Figure 5 is applicable when using design equations "A" ($A_{LP} = A_{HP}$). When design equations "B" are used ($A_{LP} = 10A_{HP}$), the resistor at pin 1 must be 10 times the resistor at pin 13 to obtain equal pass band gains above and below f_n.

In either case, the four external UAF resistors (R_G, R_Q, R_{F1} and R_{F2}) should be calculated for f_o and Q of the band reject filter desired and for A_{LP} to equal the desired passband gain. An input constraint is that the input voltage times A_{BP} must not exceed the rated peak-to-peak voltage of the band pass output, or clipping will result.

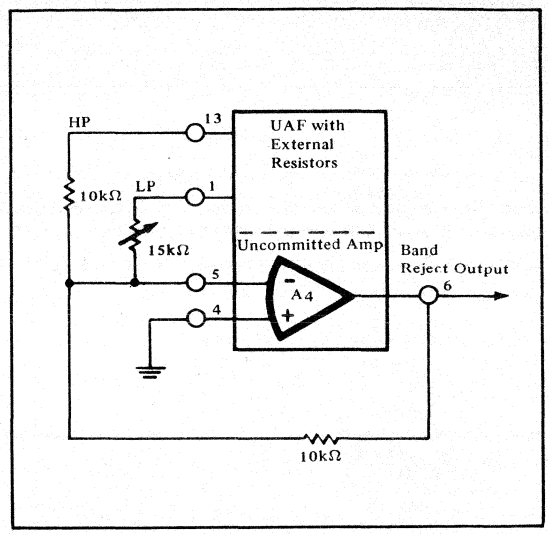


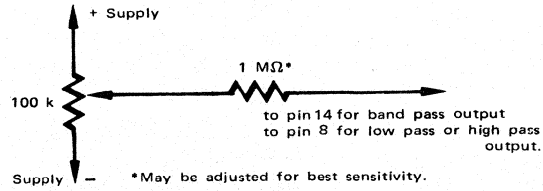
FIGURE 5. Band Reject Configuration.

OFFSET ERROR ADJUSTMENT

DC offset errors will be minimized by grounding pin 3 through a resistor equal to 1/2 the value of R_{F1} or R_{F2}.

The DC offset adjustment shown here may be used if required.

Offset errors will increase with increases in R_F.



LOW PASS TRANSFORMATION

LOW PASS TO HIGH PASS

The following simple transformation may be used for high pass filters:

$$f_n \text{ (high pass)} = \frac{1}{f_n \text{ (low pass)}}$$

$$Q \text{ (high pass)} = Q \text{ (low pass)}$$

LOW PASS TO BAND PASS

The low pass to band pass transformation to generate f_n (band pass) and Q (band pass) is much more complicated. It is tedious to do by hand but can be accomplished with the FORTRAN program given in Table III. This program automates the transformation

$s = p/2 \pm \sqrt{(p/2)^2 - 1}$.

```
      COMPLEX P,S,U
      READ 5, FN, Q, QBP
    5 FORMAT (3F12.5)
      Y=FN*SQRT(1.-(1./(Q*2.))**2)
      X=-FN/(Q*2)
      P=CMPLX(X,Y)
      U=CONJG(P)
      DO 30 I=1,2
      S=P/(2.*QBP)
      P=S**2-1.
      T=ATAN2(AIMAG(P),REAL(P))
      IF(T.GE.0) GO TO 10
      T=2.*3.14159+T
   10 T=T/2
      A=SQRT(CABS(P))*COS(T)
      B=SQRT(CABS(P))*SIN(T)
      S=S+CMPLX(A,B)
      FN=CABS(S)
      Q=-FN/(2.*REAL(S))
      PRINT 20, FN,Q
   20 FORMAT (2X"FN = "F12.5" Q = "F12.5)
      IF(AIMAG(U).EQ.0) GO TO 40
   30 P=U
   40 STOP
      END
```

TABLE III. Low Pass to Band Pass Transformation Program

PROGRAM INPUTS:

1. f_n - From Table I for the low pass filter of interest
2. Q - From Table I
3. Q_{BP} - Desired Q of the band pass filter

For filters with an odd number of poles a Q of 0.5 should be used where Q is not given in Table I. Enter 10^5 for Q when transforming zeros on the imaginary axis.

The program transforms each low pass pole into a band pass pole pair. Thus a three-pole low pass input, would result in the pole positions for a three pole pair band pass filter requiring three UAF stages.

DENORMALIZATION OF PARAMETERS

Table I shows filter parameters for many 2 to 8 pole normalized low pass filters. The Q and the normalized undamped natural frequency, f_n for each two-pole section are shown. The Q values do not have to be denormalized and may be used directly as described in the DESIGN PROCEDURE SUMMARY. f_n must be denormalized by multiplying it by the desired cutoff frequency of the actual overall filter to obtain the required frequency, f_o for the design formulas. As an example, consider a 4-pole low pass Bessel filter with a cutoff frequency of 1000 Hz. The first stage would be designed to an f_o of 1432.41 Hz and a Q of 0.52193 while the second stage would have an f_o of 1605.94 Hz and a Q of 0.80554. To combine the two stages into the composite filter the low pass output of the first stage (pin 1) would be connected to the input resistors (R_G) of the second stage.

DESIGN EQUATIONS "A" AND "B"

1. For f_o below 8 kHz, either of equations "A" or "B" may be used.

2. For f_o above 8 kHz, equations "B" must be used. If equations "A" were used above 8 kHz, the filter could become unstable.

3. Equations "A" are for the UAF as it is supplied. When using equations "B", a 5.49kΩ resistor must be placed in parallel with R_2 (between pins 12 and 13).

4. The values of R_{F1} and R_{F2} calculated with equations "B" are approximately one-third of those calculated with equations "A". Thus there may be an advantage in using equation "B" at low frequencies. Using equation "B" would require use of one more resistor, but that would not alter or affect filter performance in any manner.

5. Using the negative gain values for A_{LP} or A_{HP} or A_{BP} could result in the negative values for resistors R_G and R_Q. So the absolute value of the gain should always be used in the equations.

GAIN (A)

1. The gain (V/V) of each filter section is:
   A_{LP} - for low pass output - gain at DC
   A_{BP} - for band pass output - gain at f_o
   A_{HP} - for high pass output - gain at high frequencies.
2. Refer to Figure 2 for full power response. When selecting the gain, insure that the limits of the curve are not exceeded for the desired voltage range.

NATURAL FREQUENCY (f_o)

1. f_o for each one pole-pair band pass filter is the center frequency (f_C). f_C is defined as $f_C = \sqrt{f_1 f_2}$ where f_1 is the lower -3 dB point and f_2 is the upper -3 dB point of the pole pair response.
2. To obtain f_o below 100 Hz using practical resistor values, capacitors may be paralleled with C_1 and C_2 to reduce the size of R_{F1} and R_{F2}. If capacitors are added in parallel,

$$R_{F1}\ (\text{new}) = R_{F2}\ (\text{new}) = R_{F1}\ (\text{old})\ \frac{1000\ \text{pF}}{C + 1000\ \text{pF}}$$

where R_F (new) is the new lower value frequency resistor, C is the value of the two external capacitors placed across C_1 and C_2 (between pins 7 and 8 and pins 1 and 14 and R_{F1} (old) is the value calculated in the simplified design equations.

Q-FACTOR

1. For band pass filters $Q = \frac{f_o}{3\text{ dB bandwidth}}$

2. When designing low pass filters of more than two poles, best results will be obtained if the two pole sections with lower Q are followed by the sections with higher Q. This will eliminate any possibility of clipping due to high gain ripple in high Q sections.

3. Q repeatability (Q change from unit-to-unit) is typically ±5% for f_oQ products less than 10^4. The Q repeatability error increases as the f_oQ product increases to approximately ±10% for f_oQ products near 10^5.

Q_P PROCEDURE

1. If the "f_o times Q" product is greater than 10^5, it is possible for the measured filter Q to be different from the calculated value of Q . This effect is the result of non-ideal characteristics of operational amplifiers. It can be compensated for by introducing the parameter Qp into the design equations.

2. Calculate the f_oQ product for the filter. If the product is above 10^5 Hz, locate the corresponding f_oQ_P product in Figure 4. Divide f_oQ_P by f_o to obtain Q_P. Use Q_P as indicated in the design equations. For f_oQ products below 10^5 Hz, $Q_P = Q$.

CONFIGURATION SELECTION GUIDE

It is possible to configure the UAF41 three different ways. Each configuration produces features that may or may not be desirable for a specific application. This selection guide is given to assist in determining the most advantageous configuration for a particular application.

	NONINVERTING INPUT	INVERTING INPUT	BI QUAD
Outputs Available	BP, LP and HP	BP, LP and HP	BP and LP
Outputs Inverted with respect to the Input	BP	HP and LP	BP and LP
Q & Gain Independent of Frequency Resistors?	Yes	Yes	No
Type of Q Variation With Changes in R_F	Constant Q	Constant Q	Constant Bandwidth
Other Advantages	May eliminate one external resistor (use internal R_3 as R_G)		R_G and R_Q are small at high frequencies
Parameter Limitations	$2Q_p - A_{BP} > 1$ (Eqns. "A") $3.48Q_p - A_{BP} > 1$ (Eqns. "B")	$2Q_p + A_{BP} > 1$ (Eqns. "A") $3.48Q_p + A_{BP} > 1$ (Eqns. "B")	No HP Output
Summary: The Bi-Quad filter is particularly useful as a band pass filter if the filter bandwidth must be kept constant as the center frequency is varied. If Q must be kept constant (i.e., constant Q of a band pass or maintaining a constant response of a low pass or high pass) one of the other two configurations should be used. The Bi-Quad also has the advantage that R_G and R_Q are smaller than with the other two configurations (this is especially useful at high frequencies). The noninverting input configuration has the advantage that for $A_{BP} = 1$, $R_G = 50k\Omega$; therefore R_3 (internal) may be used so that only three external resistors are needed (R_{F1}, R_{F2}, R_Q).			

UAF41 CONFIGURATIONS AND DESIGN EQUATIONS

NONINVERTING INPUT CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$

2. $A_{BP} = Q\,A_{LP} = Q\,A_{HP}$

3. $R_G = \frac{5.0 \times 10^4\,Q}{A_{BP}\,Q_P}$

4. $R_Q = \frac{5.0 \times 10^4}{2Q_P - \frac{A_{BP}\,Q_P}{Q} - 1}$

SIMPLIFIED DESIGN EQUATIONS "B" †

Must be used for $f_o \geq 8$ kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$

2. $A_{BP} = \frac{Q}{3.16}\,A_{LP} = 3.16\,Q\,A_{HP}$

3. $R_G = \frac{5.0 \times 10^4\,Q}{A_{BP}\,Q_P}$

4. $R_Q = \frac{5.0 \times 10^4}{3.48Q_p - \frac{A_{BP}\,Q_p}{Q} - 1}$

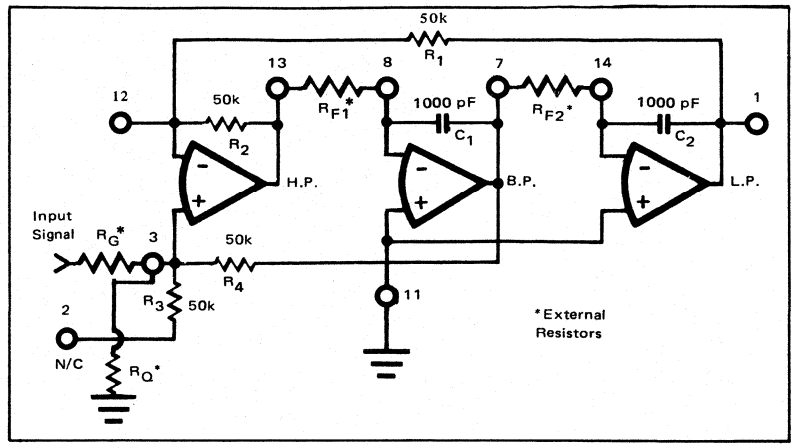


FIGURE 6. Noninverting Input Configuration.

INVERTING INPUT CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$

2. $A_{BP} = Q_P\,A_{LP} = Q_P\,A_{HP}$

3. $R_G = \frac{5.0 \times 10^4\,Q_P}{A_{BP}}$

4. $R_Q = \frac{5.0 \times 10^4}{2Q_P + A_{BP} - 1}$

SIMPLIFIED DESIGN EQUATIONS "B" †

Must be used for $f_o \geq 8$ kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$

2. $A_{BP} = \frac{Q_P}{3.16}\,A_{LP} = 3.16\,Q_P\,A_{HP}$

3. $R_G = \frac{1.58 \times 10^4\,Q_P}{A_{BP}}$

4. $R_Q = \frac{5.0 \times 10^4}{3.48\,Q_P + A_{BP} - 1}$

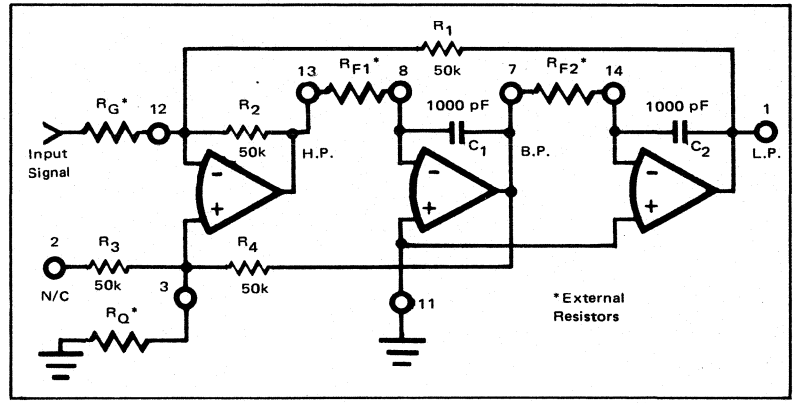


FIGURE 7. Inverting Input Configuration.

BI-QUAD CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$

2. $A_{BP} = Q\,A_{LP}$

3. $R_Q = Q_P\,R_{F1}$

4. $R_G = \frac{R_Q}{A_{BP}}$

SIMPLIFIED DESIGN EQUATIONS "B" †

Must be used for $f_o \geq 8$ kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$

2. $A_{BP} = 3.16\,Q\,A_{LP}$

3. $R_Q = 3.16\,Q_P\,R_{F1}$

4. $R_G = \frac{R_Q}{A_{BP}}$

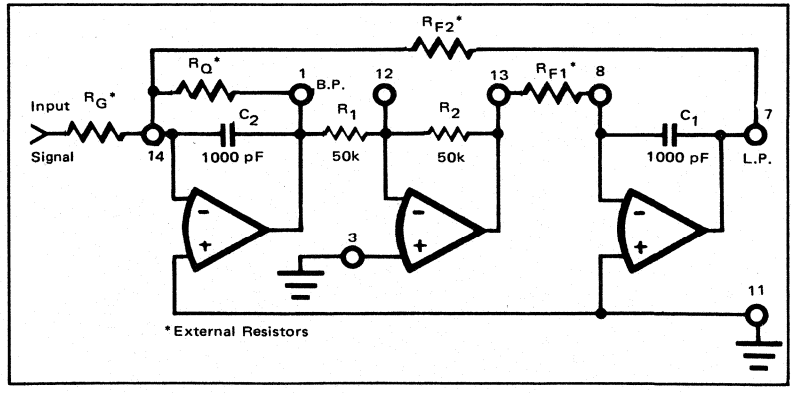


FIGURE 8. Bi-Quad Configuration.

† To use equations "B" connect a 5.49k resistor between pins 12 and 13.
Equations "B" are also valid for frequencies below 8kHz.

DETAILED TRANSFER FUNCTION EQUATIONS

The following equations show the action of all the internal and external UAF41 filter components. They are not required for regular design procedure, but could be used if a detailed analysis is required.

NONINVERTING INPUT CONFIGURATION

1. $\omega_o^2 = \dfrac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = \dfrac{1 + \dfrac{R_4 (R_G + R_Q)}{R_G R_Q}}{1 + \dfrac{R_2}{R_1}} \left(\dfrac{R_2 R_{F1} C_1}{R_1 R_{F2} C_2}\right)^{1/2}$

3. $Q A_{LP} = Q A_{HP} \left(\dfrac{R_1}{R_2}\right) = A_{BP} \left(\dfrac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$

4. $A_{LP} = \dfrac{1 + \dfrac{R_1}{R_2}}{R_G \left(\dfrac{1}{R_G} + \dfrac{1}{R_Q} + \dfrac{1}{R_4}\right)}$

5. $A_{HP} = \dfrac{R_2}{R_1} A_{LP} = \dfrac{1 + \dfrac{R_2}{R_1}}{R_G \left(\dfrac{1}{R_G} + \dfrac{1}{R_Q} + \dfrac{1}{R_4}\right)}$

6. $A_{BP} = \dfrac{R_4}{R_G}$

INVERTING INPUT CONFIGURATION

1. $\omega_o^2 = \dfrac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = \left(1 + \dfrac{R_4}{R_Q}\right) \dfrac{1}{\left(\dfrac{1}{R_1} + \dfrac{1}{R_2} + \dfrac{1}{R_G}\right)} \left(\dfrac{R_{F1} C_1}{R_1 R_2 R_{F2} C_2}\right)^{1/2}$

3. $Q A_{LP} = Q A_{HP} \left(\dfrac{R_1}{R_2}\right) = A_{BP} \left(\dfrac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$

4. $A_{LP} = \dfrac{R_1}{R_G}$

5. $A_{HP} = \dfrac{R_2}{R_1} \quad A_{LP} = \dfrac{R_2}{R_G}$

6. $A_{BP} = \left(1 + \dfrac{R_4}{R_Q}\right) \dfrac{1}{R_G \left(\dfrac{1}{R_1} + \dfrac{1}{R_2} + \dfrac{1}{R_G}\right)}$

BI-QUAD CONFIGURATION

1. $\omega_o^2 = \dfrac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = R_Q C_2 \omega_o$

3. $A_{BP} = \dfrac{Q A_{LP}}{\omega_o R_{F2} C_2} = \dfrac{R_Q}{}$

ACTIVE FILTER DESIGN EXAMPLES USING THE DESIGN PROCEDURE OUTLINED IN DESIGN STEPS SECTION.

Example 1.

It is desired to design a 3 pole, 0.5dB ripple, Chebyschev High Pass Filter; the cut off frequency $f_c = 2$ kHz, Gain $A_{HP} = +1$.

Step 1.

The type of transfer function (high pass), the type of response (Chebyschev), number of poles (3), and the cut off frequency (f_c) are chosen depending upon the particular application and are stated in the example.

Step 2.

Normalized low pass filter parameters f_n and Q are obtained from Table I (or from program shown in Table II).

Complex Poles:

$f_n = 1.068853$
$Q = 1.7062$

Simple Pole:

$f_n = 0.626456$

Step 3.

Now, since the actual response desired is high pass,the low pass to high pass transformation must be made as shown in LOW PASS TRANSFORMATION.

$$f_n \text{ (high pass)} = \frac{1}{f_n \text{ (low pass)}}, \quad Q_{HP} = Q_{LP}$$

$\therefore$ For Complex Poles:

$$f_n = \frac{1}{1.068853} = 0.935582$$

and Q = 1.7062

For Simple Pole: $f_n = \dfrac{1}{0.626456} = 1.596281$

Step 4.

Now, determine the actual (denormalized) frequency.

$f_o = f_c \times f_n = 2$ kHz x 0.935582

= 1871.2 Hz

Step 5.

Refer to the CONFIGURATION SELECTION GUIDE. Since the gain required is positive, the HP output is not inverted with respect to the input. Therefore, the noninverting input configuration must be selected. Note that the HP output is not available with the Bi-Quad configuration.

Step 6.

Since $f_o < 8$ kHz, Equations "A" would be used.

Step 7.

For the Complex Poles Stage of the filter, using the equations "A",

$$R_{F1} = R_{F2} = \frac{1.592 \times 10^8}{1871.2} = 85.08\ k\Omega$$

Step 8.

$f_o\ Q = 1871.2 \times 1.7062 = 3.19 \times 10^3$

$\therefore f_o\ Q < 10^5$

$\therefore Q_P = Q = 1.7062$

Step 9.

$A_{BP} = Q_P \times A_{HP} = 1.7062 \times 1 = 1.7062$

$$R_G = \frac{5.0 \times 10^4 \times 1.7062}{1.7062 \times 1.7062} = 29.3\ k\Omega$$

$$R_Q = \frac{5.0 \times 10^4}{2 \times 1.7062 - 1.7062 - 1} = 70.8 k\Omega$$

The above obtained resistor values are for the complex pole pair of the first stage of the required active filter. The simple pole obtained as outlined below, using the uncommitted op amp in the UAF41 makes the second stage of the required filter.

For the simple pole f_n was obtained in the step 3.

$f_n = 1.596281$

The actual (denormalized) frequency = $f_c \times f_n$

$= 2\ kHz \times 1.596281 = 3192.6\ Hz$

$$\text{Now, } f = \frac{1}{2\pi RC}$$

$$\therefore RC = \frac{1}{2\pi f} = \frac{1}{2\pi \times 3192.6} = 4.9851 \times 10^{-5}$$

Choosing C = 2200 pF (or any convenient value),

$$R = \frac{4.9851 \times 10^{-5}}{2200 \times 10^{-12}} = 22.66\ k\Omega$$

Note:

R and/or C may be chosen in any convenient manner to obtain the desired RC product.

The overall circuit for the requried filter is shown below:

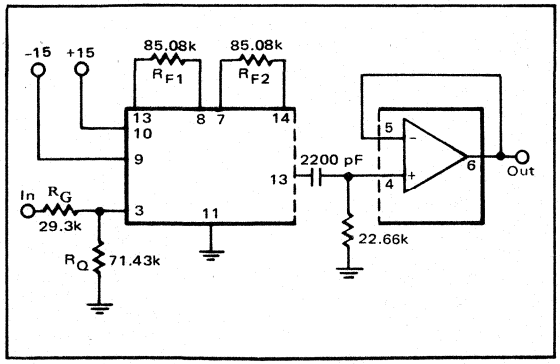


FIGURE 9. Overall Circuit - Example 1.

Example 2.

It is desired to design a 4 pole Butterworth, Band Pass Filter, with Q = 25, f_c = 19 kHz and A_{BP} = 1.

Using the computer program shown in Table III, the following values of f_n and Q are obtained.

$f_n = 1.0142435$, $Q = 35.36541$

and $f_n = 0.9859565$, $Q = 35.35886$

Using the above shown values of Q and f_n, we now will proceed to design the two stages of filter separately.

Any one of the three configurations shown in the CONFIGURATION SELECTION GUIDE can be used. We will select the noninverting input configuration.

For Stage 1

$f_o = 19\ kHz \times f_n = 19\ kHz \times 1.0142435$

$= 19270.6\ Hz$

Since $f_o > 8$ kHz, equations "B" would be used.

$$R_{F1} = R_{F2} = \frac{5.033 \times 10^7}{19270.6} = 2.6118\ k\Omega$$

$f_oQ = 19270.6 \times 35.36541 = 6.815136 \times 10^5$

Since $f_oQ > 10^5$, locate the corresponding f_oQ_p from Figure 4.

Divide f_oQ_p by f_o to obtain Q_p.

Thus $Q_p = 48.78$

$$R_G = \frac{5.0 \times 10^4 \times 35.36541}{1 \times 48.78} = 36.25 k\Omega$$

$$R_Q = \frac{5.0 \times 10^4}{3.48 \times 48.78 - \frac{48.78}{35.37} - 1} = 298.7\Omega$$

For Stage 2.

Following the same procedure as shown for Stage 1 above, the values shown below are obtained.

$f_o\ Q = 6.624 \times 10^5$, Using Figure 4, $Q_P = 48.04$

$R_{F1} = R_{F2} = 2.6867\ k\Omega$

$R_G = 36.8\ k\Omega$

and $R_Q = 303.4\ \Omega$

The overall circuit for the required filter is shown below.

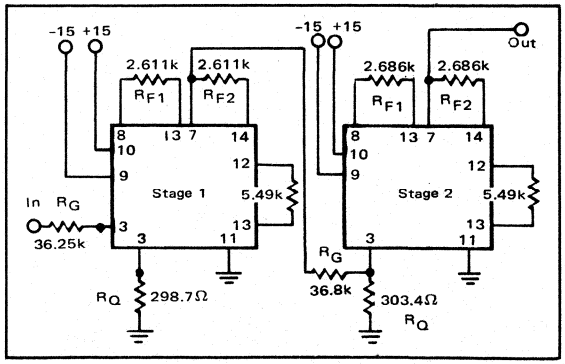


FIGURE 10. Overall Circuit - Example 2.

Example 3.

It is desired to design a 5 pole Bessel, Low Pass Filter with $f_c = 3.3$ kHz and $A_{LP} = 1$.

From Table I, the following values of f_o and Q are obtained.

Complex Poles:

$f_n = 1.55876$
$Q = 0.56354$

$f_n = 1.75812$
$Q = 0.91652$

Simple Pole:

$f_n = 1.50470$

Using the above shown values of f_n and Q, we now will proceed to design the three stages of filter separately.

Any one of the three configurations can be used. We will select inverting configuration.

For Stage 1.

$f_o = 3.3$ kHz x $f_n = 3.3$ kHz x $1.55876 = 5144$ Hz

Since $f_o < 8$ kHz, equations "A" would be used.

$$R_{F1} = R_{F2} = \frac{1.592 \times 10^8}{5144} = 30.95\ k\Omega$$

$f_o Q = 5144 \times 0.56354 = 2.9 \times 10^3$

$f_o Q < 10^5, \therefore Q_P = Q = 0.56354$

$A_{BP} = Q_P A_{LP} = 0.56354 \times 1 = 0.56354$

$$R_G = \frac{5 \times 10^4 \times 0.56354}{0.56354} = 50\ k\Omega$$

$$R_Q = \frac{5 \times 10^4}{2 \times 0.56354 + 0.56354 - 1} = 72.4\ k\Omega$$

For Stage 2.

$f_o = 3.3$ kHz x $f_n = 3.3$ kHz x $1.75812 = 5802$ Hz

Since $f_o < 8$ kHz, equations "A" would be used.

$$R_{F1} = R_{F2} = \frac{1.592 \times 10^8}{5802} = 27.44\ k\Omega$$

$f_o Q = 5802 \times 0.91652 = 5.32 \times 10^3$

$f_o Q < 10^5, \therefore Q_P = Q = 0.91652$

$A_{BP} = Q_P A_{LP} = 0.91652 \times 1 = 0.91652$

$$R_G = \frac{5 \times 10^4 \times 0.91652}{0.91652} = 50\ k\Omega$$

$$R_Q = \frac{5 \times 10^4}{2 \times 0.91652 + 0.91652 - 1} = 28.58\ k\Omega$$

For Stage 3.

$f = 3.3$ kHz x $f_n = 3.3$ kHz x $1.50470 = 4966$ Hz

For the simple pole,

$$RC = \frac{1}{2\pi f} = \frac{1}{2\pi \times 4966} = 3.2049 \times 10^{-5}$$

3300 pF (or any convenient value)

$$R = \frac{3.2049 \times 10^{-5}}{3300 \times 10^{-12}} = 9.71\ k\Omega$$

The overall circuit is shown below.

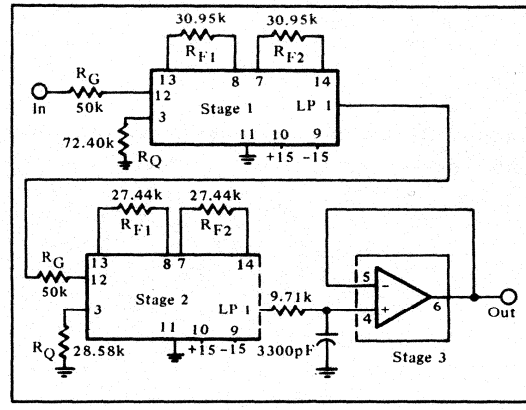
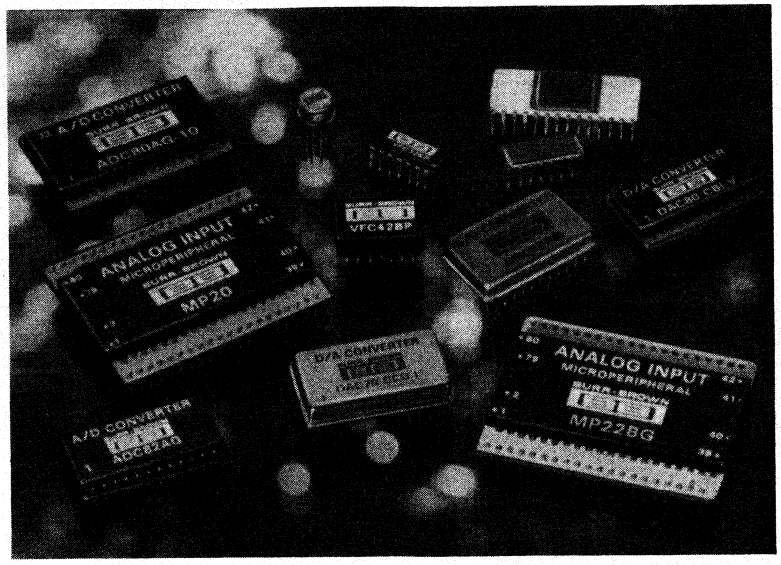


FIGURE 11. Overall Circuit - Example 3.

USEFUL REFERENCES

1. G.E. Tobey, J.G. Graeme and L.P. Huelsman, Operational Amplifiers: Design and Applications, (Chapter 8) McGraw Hill Book Co., 1971.
2. Yu Jen Wong, William E. Ott, Function Circuits: Design and Applications, (Chapter 6) McGraw Hill Book Co., 1976.
3. Richard W. Daniels, Approximation Methods for Electronic Filter Design, McGraw Hill Book Co., 1974.
4. Anatol I. Zverev, Handbook of Filter Synthesis, John Wiley and Sons Inc., New York, N.Y., 1967.
5. Gabor C. Temes, Sanjit K. Mitra, Modern Filter Theory and Design, John Wiley and Sons, New York, N.Y., 1973.

5. DATA CONVERSION AND ACQUISITION



The Burr-Brown data conversion and acquisition product line includes components necessary to multiplex and convert signals from analog to digital form and digital to analog form. These components are produced in four product types: digital-to-analog converters, analog-to-digital converters, sample/hold circuits, and multiplexers.

These products were designed to make their applications easy. Most units are complete, requiring no external components. All D/A converters include an internal reference and most have an output voltage amplifier. A/D converters come with internal clock, reference, and comparator. Many sample/hold circuits have an internal holding capacitor. The multiplexers contain input protection circuitry to prevent damage from input overvoltages.

If your system requires data acquisition and conversion, you will want to consider one of our predesigned System Data Modules (SDM). Each contains a multiplexer, instrumentation amplifier, sample/hold circuit, A/D converter, and timing and control logic. The microperipheral components are SDM's that have address decoding and specialized control logic making them compatible with most of the available microprocessors. These subsystems, tested at the factory, have a proven record of reliability.

Burr-Brown data acquisition components - quality and reliability at low cost.

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SELECTION GUIDE
Data Conversion and Acquisition

A/D CONVERTERS

Description	Model	Resolution (Bits)	Linearity, max (% of FSR)	Conversion Time, max (μsec)	Tempco Bipolar, max (ppm FSR/°C)	Input Range (V)	Power Supply Req.(V/mA)	Package		Page
Very-High Speed	ADC60-08	8	±0.195	0.88	±20	±2.5, ±5	±15/±50	Module		5-6
	ADC60-10	10	±0.0488	1.88	±20	±10, +5	+5/270	Module		5-6
	ADC60-12	12	±0.0244	3.50	±15	+10, +20		Module		5-6
Low Cost	ADC80AG-10[1]	10	±0.048	21	±23	±2.5, ±5,	±15/20	DIP		5-12
	ADC80AG-12[1]	12	±0.012	25	±23	±10, +5	+5/70	DIP		5-12
	ADC80AGZ-10[1]	10	±0.048	21	±23	+10	±12/20	DIP		5-12
	ADC80AGZ-12[1]	12	±0.012	25	±23		+5/70	DIP		5-12
Low Cost, High Speed	ADC82AG[1]	8	±0.2	2.8	±75	±2.5, ±5, ±10	±15/20	DIP		5-20
	ADC82AM[1]	8	±0.2	2.8	±75	+5, +10, +20	+5/80	DIP		5-20
	ADC84KG-10	10	±0.048	6	±23	±2.5, ±5	+15/45	DIP		5-28
	ADC84KG-12	12	±0.012	10	±23	±10, +5, +10	-15/-35,+5/70	DIP		5-28
Low Drift, High Speed	ADC85C-10	10	±0.048	6	±53	±2.5, ±5	±15/45	DIP		5-28
	ADC85-10[1]	10	±0.048	6	±28	±10, +5	-15/-35	DIP		5-28
	ADC85C-12	12	±0.012	10	±30	+10	+5/120	DIP		5-28
	ADC85-12[1]	12	±0.012	10	±19			DIP		5-28
High Resolution	ADC100-BCD	4 digits	±0.005	30msec	±10	±10	+15/25	Module		5-36
	ADC100-SMD	4 digit + sign	±0.005	30msec	±5	±10	-15/20	Module		5-36
	ADC100-USB	14 or 16	±0.005	(14)-50msec	±10	+10	+5/300	Module		5-36
	ADC100-BOB	14 or 16	±0.005	(16)-200msec	±10	±10		Module		5-36

D/A CONVERTERS

Description	Model	Resolution (Bits)	Linearity max (% of FSR)	Tempco max (ppm of FSR/°C)	Output Ranges	Settling Time (FSR, ±1/2LSB)	Power Supply Req.(V/mA)	Package		Page
Very-High Speed	DAC60-10	10	±0.048	±15[2]	0 to -5mA	40nsec	+15/45	DIP		5-44
	DAC60-12	12	±0.012	±15[2]	±2.5mA	150nsec	-15/-35	DIP		5-44
High Resolution	DAC70-CSB-I[1]	16	±0.003	±9	0 to -2mA	50μsec	±15/25	DIP		5-49
	DAC70-COB-I[1]	16	±0.003	±9	±1mA	50μsec	+5/25	DIP		5-49
	DAC70C-CSB-I	16	±0.005	±21	0 to -2mA	50μsec		DIP		5-49
	DAC70C-COB-I	16	±0.005	±21	±1mA	50μsec		DIP		5-49
	DAC70-CCD-I[1]	4 digits	±0.003	±9	0 to -2mA	50μsec		DIP		5-49
	DAC70C-CCD-I	4 digits	±0.005	±21	0 to -2mA	50μsec		DIP		5-49
Low Cost	DAC80-CBI-I	12	±0.012	±25	±1, 0 to -2mA	300nsec	±15 or ±12/25	DIP		5-57
	DAC80-CBI-V	12	±0.012	±25	±2.5, ±5, ±10 +5, +10V	5μsec	+5/20	DIP		5-57
	DAC80-CCD-I	3 digits	±0.025	±25	±1, 0 to -2mA	300nsec	[4]	DIP		5-57
	DAC80-CCD-V	3 digits	±0.025	±25	0 to +10V	5μsec		DIP		5-57
	DAC82KG	8	±0.016	±50	±2.5, ±5, ±10	2.5μsec	±15/15	DIP		5-68
	DAC82BM[1]	8	±0.016	±50	+5, +10V	2.5μsec	-15/-10	DIP		5-68
	DAC82SM[5]	8	±0.016	±50	±8, 0 to -1.6mA	2.5μsec		DIP		5-68
Low Drift [1] [6]	DAC85-CBI-I	12	±0.012	±20	±2.5, ±5, ±10	300nsec	±15/25	DIP		5-75
	DAC85-CBI-V	12	±0.012	±20	+5, +10V	5μsec	+5/20	DIP		5-75
	DAC85-CCD-I	12	±0.025	±20	+10V	300nsec		DIP		5-75
	DAC85-CCD-V	12	±0.025	±20	+10V	5μsec		DIP		5-75
	DAC85LD-CBI-I	12	±0.012	±5	±2.5, ±5, ±10	300nsec		DIP		5-75
	DAC85LD-CBI-V	12	±0.012	±5	+5, +10V	5μsec		DIP		5-75
Monolithic	DAC90-BG[1]	12	±0.4	±75	±1, -2mA	200nsec	±15 or ±12/7	DIP		5-83
	DAC90SG[2]	12	±0.4	±75	±1, -2mA	200nsec	±15 or ±12/7	DIP		5-83
I.C. Low Cost	*DAC862KG-BIN	12	±0.012	±9	0 to -2mA	3.5μsec	+5, 15	DIP		5-88
	DAC862BG-BIN	12	±0.006	±9	±1mA	3.5μsec	+15, 15	DIP		5-88
	DAC862SG-BIN	12	±0.006	±9		3.5μsec	-15, 20	DIP		5-88

Operating temperature range 0°C to 70°C, and parameters are typical unless otherwise noted.

1) -25°C to +85°C. 2) When used with an external op amp which uses the internal feedback resistor. 3) Prices are for quantities (1-9) (10-24) (25-99). 4) For ±12V supply operation, order DAC80Z. 5) -55°C to +125°C. 6) Each DAC85 listed has a corresponding 0°C to 70°C part.

*New

V/F CONVERTERS

Description	Model	V_{IN} Range (V)	F_{OUT} Range (kHz)	Linearity (% of FSR) max	Tempco (ppm of FSR/°C) max	Package		Page
Low Drift, Complete	VFC12	0 to +10	0 to 10	±0.01	50	Module		5-179
	VFC15	0 to +10	0 to 10	±0.01	10	Module		5-179
Very-Low Drift, Complete	VFC12LD	0 to +20	0 to 20	±0.005	50	Module		5-179
	VFC15LD	0 to +20	0 to 20	±0.005	10	Module		5-179
Low Cost, Monolithic	VFC32KP	User-selected	User-selected (500kHz max)	±0.01 at 10kHz	±150	DIP		5-186
	VFC32BM[1]	User-selected		±0.05 at 100kHz	±100	TO-100[10]		5-186
	VFC32SM[2]	User-selected		±0.2 at 500kHz	±150	TO-100[10]		5-186
Low Cost, Complete, Hybrid	*VFC42BP[1]	0 to +10	0 to 10	±0.01	±100	DIP		5-192
	VFC52BP[1]	0 to +10	0 to 100	±0.05	±100	DIP		5-192

POWER DACS

Description	Model	Input Coding	Accuracy	Tempco (ppm FSR/°C)	Output Voltage (V)	Output Current (mA)	Package		Page
Full Digital Control	4800	12-bit binary plus sign	±0.012% of FSR	22	±10V, ±60V	±200	Module		5-198
	4801	3-digit BCD plus sign	±0.012% of FSR	22	±10V, ±60V	±200	Module		5-198
Low Cost, Open PC Card	4804	12-bit binary	±0.05% of reading	50, max	User-selected to ±30	±2000	PC card		5-209

MICROPROCESSOR INTERFACED ANALOG INPUT SYSTEMS

Description	Model	Channels	Resolution	Accuracy (% of FSR)max	Tempco (ppm/°C)max	Package		Page
8080-, SC/MP-Compatible	MP20	8 differential 16 single-ended	8-bits	±0.8, high ±0.4, low	±40	DIP		5-103
6800-, 6502-Compatible	MP21	8 differential 16 single-ended	8-bits	±0.8, high ±0.4, low	±40	DIP		5-115
Universal	*MP22BG[1]	8 differential 16 single-ended	12-bits	±0.4, high ±0.1, low	±25[8]	DIP		5-127

MICROPROCESSOR INTERFACED ANALOG OUTPUT SYSTEMS

8080-, SC/MP-Compatible	MP10	2	8-bits	±0.4	±80	DIP		5-95
6800-, 6502-Compatible	MP11	2	8-bits	±0.4	±80	DIP		5-95

SAMPLE/HOLD CIRCUITS

Description	Model	Gain/Offset Error (%) (mV)	Charge Offset (mV)	Droop Rate (mV/msec)	Tempco (ppm of 20V/°C)	Acquisition Time (μsec)[9]	Package		Page
Low Cost, Complete	SCH80KP	±0.01, ±2 max	±2 max	0.5 max	3	10 max	DIP		5-161
	SHC80BM[1]	±0.01, ±2 max	±2 max	0.5 max	3	10 max	DIP[10]		5-161
High Speed, Complete	SHC85	±0.01, ±2 max	±2 max	0.5 max	3	4.5 max	DIP[10]		5-165
Low Cost, Monolithic	*SHC298AM[1]	±0.01, ±7 max	±25 max	10 max[11]	4	10 max	TO-99[10]		5-169
Very-High Speed	SHM60	±0.01, ±1.5	±1.5	5	2	1 max	Module		5-175

MULTIPLEXERS

Description	Model	Channels	Input Range (V)	On Resistance (kΩ) max	Crosstalk (% of OFF Channel Signal)	Settling Time (to 0.01%) (μsec)	Package		Page
CMOS	MPC8S	8 single	±15	1.8	0.005	5	DIP		5-135
CMOS	MPC4D	4 differential	±15	1.8	0.005	5	DIP		5-135
CMOS	MPC16S	16 single	±15	1.8	0.005	7	DIP		5-142
CMOS	MPC8D	8 differential	±15	1.8	0.005	7	DIP		5-142

DATA ACQUISITION SYSTEMS

Description	Model	Channels	Resolution (Bits)	Throughput Accuracy (% of FSR)	Throughput Rate (kHz)	Package		Page
Modular, Low Level	SDM853	16 single-ended 8 differential	12	±0.025	30[12]	Module		5-149
Hybrid	*SDM856JG	16 single-ended 8 differential	12	±0.048	33	DIP		5-155
	SDM856KG		12	±0.024	25	DIP		5-155
Hybrid Low Level	SDM857JG		12	±0.048	25	DIP		5-155
	SDM857KG		12	±0.024	18	DIP		5-155

7) Prices for quantities (1-9)(10-24). 8) Unipolar, excluding 1A. 9) 10V step to 0.01% of final value. 10) Hermetic. 11) With 1000pF external holding capacitor. 12) can be increased if short-cycled to 8- or 10-bit resolution.

GLOSSARY OF TERMS & DEFINITIONS
Data Conversion and Acquisition

ACQUISITION TIME

The time the output of a sample/hold circuit takes to change from its previous value to a new value when the circuit is switched from the hold mode to sample mode. It includes the slew time and settling time to within a certain error band of the final value and is usually specified for a full-scale change.

APERTURE TIME

When a sample/hold circuit is switched from sample to hold, a finite amount of time is required for the internal electronics to turn off. Aperture time is the time between the sample-to-hold command transition and the point at which the output ceases to follow the input.

APERTURE TIME UNCERTAINTY

The possible deviation in aperture time from one sample-to-hold transition to the next.

COMPLIANCE VOLTAGE

Some D/A converters have an output current proportional to the input digital code. The compliance voltage is that voltage which may be impressed on the output current pin without degrading the specified accuracy of the converter.

CONVERSION SPEED

The measure of how long it takes an A/D converter to arrive at the proper output code. It is the time between the edge of the convert command pulse that starts conversion and the rising edge of the end-of-convert signal that indicates the conversion is complete.

CHARGE OFFSET

During the sample-to-hold transition of a sample/hold circuit, a small amount of charge is transferred to the holding capacitor because of the switching process. This is known as the charge offset and is usually expressed in millivolts.

CROSSTALK

The measure of effect an off-channel signal has on the on-channel signal in a multiplexer, expressed in terms of dB of attenuation of the off-channel signal.

DIFFERENTIAL LINEARITY

The measure of the linearity from one digital state to the next. It applies to A/D and D/A converters. If the differential linearity is specified as +1/2LSB, the step size from one state to the next may be from 1/2 to 3/2 of an ideal 1LSB step.

DROOP RATE

A sample/hold circuit in the hold mode has a charge stored on a capacitor that is proportional to the input voltage at the time it was switched to the hold mode. Charge leaks off the capacitor because of the bias current of the buffer amplifier and switch leakage current. The droop rate is an expression of how fast the charge leaks off the capacitor and is given as a voltage per-unit-of-time.

FEEDTHROUGH

The measure of the change of the output voltage of a sample/hold in the hold mode due to a voltage change in the input, expressed as dB of attenuation.

GAIN ERROR

The error in the input-to-output ratio, usually expressed in percent. It is manifest as a rotation about the most negative full scale point of the transfer function curve. It is nulled in A/D, D/A, or V/F converters after the offset error is nulled by setting the input for a full-scale output and adjusting an external trim pot for the correct output.

LEAKAGE CURRENT

Multiplexer input current that does not flow through to the output but is shunted internally. It is also current that flows from OFF channels into the ON channel. In a current output D/A converter, there is a digital input code that ideally yields zero output current. If current flows with that input code, it is called leakage current. It is analogous to output voltage offset in a voltage-output D/A converter.

LEAST SIGNIFICANT BIT (LSB)

The lowest-order bit or the bit with the least weight.

LINEARITY

The maximum deviation of an actual output from an ideal output defined by a straight-line drawn through the end points of the transfer function. This is the error that remains after offset and gain errors have been nulled. It applies to A/D, D/A, and V/F converters. Linearity can be expressed in terms of percent of full scale range or fractions of a least significant bit (LSB). A converter must be linear to within ±1/2LSB to be accurate to its full resolution.

MONOTONICITY

In a D/A converter, if the output analog signal either increases or stays the same for an increase in input digital code, it is said to be monotonic. In an A/D converter, if

the output digital code increases or stays the same for a 1LSB increase in input voltage, it is said to be monotonic. If the differential linearity is within ±1LSB, the device will be monotonic. Monotonicity is especially important in control loops where convergence is necessary.

MOST SIGNIFICANT BIT (MSB)

The highest-order bit or the bit with the greatest weight.

NO MISSING CODES

This is a property of an A/D converter that is related to, but is more stringent than, monotonicity. If a converter is guaranteed to have no missing codes, there will be no output digital state that will be skipped when the input voltage is varied over the entire range.

OFFSET ERROR

This is an error in the reference point of the transfer function. It appears as a constant amplitude error signal at a D/A output or A/D input. It also appears as a constant frequency shift in the output of a V/F converter. It is nulled prior to adjusting gain error by setting the input to the most-negative input and adjusting the output to the proper value.

POWER SUPPLY REJECTION RATIO

The measure of output signal change due to power supply voltage change. It is expressed as dB of attenuation or % output change per % supply change.

QUANTIZING ERROR

In an A/D converter, there is an infinite number of possible input voltages, but only 2^n output codes (n = number of bits). Therefore, there will be an error as great as 1/2LSB because of this quantizing effect and the greatest error will occur at the transition voltage where the output changes state.

RESOLUTION

The number of bits on the input or output of an A/D or D/A converter. The number of discrete steps or states is equal to 2^n where n is the resolution of the converter, however, n bits of resolution does not guarantee n bits of accuracy.

SETTLING TIME

The time delay between a change of input signal value and the effected change in the output signal. It is usually expressed in terms of how long it takes the output to arrive at, and remain within, a certain error band around the final value and is often given for several different magnitudes of input step change.

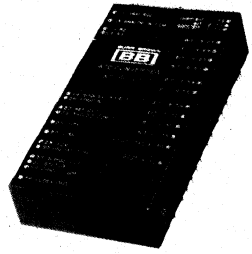
SWITCHING TIME

The time it takes for a multiplexer to change from one channel to the next with the new output signal being within a certain percentage of its final value. It is expressed for a maximum voltage transition.

THROUGHPUT RATE

An A/D converter or a data acquisition system has a finite number of points that it can convert in any given time. Throughput rate is an expression of that quantity. It is dependent on the time it takes to make a conversion and the time required to set up to make the next conversion. In a data acquisition system this time includes the composite delay due to switching and settling times of the mux, settling time of the amplifier and acquisition time of the sample-and-hold.

BURR-BROWN



ADC60

High Speed ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **FAST CONVERSION SPEED:**
  12-bits - 3.5μsec, max
  10-bits - 1.88μsec, max
  8-bits - 0.88μsec, max
  Throughput sampling rates from 250kHz (12-bits) to 1MHz (8-bits) can be attained
- **PIN-PROGRAMMABLE UNIPOLAR OR BIPOLAR**
- **ANALOG SIGNALS**
- **SERIAL AND PARALLEL DATA OUTPUTS**
- **SELF-CONTAINED WITH INTERNAL CLOCK & REFERENCE**
  Simplifies system design and reduces cost
- **±1/2LSB LINEARITY**
  Provides accurate conversion
- **NO MISSING CODES**

DESCRIPTION

The Model ADC60 is a very high speed, successive approximation A/D converter than is designed for applications requiring system throughput sampling rates from 250kHz to 1MHz. The fast conversion speed is accomplished with proprietary fast settling circuits which preserve linearity and drift while permitting conversion speeds up to 100nsec/bit.

Available in 8-, 10-, and 12-bit resolutions the ADC60 contains an internal reference and clock. Internal components are provided for pin-programmable analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

Digital data is available in both serial and parallel, binary form with corresponding timing signals. All digital input and output signals are DTL/TTL-compatible.

The ADC60 operates from ±15VDC and +5VDC power, and is housed in a 2" x 4" x 0.75" module with screened-on pin function identification.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-319 Printed in U.S.A. July, 1978

THEORY OF OPERATION

Upon receipt of an external CONVERT command, the previous data sample is cleared from the output register. Each bit is then successively compared against the amplitude of the input signal, and is either held as a "0" or turned on as a "1" until all bits have been tried. The parallel data output is not available for transfer to external devices until the STATUS output changes form logic "1" to logic "0".

Serial data is only available during conversion, and must be transferred to external devices with the CLOCK and STATUS signals beginning with the first clock pulse following a change in STATUS from "0" to logic "1".

TIMING CONSIDERATIONS

Data is available in both serial and parallel form. Timing signals are available for the transfer of data to external devices. For parallel data transfer, STATUS and its compliment $\overline{\text{STATUS}}$ indicate when the conversion is complete. For serial data transfer, the CLOCK OUT signal starts on the trailing edge of the CONVERT COMMAND; and serial data is valid before the positive going edge of the CLOCK OUT signal. The CLOCK ceases operation when the conversion is complete. There will be one more clock pulse than the number of bits converted (resolution). Figure 1 shows the timing details of the ADC60.

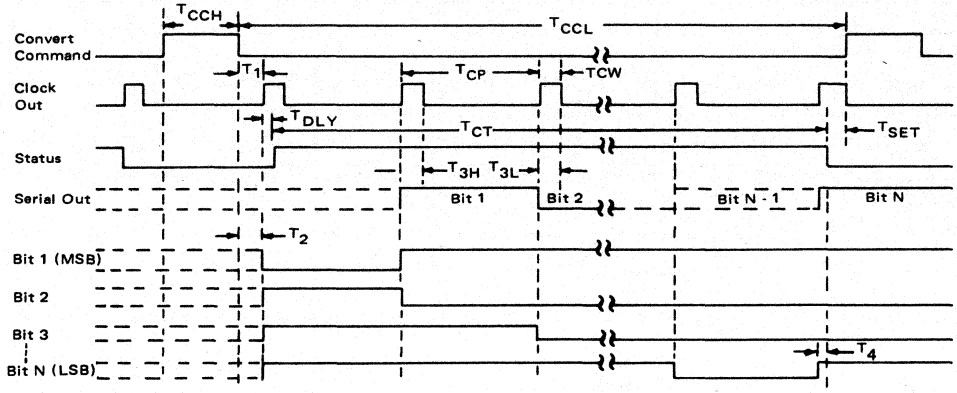


FIGURE 1. ADC60 Timing Diagram.

SYMBOL	DESCRIPTION	PARAMETER MIN.	TYP.	MAX.	UNITS
T_{CT}	Conversion Time - 12 Bit	2.50	3.45	3.50	µs
	10 Bit	1.20	1.83	1.88	µs
	8 Bit	0.80	0.84	0.88	µs
T_{CCH}	Width of Convert Command Pulse	30	---	---	ns
T_{CCL}	Internal Between Convert Command Pulses – $(T_{CT} + T_1 + T_{DLY})$	NOTE 1			
T_1	Delay From Trailing Edge of Conv. Command To Leading Edge of Clock Out	30	41	60	ns
T_2	Delay from Conv. Command To Reset	26	40	68	ns
T_{3H}	Delay From Valid High Output To Trailing Edge of Clock Out	22	43	70	ns
T_{3L}	Delay From Valid Low Output To Trailing Edge of Clock Out	30	51	72	ns
T_4	Delay From Valid Data to STATUS LOW	12	18	37	ns
T_{DLY}	Delay From Clock Out to STATUS HIGH	22	44	60	ns
T_{SET}	Setup Time from Status to Conv. Command - Note 2	0	---	---	ns
T_{CW}	Clock Out Width	40	50	60	ns
T_{CP}	Clock Out Period - Note 3 - 12 Bit	192	265	270	ns
	10 Bit	104	165	171	ns
	8 Bit	88	95	98	ns

TABLE 1. Switching Characteristics.

NOTES: (1) ADC60 internal clock may be inhibited by returning the convert command to "1". By this technique, the converter may be cycled through an entire conversion one clock pulse at a time. This technique allows the conversion time to be extended to virtually any conversion time.

(2) The convert command may rise as soon as the last clock out pulse rises.

(3) The clock period for ADC60 is not necessarily constant throughout the conversion time.

SPECIFICATIONS

(Typical at 25°C and rated power supplies unless otherwise noted)

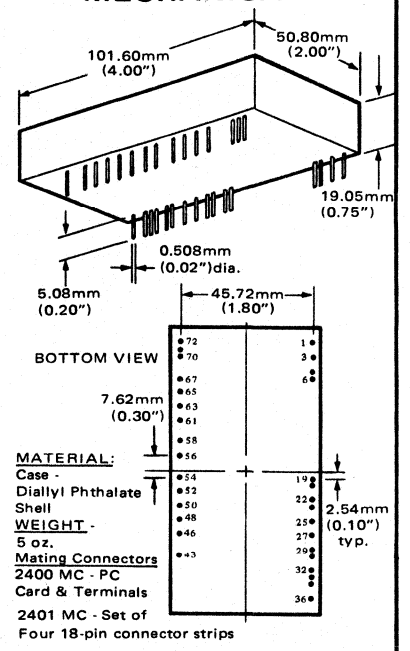
ELECTRICAL

MODEL	ADC60-08	ADC60-10	ADC60-12	UNITS
RESOLUTION	8	10	12	Bits
INPUT				
ANALOG INPUTS				
Voltage Ranges Bipolar	±2.5, ±5, ±10			Volts
Unipolar	0 to +5, 0 to +10, 0 to +20			Volts
Impedance	0.2			kΩ/V FSR
DIGITAL INPUTS(1)				
Convert Command	Positive Pulse 30 ns wide (min.) Trailing edge ("1" to "0") initiates conversion.			
Logic Loading	2			TTL Loads
TRANSFER CHARACTERISTICS				
ERROR(2)				
Gain Error(2)	±0.2	±0.1	±0.1	% of FSR(3)
Offset Error(2)	±0.2	±0.1	±0.1	% of FSR
Linearity Error, max	±0.195	±0.0488	±0.0244	% of FSR
Inherent Quantization Error	±0.19	±0.048	±0.012	% of FSR
Differential Linearity Error, max	±0.27	±0.068	+0.024,-0.019	% of FSR
Monotonicity	*	Guaranteed	*	
No Missing Codes	*	Guaranteed	*	
Power Supply Sensitivity	*	±0.002	*	% of FSR/%
DRIFT				
0°C to +70°C, max	±20	±20	±15	ppm/°C
-25°C to +85°C, max	±40	±40	±30	ppm/°C
CONVERSION SPEED, max	0.88	1.88	3.5	μsec
OUTPUT(4)				
DIGITAL DATA				
Parallel				
Output Codes, Unipolar	USB (straight Binary)			
Bipolar	BOB (offset Binary) and BTC (Two's Complement)			
Output Drive	6			TTL Loads
Serial Data				
Output Drive	6			TTL Loads
Status	"1" During Conversion			
$\overline{\text{Status}}$	"0" During Conversion			
Output Drive of Status and $\overline{\text{Status}}$	6			TTL Loads
Clock	A Positive Pulse Train Used for Strobing Serial Data into an External Register.			
Clock Output Drive	9			TTL Loads
INTERNAL REF. VOLTAGE	6.3			Volts
Max External Current with no degradation of Specifications	200			μA
POWER REQUIREMENTS				
Rated Voltages	±15 and +5			Volts
Range for Rated Accuracy	±14.5 to ±15.5 and +4.75 to +5.25			Volts
Supply Drain +15V	+50			mA
(max) -15V	-50			mA
+5V	+270			mA
PACKAGE	2"x 4"x 0.75"			
TEMPERATURE RANGE				
Specification	0 to +70			°C
Operating (reduced drift specs-see above)	-25 to +85			°C
Storage	-55 to +100			°C

(1) All digital inputs in the ADC60 are TTL compatible. i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V, min.
(2) Gain and Offset Errors may be adjusted to zero with external trimming.
(3) FSR - Full Scale Range.
(4) TTL Compatible, Logic "0" = +0.4V max, Logic "1" = +2.4V min.

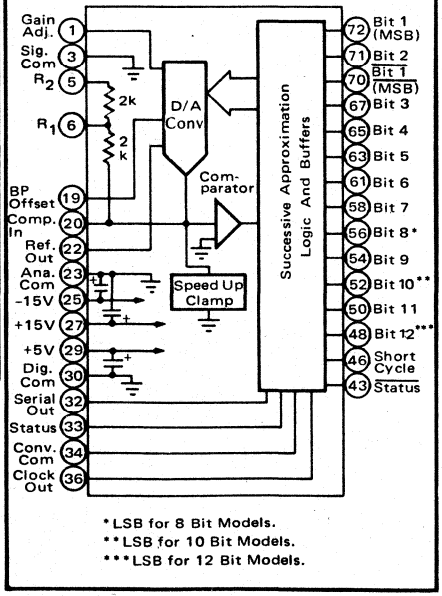
* Specifications same for all models.

MECHANICAL



Pin spacing located on 2.54mm (0.10") grid.
Allow 5.08mm (0.20") between pins 18-19 and 54-55.
Pin material and plating composition meet method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).

CONNECTION DIAGRAM



*LSB for 8 Bit Models.
**LSB for 10 Bit Models.
***LSB for 12 Bit Models.

DISCUSSION OF PERFORMANCE

ACCURACY

A/D converter error contributors are QUANTIZATION ERROR, LINEARITY ERROR, DRIFT, GAIN and OFFSET errors. Figure 2 shows the transfer function of an ideal bipolar A/D converter, and describes the quantization and linearity error bands at a single temperature. Initial gain and offset errors are trimmed to zero. Gain drift rotates the line about the minus full scale point (or around zero for a unipolar A/D converter). Offset drift contributes an offset shift to the transfer function over the operating temperature range.

LINEARITY ERROR

LINEARITY ERROR is measured as the difference, in LSB, between the actual input voltage signal and the ideal transition voltage as shown in Figure 2. This measurement is made with GAIN and OFFSET errors adjusted to zero. Thus, the LINEARITY ERROR, neglecting QUANTIZING ERROR, expresses the true accuracy of an A/D converter relative to the reading.

DIFFERENTIAL LINEARITY ERROR

DIFFERENTIAL LINEARITY ERROR is defined as the difference between actual adjacent transition values and an ideal 1 LSB step. A DIFFERENTIAL LINEARITY ERROR of 1/2 LSB means that the size of a horizontal step can range from 1/2 LSB to 3/2 LSB. The size of the smallest step must be greater than 0.2 LSB to guarantee no missing codes in an A/D converter. Expressed mathematically, Differential Linearity (D.L.) $\triangleq \frac{(v_{j+1} - v_j) - \text{LSB}}{\text{LSB}}$ where $\text{LSB} \triangleq V_{j+1} - V_j$.

MONOTONICITY

An A/D converter is monotonic when the digital output code increases or remains the same for increasing analog input signals. The ADC60 is monotonic over the full scale range.

DIGITAL OUTPUT CODES

Three binary digital codes may be derived from the ADC60. They are Unipolar Straight Binary (USB) for unipolar analog input signals, and Bipolar Offset Binary (BOB) and Bipolar Two's Complement (BTC) for bipolar analog input signals. These codes are defined below in Table II.

A more detailed discussion of these and other A/D converters specifications is given in a separate Burr-Brown Application Note – AN53.

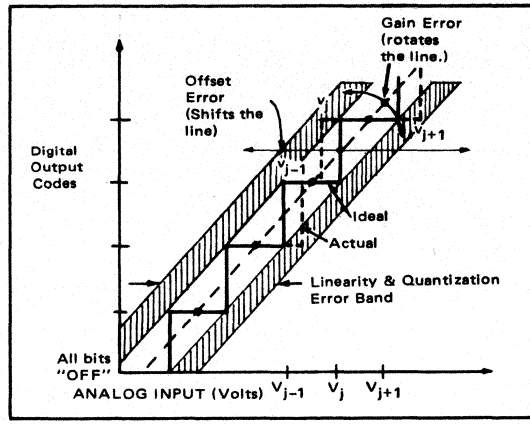


FIGURE 2. A/D Converter Definition of Specifications.

DEFINITION OF DIGITAL CODES

Three binary codes are available on the ADC60 parallel output; these are USB for unipolar input signals, and BOB or BTC for bipolar input signals. The LSB values and code definitions for each analog input signal range are shown below.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Signal Range	Defined As:	±10V	±5V	±2.5V	0 to +20V	0 to +10V	0 to +5V
Code Designation		BOB or BTC*	BOB or BTC*	BOB or BTC*	USB**	USB**	USB**
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13 mV	39.06 mV	19.53 mV	78.13 mV	39.06 mV	19.53 mV
	n = 10	19.53 mV	9.77 mV	4.88 mV	19.53 mV	9.77 mV	4.88 mV
	n = 12	4.88 mV	2.44 mV	1.22 mV	4.88 mV	2.44 mV	1.22 mV
MSB LSB –							
111....111***	+Full Scale	+10V -½ LSB	+5V -½ LSB	+2.5V-½ LSB	+20V -½ LSB	+10V -½ LSB	+5V -½ LSB
100....000	Mid Scale	0	0	0	+10V	+5V	+2.5V
000....001	-Full Scale	-10V +½ LSB	-5V +½ LSB	-2.5V +½ LSB	0 + ½ LSB	0 + ½ LSB	0 + ½ LSB

*BOB = Bipolar Offset Binary
**USB = Unipolar Straight Binary
BTC = Bipolar Two's complement - obtained by using the complement of the most significant bit (MSB). MSB is available on pin 70 of the module.
*** Voltages given are the nominal value for transition to the code specified.

TABLE II. Input Voltages, LSB Values, and Code Definitions.

INSTALLATION AND OPERATING INSTRUCTIONS

The ADC60 is available with binary code resolutions of 8, 10 and 12 bits. Six input signal ranges are pin programmable over the following ranges: 0 to +5, +20, +10, ±2.5, ±5 and ±10 volts.

Single polarity binary ranges are designated USB and dual polarity binary ranges are designated BOB or BTC. Connections for specific codes are detailed in Table III.

OPTIONAL GAIN AND OFFSET ADJUST

Although GAIN and OFFSET are factory trimmed to ±0.1%, these parameters may be trimmed to zero error using external trim adjustments as shown in Figure 3. Due to component aging, these external adjustments may be required later on to recalibrate the ADC60 after 3 to 6 months.

To avoid interaction between adjustments, the offset should be adjusted first. Use multi-turn potentiometers with TCR of 150 ppm/°C or better.

OFFSET is adjusted by sweeping the input through the end point transition voltage that causes an output transition to "all bits OFF". Adjust the OFFSET potentiometers until the actual end point transition voltage occurs at the value shown in Table II.

GAIN is adjusted by sweeping the input voltage through the end point transition that causes an output digital code of "all bits ON". See Table II for end point transition values.

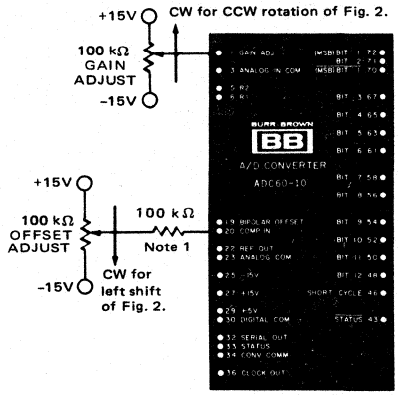


FIGURE 3. ADC60 Installation Diagram.

NOTES:

1. If GAIN and/or OFFSET trim adjustments are not used simply leave pin 1 and/or pin 20 open. The minimum range of adjustment for OFFSET is ±0.25% of full scale range; for GAIN it is ±0.3% of full scale range. Locate the 100 kΩ resistor as close as possible to pin 20.

GENERAL NOTES:

- If an input buffer amplifier is required, the BB3550 is recommended.
- Use BB SHM60 Sample/Hold if a Sample/Hold is required (1 μsec acquisition time).

INPUT SCALING

To utilize the maximum resolution of the ADC60, the input FSR must be selected to match the expected full scale range of the input signal. Table III and Figure 4 show the connections required for input scaling.

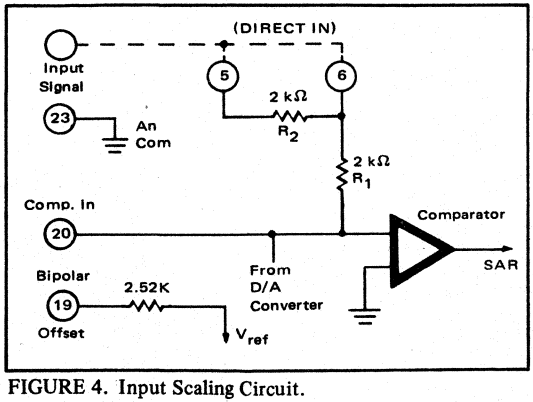


FIGURE 4. Input Scaling Circuit.

INPUT SIGNAL RANGE	DIGITAL OUTPUT CODE	CONNECT PIN 19 TO	CONNECT PIN 5 TO	CONNECT INPUT SIGNAL TO
±2.5V	BOB or BTC	PIN 20	PIN 20	PIN 6
0 to +5V	USB	PIN 23	PIN 20	PIN 6
±5V	BOB or BTC	PIN 20	OPEN	PIN 6
0 to +10V	USB	PIN 23	OPEN	PIN 6
0 to +20V	USB	PIN 23	INPUT	PIN 5
±10V	BOB or BTC	PIN 20	INPUT	PIN 5

TABLE III. ADC60 Input Scaling Connections.

SYSTEM TIMING

The basic system timing diagram is shown in Figure 1.

CONVERT COMMAND

A pulse of at least 30 nanoseconds duration (positive going) is required at pin 34 to start each conversion. Conversion starts after the NEGATIVE GOING edge of the CONVERT COMMAND.

STATUS

The STATUS output switches to a logical "1" on the NEGATIVE EDGE of the CONVERT COMMAND pulse. It returns to a logical "0" at the end of conversion. The $\overline{\text{STATUS}}$ output leads STATUS by one normal gate delay (10 nsec).

SHORT CYCLE

The ADC60 may be short-cycled for obtaining lower resolutions and corresponding faster conversion speeds. Connect "Short Cycle" (pin 46) of the ADC60 to bit N + 1 as shown in Table IV.

The SHORT CYCLE feature must be used for the 8 and 10 bit models as outlined in Table IV. For 12 bit models, the SHORT CYCLE is not used and may be left open; however, in a high noise environment, the SHORT CYCLE input, pin 46, should be tied to +5 volts (pin 29) through a 1000 ohm resistor.

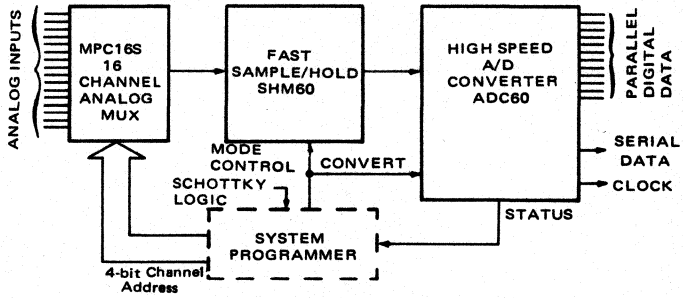
RESOLUTION (BITS)	CONNECT PIN 46 TO PIN	MAXIMUM CONVERSION TIME (μSEC) MODEL		
		8	10	12
12	N/A	–	–	3.50
11	48	–	–	3.24
10	50	–	1.88	2.97
9	52	–	1.71	2.70
8	54	0.88	1.53	2.43
7	56	0.79	1.37	2.16
6	58	0.69	1.20	1.89
5	61	0.59	1.03	1.62
4	63	0.49	0.85	1.35

TABLE IV. Short cycle connections for ADC60 and corresponding conversion speeds.

APPLICATION NOTE

HIGH SPEED DATA ACQUISITION SYSTEM

A high speed 16 channel data acquisition system with up to 625 kHz system sampling rate is shown below. (If the ADC60 is used without a multiplexer or sample/hold for single channel applications, sampling rates up to 1 MHz are possible.)



The system shown uses an overlapped mode programmer to eliminate or reduce the settling effects of the multiplexer and sample/hold and maximizes system throughput speed.

Typical system sampling speeds for the input signal ranges using these components are shown in Table V.

RESOLUTION (BITS)	INPUT SIGNAL RANGE (volts)	SYSTEM THROUGHPUT SAMPLING RATE (max)	TYPICAL SYSTEM ACCURACY *RSS
12	±10	200 kHz	±0.04%
12	0 to +10	220 kHz	±0.04%
10	±10	325 kHz	±0.125%
10	0 to +10	370 kHz	±0.125%
8	±10	530 kHz	±0.25%
8	0 to +10	625 kHz	±0.25%

TABLE V. Typical System Characteristics. *RSS = Root Sum Squared.

BURR-BROWN

ADC80

IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **COMPACT DESIGN** - Self-contained with internal clock, comparator, and reference

  32-pin ceramic package

- **FAST CONVERSION SPEEDS**
  Provide fast signal sampling rates
  12-bits - 25μsec, 10-bits - 21μsec
  Faster conversion speeds obtainable with "Short-Cycling" and optional external clock

- **LOW COST**

- **WIDE SUPPLY RANGE** - Will operate with ±10.8V to ±16V supplies (Z models)

DESCRIPTION

The Model ADC80AG-10 and ADC80AG-12 are 10- and 12-bit successive approximation A/D converters. They utilize state-of-the-art IC and laser-trimmed thin-film components, and are packaged in a compact 32-pin ceramic package.

Complete with internal reference, the ADC80 offers versatility and performance formerly offered only in larger modular or rack-mount packages.

Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V or 0 to +10V.

Gain and offset errors may be externally trimmed to zero, offering initial accuracies of better than ±0.0122% (±1/2LSB). The model ADC80 is specified for -25°C to +85°C operation.

The fast conversion speeds of 25Msec for 12-bit and 21Msec for 10-bit resolution make the ADC80 excellent for a wide range of applications where system throughput sampling rates from 40kHz to 47kHz are required. In addition, the ADC80 may be short cycled and an external clock may be used to obtain faster conversion speeds at lower resolutions.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are DTL/TTL-compatible. Two power supply ranges are available: ±15V and ±12V (Z models). A +5V logic supply is also required.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-333E

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DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent QUANTIZATION ERROR of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including GAIN, OFFSET, LINEARITY, DIFFERENTIAL LINEARITY and POWER SUPPLY SENSITIVITY. Initial GAIN and OFFSET errors may be adjusted to zero. GAIN drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits OFF) and OFFSET drift shifts the line left or right over the operating temperature range. LINEARITY error is unadjustable and is the most meaningful indicator of A/D converter accuracy. LINEARITY error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A DIFFERENTIAL LINEARITY error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB ±1/2LSB.

The ADC80 is also MONOTONIC, assuring that the output digital code either increases or remains the same for increasing analog input signals. A monotonic converter can have missing codes; therefore, Burr-Brown specifies no missing codes over a temperature range.

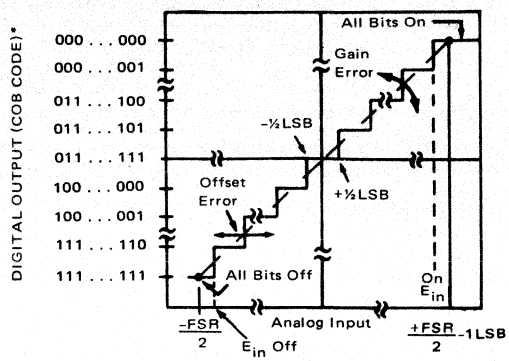


FIGURE 1. Input vs output for an ideal bipolar A/D converter.
*See Table I for digital code definitions.

TIMING CONSIDERATIONS

The timing diagram of the ADC80 (Figure 2) assumes an analog input such that the positive true digital word 10011000-1001 exists. The output will be complementary as shown in Figure 2 (011001110110 is the digital output).

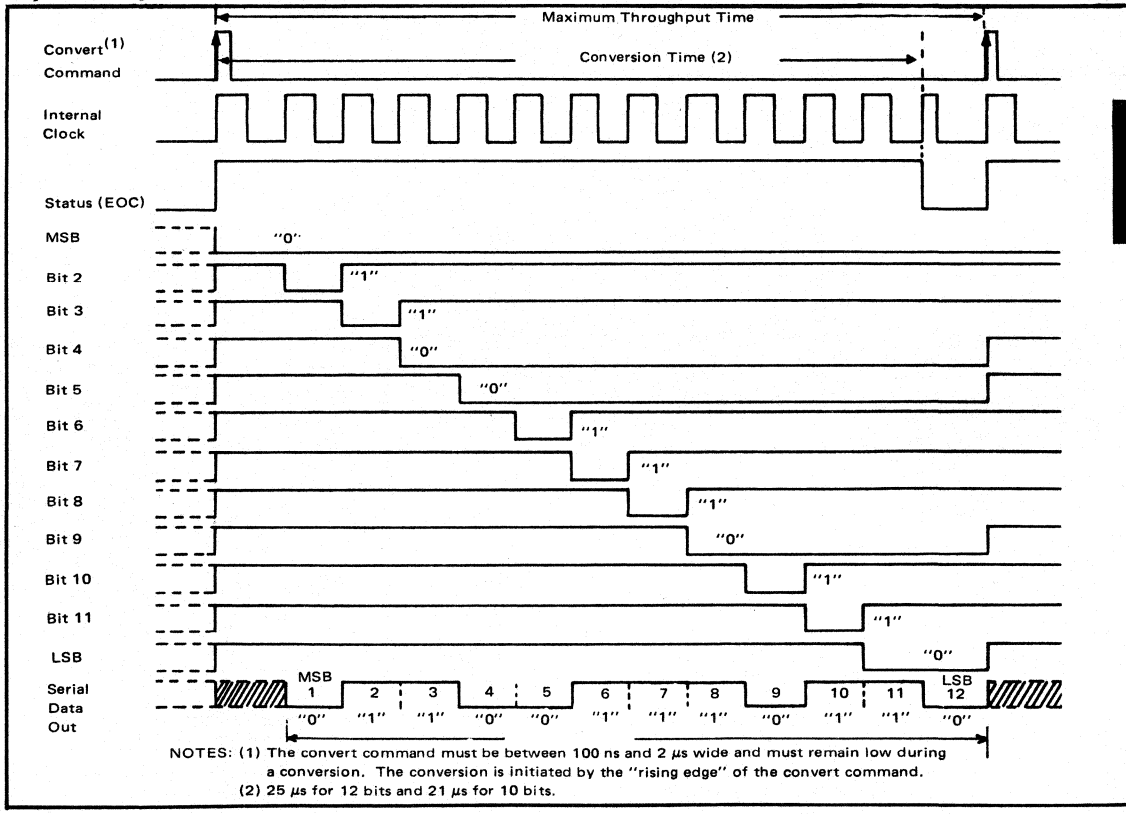


FIGURE 2. ADC80 Timing Diagram.

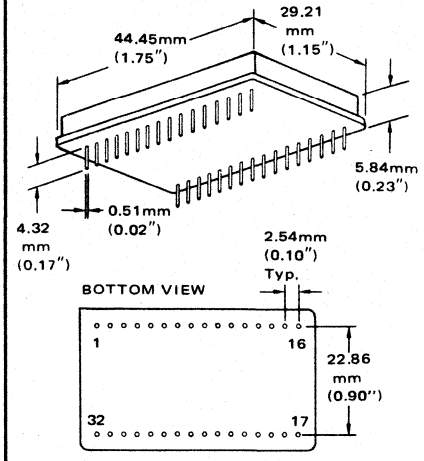
ELECTRICAL SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	ADC80AGZ-12 ADC80AG-12	ADC80AGZ-10 ADC80AG-10	Units
RESOLUTION	12	10	Bits
INPUT			
ANALOG INPUTS			
Voltage Ranges - Bipolar	±2.5, ±5, ±10		V
- Unipolar	0 to +5, 0 to +10		V
Impedance (Direct Input)			
0 to +5V, ±2.5V	2.5		kΩ
0 to +10V, ±5V	5		kΩ
±10V	10		kΩ
DIGITAL INPUTS[1]			
Convert Command	Positive Pulse 100ns Wide (min) 2µsec Wide (max).		
Logic Loading	1		TTL Load
External Clock	1		TTL Load
TRANSFER CHARACTERISTICS			
ERROR			
Gain Error[3]	±0.1		%
Offset Error[3] - Unipolar	±0.05		% of FSR[2]
- Bipolar	±0.1		% of FSR
Linearity Error (max)[4]	±0.012	±0.048	% of FSR
Inherent Quantization Error	±1/2		LSB
Differential Linearity Error	±1/2		LSB
No Missing Codes Temp. Range	0 to +50	0 to +70	°C
Power Supply Sensitivity			
±15V	±0.0030		% of FSR/%V,
+5V	±0.0015		% of FSR/%V,
DRIFT			
Specification Temperature Range	-25 to +85		°C
Total accuracy, bipolar (max)[8]	±23		ppm/°C
Gain, (max)	±30		ppm/°C
Offset - Unipolar	±3		ppm of FSR/°C
- Bipolar, (max)	±15		ppm of FSR/°C
Linearity, (max)	±3		ppm of FSR/°C
Monotonicity	GUARANTEED		
CONVERSION SPEED(max)[5]	25	21	µsec
OUTPUT			
DIGITAL DATA			
(all codes complementary)			
Parallel			
Output Codes[6] - Unipolar	CSB		
- Bipolar	COB, CTC		
Output Drive	2		TTL Loads
Serial Data Codes (NRZ)	CSB, COB		
Output Drive	2		TTL Loads
Status	Logic "1" during conversion		
Status Output Drive	2		TTL Loads
Internal Clock			
Clock Output Drive	2		TTL Loads
Frequency[7]	500		kHz
INTERNAL REF. VOLTAGE	6.3		V
Max. External Current (with no degradation of specifications)	200		µA
Tempco of Drift (max)	±20		ppm/°C
POWER REQUIREMENTS			
Rated Voltages	±15, +5		V
Z models	±12, +5		V
Range for Rated Accuracy	4.75 to 5.25 and ±14.0 to ±16.0		V
Z models	4.75 to 5.25 and ±10.8 to ±16.0		V
Supply Drain +15V or +12V	+20		mA
-15V or -12V	-20		mA
+5V	+70		mA
TEMPERATURE RANGE			
Specification	-25 to +85		°C
Operating (derated spec)	-55 to +100		°C
Storage	-55 to +125		°C

1. DTL/TTL compatible i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V min for inputs and for digital outputs. Logic "0" = +0.4V max and "1" = 2.4V min.
2. FSR means Full Scale Range - for example, unit connected for ±10V range has 20V FSR.
3. Adjustable to zero with external trimpots.
4. Error shown is the same as ±1/2 LSB max for resolution of A/D converter.
5. Conversion time with internal clock.
6. See Table I. CSB - Complementary Straight Binary.
   COB - Complementary Offset Binary.
   CTC - Complementary Two's Complementary.
7. For conversion speeds specified.
8. Includes drift due to linearity, gain, and offset drifts.

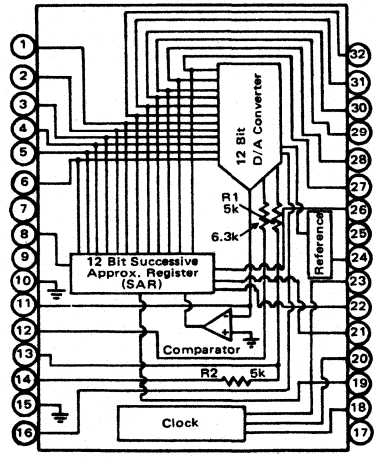
MECHANICAL



PINS: Pin material and plating composition conform to method 2003 (Solderability) of Mil-Std-883 (except paragraph 3.2).
CASE: Ceramic
MATING CONNECTOR: 2302MC - Set of two 16 pin strips
WEIGHT: 13 grams (0.46 oz).

Connection Diagram

TOP VIEW



PIN CONNECTIONS

1 Bit 6	32 Bit 7
2 Bit 5	31 Bit 8
3 Bit 4	30 Bit 9
4 Bit 3	29 Bit 10 (LSB-10 Bits)
5 Bit 2	28 Bit 11
6 Bit 1 (MSB)	27 Bit 12 (LSB-12 Bits)
7 +5V Analog Supply	26 Serial Out
8 Bit 1 (MSB)	25 -15V or -12V (Z Models)
9 +5V Digital Supply	24 Ref Out (+6.3V)
10 Digital Common	23 Clock Out
11 Comparator IN	22 Status
12 Bipolar Offset	21 Short Cycle
13 R1 10V Range	20 Clock Inhibit
14 R2 20V Range	19 External Clock
15 Analog Common	18 Convert Command
16 Gain Adjust	17 +15V or +12V (Z Models)

TYPICAL PERFORMANCE CURVES

FIGURE 3. Linearity error vs conversion time.

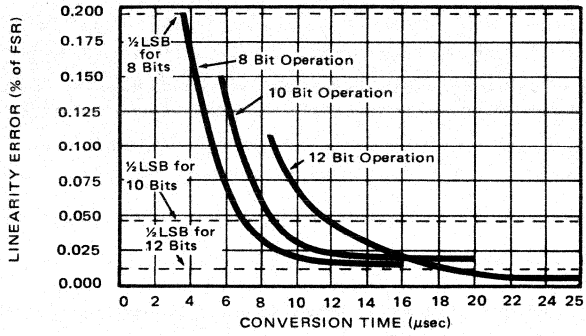


FIGURE 4. Differential linearity error vs conversion time.

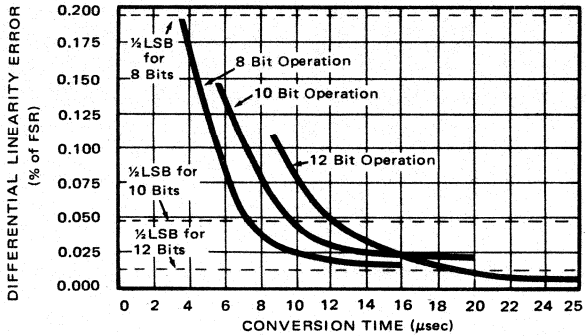


FIGURE 5. Gain drift error (% of FSR) vs temperature.

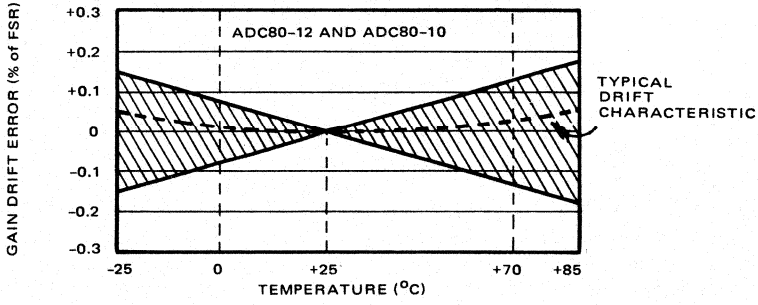
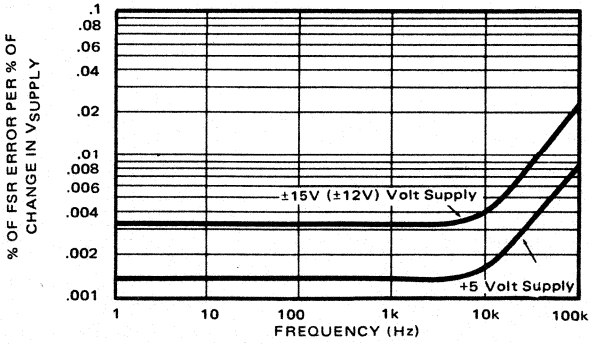


FIGURE 6. Power supply rejection vs power supply ripple frequency.



DEFINITION OF DIGITAL CODES

PARALLEL DATA

Three binary codes are available on the ADC80 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary two's complement (CTC) and complementary offset binary (COB) for bipolar input signal ranges.

Table I describes the LSB, transition values and code definitions for each possible ADC80 analog input signal range for 8, 10 and 12 bit resolutions.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line of the ADC80; they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occuring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES					
Analog Input Voltage Range	Defined As:	±10V	+5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB or CTC*	COB or CTC*	COB or CTC*	CSB**	CSB**
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000...000***	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V
111...110	-Full Scale	-10V +½LSB	-5V +½LSB	-2.5V +½LSB	0 + ½LSB	0 +½LSB

* COB = Complementary Offset Binary
** CSB = Complementary Straight Binary
*CTC = Complementary Two's complement - obtained by using the complement of the msot significant bit (MSB). $\overline{MSB}$ is available on pin 8.
*** Voltages given are the nominal value for transition to the code specified.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

DISCUSSION OF SPECIFICATIONS

The ADC80 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors and conversion speed effects on accuracy. The ADC80 is factory trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial GAIN and OFFSET errors are factory trimmed to ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown on page 5-17.

ACCURACY DRIFT VS TEMPERATURE

Three major drift parameters degrade A/D converter accuracy over temperature; they are gain, offset and linearity drift. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum-squared (RSS) or 1σ errors as follows:

$$RSS = \sqrt{\epsilon_g^2 + \epsilon_o^2 + \epsilon_e^2}$$

where ϵ_g = gain drift error (ppm/°C)
ϵ_o = offset drift error (ppm of FSR/°C)
ϵ_e = linearity error (ppm of FSR/°C)

For unipolar operation, the total RSS drift is ±30.3ppm/°C and for bipolar operation, the total RSS drift is ±33.7ppm/°C.

ACCURACY VS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC80 are shown in Figures 3 and 4.

The ADC80 conversion speeds are specified for a maximum linearity error of ±½LSB and a differential linearity error of ±½LSB with the internal clock. Faster conversion speeds up to 23μs for 12 bits, 12μsec for 10 bits and 6μs for 8 bits are possible with an external clock (see page 5-18).

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect the accuracy of the ADC80. The ADC80 power supply sensitivity is specified for ±0.003% of FSR/%Vs for ±15V (±12V) supplies and ±0.0015% of FSR/%Vs for +5V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with the ADC80. See layout precautions and power supply decoupling on page 5-17.

LAYOUT and OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected internally in the ADC80 but should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC80. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. Analog and digital +5 volt supplies are also not connected internally; they should be connected together at the unit as shown below in Figure 7 (Pins 7 and 9).

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 7 to obtain noise free operation. These capacitors should be located close to the ADC80. 1μF electrolytic type capacitors should be bypassed with 0.01μF ceramic capacitors for improved high frequency performance.

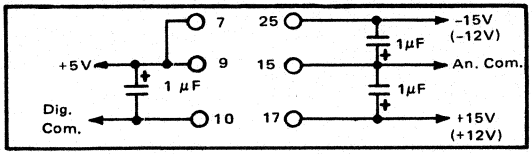


FIGURE 7. Recommended power supply decoupling.

INPUT SCALING

The ADC80 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 8 for circuit details.

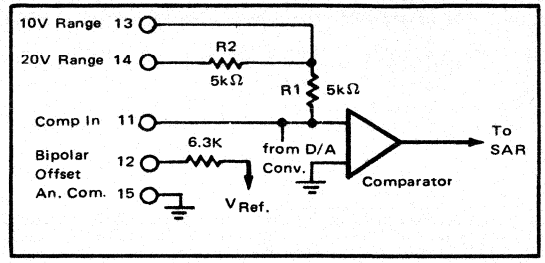


FIGURE 8. ADC80 Input scaling circuit.

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0 to +5V	CSB	15	Pin 11	13
0 to +10V	CSB	15	Open	13

TABLE II. ADC80 Input scaling connections.

Optional External Gain and Offset Adjustments

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC80 as shown in Figures 9 and 10. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10 kΩ to 100 kΩ. All resistors should be 20% carbon or better. Pin 16 (Gain Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET - Connect the OFFSET potentiometer as shown in Figure 9. Sweep the input through the end point transition voltage that should cause an output transition to all ones.

Adjust the OFFSET potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF} The ideal transition voltage values of the input are given in Table I.

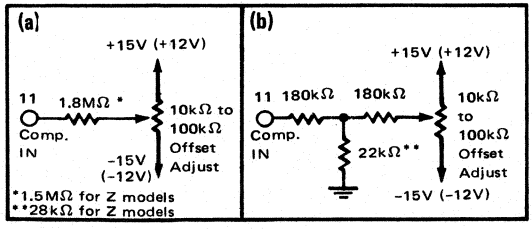


FIGURE 9. Two methods of connecting optional offset adjust with a 0.4% of FSR range of adjustment.

GAIN - Connect the GAIN adjust potentiometer as shown in Figure 10. Sweep the input through the end point transition voltage that should cause an output transition to all zeros.

Adjust the GAIN potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

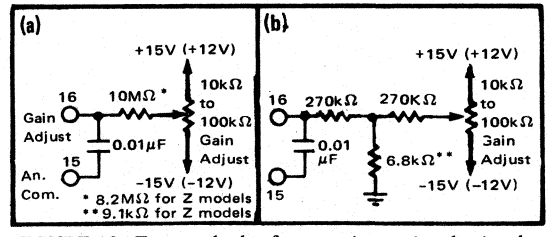


FIGURE 10. Two methods of connecting optional gain adjust with a 0.6% range of adjustment.

Clock Options

The ADC80 is extremely versatile in that it can be operated in several different modes with either internal or external clock. Most of these options can be implemented with nothing more than an inexpensive quad 2-input NAND gate (7400) as shown in Figures 11 through 14.

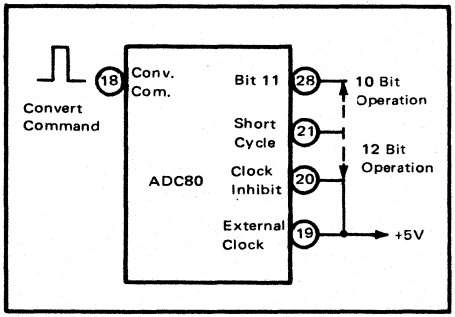


FIGURE 11. INTERNAL CLOCK – NORMAL OPERATING MODE. Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.

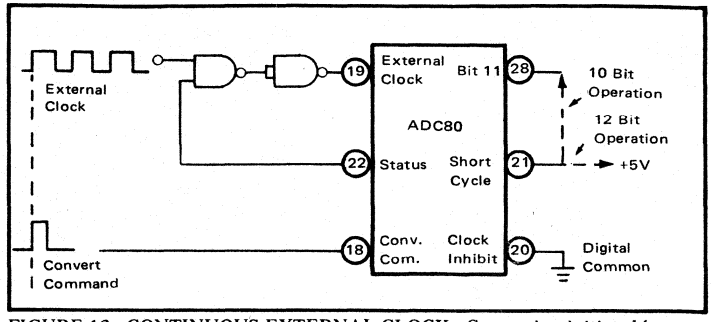


FIGURE 13. CONTINUOUS EXTERNAL CLOCK. Conversion initiated by rising edge of convert command. The convert command must be synchronized with clock.

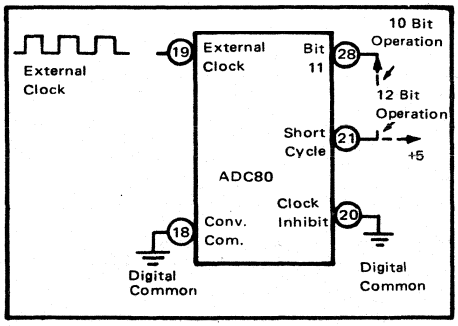


FIGURE 12. CONTINUOUS CONVERSION WITH EXTERNAL CLOCK. Conversion is initiated by 14th clock pulse. Clock runs continuously.

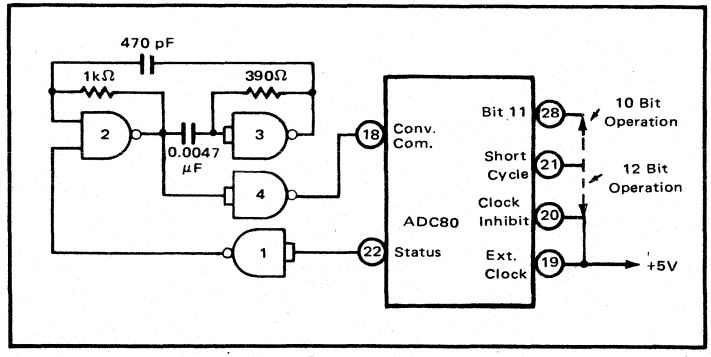


FIGURE 14. CONTINUOUS CONVERSION WITH INTERNAL CLOCK. Conversion is initiated by the 14th clock pulse. Clock runs continuously. The oscillator formed by gates 2 and 3 insures that the conversion process will start when logic power is first turned on.

Short Cycle Feature

The ADC80 may be operated at faster speeds for resolutions less than 10 or 12 bits, depending on the model selected, by connecting the short cycle pin, pin 21, as shown in Table III. Conversion speeds, linearity, and resolutions are shown for reference.

RESOLUTION (BITS)	12	10	8
Connect Pin 21 to	Pin 9	Pin 26	Pin 30
Maximum Conversion Time(1)			
Internal Clock (μsec)	25	22	18
External Clock (μsec)	23	12	6
Maximum Nonlinearity At +25°C (% of FSR)	0.012(2)	0.048(3)	0.20(3)

NOTES: (1) Max conversion time to maintain ±½LSB Nonlinearity error.
(2) 12 Bit Models only.
(3) 10 or 12 Bit Models.

TABLE III. Short cycle connections and resolutions for 8 to 12 bit resolutions - ADC80.

Output Drive

Normally all ADC80 logic outputs will drive 2 standard TTL loads; however if long digital lines must be driven, external logic buffers are recommended.

APPLICATIONS

LOW COST
DATA ACQUISITION
SYSTEM

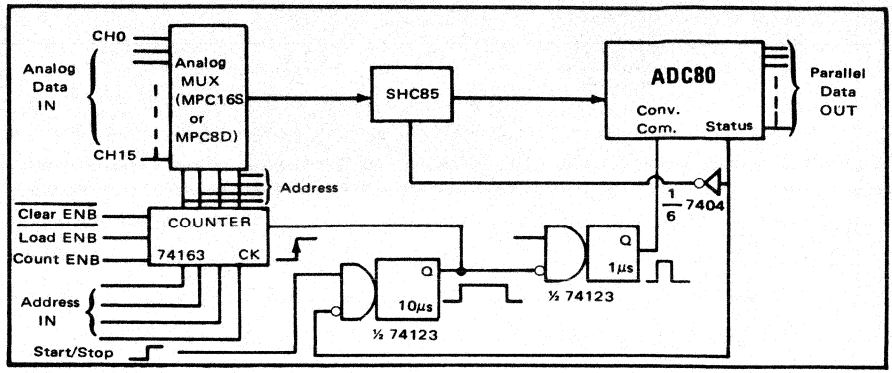


FIGURE 15. Low Cost Data Acquisition System.

ZERO DROOP SAMPLE/HOLD

A zero droop - infinite hold sample/hold can be constructed with the ADC80 with the circuit shown in Figure 16. A sample command will cause the relay to switch the analog input to the ADC80 input and also generate a convert command to the ADC80. The sample pulse width (T_A) should be greater than the combined switching and settling time of the relay and driver circuit and the ADC80 conversion time.

In the HOLD mode, the analog value can be held indefinitely with zero droop. The period of the first one-shot multivibrator must be equal to or greater than T_R, the switching time of the relay.

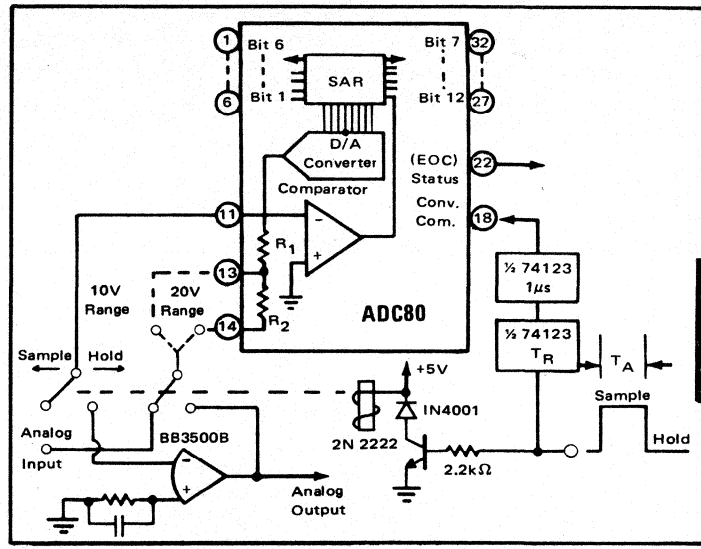


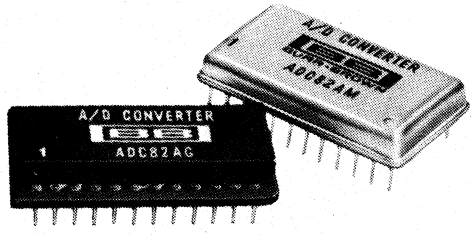
FIGURE 16. Zero Droop Infinite Hold Sample/Hold using ADC80 and a few external components.

ORDERING INFORMATION

ADC80AG – XX

A/D Converter family A = -25°C to +85°C G = Ceramic Package	Blank - ±14.0V to ±16.0V supply range Z - ±10.8V to ±16.0V Supply range	Resolution (No. of Bits) 10 = 10 Bits 12 = 12 Bits

BURR-BROWN



ADC82

IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **FAST CONVERSION SPEED - 2.8µsec, max**
  Throughput sampling rates of over 300kHz
  Faster conversion speeds obtainable with optional external clock
- **COMPLETELY SELF-CONTAINED - Internal clock, comparator, and reference**
- **ABSOLUTE ACCURACY - No external gain or offset adjustments are required for 0 to +10V or ±10V signal ranges**
- **PRECISION - ±1/2LSB maximum nonlinearity error**
- **COMPACT DESIGN - 24-pin ceramic or metal dual-in-line package**
- **LOW COST - Ceramic packaged ADC82AG**

DESCRIPTION

The model ADC82AG and ADC82AM are high-speed, 8-bit successive-approximation A/D converters designed for applications requiring system throughput sampling rates of over 300kHz. They utilize state-of-the-art IC and laser-trimmed thin-film components, and are packaged in a 24-pin ceramic (ADC82AG) or metal (ADC82AM) package.

Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V, or 0 to +20V.

No external adjustments are required to obtain initial absolute accuracies of better than ±1LSB for the 0 to +10V or ±10V signal ranges. Gain and offset errors may be externally trimmed to zero, to obtain even greater accuracy.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are DTL/TTL-compatible. Power supply voltages are ±15VDC and +5VDC.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-351B Printed in U.S.A. July, 1978

DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent QUANTIZATION ERROR of ±1/2 LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors, including GAIN, OFFSET, LINEARITY, DIFFERENTIAL LINEARITY and POWER SUPPLY SENSITIVITY. Initial GAIN and OFFSET errors may be adjusted to zero. GAIN drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits OFF) and OFFSET drift shifts the line left or right over the operating temperature range. LINEARITY error is unadjustable and is the most meaningful indicator of A/D converter accuracy. LINEARITY error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A DIFFERENTIAL LINEARITY error of ±1/2 LSB means that the width of each bit step over the range of the A/D converter is 1 LSB ±1/2 LSB.

The ADC82 is also MONOTONIC, assuring that the output digital code either increases or remains the same for increasing analog input signals. A monotonic converter can have missing codes; therefore, Burr-Brown specifies no missing codes over a temperature range.

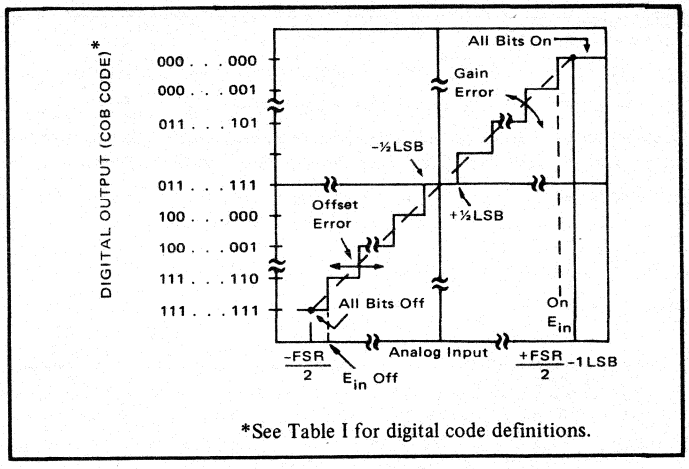


FIGURE 1. Input vs Output For An Ideal Bipolar A/D Converter.

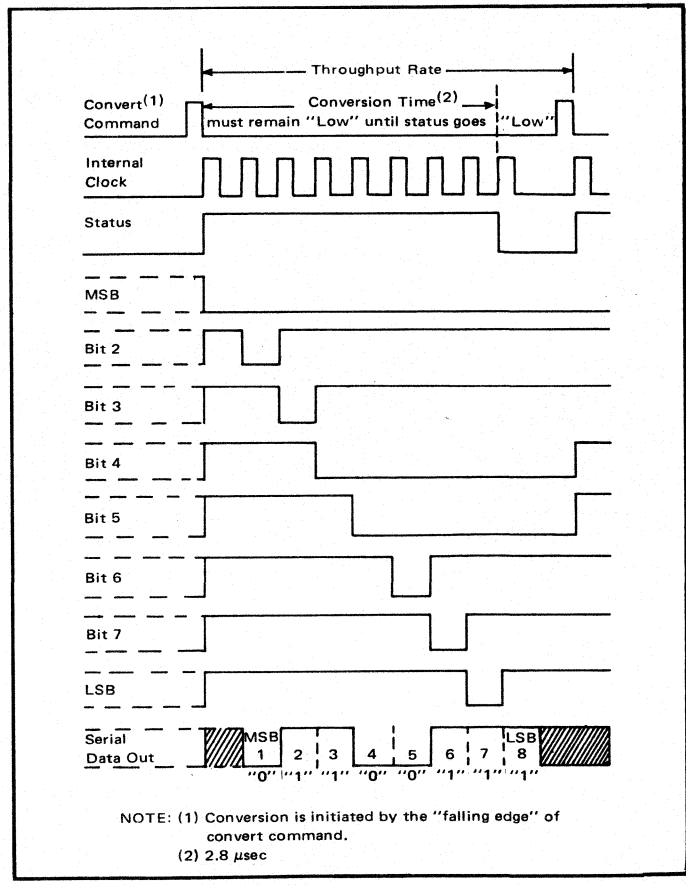


FIGURE 2. ADC82 Timing Diagram.

TIMING CONSIDERATIONS

The timing diagram of the ADC82 (Figure 2) assumes an analog input such that the positive true digital word 10011000 exists. The output will be complementary as shown in Figure 2 (01100111 is the digital output).

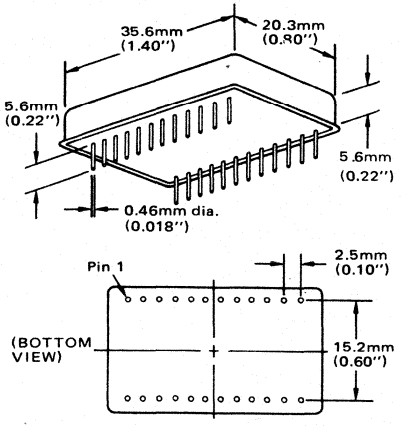
SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

ELECTRICAL

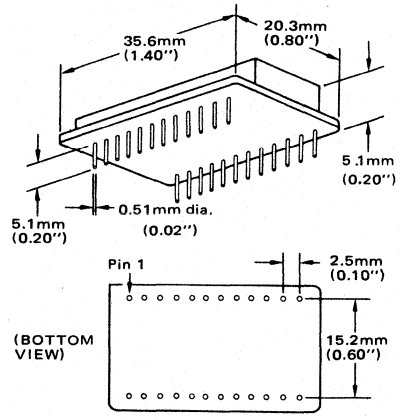
MODEL	ADC82AG	ADC82AM	UNITS
RESOLUTION	8		Bits
INPUT			
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±2.5, ±5, ±10		V
Unipolar	0 to +5, 0 to +10, 0 to +20		V
Impedance (Direct Inputs)			
0 to +5V, ±2.5V	3.125		kΩ
0 to +10V, ±5V	6.25		kΩ
0 to +20V, ±10V	12.50		kΩ
DIGITAL INPUTS(1)			
Convert Command	Positive pulse 50ns wide (min) trailing edge ("1" to "0") initiates conversion		
Logic Loading	1		TTL Load
External Clock	1		TTL Load
TRANSFER CHARACTERISTICS			
ERROR			
Total Accuracy Error (max)	±1		LSB
Gain Error(3)	±0.1		%
Offset Error(3)			
Unipolar	±0.05		% of FSR(2)
Bipolar	±0.05		% of FSR
Linearity Error (max)(4)	±0.2		% of FSR
Inherent Quantization Error	±½		LSB
Differential Linearity Error	±½		LSB
No Missing Codes Temp. Range	0 to 70		°C
Power Supply Sensitivity			
+15V	±0.02		% of FSR/%Vs
+5V and -15V	±0.006		% of FSR/%Vs
DRIFT			
Specification Temp. Range	-25 to +85		°C
Gain, (max)	±40		ppm/°C
Offset			
Unipolar	±20		ppm of FSR/°C
Bipolar, (max)	±35		ppm of FSR/°C
Linearity, (max)	±20		ppm of FSR/°C
Monotonicity	Guaranteed		
CONVERSION SPEED (max)5	2.8		μsec
OUTPUT			
DIGITAL DATA (All codes complementary)			
Parallel			
Output Codes(6)			
Unipolar	CSB		
Bipolar	COB, CTC		
Output Drive	5		TTL Loads
Serial Data Codes (NRZ)	CSB, COB		
Output Drive	5		TTL Loads
Status	Logic "1" during conversion		
Status Output Drive	5		TTL Loads
Internal Clock			
Clock Output Drive	4		TTL Loads
Frequency(7)	2.85		MHz
POWER REQUIREMENTS			
Rated Voltages	±15, +5		V
Range for Rated Accuracy(8)	+4.75 to +5.25, ±14.5 to ±15.5		V
Supply Drain +15V	+20		mA
-15V	-20		mA
+5V	+80		mA
TEMPERATURE RANGE			
Specification	-25 to +85		°C
Operating (derated specs)	-55 to +100		°C
Storage	-55 to +125		°C

MECHANICAL ADC82AM



CASE: Kovar, Gold Plated
Mating Connector 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
WEIGHT: 8 grams, (0.28 oz.)

ADC82AG



CASE: Black Ceramic
Mating Connector 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
WEIGHT: 7 grams, (0.25 oz.)

1) DTL/TTL compatible i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V min.
2) FSR means Full Scale Range – for example, unit connected for ±10V range has 20V FSR.
3) Adjustable to zero with external trimpots.
4) Error shown is the same as ±½LSB max for resolution of A/D converter.
5) Conversion time with internal clock.
6) See Table I. CSB – Complementary Binary. COB – Complementary Offset Binary. CTC – Complementary Two's Complement.
7) For conversion speeds specified.
8) ±14.0V to ±16.0V for ±1¼LSB total accuracy error.

TYPICAL PERFORMANCE CURVES

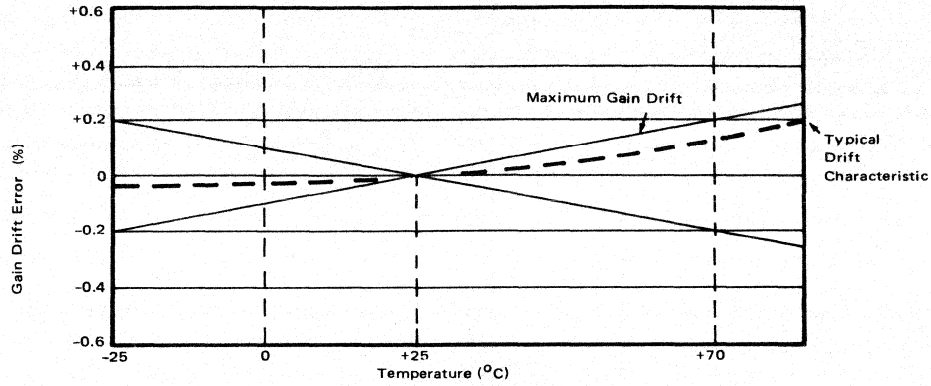


FIGURE 3. Gain Drift Error (%) vs. Temperature.

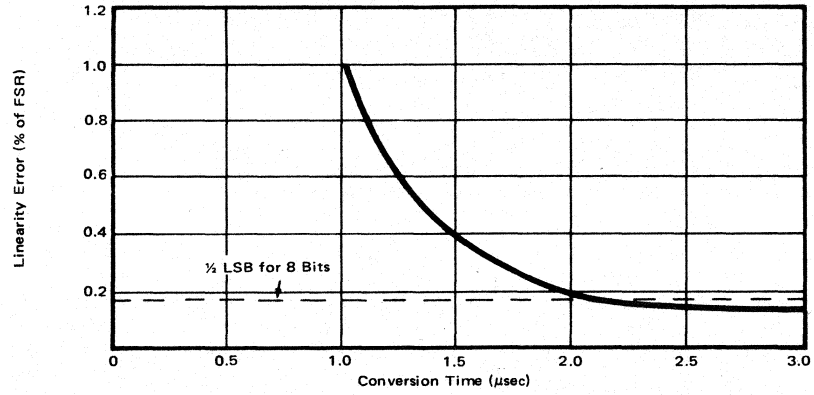


FIGURE 4. Linearity Error vs. Conversion Time.

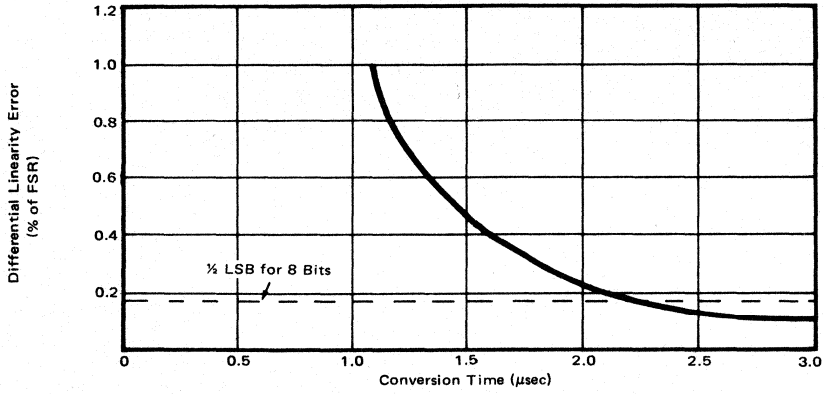
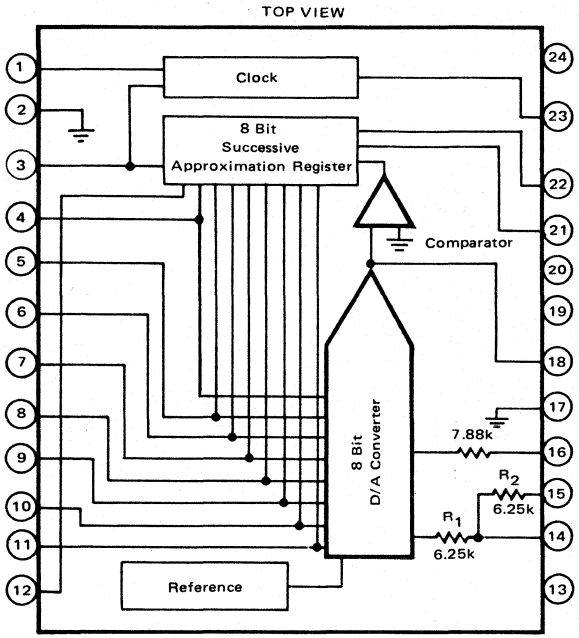


FIGURE 5. Differential Linearity Error vs. Conversion Time.



Pin Connections

1. Clock Out
2. Digital Common *
3. Status
4. Bit 8 (LSB)
5. Bit 7
6. Bit 6
7. Bit 5
8. Bit 4
9. Bit 3
10. Bit 2
11. Bit 1 (MSB)
12. $\overline{\text{Bit 1 (MSB)}}$
13. Gain Adjust
14. R_1 (10V Range)
15. R_2 (20V Range)
16. Bipolar Offset
17. Analog Common
18. Comparator Input
19. +15V
20. -15V
21. Serial Out
22. Clock In
23. Convert Command
24. +5V

* Internally connected to case on ADC82AM

DEFINITION OF DIGITAL CODES

PARALLEL DATA

Three binary codes are available on the ADC82 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary two's complement (CTC) and complementary offset binary (COB) for bipolar input signal ranges.

Table I describes the LSB, transition values and code definitions for each possible ADC82 analog input signal range.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line of the ADC82; they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occuring first. The serial data is snychronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Ranges	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB or CTC*	COB or CTC*	COB or CTC*	CSB**	CSB**	CSB**
One Least Significant Bit (LSB)	FSR / 2^n	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV	78.13mV
Transition Values							
MSB LSB							
000 . . . 000***	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111 . . . 110	-Full Scale	-10V +½LSB	-5V +½LSB	-2.5V +½LSB	0 + ½LSB	0 + ½LSB	0 + ½LSB

* COB = Complementary Offset Binary
** CSB = Complementary Straight Binary
*CTC = Complementary Two's complement - obtained by using the complement of the most significant bit ($\overline{\text{MSB}}$). $\overline{\text{MSB}}$ is available on pin 12.
*** Ø is the Transition Bit. Voltages given are the nominal value for transition to the code specified.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

DISCUSSION OF SPECIFICATIONS

The ADC82 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. The ADC82 is factory trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial gain and offset errors are factory trimmed to ±0.05% of FSR at +25°C for both the 0 to +10 and ±10V ranges. No external adjustment is required to obtain initial absolute accuracies of ±1 LSB. When using one of the other input signal ranges or when even greater initial accuracy is desired these errors may be trimmed to zero by connecting external potentiometers as shown on in Figures 12 and 13.

ACCURACY DRIFT VS TEMPERATURE

Three major dirft parameters degrade A/D converter accuracy over temperature; they are gain, offset and linearity drift. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum-squared (RSS) or lo errors as follows:

$$RSS = \sqrt{\epsilon_g^2 + \epsilon_o^2 + \epsilon_e^2}$$

Where ϵ_g = gain drift error (ppm/°C)

ϵ_o = offset drift error (ppm of FSR/°C)

ϵ_e = linearity error (ppm of FSR/°C)

For unipolar operation, the total RSS drift is ±49.0 ppm/°C and for bipolar operation, the total RSS drift is ±56.8 ppm/°C.

ACCURACY VS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC82 are shown in Figures 3 and 4.

The ADC82 conversion speeds are specified for a maximum linearity error of ±½ LSB and a differential linearity error of ±½ LSB with the internal clock. Faster conversion speeds are possible with an external clock (see Figures 9 and 10).

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect the accuracy of the ADC82. The ADC82 power supply sensitivity is specified for ±0.006% of FSR/%Vs for -15V and +5V supplies and ±0.02% of FSR/%Vs for +15V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with the ADC82. See layout precautions and power supply decoupling below.

LAYOUT & OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected internally in the ADC82 but should be connected together as close to the unit as possible, perferably to a large ground plane under the ADC82. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 6 to obtain noise free operation. These capacitors should be located close to the ADC82. 1μF electrolytic type capacitors should be bypassed with 0.01μF ceramic capacitors for improved high frequency performance.

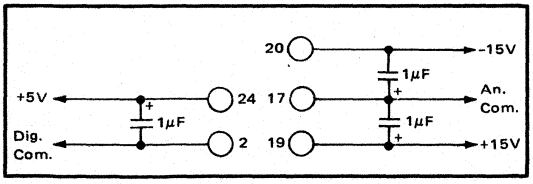


FIGURE 6. Recommended Power Supply Decoupling.

INPUT SCALING

The ADC82 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 7 for circuit details.

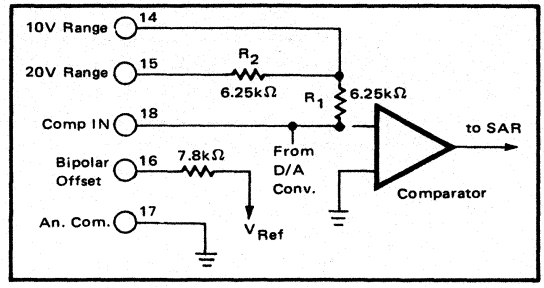


FIGURE 7. ADC82 Input Scaling Circuit.

Input Signal Range	Output Code	Connect Pin 16 To Pin	Connect Pin 15 to	Connect Input Signal to
±10V	COB or CTC	18	Input Signal	15
± 5V	COB or CTC	18	Open	14
±2.5V	COB or CTC	18	Pin 18	14
0 to +5V	CSB	17	Pin 18	14
0 to +10V	CSB	17	Open	14
0 to +20V	CSB	17	Input Signal	15

TABLE II. ADC82 Input Scaling Connection.

Clock Options

The ADC82 is extremely versatile in that it can be operated in several different modes with either internal or external clock. Most of these options can be implemented with nothing more than an inexpensive quad 2-input NAND Gate (7400) as shown in Figure 8 through 11.

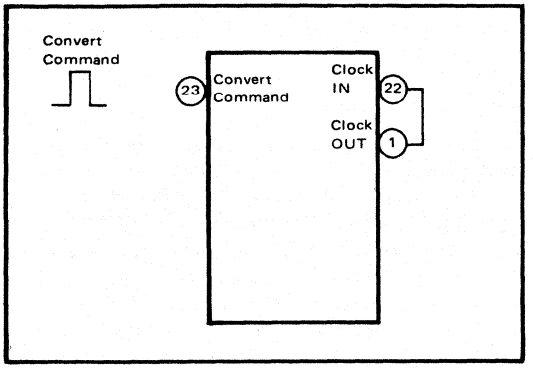


FIGURE 8. INTERNAL CLOCK-NORMAL OPERATING MODE. Conversion initiated by falling edge of the convert command. The internal clock runs only during conversion.

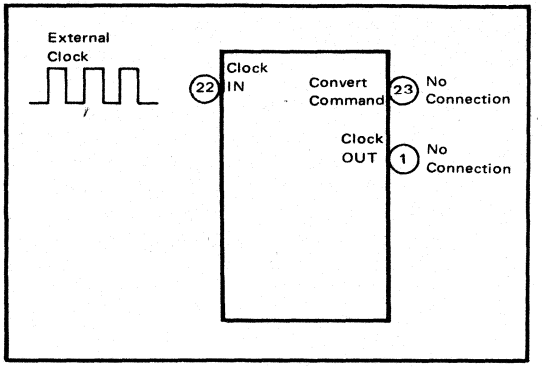


FIGURE 9. CONTINUOUS CONVERISON WITH EXTERNAL CLOCK. Conversion is initiated by 10th clock pulse. Clock runs continuously.

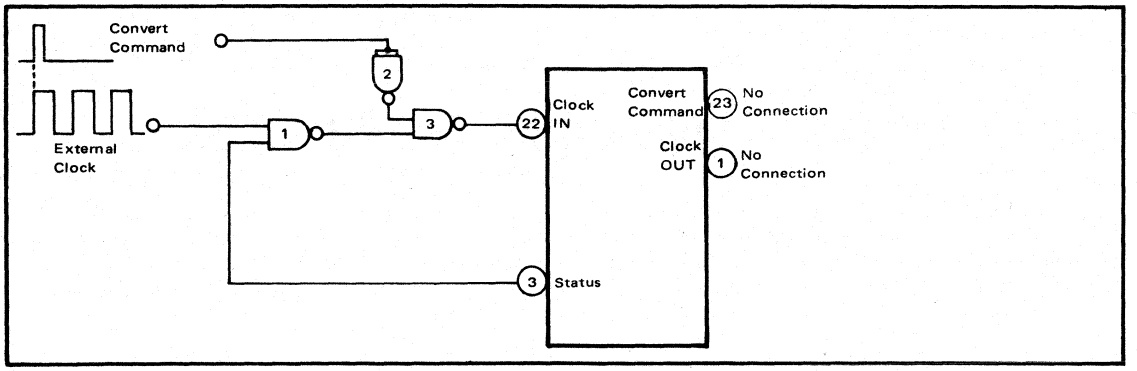


FIGURE 10. CONTINUOUS EXTERNAL CLOCK. Conversion initiated by rising edge of Convert Command. The convert command must be synchronized with clock. Convert command must be low during conversion.

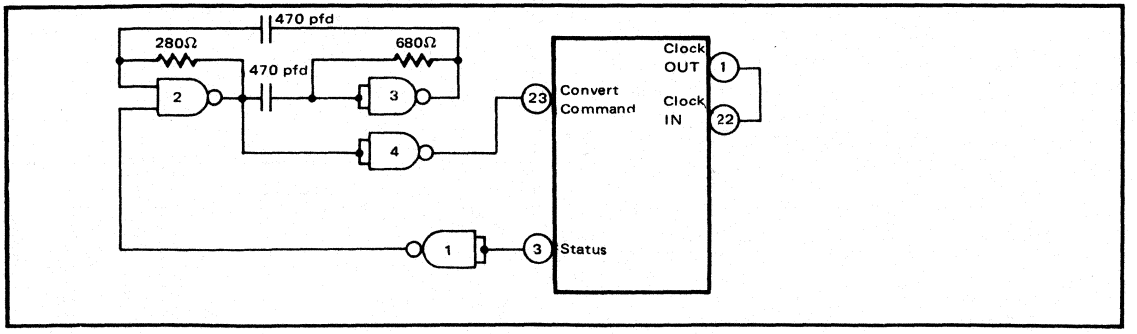


FIGURE 11. CONTINUOUS CONVERSION WITH INTERNAL CLOCK. Conversion is initiated by the 10th clock pulse. Clock runs continuously. The oscillator formed by Gates 2 and 3 insure that the conversion process will start when logic power is first turned on. (These values give a 200 nsec convert command).

Optional External Gain and Offset Adjustments

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC82 as shown in Figures 11 and 12. Multiturn potentiometers with 100 ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 13 (Gain Adjust) may be left open of no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET – Connect the OFFSET potentiometer as shown in Figure 12. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the OFFSET potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

GAIN – Connect the GAIN adjsut potentiometer as shown in Figure 13. Sweep the input through the end point transition voltage that should cause output transitions to all bits on (E_{IN}^{ON}). Adjust the GAIN potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}

TABLE I details the transition voltage levels required.

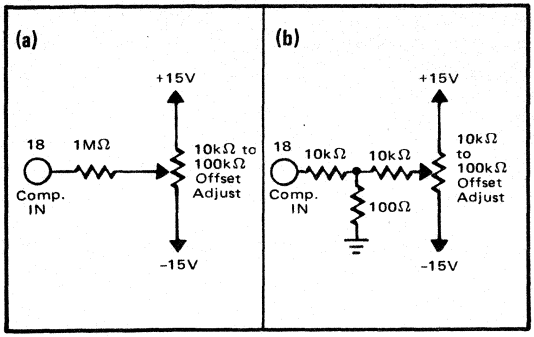


FIGURE 12. Two methods of connecting optional offset adjust with a ±1.0% of FSR range of adjustment.

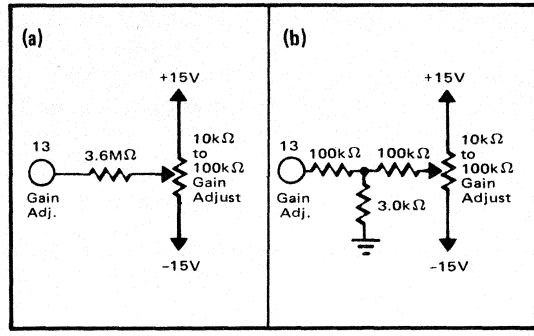


FIGURE 13. Two methods of connecting optional gain adjust with a ±1.0% range of adjustment.

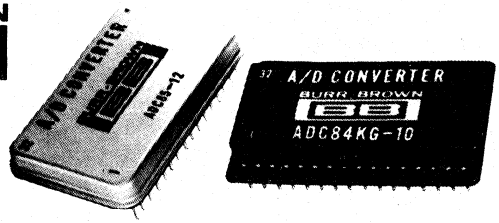
ORDERING INFORMATION

ADC82 A X

A/D Converter Family
A = 25°C to +85°C

G = Ceramic Package
M = Metal Hermetic Package

BURR-BROWN



ADC84
ADC85

IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **COMPACT DESIGN - Self-contained with internal clock, comparator, reference, and input buffer amplifier 32-pin ceramic or hermetic metal package**
- **FAST CONVERSION SPEEDS**
  Provide Fast Signal Sampling Rates
  12-bits - 10μsec, 10-bits - 6μsec
  Faster conversion speeds obtainable with "Short-Cycling" and adjustable clock rate
- **LOW COST - ADC84KG-12**

DESCRIPTION

The ADC84 and ADC85 families of 10- and 12-bit analog-to-digital converters utilize state-of-the-art IC and laser-trimmed thin-film components, and are packaged in compact 32-pin dual-in-line packages.

Complete with internal reference and input buffer amplifier, they offer versatility and performance formerly offered only in larger modular or rack-mount packages.

Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V or 0 to +10V. Gain and offset errors may be externally trimmed to zero, offering initial accuracies of better than ±0.012% (±1/2LSB).

The fast conversion speeds of 10μsec for 12-bit and 6μsec for 10-bit resolution make these ADC's excellent for a wide range of applications where system throughput sampling rates from 100kHz to 120kHz are required. In addition, they may be short cycled and the clock rate control may be used to obtain faster conversion speeds at low resolutions.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are DTL/TTL-compatible. Power supply voltages are ±15VDC and +5VDC.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-355A Printed in U.S.A. July, 1978

DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent QUANTIZATION ERROR of ±1/2 LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including GAIN, OFFSET, LINEARITY, DIFFERENTIAL LINEARITY and POWER SUPPLY SENSITIVITY. Initial GAIN and OFFSET errors may be adjusted to zero. GAIN drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits OFF) and OFFSET drift shifts the line left or right over the operating temperature range. LINEARITY error is unadjustable and is the most meaningful indicator of A/D converter accuracy. LINEARITY error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A DIFFERENTIAL LINEARITY error of ±1/2 LSB means that the width of each bit step over the range of the A/D converter is 1 LSB ±1/2 LSB.

The ADC84 and ADC85 are also MONOTONIC, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that these converters will have no missing codes over a specified temperature range.

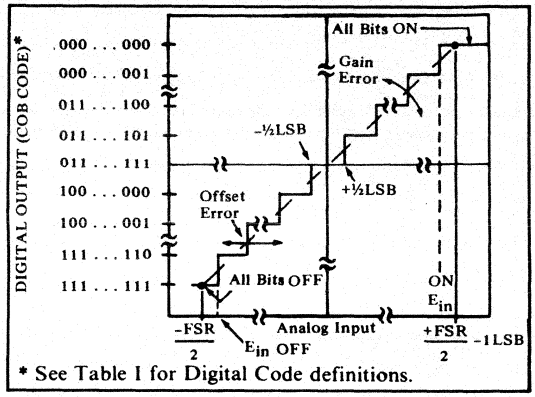


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram of the ADC's (Figure 2) assumes an analog input such that the positive true digital word 100110001001 exists. The output will be complementary as shown in Figure 2 (011001110110 is the digital output).

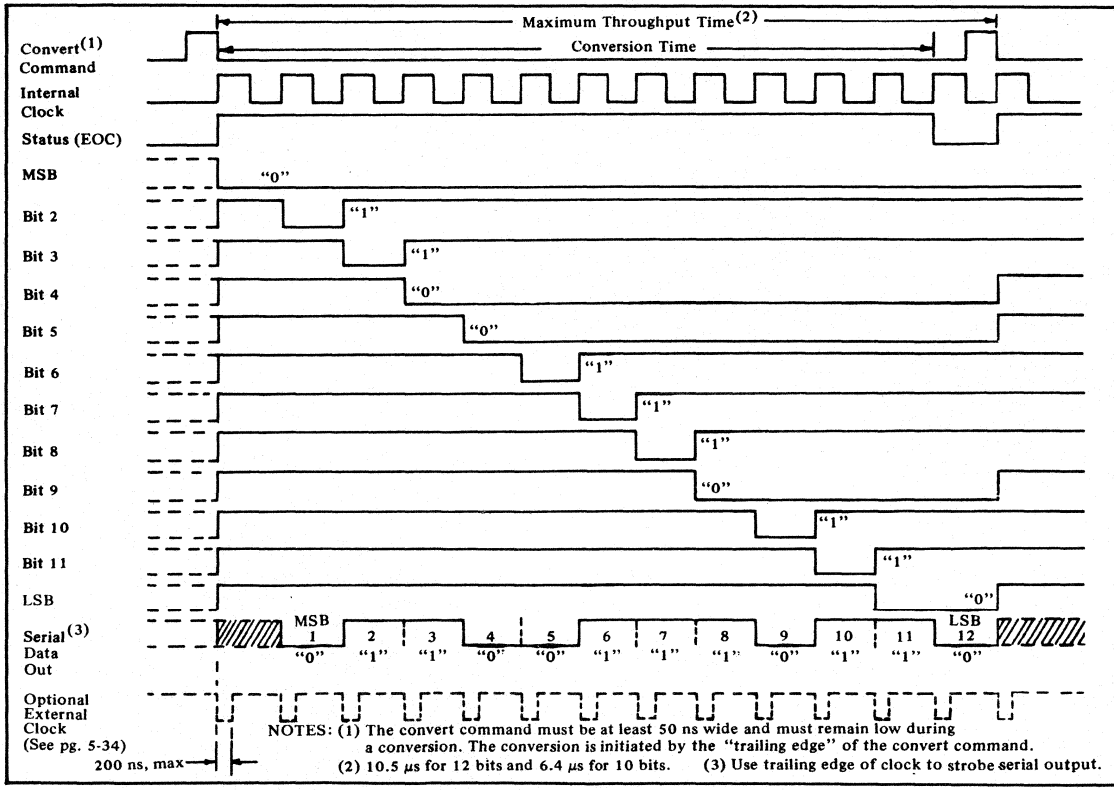


FIGURE 2. ADC84 and ADC85 Timing Diagram

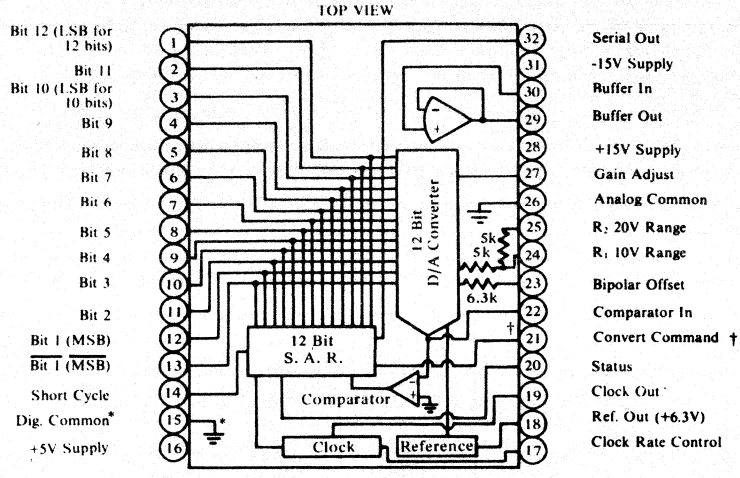
ELECTRICAL SPECIFICATIONS

(Typical at 25°C and rated power supplies otherwise noted.)

MODEL	ADC85		ADC85C		ADC84KG		UNITS
RESOLUTION	10	12	10	12	10	12	BITS
INPUT							
ANALOG INPUTS							
Voltage Ranges							
Bipolar			±2.5, ±5, ±10				Volts
Unipolar			0 to +5, 0 to +10				Volts
Impedance (Direct Input)							
0 to +5V, ±2.5V			2.5				kΩ
0 to +10V, ±5V			5				kΩ
±10V			10				kΩ
Buffer Amplifier							
Impedance (min)			100				Meg Ω
Bias Current			50				nA
Settling Time							
to 0.01% for 20V step[1]			2				μs
DIGITAL INPUTS[2]							
Convert Command			Positive Pulse 50ns wide (min) Trailing Edge ("1" to "0" initiates conversion)				
Logic Loading			1				TTL Load
External Clock			See Page 5-34				
TRANSFER CHARACTERISTICS							
ERROR							%
Gain Error			±0.1 (Adjustable to zero)				
Offset Error			Adjustable to zero				% of FSR[3]
Unipolar			±0.05				% of FSR
Bipolar			±0.1				% of FSR
Linearity Error (max)[4]	±0.048	±0.012	±0.048	±0.012	±0.048	±0.012	LSB
Inherent Quantization Error			±1/2				LSB
Differential Linearity Error			±1/2				LSB
No Missing Codes	-25 to +85	0 to +50	0 to +70	0 to +50	0 to +70	0 to +50	°C
Power Supply Sensitivity							
±15V			±0.004				% of FSR/%V_S
+5V			±0.001				% of FSR/%V_S
DRIFT							
Specification Temperature Range	-25 to +85		0 to +70		0 to +70		°C
Gain, (max)	±20	±15	±40	±25	±30		ppm/°C
Offset							
Unipolar	±3	±3	±3	±3	±3	±3	ppm of FSR/°C
Bipolar, (max)	±10	±7	±20	±12	±15	±15	ppm of FSR/°C
Linearity, (max)	±3	±2	±3	±3	±3	±3	ppm of FSR/°C
Monotonicity			GUARANTEED				
CONVERSION SPEED (max)[5][6]	6	10	6	10	6	10	μsec
OUTPUT							
DIGITAL DATA							
(All codes complementary)							
Parallel							
Output Codes[7]							
Unipolar			CSB				
Bipolar			COB, CTC				
Output Drive			2				TTL Loads
Serial Data Codes (NRZ)			CSB, COB				
Output Drive			2				TTL Loads
Status			Logic "1" during conversion				
Status Output Drive			2				TTL Loads
Internal Clock							
Clock Output Drive			2				TTL Loads
Frequency[6]	1.9	1.35	1.9	1.35	1.9	1.35	MHz
INTERNAL REF. VOLTAGE			6.3				Volts
Max External Current With no degration of Specifications			200				μA
Tempco of Drift, max	±5	±5	±10	±10	±20	±20	ppm/°C
POWER REQUIREMENTS							
Rated Voltages			±15, +5				Volts
Range for Rated Accuracy			4.75 to 5.25 and ±14.5 to ±15.5				Volts
Supply Drain +15V			+45		+45		mA
-15V			-35		-35		mA
+5V			+120		+70		mA
TEMPERATURE RANGE							
Specification	-25 to +85		0 to +70		0 to +70		°C
Operating (derated specs)			-55 to +85 (110°C case Temp.)				°C
Storage	-55 to +125		-55 to +125		-55 to +125		°C
PACKAGE (see page 5-35)	Metal (Hermetic)				Ceramic		

1. This settling time adds to conversion speed when buffer is connected to input.
2. DTL/TTL compatible; i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V, min for inputs. For digital outputs, Logic "0" = +0.4V max, Logic "1" = 2.4V, min.
3. FSR means Full Scale Range - for example, unit connected for ±10V range has 20V FSR.
4. Error shown is the same as ±1/2 LSB max linearity error in % of FSR.
5. Conversion time may be shortened with "short cycle" set for lower resolution, see page 5-34.
6. Internal Clock is externally adjustable, see page 5-34.
7. See Table II.
   CSB - Complementary Straight Binary
   COB - Complementary Offset Binary
   CTC - Complementary Two's Complement

CONNECTION DIAGRAM



* Digital Common is internally connected to case. (ADC85 and ADC85C only)
† If an external clock is used, connect the clock to Pin 21 (conv. command). (See Figure 2 and 5-33).

TYPICAL PERFORMANCE CURVES

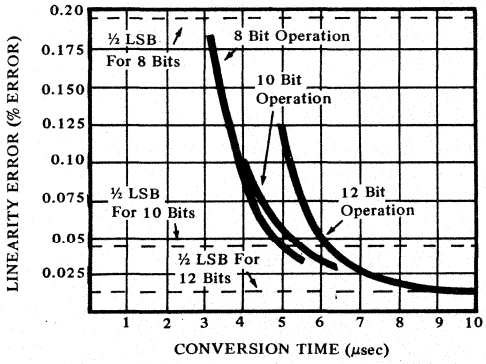


FIGURE 3. Linearity Error vs. Conversion Speed.

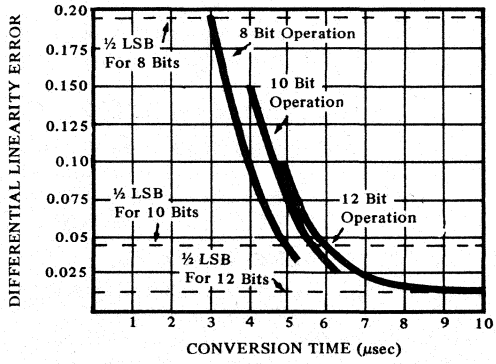


FIGURE 4. Differential Linearity vs. Conversion Speed.

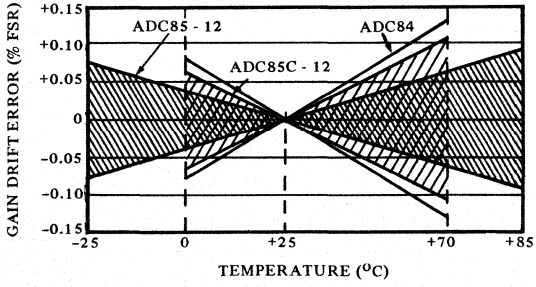


FIGURE 5. Gain Drift Error (% FSR) vs. Temp.

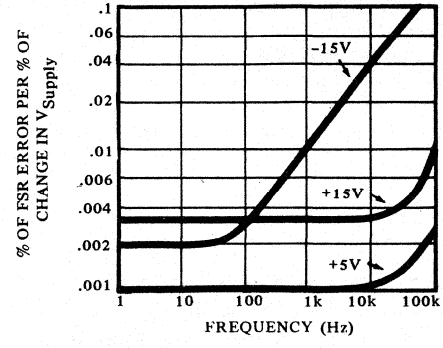


FIGURE 6. Power Supply Rejection vs. Power Supply Ripple Frequency.

DEFINITION OF DIGITAL CODES

PARALLEL DATA

Three binary codes are available on the ADC84 and ADC85 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary two's complement (CTC) and complementary offset binary (COB) for bipolar input signal ranges.

Table I describes the LSB, transition values and code definitions for each possible analog input signal range for 8, 10 and 12 bit resolutions.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line; they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES					
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB* or CTC***	COB* or CTC***	COB* or CTC***	CSB**	CSB**
One Least Significant Bit (LSB)	FSR	20V	10V	5V	10V	5V
	2^n	2^n	2^n	2^n	2^n	2^n
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000 ... 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 ... 111	Mil Scale	0	0	0	+5V	+2.5V
111 ... 110	-Full Scale	-10V + 1/2LSB	-5V + 1/2LSB	-2.5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

*COB = Complementary Offset Binary
**CSB = Complementary Straight Binary
***CTC = Complementary, Two's complement - obtained by using the complement of the most significant bit (MSB). MSB is available on pin 13.
****Voltages given are the nominal value for transition to the code specified.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

DISCUSSION OF SPECIFICATIONS

The ADC84 and ADC85 are specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors and conversion speed effects on accuracy. These ADC's are factory trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial GAIN and OFFSET errors are factory trimmed to ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown on page 5-33.

ACCURACY DRIFT VS TEMPERATURE

Three major drift parameters degrade A/D converter accuracy over temperature; they are gain, offset and linearity drift. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum-squared (RSS) or 1σ errors as follows:

$$RSS = \sqrt{\epsilon g^2 + \epsilon o^2 + \epsilon e^2}$$

where ϵg = gain drift error (ppm/°C)

ϵo = offset drift error (ppm of FSR/°C)

ϵe = linearity error (ppm of FSR/°C)

For the ADC85-12 operating in the unipolar mode the total RSS drift is ±15.42ppm/°C and for bipolar operation the total RSS drift is ±16.7ppm/°C.

ACCURACY VS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC84 and ADC85 are shown in Figures 3 and 4.

The conversion speeds are specified for a maximum linearity error of ±1/2 LSB with the internal clock. Faster conversion speeds are possible with optional clock rate control (see page 5-34).

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The ADC84 and the ADC85 power supply sensitivity is specified for ±0.003% of FSR/%Vs for ±15V supplies and ±0.0015% of FSR/%Vs for +5V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with these ADC's. See layout precautions and power supply decoupling on page 5-33.

LAYOUT and OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected internally in the ADC84 and ADC85, but should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 7 to obtain noise free operation. These capacitors should be located close to the ADC. 1 μF electrolytic type capacitors should be bypassed with 0.01 μF ceramic capacitors for improved high frequency performance.

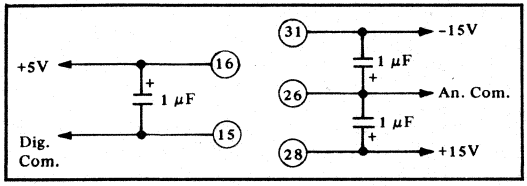


FIGURE 7. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 8 for circuit details.

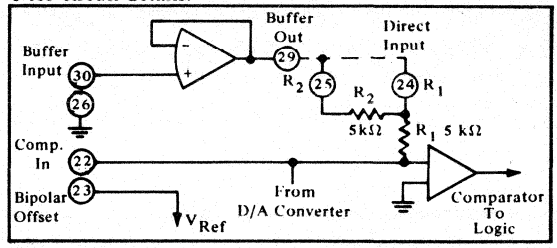


FIGURE 8. Input Scaling Circuit - ADC84 and ADC85.

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Buffered Input* Connect Pin 29 To Pin	For Direct Input (see note) Connect Input Signal To Pin
±10V	COB or CTC	22	Input Signal**	25	25
±5V	COB or CTC	22	Open	24	24
±2.5V	COB or CTC	22	Pin 22	24	24
0 to +5V	CSB	26	Pin 22	24	24
0 to +10V	CSB	26	Open	24	24

* Connect to Pin 29 or input signal as shown in next two columns.
** The input signal is connected to Pin 30 if the buffer amplifier is used.
NOTE: If the buffer amplifier is not used, the input Pin 30 must be grounded (Pin 26).

TABLE II. ADC84 and ADC85 Input Scaling Connections.

Optional External Gain and Offset Adjustments

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 9 and 10. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10 kΩ to 100 kΩ. All resistors should be 20% carbon or better. Pin 27 (Gain Adjust) and Pin 22 (Offset Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET - Connect the OFFSET potentiometer as shown in Figure 9. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the OFFSET potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

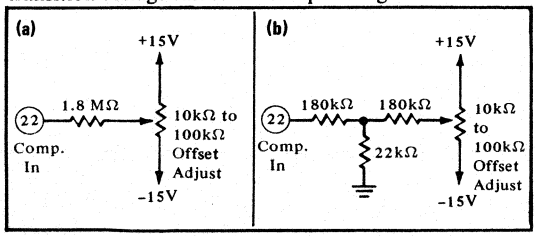


FIGURE 9. Two methods of connecting optional offset adjust with a 0.4% of FSR range of adjustment.

GAIN - Connect the GAIN adjust potentiometer as shown in Figure 10. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the GAIN potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

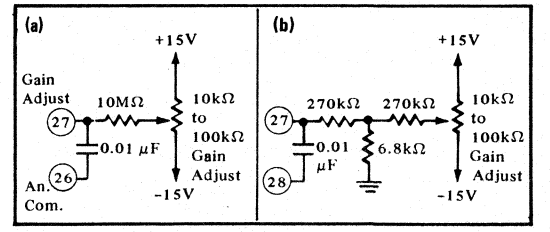


FIGURE 10. Two methods of connecting optional gain adjust with a 0.6% range of adjustment.

CLOCK RATE CONTROL ALTERNATE CONNECTIONS

If adjustment of the CLOCK RATE is desired for faster conversion speeds, the CLOCK RATE CONTROL may be connected to an external multi-turn trim potentiometer with a TCR of ±100ppm/°C or less as shown in Figures 11A and 11B. If the potentiometer is connected to -15V, conversion time can be increased as shown in Figure 12. If these adjustments are used, delete the connections shown in Table III for pin 17. See Figure 3 for nonlinearity error vs. clock frequency, and Figure 12 for the effect of the control voltage on clock speed.

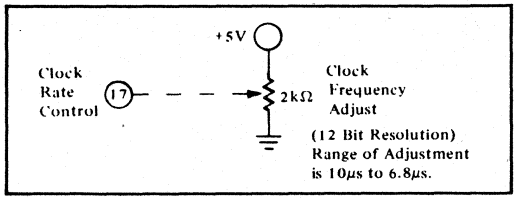


FIGURE 11A. 12 Bit Clock Rate Control Optional Fine Adjust.

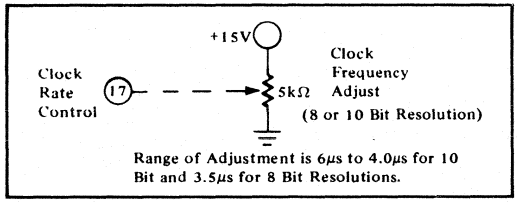


FIGURE 11B. 8 Bit Clock Rate Control Optional Fine Adjust.

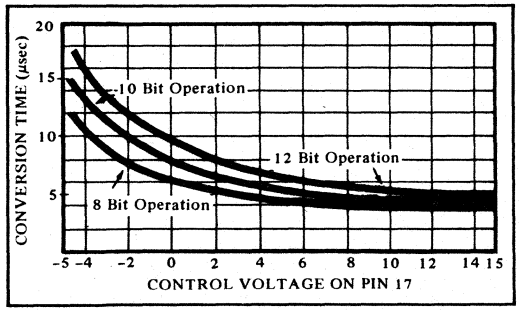


FIGURE 12. Conversion Time vs Clock Speed Control Voltage.

EXTERNAL CLOCK

If an external clock is used, connect the external clock to convert command, pin 21. The convert command shown in Figure 2 is not used. After each conversion is completed, a new conversion cycle will automatically start on the first falling edge of the external clock following the completion of conversion. The clock out signal will remain as shown in Figure 2 even if an external clock is used. The external clock pulse must be a negative going pulse with a width between 100 and 200 nanoseconds as shown in Figure 2.

ADDITIONAL CONNECTIONS REQUIRED

The ADC84 and ADC85 may be operated at faster speeds for resolutions less than 12 or 10 bits depending on the model selected, by connecting the SHORT CYCLE input, pin 14, as shown in Table III. Conversion speeds, linearity and resolutions are shown for reference:

Resolution (Bits)	12	10	8
Connect Pin 17 to[1]	Pin 15	Pin 16	Pin 28
Connect Pin 14 to	Pin 16	Pin 2	Pin 4
Maximum Conversion Speed (μsec)[2]	10	6	4
Maximum Nonlinearity at 25°C (% of FSR)	0.012[3]	0.048[4]	0.20[4]

TABLE III. Short cycle connections and specifications for 8 to 12 bit resolutions

Notes:

(1) Connect only if clock rate control is not used.
(2) Max. conversion speeds to maintain ±1/2 LSB nonlinearity error.
(3) 12 bit models only.
(4) 10 or 12 bit models.

OUTPUT DRIVE

Normally all ADC84 and ADC85 logic outputs will drive 2 standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

HEAT DISSIPATION

The ADC84 and ADC85 dissipate approximately 1.2W and the packages have a case-to-ambient thermal resistance (Θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. See Figure 13 for Θ_{CA} requirement above 70°C. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the case can be achieved using a silicone heat sink compound. On a .062 inch thick PC card with 16 square inch min. area, this technique will allow operation to 85°C.

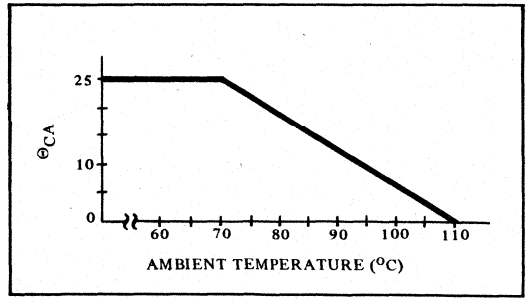


FIGURE 13. Θ_{CA} Requirement Above 70°C.

HIGH RELIABILITY A/D CONVERTERS

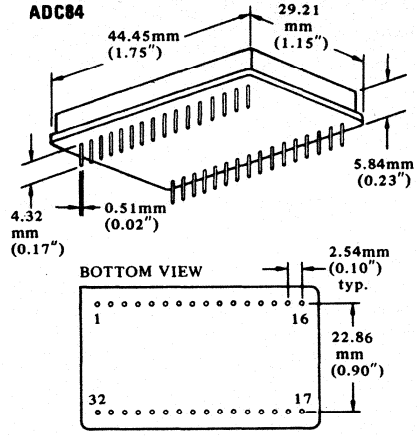
Each of the ADC85 models are available screened to the requirements of the Burr-Brown Q Program, which consists of a sequence of thermal and mechanical stress procedures, plus a verification of package hermeticity. The diagram below illustrates the screening sequence which is applied to 100% of the Q screened A/D converters.

High Temp. Storage (Mil-Std-883)	Temperature Cycling (Mil-Std-883)	Hermeticity Gross Leak (Mil-Std-883)	Hermeticity Fine Leak (Mil-Std-883)	Burn-In (Mil-Std-883)	Centrifuge (Mil-Std-883)
Method 1008 Condition B +125°C, 24 Hours	Method 1010 Condition B -55°C to +125°C 10 Cycles	Method 1014 Condition C Step 1 Fluorocarbon	Method 1014 Condition A Helium 5×10^{-7} cc/sec	Method 1015 Condition D 168 Hours +70°C (ADC85C) +85°C (ADC85)	Method 2001 2,000 G Y_1 Axis

Screened Models Available	
ADC85Q - 12 ADC85Q - 10 ADC85CQ - 12 ADC85CQ - 10	

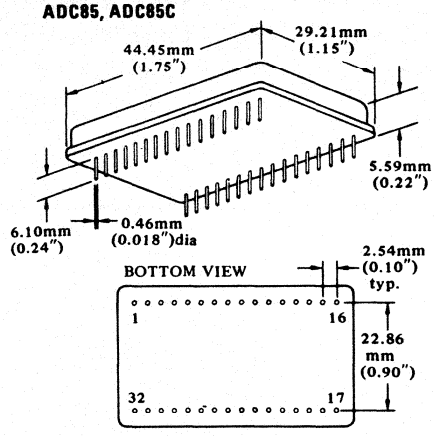
MECHANICAL SPECIFICATIONS

ADC84



PINS: Pin material and plating composition conform to method 2003 (Solderability) of Mil-Std-883 (except paragraph 3.2).
CASE: Ceramic
MATING CONNECTOR: 2302MC - Set of two 16 pin strips
WEIGHT: 13 grams (0.46 oz).
HERMETICITY: Conforms to method 1014 Condition C Step 1 (fluorocarbon) of Mil-Std-883 (Gross Leak)

ADC85, ADC85C



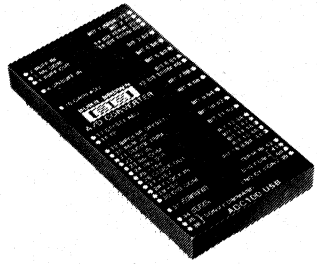
PINS: Pin material and plating composition conform to method 2003 (Solderability) of Mil-Std-883 (except paragraph 3.2).
CASE: Kovar, Gold or Nickel plated
MATING CONNECTOR: 2302MC - Set of two 16 pin strips
WEIGHT: 13 grams (0.46 oz).
HERMETICITY: Conforms to method 1014 Condition C Step 1 (fluorocarbon) of Mil-Std-883 (Gross Leak)

ORDERING INFORMATION

ADCXX XX XX

A/D Converter Family:	Grade:	Resolution:
ADC85 ADC84	Blank (-25, +85°C)(ADC85 only) C (0°C, +70°C)(ADC85 only) KG (0°C, +70°C)(ADC84 only)	10 = 10 bits 12 = 12 bits

BURR-BROWN



ADC100

High Resolution - Integrating ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 16-BIT RESOLUTION
- SELF-CONTAINED MODULAR PACKAGE
- LOW DRIFT
- USER-ADJUSTABLE LINEARITY
- EXPANDABLE TO 5-DIGIT BCD RESOLUTION

DESCRIPTION

The Burr-Brown Model ADC100 A/D Converter is an integrating A/D Converter that utilizes the delta sigma modulation principle. The digital equivalent of analog signals is developed by counting a number of pulses whose average repetition rate is proportional to the amplitude of the input signal over a fixed integration period. The internal clock is externally-adjustable to provide integration periods which are integral multiples of 50Hz or 60Hz periods for maximum powerline noise rejection. The closed conversion loop assures linear performance of ±0.005% ±1 count that is independent of clock frequency deviations over the specified temperature range of 0°C to ±70°C.

The ADC100 is housed in a 2" x 4" x 0.4" module and operates from ±15VDC and +5VDC power. All digital input and output signals are TTL-compatible.

Four basic models are offered: Unipolar 4 digit BCD, 4-digit plus sign BCD, unipolar and bipolar 16-bit binary. The binary units are pin-programmable for 12-, 14-, or 16-bit resolution.

The ADC100 is excellent for applications which require good accuracy and high resolution, but where speed is not too important. Conversion speeds range from 12msec for 12-bit binary to 30msec for 4-digit plus sign BCD codes.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-286D

Printed in U.S.A. July, 1978

SPECIFICATIONS

Typical at 25°C and rated power supply unless otherwise noted.

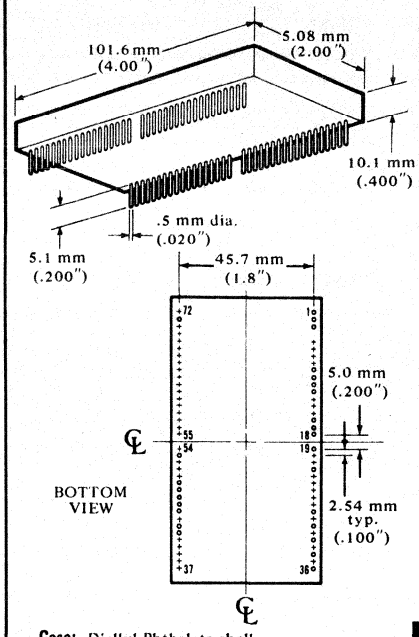
ELECTRICAL

MODEL	DECIMAL		BINARY		UNITS
ADC100	BCD	SMD	Unipolar USB	Bipolar BOB	
RESOLUTION	4 digits	4 digits + sign	14 or 16 bits	14 or 16 bits	
INPUT					
ANALOG INPUT					
Voltage Range	0 to +10	±10	0 to +10	±10	Volts
Maximum Safe Input Signal	±25V or supply voltage, whichever is less				
Input Bias Current typ max	20				nA
Impedance	200				nA
Buffered	200	200	200	200	MΩ
Unbuffered	10	10(1)	10	25	kΩ
Settling Time (to 0.003%) (F.S.R. (2) step)					
Buffered (max)	25	50	25	50	μsec
Unbuffered (max)	1	1	1	1	μsec
DIGITAL INPUT	TTL/DTL Compatible Logical "1" for at least one clock period @ 2 TTL Loads (Approximately 3μsec with internal clock)				
Convert Command					
External Clock	See Page 5-40				
TRANSFER CHARACTERISTICS					
ACCURACY(3)					
Gain Error	.05	.05	.05	.05	% of F.S.R.
Offset Error	.02	.02	.02	.05	% of F.S.R.
Linearity Error (max) (4)	±0.005	±0.005	±0.005	±0.005	% of F.S.R.(2)
Quantizing Error	±1 count				
ACCURACY DRIFT					
Temperature Coefficient (max)	±10	±5	±10	±10	ppm of FSR/°C
POWER SUPPLY SENSITIVITY					
Power Supply Sensitivity (max)					
±15 V	±0.007	±0.004	±0.0002	±0.0002	% of F.S.R./% of P.S. Voltage (15V)
+5 V	±0.002	±0.001	±0.002	±0.001	% of F.S.R./% of P.S. Voltage (5V)
CONVERSION TIME					
(maximum with Internal Clock)	30	30	For 12 bits - 12.5 14 bits - 50 16 bits - 200		ms
OUTPUT					
DIGITAL OUTPUTS	TTL/DTL Compatible All digital outputs will drive 6 TTL loads except the sign bit (for SMD units) which will drive 4 TTL loads.				
End of Conversion	"0" during conversion				
TEMPERATURE					
Specification	0 to +70				°C
Operating (reduced specs)	-25 to +85				°C
Storage	-55 to +100				°C
POWER SUPPLY					
Rated Voltage	±15 and +5				Volts
Range (max)	±14.5 to ±15.5 and +4.75 to +5.25				Volts
Supply Drain					
+15 V	25	25	25	25	mA
-15 V	20	20	15	15	mA
+5 V	300	300	300	300	mA

1) The internal buffer may be bypassed by connecting the input directly to unbuffered inputs. For SMD units this connection bypasses the sign magnitude circuitry and results in a unipolar BCD unit.
2) F.S.R. is Full Scale Range; 10V for unipolar, 20V for bipolar converters.
3) Gain and Offset Error may be externally adjusted to zero.
4) Linearity is factory adjusted for 4 digit or 14 bit operation and is user adjustable to typically 0.002%.

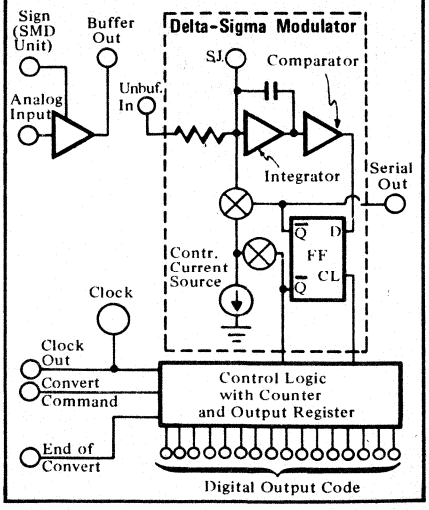
MECHANICAL

Dimensions in parentheses are in inches



Case: Diallyl Phthalate shell
Pins: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].
Weight: 4 oz (114 grams)
Actual pin assignments not shown on this diagram.
Mating Connectors: 2400MC - P.C. Card with solder terminals or 2401MC - Set of 4 - 18 pin connector strips

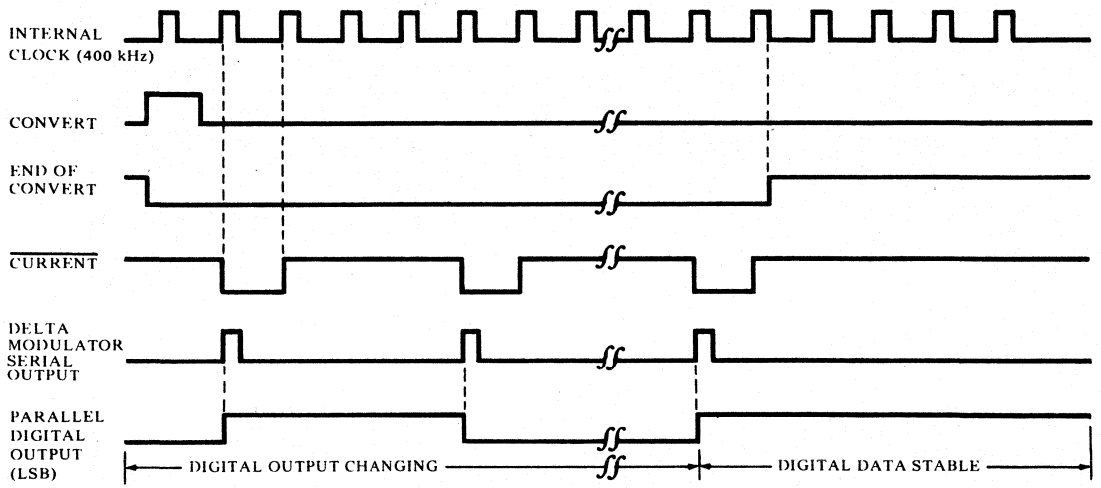
SIMPLIFIED BLOCK DIAGRAM



Method of Conversion

DELTA-SIGMA MODULATION

The Burr-Brown Model ADC100 A/D Converter utilizes the delta-sigma conversion technique which produces a train of pulses whose rate is proportional to the amplitude of the input analog signal. For a given internal clock frequency (400 kHz) the delta-sigma modulator output is a train of pulses whose average frequency varies from zero to 400 kHz. The width of these pulses are constant, but the number of pulses varies in relation to input signal amplitude. These pulses are counted in a binary (or BCD) counter over the integration interval resulting in a direct digital output that is equivalent to the analog input. The ADC100 timing diagram is shown in Figure 1.



DISCUSSION OF SPECIFICATIONS

ANALOG INPUT SETTLING TIME is the time required after a F.S.R. input step for the converter's input circuitry to settle to specified accuracy. The CONVERT COMMAND should be delayed by this period of time after any large input voltage change to preserve the converter's accuracy.

ACCURACY - The basic accuracy of the ADC100 is defined by linearity and quantizing errors. When gain and offset errors are adjusted as described on page 5-41, the accuracy of the ADC100 is 0.005% ±1 count.

LINEARITY ERROR is a measure of the deviation of the converter's actual transfer characteristic from the ideal. It is defined as the maximum deviation of the actual converter transfer function from the best fit straight line through it. If the linearity error is also adjusted (see page 5-42) the accuracy will typically be 0.002% ±1 count.

QUANTIZING ERROR is inherent in any A/D converter simply because a converter's analog input is continuous while its digital output must be discrete codes. The ADC 100 is designed such that increased resolution may be obtained by interpolation of several successive conversions of the same input voltage. For example, if the output code is zero for three conversions and one LSB for one conversion, the actual input voltage is one quarter of an LSB.

ACCURACY DRIFT is the maximum change with temperature of any point on the converter's transfer characteristic.

OFFSET ERROR is the deviation from the ideal input required to produce an output of all logical zeroes (all bits OFF). GAIN ERROR is the deviation from the ideal input required to produce an output of all logical ones (all bits ON) with the offset error adjusted to zero.

SERIAL OUTPUT

The serial output of the ADC100 may be used to transmit data remotely over a single line. Details for implementing this method of data transmission are shown on page 5-43 of this data sheet.

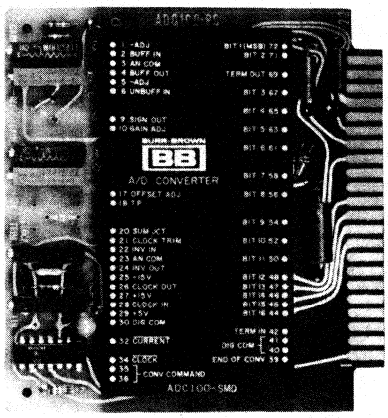
DIGITAL OUTPUT CODES

For unipolar analog input signals, 4 digit BCD or 16 bit straight binary (USB) digital output codes are offered; for bipolar analog input signals, 4 digit plus sign BCD (SMD) or 16 bit offset binary (BOB) digital output codes are offered. The LSB & full scale analog values and equivalent digital codes are shown in Table I.

PACKAGING OPTIONS

P.C. CARD OPTION

The ADC100 is available mounted on a PC card. Gain, offset linearity and clock adjust circuitry as well as power supply decoupling capacitors are included. A flip-flop is provided for SMD units to hold the output sign bit at the end of conversion. The PC option is ordered by adding "-PC" to the model number of the modular unit.



Component Side - Pin 1
Non-Component Side - Pin A

Component Side		Non-Component Side	
Pin	Function	Pin	Function
22	N/C	Z	End of Conv.
21	Analog Input Com	W	N/C
20	Analog Input	V	Conv. Com.
19	Analog Common	U	N/C
18	N/C	T	+5V
17	+15V	S	Clock In
16	-15V	R	Clock Out
15	Dig. Common	P	N/C
14	N/C	N	Bit 12
13	N/C	M	Bit 11
12	Bit 13	L	Bit 10
11	Bit 14	K	Bit 9
10	Bit 15	J	Bit 8
9	Bit 16	H	Bit 7
8	N/C	F	Bit 6
2	N/C	E	Bit 5
1	Sign Out	D	Bit 4
		C	Bit 3
		B	Bit 2
		A	Bit 1

A Connector (Burr-Brown Model Number 2200 MC) is supplied with each unit.

Dimensions in parentheses in inches.

ORDERING INFORMATION

The ADC 100 may be ordered by using the ordering code below.

ADC100 – XXX - XX

- ADC100 – Converter Family
- XXX – OUTPUT CODE
  - BCD - Binary Coded Decimal
  - SMD - Sign Magnitude BCD
  - USB - Unipolar Straight Binary
  - BOB - Bipolar Offset Binary
- XX – PACKAGE OPTION
  - PC - Printed Circuit Card
  - Not used with modular units

INSTALLATION and OPERATING INSTRUCTIONS

CLOCK OPERATION

The ADC100 may be operated from the internal clock, or from a user supplied external clock.

A clock period faster than 2.5 μseconds or slower than 25μseconds will degrade the performance of the ADC100. 50 Hz or 60 Hz rejection may be achieved by adjusting the clock frequency such that the CONVERT COMPLETE pulse is an integral number of 50 or 60 Hz periods (i.e., a multiple of 16.67 ms for 60 Hz rejection or 20.00 ms for 50 Hz rejection). For example, SMD or BCD units convert in 30 millisec with a clock period of 3 μsec. The closest multiple for 60 Hz rejection is 33.33 ms integration time.

EXTERNAL CLOCK

An external clock may be used by leaving CLOCK OUT, pin 26, open and connecting the external clock to CLOCK IN, pin 28. The duty cycle of the external clock should be 80% to 90% as shown in Figure 3.

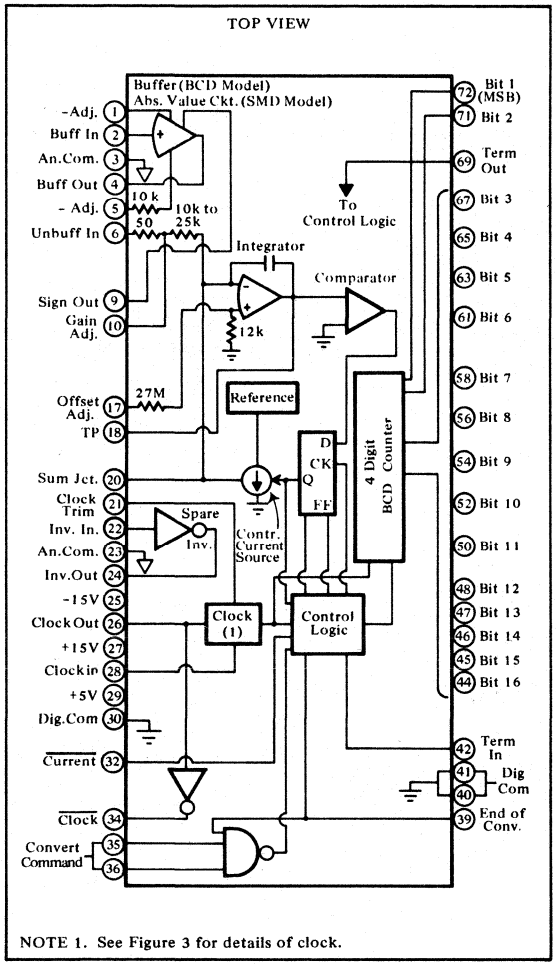
INTERNAL CLOCK

If the internal clock is used, CLOCK OUT, pin 26, and CLOCK IN, pin 28, must be connected together.

The approximate period of the internal clock is 3 μseconds.

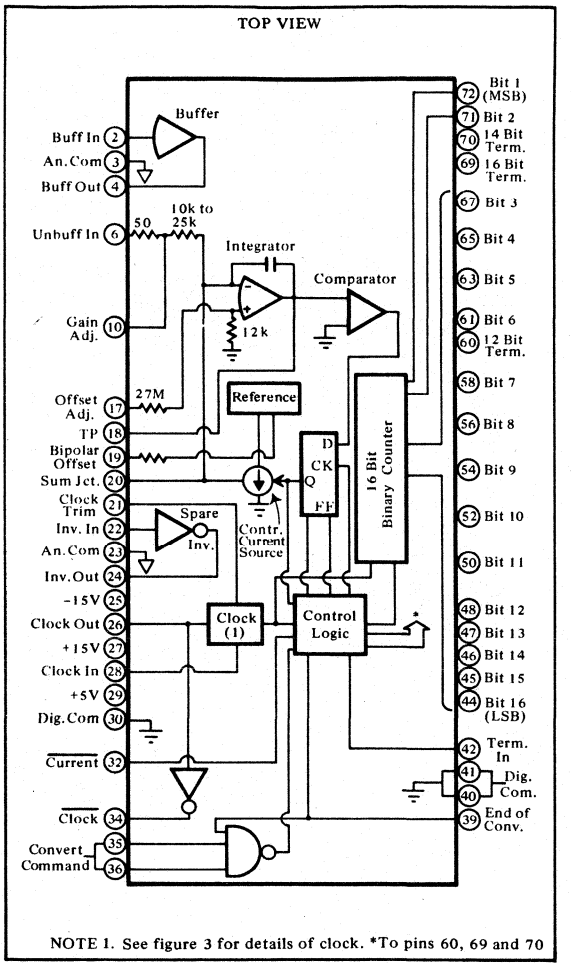
The internal clock frequency may be adjusted using the circuit shown in Figure 5 over a range of approximately 2.5 μsec to 25 μsec. If the clock frequency is not adjusted, pin 21 should simply be left open.

CONNECTION DIAGRAMS



NOTE 1. See Figure 3 for details of clock.

FIGURE 2a. BCD and SMD Models.



NOTE 1. See figure 3 for details of clock. *To pins 60, 69 and 70

FIGURE 2b. USB and BOB Models.

ANALOG COMMON, pins 3 and 23, are connected together internally as are DIGITAL COMMON, pins 30, 40 and 41. Digital and Analog Common are not connected internally; but they should be tied together at some point in the system as close as possible to the ADC100 to prevent any difference voltage between them.

All units have available a spare inverter (SN7404) whose input is pin 22 and output is pin 24.

USB and BOB units are marked as shown in Figure 3, the BOB units only will have a connection for BIPOLAR OFFSET, pin 19. The BOB units must have pin 19 externally connected by the user to SUMMING JUNCTION, pin 20.

For USB and BOB units, either 16-BIT TERMINATE, pin 69, 14-BIT TERMINATE, pin 70, or 12-BIT TERMINATE, pin 60, must be connected to TERMINATE IN, pin 42. The LSB will always be on pin 44, the MSB for 16 bits is on pin 72, for 14 bits is on pin 67, for 12 bits is on pin 63.

BCD and SMD units are marked as shown in Figure 4, the SMD units only will have connections for ADJ, pin 1 and pin 5, and SIGN OUT, pin 9.

For BCD and SMD units, TERMINATE OUT, pin 69, should be connected to TERMINATE IN, pin 42, for 4-digit operation (see page 5-43 for increased resolution).

NOTE:

For SMD units, the output sign bit operates continuously. That is, the sign bit output will change with the input voltage polarity even though the end of conversion output is "high". Therefore an output flip flop (such as the 7474 IC shown on page 5-41) may be used to store the sign bit at the end of conversion. (The PC mount option includes this flip-flop).

CONNECTIONS FOR INPUT SIGNAL, EXTERNAL GAIN and OFFSET TRIM

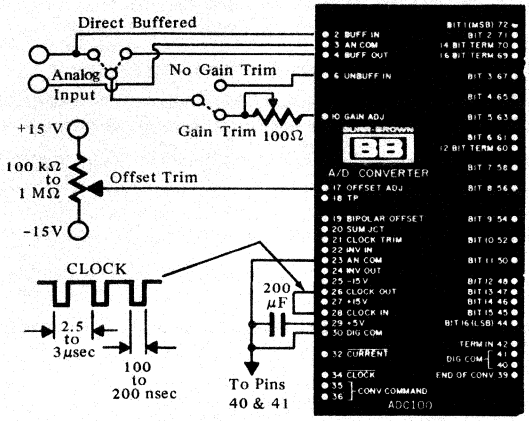


FIGURE 3. GAIN and OFFSET Adjustments for all Converters.

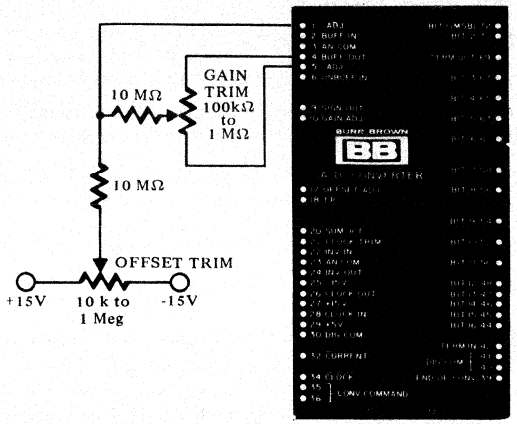


FIGURE 4. Additional NEGATIVE GAIN and OFFSET Adjustments required for SMD Converters.

The connections shown in Figure 3 illustrate various input and trim connection options; it is not necessary to include switches or jumpers as indicated unless that level of flexibility is desired. If linearity is not externally adjusted, the transfer characteristic of the ADC100 can be adjusted for minimum errors using only the GAIN and OFFSET adjustments. Table I shows the input voltage and respective output codes for these adjustments.

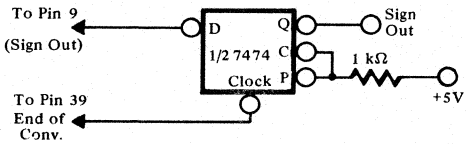
BCD and USB MODELS

Adjust to the proper output code with an input of +2.5000 volts using the OFFSET adjustment; then adjust to the proper output code with +7.5000 volts input using the GAIN adjustment (see Figure 3 for circuitry and Table I for input/output values). Repeat until both are optimum.

SMD MODELS

Adjust to the proper output codes as described above for BCD and USB models at 2.500 and +7.500 volts; then use the negative OFFSET adjustment (as shown in Figure 4) to provide the proper output code with -10 mV input and the negative GAIN adjustment (also in Figure 4) to provide the proper output code with -9.9900 volts input (see Table I).

SMD SIGN BIT STORAGE (see note on page 5-40).



BOB MODELS

Using the OFFSET adjustment, adjust to the output code of 0100 . . . . 00 with an input of -5.0000 volts; then find the input voltage, (near +5.00 volts), that causes an output code of 1100 . . . 000. Set the input voltage to a point halfway between e and 5.0000 volts. Use the GAIN adjustment to provide an output of 1100 . . . 000. Repeat the OFFSET adjustment at -5.0000 volts and check to see that an input of +5.00000 volts produces an output code of 1100 . . . 000. (See Table I). Repeat until both are optimum.

WIRING PRECAUTIONS

All connections between the ADC100 and external components should be as short as possible to minimize coupling effects and noise pickup. The +5V logic supply must be bypassed with a 100 to 200 μF tantalum capacitor to digital common to preserve ADC100 linearity, particularly near mid-scale. Experimenting by setting full scale and zero exactly correct and checking at or near mid-scale while varying the power supply decoupling will demonstrate the quality of the bypassing. This should be done first without any of the clock and/or linearity adjust circuitry, and then with the circuitry if it is to be used.

UNUSED ADJUSTMENTS

All unused adjustments should be left open except OFFSET adjust which should be grounded.

	CODE	One LSB (mV)	1/4 Scale OFFSET Adjust		3/4 Scale GAIN Adjust	
			Input Voltage	OUTPUT CODE	Input Voltage	OUTPUT CODE
	BCD 4 digit	1.00	+2.5000	MSB LSB 0010 0101 0000 0000	+7.5000	MSB LSB 0111 0101 0000 0000
USB	12 bits	2.44	+2.5000	010000000000	+7.5000	110000000000
USB	14 bits	0.61	+2.5000	01000000000000	+7.5000	11000000000000
USB	16 bits	0.15	+2.5000	0100000000000000	+7.50000	1100000000000000
SMD	Positive	1.00	+2.5000	1 0010 0101 0000 0000	+7.5000	1 0111 0101 0000 0000
SMD	Negative		-0.0100	0 0000 0000 0001 0000	-9.9900	0 1001 1001 1001 0000
BOB	12 bits	4.88	-5.0000	010000000000	+5.0000	110000000000
BOB	14 bits	1.22	-5.0000	01000000000000	+5.0000	11000000000000
BOB	16 bits	0.31	-5.00000	0100000000000000	+5.00000	1100000000000000

NOTE: Negative full scale is 0.000V for unipolar and -10.000V for bipolar models. Positive full scale is +10.000V -1 LSB.

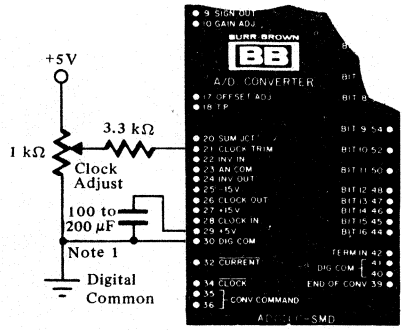
TABLE 1. GAIN and OFFSET Adjustments without LINEARITY Trim.

CLOCK and LINEARITY ADJUSTMENTS

CLOCK ADJUST

It may be necessary to adjust the clock frequency if optimum noise rejection to 50 or 60 Hz power line frequency is desired, or else a specific conversion period is desired. Otherwise, an external clock adjustment is not required. The CLOCK ADJUST trim circuitry shown in Figure 5 may affect linearity, particularly where there is already a bypassing problem with the 5 volt logic supply. If clock trim is employed, it may also be necessary to perform the linearity adjustment described below. The external wiring at pin 21 should be as short as possible to minimize this problem.

NOTE: The 400 kHz clock frequency will vary up to 1% per degree Centigrade. This will have a very small affect on the accuracy of the ADC100, but it can cause problems in some systems applications since the total conversion time will vary inversely with this frequency.



NOTE 1. Use tantalum capacitor.

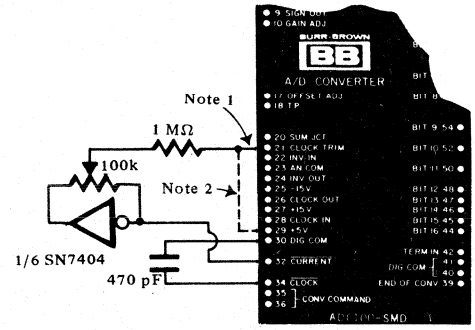
FIGURE 5. CLOCK ADJUST Circuit.

LINEARITY ADJUSTMENT

Linearity errors can typically be adjusted to less than 0.002% with the circuitry shown in Figure 6. This adjustment can be done only when the internal clock is used.

If the LINEARITY adjust circuitry is used, the OFFSET adjustment should be made near negative full scale, the GAIN adjustment should be made near positive full scale, and linearity adjusted near mid-scale. See Table II for the proper input voltages and output codes.

With GAIN and OFFSET adjusted per above, the linearity error should be adjusted to zero near mid-scale. Supply the ADC100 input with the mid-scale voltage shown in Table II and adjust the linearity potentiometer to obtain the output code also specified in Table II.



NOTES:
1. This wire should be as short as possible
2. This connection required only when external clock is used.

FIGURE 6. LINEARITY Adjustment Circuit.

CODE	OFFSET Adjustment		GAIN Adjustment		Mid-Scale LINEARITY Adjust	
	Input Voltage	Output Code	Input Voltage	Output Code	Input Voltage	Output Code
BCD		MSB LSB		MSB LSB		MSB LSB
4 digit	+0.0100	0000 0000 0001 0000	+9.9900	1001 1001 1001 0000	+5.010	0101 0000 0001 0000
USB						
12 bits	+0.00976	000000000100	+9.9878	111111111011	+5.00488	100000000010
14 bits	+0.00976	00000000010000	+9.9896	11111111101111	+5.00488	10000000001000
16 bits	+0.00976	0000000001000000	+9.9901	1111111110111111	+5.00488	1000000000100000
SMD						
Positve	+0.0100	1 0000 0000 0001 0000	+9.9900	1 1001 1001 1001 0000	+5.010	1 0101 0000 0001 0000
Negative	-0.0100	0 0000 0000 0001 0000	-9.9900	0 1001 1001 1001 0000	– –	– –
BOB						
12 bits	-9.99024	000000000010	+9.9854	111111111101	+0.00976	100000000010
14 bits	-9.99024	00000000001000	+9.9890	11111111110111	+0.00976	10000000001000
16 bits	-9.99024	000000000010000	+9.9898	1111111111011111	+0.00976	1000000000100000

TABLE II. GAIN and OFFSET Adjustments with LINEARITY Trim.

APPLICATIONS

VOLTAGE TO FREQUENCY CONVERTER

The $\overline{\text{CURRENT}}$ output, pin 32, and the $\overline{\text{CLOCK}}$ output, pin 34, may be used to provide a continuous serial output pulse train whose average repetition rate is proportional to the analog input voltage. This circuitry is shown in solid lines in Figure 8. The END OF CONVERSION output, pin 39, can be gated with the serial output using the additional circuitry shown with dotted lines. The gated output pulse train is available only during conversion and the number of pulses in that period is proportional to the input voltage, as shown in Figure 7.

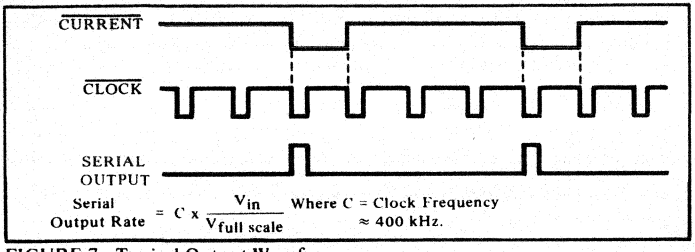


FIGURE 7. Typical Output Waveforms.

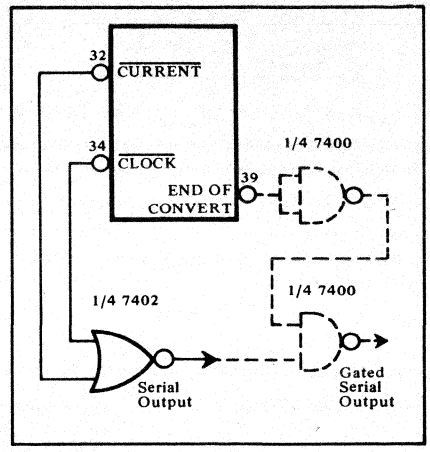


FIGURE 8. Voltage to Frequency Converter

5 DIGIT ADC100

The resolution of BCD and SMD models may be expanded to 4-1/2 or 5 digits with a minimum of external circuitry. Expansion to 4-1/2 digits will double the conversion time to about 60 milliseconds while 5 digit conversion will require 300 milliseconds. Figure 9 shows the application of two SN 7490 decade counters to provide an extra digit output.

If the ADC100 is used for five digit operation, it is recommended that the linearity adjustment circuitry shown on page 5-42 be used to provide accuracy consistent with the resolution. With five digit operation, the positive full scale input voltage is +9.99990 volts while the negative full scale input is 0.00000 volts (BCD) or -9.99990 (SMD). A good mid-scale input voltage to use for the linearity adjustment is 5.00500 volts (output code 0101 0000 0000 0101 0000).

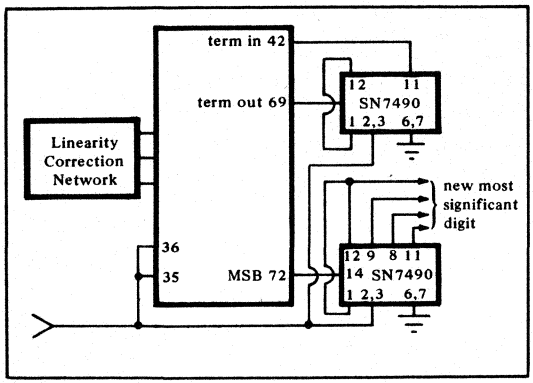


FIGURE 9. Extending ADC100 to 5 Digits.

The ADC100 may be used as the heat of a 5 digit DPM with accuracy much better than that of any moderately priced digital panel meters at a lower cost.

The components required in addition to the ADC100 are:

(1) Two decade counters (such as TI's SN7490)
(2) Five BCD to seven segment decoders (such at TI's SN7447A)
(3) A display (such as RCA's DR2100 Numitron series)
(4) Power Supplies, ±15 volts and +5 volts (such as Burr-Brown's Model 551 and Model 562).

ADC100 PREAMPLIFIER

An instrumentation amplifier may be used as the input to the ADC100. An input instrumentation amplifier such as Burr-Brown's 3625 will provide differential inputs with common mode rejection as well as gain. The circuitry shown below will provide a gain of 10 (i.e., 1 volt instead of 10 volt input range) and 74 dB CMR.

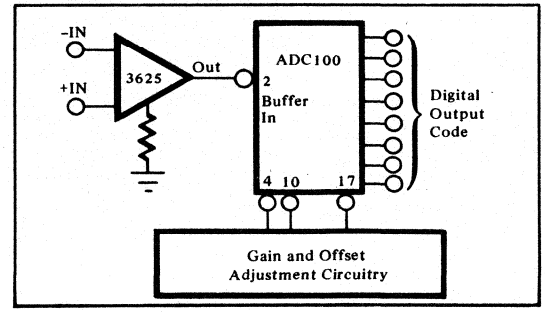
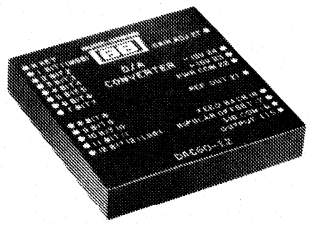


FIGURE 10. Differential Input ADC100.

The offset adjustment of the ADC100 has enough range to compensate for the small output offset of the 3625 and its' gain adjustment can compensate for the gain errors of the 3625

The 3625B will add no more than 10 ppm/°C gain drift and 1 ppm/°C offset drift while contributing only 0.002% linearity errors.

BURR-BROWN



DAC60

Ultra-high Speed DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 40nsec SETTLING TIME
- 10- AND 12-BITS
- LOW COST
- MONOTONIC
- 1/2LSB DIFFERENTIAL LINEARITY

DESCRIPTION

The DAC60 is a high speed digital-to-analog converter designed for high speed display applications, for use in high speed A/D converters, and for use as a high speed, precision waveform generator. The DAC60 is available in 10- and 12-bit accuracy. The extremely high speed of the DAC60 is accomplished with low impedance current switching techniques. The typical settling time to 0.05% for an LSB step is 25nsec. The maximum settling time for the major carry or for a full scale transition is only 40nsec to 0.05%. (The major carry is the LSB transition from 011 ... 11 to 100 ... 00).

The DAC60 produces a current output proportional to the digital input. The most significant bit (MSB) produces an output of -2.5mA. The DAC60 is pin-programmable to obtain unipolar or bipolar output signals. The current output may be fed directly into the summing junction of an external high speed operational amplifier, or onto an external summing resistor. An internal 2kΩ feedback resistor is included in the DAC60 for use with an external operational amplifier. This resistor provides voltage output ranges of 0 to +10V or ±5V and compensates for temperature drift of the DAC60.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-303C

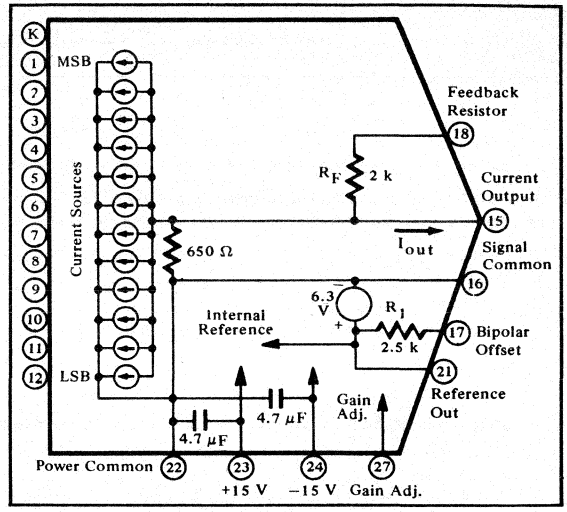
Printed in U.S.A. July, 1978

SPECIFICATIONS

Specifications typical at 25°C and with rated supply unless otherwise noted.

ELECTRICAL

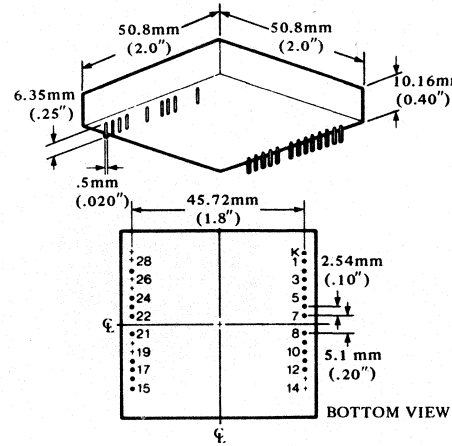
MODEL	DAC60
DIGITAL INPUTS	**10 Bits and 12 Bits**
Data Input Codes	TTL/DTL Compatible Complementary Logic
TRANSFER CHARACTERISTICS	
ACCURACY	
Linearity Error	±1/2 LSB
Differential Linearity Error (max)	±1/2 LSB
Gain Error (adjustable to zero)	±0.05% of FSR (3)
Offset Error (adjustable to zero)	
Unipolar	±0.001% of FSR
Bipolar	±0.05% of FSR
ACCURACY DRIFT	
Voltage Output (1)	±15 ppm/°C
Current Output	+30 ppm/°C
Differential Linearity Error (0° to +70°C)	
10 bits	±1/2 LSB
12 bits	±1 LSB
Monotonicity (0° to +70°C)	Guaranteed
CONVERSION SPEED	
Settling Time for 1 LSB Change (2)	
to 0.05%	25 ns
to 0.0125%	40 ns
for full scale change or major carry change	
to 0.05% (max)	40 ns
to 0.0125%	150 ns
POWER SUPPLY SENSITIVITY (4)	
±15 Volt Supply	±0.002 %/% P.S. Change
OUTPUT	
Unipolar Output Range (5)	0 to -5 mA
Compliance	3.2 V
Output Impedance	650 Ω
Bipolar Output Range (5)	±2.5 mA
Compliance	0.70 V
Output Impedance	516 Ω
POWER SUPPLY REQUIREMENTS	
Rated Power Supplies	±15 V
Power Supply Range	±14.5 to ±15.5 V
Supply Drain (max)	+45 mA, -35 mA
TEMPERATURE RANGE	
Specification	0° to +70°C
Operating (reduced specs)	-25°C to +85°C
Storage	-55°C to +100°C



Simplified DAC60 Schematic.

MECHANICAL

Dimensions in parentheses are in inches.



Material
Case - Diallyl Phtalate Shell
"Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)."
Connector - 2301MC
or - 2302MC

(1) When in the voltage output mode using an external op amp and the internal feedback resistor as shown in figure 1.
(2) For any data change not involving the four most significant bits.
(3) FSR is Full Scale Range (5 mA).
(4) The percent change in the output level with a one percent change in power supply voltage.
(5) The unipolar output may be fed into a resistive load providing a 3.2 volt or less swing. It is recommended that the bipolar output be fed into the summing junction of an op amp or a resistive load low enough to limit the swing to less than 100 mV.

DEFINITION OF SPECIFICATIONS

DIFFERENTIAL LINEARITY ERROR

The differential linearity of the DAC60 is ±1/2 LSB. This means that any 1 LSB digital input change will produce an output change of 1 LSB ±1/2 LSB (1/2 LSB to 3/2 LSB). This specification is especially important in CRT display systems because the eye is sensitive to differential linearity errors greater than ±1/2 LSB.

LINEARITY ERROR

Linearity error is the deviation of any output state from an ideal straight line drawn between the end points (all bits ON and all bits OFF)

MONOTONICITY

The DAC60 is guaranteed to be monotonic over 0 to 70°C. This means that the output will never decrease for an increase in the digital input.

COMPLIANCE

The compliance voltage of the DAC60 is the maximum voltage swing allowed on the current output node in order to maintain the specified accuracy; it is 0.70 volts for the bipolar current range of ±2.5 mA and is 3.6 volts for the unipolar current range of 0 to -5 mA. The maximum safe voltage swing allowed with no damage to the DAC60 output is ±5 volts.

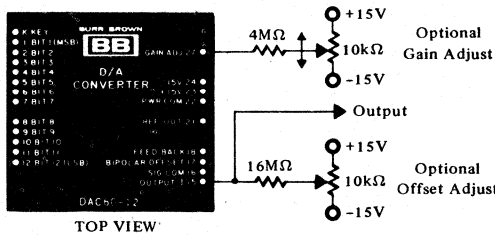
DEFINITION OF DIGITAL INPUT CODES

The DAC60 is available with complementary binary coding. The user may pin strap the output for bipolar complementary offset binary or unipolar complementary straight binary.

INPUT		OUTPUT CURRENT(1)		OUTPUT VOLTAGE(2)		OUTPUT VOLTAGE(3) when driving 50 Ω
MSB	LSB	BIPOLAR	UNIPOLAR	BIPOLAR	UNIPOLAR	UNIPOLAR
111 ...	111	+2.5 mA	0 mA	-5.0 V	0.0 V	0.00 mV
011 ...	111	0 mA	-2.5 mA	0.0 V	+5.0 V	-116.07 mV
000 ...	000	-(2.5 mA -1 LSB)	-(5 mA -1 LSB)	+5.0V -1 LSB	+10.0V -1 LSB	-(232.14 mV -1 LSB)
One LSB						
10 bits		4.88 μA	4.88 μA	9.76 mV	9.76 mV	0.227 mV
12 bits		1.22 μA	1.22 μA	2.44 mV	2.44 mV	0.057 mV

(1) Short circuit current
(2) Op-Amp output when driving summing junction and using the internal R_F (see Figure 1)
(3) See Figures 2 and 3.

INSTALLATION AND OPERATING INSTRUCTIONS



TOP VIEW
Optional GAIN and OFFSET Adjustments

- BIPOLAR OFFSET, pin 17, should be connected to I OUTPUT, pin 15, for bipolar operation or to POWER COMMON, pin 22, for unipolar operation.
- GAIN Adjustment Range: ±0.15% of FSR
- Offset Adjustment Range: ±0.15% of FSR
- If the GAIN ADJUST is not used, leave pin 27 open.
- REF OUT, pin 21 may be used to provide a low drift (5 ppm/°C) reference for external circuitry as long as less than ±100 μA is drawn from it.
- Internal 4.7 μF bypass capacitors between the ±15 Vdc power inputs and ground are included so that the DAC60 does not require external bypass capacitors.
- Both the DAC60-10 and DAC60-12 provide 12 digital inputs. Digital inputs that are not used should be tied to "1" (+5 volts). (Bits 11 and 12 on the DAC60-10 should be tied to +5 V if not used.)

INTERNAL FEEDBACK RESISTOR

Burr-Brown includes a 2 kΩ feedback resistor in the high speed resistor network (pin 18). The feedback resistor's temperature coefficient of resistance (TCR) is matched with that of the resistor network. Since the TCR of the resistor network contributes much of the current output drift of the DAC60, use of the feedback resistor with an external op amp reduces the effective drift of the voltage output. This is why the voltage output drift in the electrical specifications table is significantly better than the current output drift.

OPTIONAL OPERATING CONFIGURATIONS

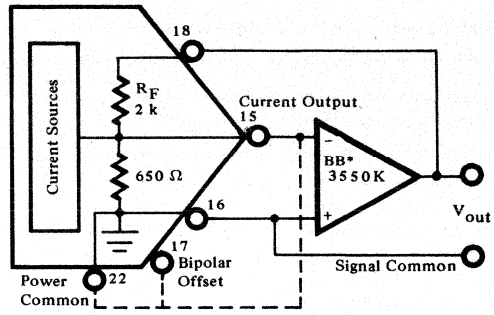
DRIVING AN OP AMP SUMMING JUNCTION

The DAC60 will drive the summing junction of an op amp (op amp being used as a current to voltage converter) to produce an output voltage:

$$V_{OUT} = -(I_{OUT})(R_F)$$

where I_{OUT} is the DAC60 short circuit output current and R_F is the op amp feedback resistor. Use of the internal feedback resistor (pin 18) will result in a 0 to +10 volt or ±5 volt output range. A 16 kΩ feedback resistor would produce output ranges of 0 to +50 volts or ±25 volts.

Use of the internal 2 kΩ feedback resistor will result in output voltage drifts as indicated in the specification table because the internal R_F drift is matched to that of the current sources. When using external feedback resistors, their temperature coefficient of resistance (TCR) should be directly added to the current output drift of the DAC60 to obtain the drift of the voltage output.



* Burr-Brown's 3400, 3401 and 3402 may also be used.

FIGURE 1. Driving an op amp summing junction.

DRIVING A RESISTIVE LOAD

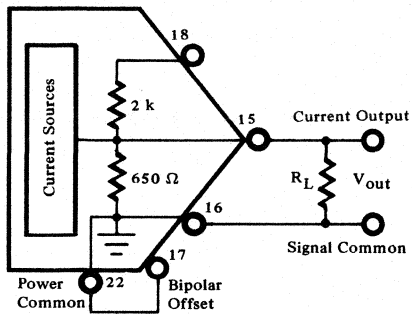


FIGURE 2. Driving a resistive load.

When driving a resistive load, the voltage output of the DAC60 is the short circuit output current times the equivalent load resistance. The DAC60 output impedance is approximately 650 ohms (in parallel with the load resistance, R_L). The output voltage is:

$$V_{OUT} = (I_{OUT})\left(\frac{R_L \times 650\ \Omega}{R_L + 650\ \Omega}\right)$$

With an R_L of 100 kΩ or higher, the full scale output voltage will be approximately 3.2 volts. An R_L of 300 ohms will provide a full scale output voltage of approximately 1 volt.

NOTE: For bipolar use, the output voltage should be less than 700 mV for acceptable output accuracy.

DRIVING A CABLE

The DAC60 can drive long lengths of cable with a circuit as shown in Figure 3. With just the 93 ohm terminating resistor used, the full scale output will be approximately 500 mV. The 120 ohm resistor across pins 15 and 16 will minimize output re-reflections due to mismatches between the characteristic impedance of the cable and the output impedance of the DAC60. The reflection factor of a cable is $\frac{Z_O - Z_t}{Z_O + Z_t}$ where Z_O is the characteristic impedance of the cable and Z_t is the termination resistance. A 1% mismatch between Z_O and Z_t will reflect back 1% of the output voltage to the cable input where the termination resistance normally seen is the 650 ohm output impedance of the DAC60. The reflection factor at the cable input would then be .75. The 120 ohm resistor reduces this reflection factor to 0.06 and significantly reduces glitches caused by reflections. Of course the 120 ohm resistor will reduce the full scale output voltage to about 250 mV.

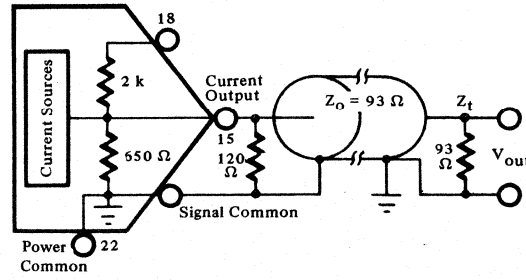


FIGURE 3. Driving a cable.

APPLICATIONS

DEGLITCHED VOLTAGE OUTPUT

Output transients when switching from one state to another are always a problem with high speed D/A converters. These transients, sometimes called glitches, are the result of unequal turn on and turn off times of the digital and analog components. A major contributor to glitch amplitude for the DAC 60 is the data skew of the digital inputs. Data skew is the time difference between the time one bit input changes state to the time other bit inputs change state. With data skew of less than 2 nanoseconds the DAC60 glitch area will typically be 25 picoamp seconds.

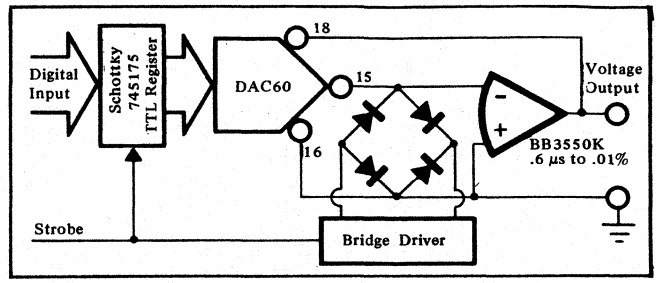


FIGURE 4. Deglitcher on DAC60 Output.

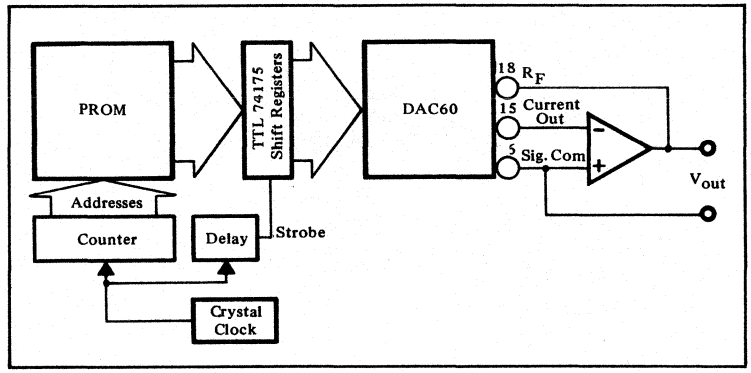
If a high speed amplifier, such as BB Model 3550 is used on the DAC60 output, a bridge clamping circuit on the summing junction will reduce the glitch amplitude. The deglitching bridge and bridge driver should be connected as shown in Figure 4. A high speed Schottky digital storage buffer should be used to reduce skew to 2 nanoseconds or less.

The deglitcher performance depends on the switching speed and matching of the bridge diodes. The bridge essentially clamps the summing junction near ground, preventing voltage glitches from appearing at the amplifier output. This technique can essentially eliminate or significantly reduce glitch amplitudes to 5 LSB or less at the output.

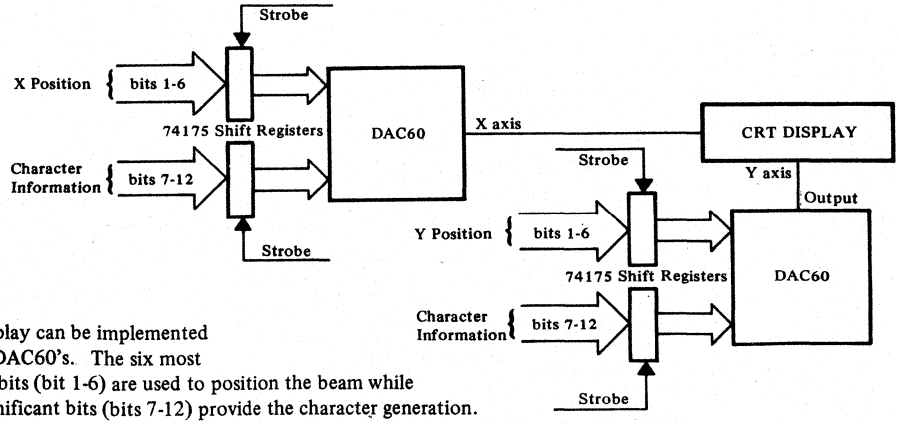
WAVEFORM GENERATORS

The DAC60 may be used as a high speed, precision signal generator with the help of a programmable read-only memory.

The counter updates the PROM addresses once each clock cycle. The delay provides a strobe pulse for the shift register when the PROM outputs have settled to a new word. This circuitry may be programmed to provide almost any complex, high speed waveform with up to 0.01% accuracy.

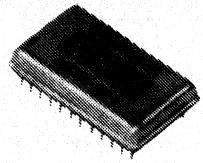


CRT DISPLAY CHARACTER GENERATOR



A CRT display can be implemented using two DAC60's. The six most significant bits (bit 1-6) are used to position the beam while the less significant bits (bits 7-12) provide the character generation.

BURR-BROWN



DAC70

High Resolution DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **PROVIDES ACCURATE ANALOG SIGNALS EXCELLENT FOR CALIBRATION STANDARD AND HIGH RESOLUTION APPLICATIONS**
  - **16-bit resolution**
  - **Laser-trimmed to ±0.003% maximum nonlinearity**
  - **Ultra-low drift - ±4ppm/°C, max**
- **SMALL SIZE SAVES SPACE AND WEIGHT**
  - **Hermetic Dual-in-line Package**
  - **Low Cost**

DESCRIPTION

The DAC70 is a high quality 16-bit hybrid IC D/A converter in a 24-pin DIP-compatible hermetic metal package. Constructed with laser-trimmed and drift-matched thin-film resistor network and fast-settling bipolar IC current switches, the DAC70 settles in 50μsec to a maximum nonlinearity of ±0.003% of full scale range (FSR) and has a very low maximum gain drift of ±4ppm/°C over 15°C to 50°C. Three basic models accept complementary unipolar or bipolar 16-bit binary or complementary 4-digit BCD TTL-compatible input codes. Each model is available in two grades of drift, linearity and operating temperature range. The Model DAC 70 (-25°C to +85°C) offers ±0.003% of FSR maximum nonlinearity and ±7ppm/°C maximum gain drift. The Model DAC70C (0°C to +70°C) offers ±0.005% of FSR maximum nonlinearity and ±14ppm/°C maximum gain drift.

These units provide output current signals of ±1mA or 0 to -2mA, and contain the scaling resistors for connecting an external amplifier to provide 0 to +10V (CSB, CCD) or ±10V (COB) output voltage ranges. Input power is ±15VDC and +5VDC.

Excellent stability, long life and quality product performance is assured because each DAC70 is burned-in for 96 hours at +100°C. Calibration equipment used to test the DAC70 is traceable to the National Bureau of Standards.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-332B

Printed in U.S.A. July, 1978

SPECIFICATIONS

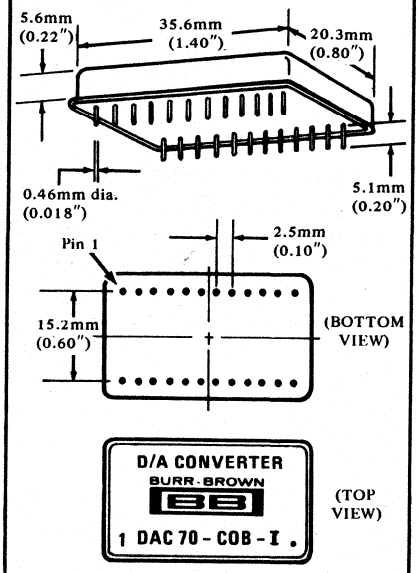
ELECTRICAL

(Typical at 25°C with rated power supplies unless otherwise noted.)

MODEL	DAC70	DAC70C	UNITS
INPUT			
DIGITAL INPUTS	TTL/DTL Compatible		
Data Input Codes	Complementary: 16 bit Binary/ 4 digit BCD		
Logic Levels (1)			
Logic "1"	+2.4<e_d<5.5@40μA Source		V
Logic "0"	0<e_d<+0.4 max @ 1.0mA sink		V
TRANSFER CHARACTERISTICS			
ACCURACY (25°C)			
Linearity Error (max)	±0.003	±0.005	% of FSR(2)
Gain Error, (max)(3)	±0.05		%
Offset Error, (max)(3)	±0.05		% of FSR
Monotonicity Guaranteed (10°C to 40°C)	14	13	bits
DRIFT(4)			
Gain (max) (0°C to +70°C)	---	±14	ppm/°C
(max) (-25°C to +85°C)	±7	--	ppm/°C
(max) (+15°C to 50°C)	±4	±8	ppm/°C
Offset			
Unipolar	±1		ppm of FSR/°C
Bipolar (max)	±5	±10	ppm of FSR/°C
Linearity (max)	±2	± 2	ppm of FSR/°C
SETTLING TIME(4) (to 0.003% FSR)			
Voltage Output(5) (max) 20 V step	100		μsec
.6 mV step	50		μsec
Current Output 2 mA step	50		μsec
Output Switching Transient	500		mV
Slew Rate	1		V/μsec
POWER SUPPLY SENSITIVITY			
Unipolar Offset			
±15 V	±1		ppm of FSR/%
+5 V	±0.1		ppm of FSR/%
Bipolar Offset			
±15 V	±4		ppm of FSR/%
+5 V	±1		ppm of FSR/%
Gain			
±15 V	±10		ppm/%
+5 V	±5		ppm/%
OUTPUT			
ANALOG OUTPUT			
Voltage Mode(5)			
CSB and CCD Models	0 to +10		V
COB Model	±10		V
Output Current (min)	5		mA
Output Impedance (DC)	0.05		Ω
RMS Noise (10 Hz to 10 kHz)	0.003		% FSR
Current Mode			
CSB and CCD Models	0 to -2		mA
COB Model	±1		mA
Compliance(6)	±2.5		V
Output Impedance (DC)			
Bipolar	4.4		kΩ
Unipolar	15		kΩ
INTERNAL REFERENCE VOLTAGE (V_r)	6.3		V
Maximum External Current(7)	200		μA
POWER SUPPLY REQUIREMENTS			
Rated Voltage	±15 and +5		V
Range	±14.5 to ±15.5 & +4.75 to +5.25		V
Supply Drain			
±15 V (including 5 mA load)	30		mA
+5 V	25		mA
TEMPERATURE RANGE			
Specification	-25 to +85	0 to +70	°C
Operating (Double above drift specs)	-55 to +100	-25 to +85	°C
Storage	-55 to +125		°C

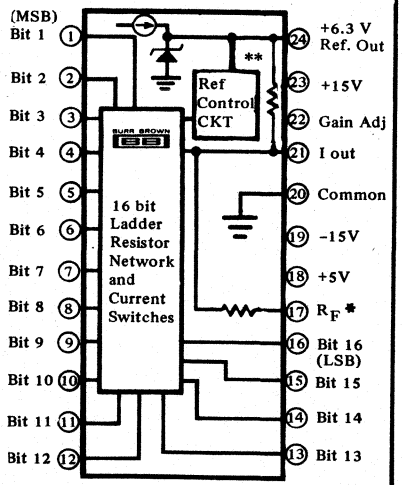
(1) It is recommended that the digital input lines to the DAC70 be drawn from TTL devices (inverters or registers) that drive only the DAC to obtain the specified accuracy.
(2) FSR means full scale range and is 20V for ±10V range, 10V for 0 to +10V range, etc.
(3) Gain and offset are externally adjustable to zero (see page 5-52).
(4) Worse case conditions measured at the worst case major carry (mid-scale).
(5) With external Burr-Brown Model 3500C op amp or equivalent, using internal feedback resistors.
(6) The current output should be connected to the virtual ground of an amplifier summing junction to obtain specified accuracy.
(7) With no degredation of specifications.

MECHANICAL



CASE: Kovar, Gold Plated
Mating Connector 245MC
PIN: Pin material and plating composition conform to method 2003 (solderabiltiy) of Mil-Std-883 (except paragraph 3.2).
WEIGHT: 9 grams (.32 oz)

CONNECTION DIAGRAM



* R_F = 5k (CSB) 10k (COB) 8k (CCD)
** 6.3k Bipolar Offset Resistor (COB only)

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC70 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The COB model may be user connected for either complementary offset binary (COB) or complementary two's complement (CTC) codes as shown in Table I.

DIGITAL INPUT CODES					
	Logic Inputs		CSB	COB	CTC*
	MSB	LSB	Compl. Straight Binary	Compl. Offset Binary	Compl. Two's Complement
CBI Models	All bits OFF	0000 ... 000	+Full Scale	+Full Scale	-1 LSB
	Mid Scale	0111 ... 111	+½Full Scale	Zero	-Full Scale
	All bits ON	1111 ... 111	Zero	-Full Scale	Zero
		1000 ... 000	Mid Scale -1 LSB	-1 LSB	+Full Scale
CCD Models			CCD (Complementary Coded Decimal) 3 Digits		*Invert the MSB of the COB code with an external inverter to obtain CTC code.
	F.S. bits OFF	0110 ... 0110	+Full Scale		
	All bits ON	1111 ... 1111	Zero		

TABLE I. Digital Input Codes.

ACCURACY†

LINEARITY

This specification describes one of the truest measures of D/A converter accuracy. As defined it means that the analog output will not vary by more than ±0.003% of FSR max (DAC 70) or ±0.005% of FSR max (DAC70C) from a straight line drawn through the end points (all bits ON and all bits OFF) at 25°C.

DIFFERENTIAL LINEARITY

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2 LSB means that the output voltage step sizes can be anywhere from 1/2 LSB to 3/2 LSB when the input changes from one adjacent input state to the next.

MONOTONICITY

Monotonicity over 10 to +40°C is guaranteed in the DAC70. This insures that the analog output will increase or remain the same for increasing 14 bit input digital codes. It is 13 bits over the same temperature range for the DAC70C.

DRIFT†

GAIN DRIFT is a measure of the change in the full scale range analog output over temperature expressed in parts per million per °C (ppm/°C). The GAIN DRIFT is determined by testing the end point differences at -25°C or 0°C, +25°C and +70°C or +85°C for each model and calculating the GAIN ERROR with respect to the 25°C value and dividing by the temperature change. This specification is expressed in ppm/°C and is shown in Figure 1.

OFFSET DRIFT

OFFSET DRIFT is a measure of the actual change in the output with all bits OFF $\left(V_{OUT}^{OFF}\right)$ over the specified temperature range. V_{OUT}^{OFF} is measured at -25°C or 0°C, +25°C and +70°C or +85°C. The maximum charge in OFFSET is referenced to the OFFSET at 25°C divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME†

The settling time for each model DAC70 is the total time (including slew time) for the output to settle to within an error band about its final value after a change in the input. Two settling times are specified to ±0.003% of full scale range (FSR); one for a maximum full scale range change of 20V and also for a 1 LSB change. The 1 LSB change is measured at the major carry (0111 ... 11 to 1000 ... 00) since this is the point where the worst case settling time occurs. This measurement is made with an external BB3500C op amp. (See Figure 3.)

OUTPUT SIGNAL RANGES

For optimum operation and performance to specification, an external operational amplifier (BB Model 3500C) should be used with the DAC70. A laser trimmed low-drift thin film feedback resistor (R_F) is provided in each DAC70 to provide an output voltage range of ±10V for the COB model or 0 to +10V for the CSB or CCD models. The internal feedback resistor must be used to obtain low gain drift.

COMPLIANCE

The compliance voltage of the DAC70 is the maximum voltage swing allowed on the current output mode in order to maintain the specified accuracy; it is ±2.5V and is compatible with an external op amp summing junction. The maximum safe voltage swing allowed with no damage to the DAC70 output is ±5 volts.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of power supply voltage change on the D/A converter output. It is defined as ppm of FSR per percent of change in either the +15 volt or - 15 volt and +5 power supplies about the nominal power supply voltages. Figure 2 shows Power Supply rejection vs. Frequency.

[†All specifications are tested with a BB3500C operational amplifier connected to the DAC70 output.]

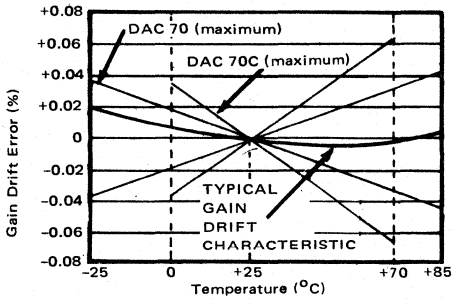


FIGURE 1. Gain drift error (%) vs. temperature.

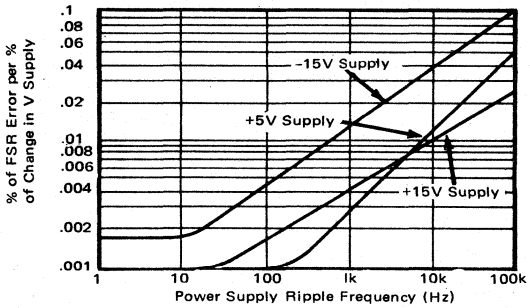


FIGURE 2. Power supply rejection vs. power supply ripple frequency.

TYPICAL PERFORMANCE CURVES

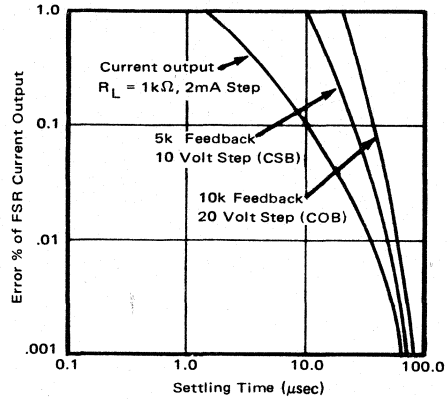


FIGURE 3. Full scale range settling time vs. accuracy.

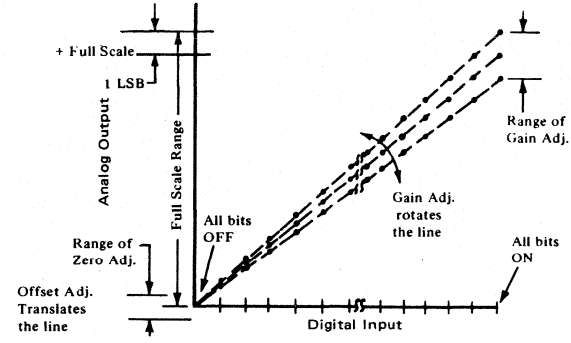


FIGURE 4. Relationship of OFFSET and GAIN adjustments for a UNIPOLAR D/A converter.

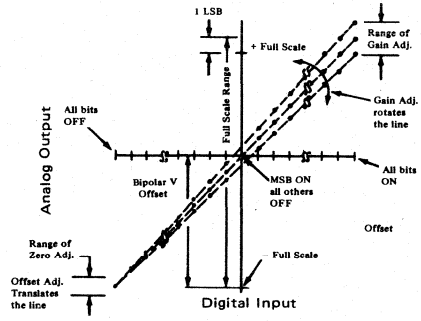


FIGURE 5. Relationship of OFFSET and GAIN adjustments for a BIPOLAR D/A converter.

DIGITAL INPUT AND ANALOG OUTPUT RELATIONSHIPS

DIGITAL INPUT CODE	OUTPUT CODE			
	VOLTAGE (1)		CURRENT	
	16 Bit Resolution	14 Bit Resolution	16 Bit Resolution	14 Bit Resolution
Complementary Unipolar Straight Binary (CSB) 0 to +10V or 0 to -2mA				
One LSB	+153μV	+610μV	0.031mA	0.122μA
All Bits off	+9.99985V	+9.99939	-1.99997mA	-1.99988mA
All Bits on	Zero	Zero	Zero	Zero
Complementary Bipolar Offset Binary (COB) ±10V or ±1mA				
One LSB	+305μV	+1.22mV	0.031μA	0.122μA
All Bits off	+9.99969V	+9.99878V	-0.99997mA	-0.99988mA
All Bits on	-10.0000V	-10.0000V	+1.0000mA	+1.0000mA
Complementary Binary Coded Decimal (CCD) 0 to +10V or 0 to -1.25mA	4 Digit Resolution	N/A	4 Digit Resolution	N/A
One LSB	+1.0mV		0.125μA	
F.S. Bits off	+9.999V		-1.24987mA	
All Bits on	Zero		Zero	

TABLE II. Ideal output voltage and current.

INSTALLATION CONSIDERATIONS

The DAC70 is laser trimmed to 14 bit linearity. The design of the device makes the 16 bit resolution available on binary units. If 16 bit resolution is not required, bit 15 (pin 15) and bit 16 (pin 16) should be connected to +5 V through a single 1 k Ω resistor.

Due to the extremely high resolution and linearity of the DAC70, system design problems such as grounding and contact resistance become very important. For a 16 bit converter with a +10 volt full scale range, one LSB is 153μV. With a load current of 5 mA and series wiring and connector resistance of only 30 mΩ, the output will be in error by 1 LSB. To understand what this means in terms of a system layout, the impedance of #18 wire is about 0.064 Ω/ft. Neglecting contact resistance, less than 6 inches of wire will produce a 1 LSB error in the analog output voltage! Although the problems involved seem enormous, care in the installation planning can minimize the potential causes of error.

The output can be made essentially independent of lead resistance by sensing the output at the load itself as shown in Figure 6. The lead and contact resistance, Z_i, is reduced by the loop gain to acceptable values.

The DAC70 and the wiring to its connector should be located so as to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pick-up is loop area. Therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field. This reduces radiation pick-up in the circuit. The metal case of the unit is internally connected to the common pin to further minimize pick-up. The DAC70 case is made of gold plated Kovar which also provides some electromagnetic shielding.

NOTE:

It is recommended that the digital input lines of the DAC70 be driven from inverters of TTL input registers to obtain specified accuracy.

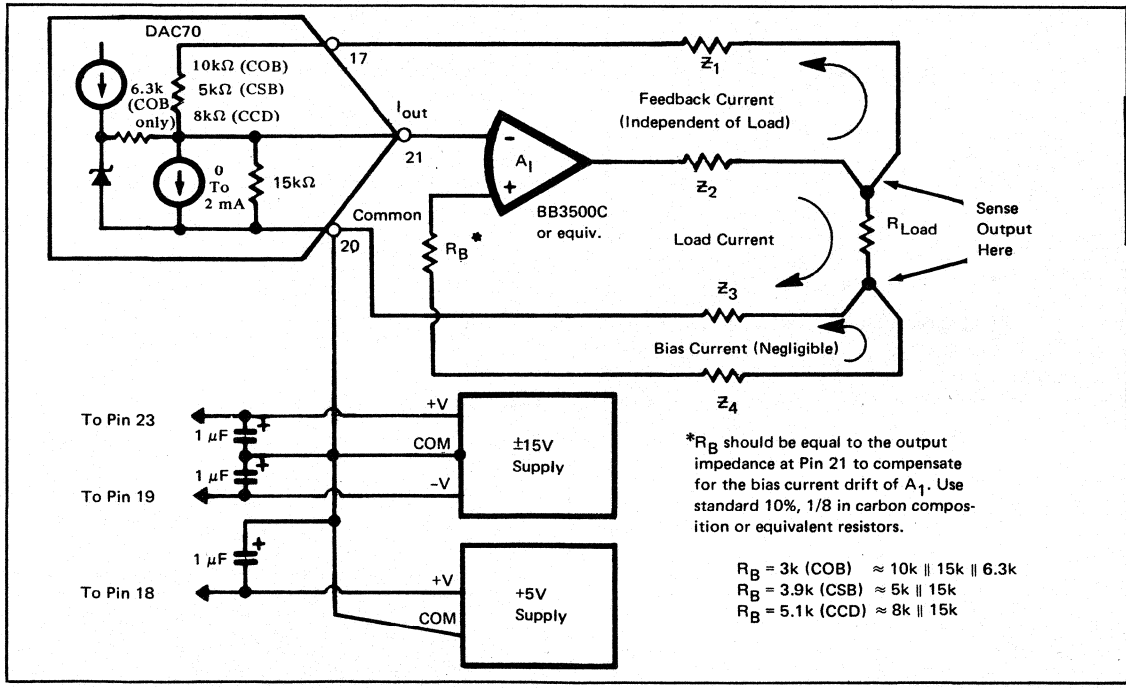


FIGURE 6. Output CIRCUIT for making LOAD VOLTAGE essentially independent of LEAD RESISTANCE.

SUPPLY DECOUPLING

For best performance and noise rejection, power supply decoupling capacitors should be connected as shown in Figure 6. These capacitors should be located close to the DAC70 and should be tantalum or electrolytic types bypassed with a 0.01μF ceramic capacitor for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJ.

Offset and gain may be trimmed by the user with externally connected offset and gain potentiometers. Connection of these potentiometers and the method of adjustment is outlined below. In each case a simplified schematic of the DAC 70 as seen from the adjustment point is given to assist the user in designing his own adjustment networks. Adjust offset first and then gain to avoid interaction (see Figures 4 and 5 for Gain & Offset definitions). If gain adjust circuit not used, leave pin 22 open.

OFFSET ADJUSTMENT

For unipolar (CSB, CCD) D/A converters, apply the digital input code that should give zero volts output and adjust the offset potentiometer for zero volts output. For bipolar (COB) D/A converters, apply the digital input code that should give minus full scale (-10 volts) and adjust the offset potentiometer for an output voltage of -10 volts. Two methods of offset adjustment are shown in Figures 7 & 8.

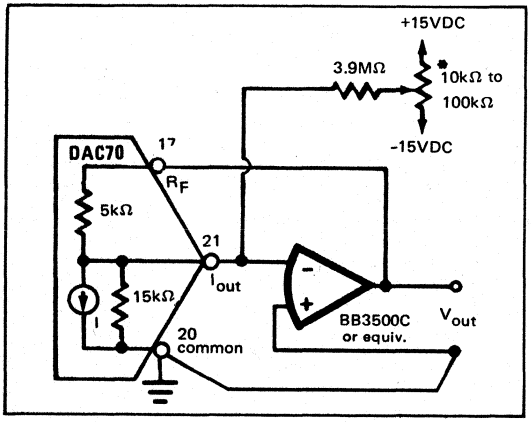


FIGURE 7. Offset adjustment with ±0.2% of FSR range of adjustment. DAC70–CSB–I with external op amp.

In some applications the use of such a large offset adjustment resistor might be undesirable. An alternative method of offset adjustment is shown in Figure 8:

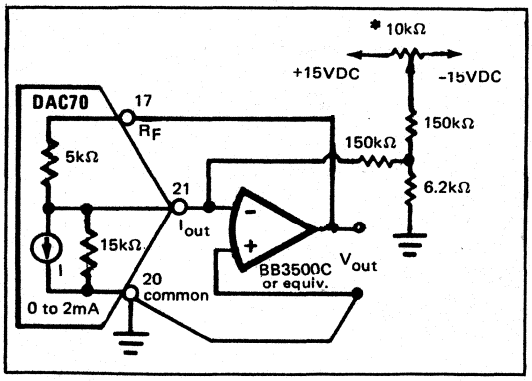


FIGURE 8. Alternative method of offset adjustment with ±0.2% of FSR range of adjustment for DAC70-CSB-I with external op amp.

GAIN ADJUSTMENT

For either unipolar (CSB, CCD) or bipolar (COB) models, apply the digital input that should give the maximum positive current or voltage output. Adjust the gain potentiometer for this full scale value. The positive full scale voltage and currents for the DAC70 are given in Table II.

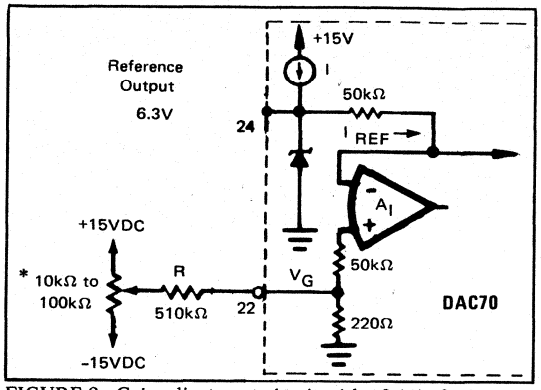


FIGURE 9. Gain adjustment circuit with ±0.1% of FSR range of adjustment.

Figure 9 shows how the gain adjust works on the DAC70. The gain of the DAC70 is determined by the reference current I_{ref}. Due to the high gain and low bias current of A_1, the voltage at the positive input of A_1 is approximately equal to the voltage at the gain adjust pin V_G. Therefore, the reference current is

$$I_{REF} = \frac{6.3\ V - V_G}{50\ k}$$

Since V_G is approximately equal to zero initially, a simple formula for determining the voltage range necessary at the gain adjust pin for a given percentage change in gain is

$$\Delta V_G = \frac{\%\ Gain\ Change}{100} \times 6.3\ volts$$

The full scale output voltage of the DAC70 with an external output amplifier and internal feedback resistor is laser trimmed to less than ±0.05% of FSR.

REFERENCE SUPPLY

All DAC70 and DAC70C models are supplied with an internal +6.3V reference voltage supply. This reference voltage (pin 24) has a tolerance of ±5% and is connected internally for specified operation. The zener is selected for a gain drift of typically ±3 ppm/°C and is burned in for a total of 168 hours for guaranteed reliability.

This reference may also be used externally but the current drain is limited to 200 μA. An external buffer amplifier is recommended if the DAC70 internal reference will be used externally in order to supply a constant load to the reference supply output.

NOTE: An external reference cannot be used. The DAC70 internal reference must be used.

* High quality multi-turn (10 turns if possible) potentiometers with less than 100 ppm/°C, T.C.R. should be used.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP

The DAC70 is a current output device and will drive the summing junction of an op amp to produce an output voltage (see Figure 10). The op amp output voltage is:

$$V_{out} = -I_{out} R_f$$

Where I_{out} is the DAC70 output current and R_f is the feedback resistor. Use of the internal feedback resistor (Pin 17) is required to obtain specified gain accuracy and low gain drift.

The DAC70 can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±25 ppm/°C. The resistors in the DAC70 are chosen for ratio tracking of ±1 ppm/°C and not absolute T.C.R. (which may be as high as ±25 ppm/°C).

An alternative method of scaling the output voltage of the DAC70 and preserving the low gain drift is shown in Figure 11.

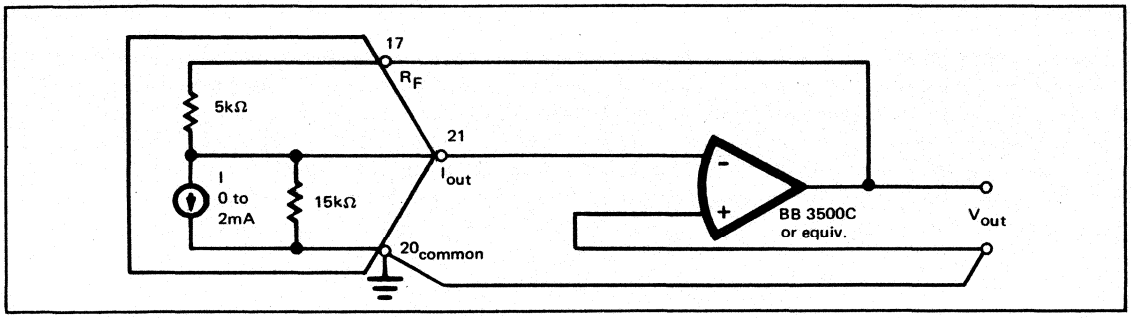


FIGURE 10. External op amp using internal feedback resistors.

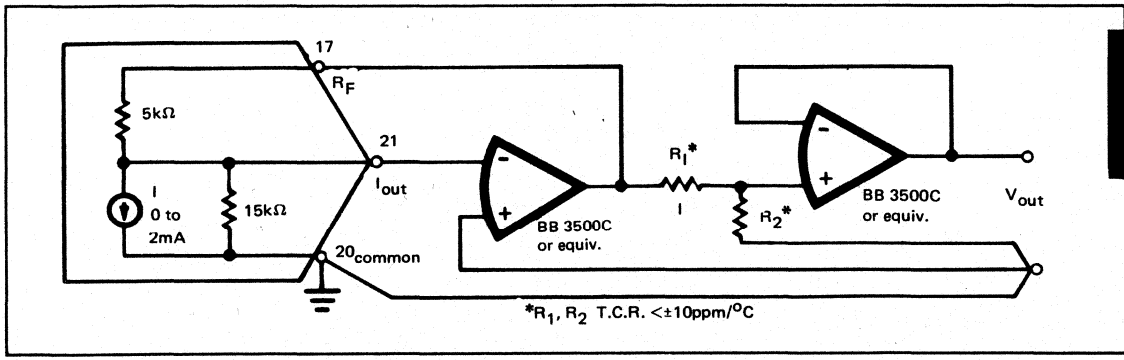


FIGURE 11. External op amp using internal and external feedback resistors to maintain low gain drift.

OUTPUTS LARGER THAN 20 VOLT RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{out} values of ±1 mA for bipolar voltage ranges and -2 mA for unipolar voltage ranges (see Figure 12). Use protection diodes when a high voltage op amp is used.

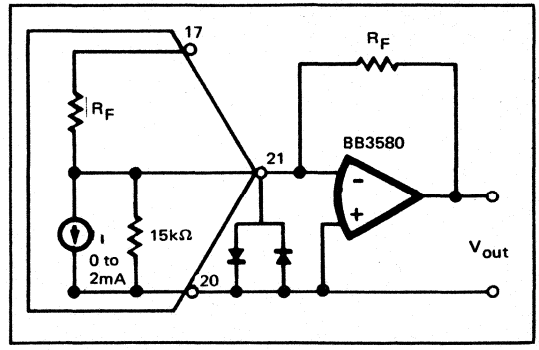
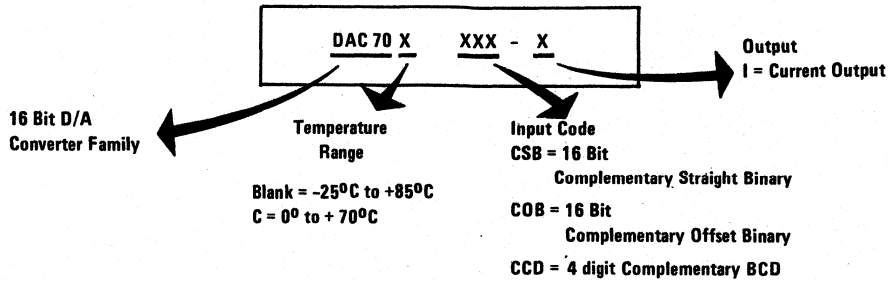


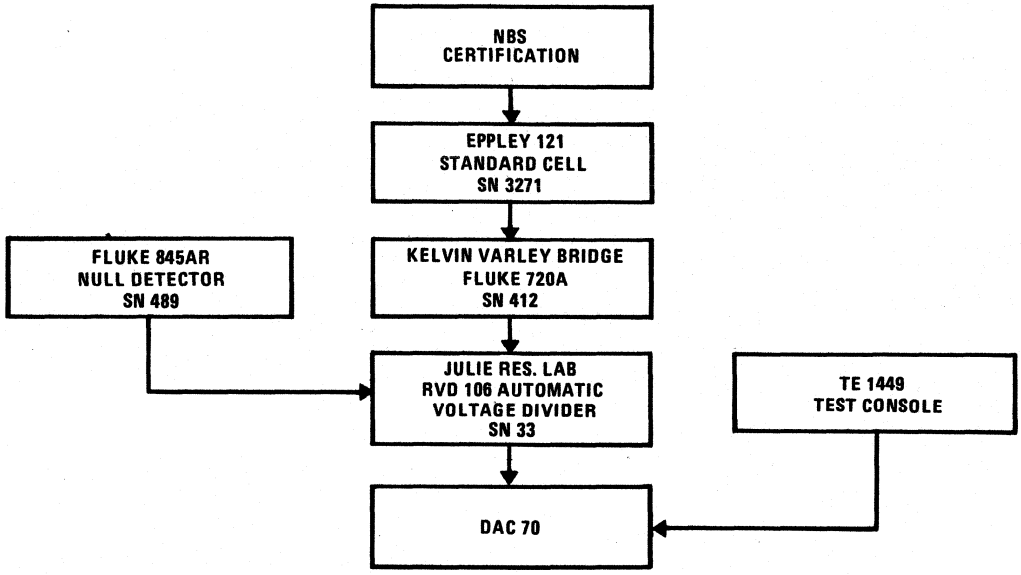
FIGURE 12. External op amp using external feedback resistors.

ORDER INFORMATION



NBS TRACEABILITY

The reference zener is burned-in for a total of 168 hours. The entire unit is burned-in for 96 hours at +100°C to age and stabilize the components and insure long life, excellent stability, and high quality performance.



BURR-BROWN

DAC80

IC DIGITAL-TO-ANALOG CONVERTER

FEATURES

- WIDE POWER SUPPLY RANGE MODELS AVAILABLE (Z MODELS)
- 12-BIT, 3 DIGIT RESOLUTION
- ±½LSB MAXIMUM NONLINEARITY
- COMPLETE WITH INTERNAL REFERENCE AND OUTPUT AMPLIFIER (V MODELS)
- FAST SETTLING - 300nsec to ±.01% (I MODELS)
- CERAMIC DUAL-IN-LINE PACKAGE
- LOW COST

DESCRIPTION

Use this popular 12 bit digital-to-analog converter for low cost precision performance applications.

DAC80, with internal reference and optional output amplifier, offers a maximum nonlinearity error of ±0.012%, ±30ppm/°C maximum gain drift, and monotonicity - all over a 0 to 70°C operating range. In the bipolar configuration, total accuracy drift is guaranteed to be less than ±25ppm/°C. Select TTL compatible complementary 12 bit binary (CBI) or 3 digit BCD (CCD) input codes.

Packaged within DAC80's 24 pin dual-in-line ceramic case are fast settling switches and stable, laser trimmed thin-film resistors that let you select output voltage ranges of ±2.5, ±5, ±10, 0 to +5, 0 to +10 volts (V models) or output current ranges of ±1mA or 0 to -2mA (I models). Voltage output models settle to ±0.01% of FSR in 3 microseconds for a 10 volt step change.

By specifying the new DAC80Z model with a supply range of ±11.4 to ±16.0 volts, you can use this proven D/A converter in microprocessor and semiconductor memory systems.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-322E

Printed in U.S.A. July, 1978

ELECTRICAL SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	DAC80-CBI			DAC80-CCD			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DIGITAL INPUT							
Resolution			12				Bits
						3	Digits
Logic Levels (TTL/Compatible)[1]							
Logical "1" (at +40μA)	+2		+5.5	+2		+5.5	VDC
Logical "0" (at -1.0mA)	0		+0.8	0		+0.8	VDC
ACCURACY							
Linearity Error at 25°C		±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error		±1/2	+1, -3/4		±1/4	±1/2	LSB
Gain Error[2]		±0.1	±0.3		±0.1	±0.3	%
Offset Error[2]		±0.05	±0.15		±0.05	±0.15	% of FSR[3]
Monotonicity Temp. Range, min	0		+70	0		+70	°C
DRIFT[4] (0°C to +70°C)							
Total bipolar drift, max (includes gain, offset, and linearity drifts)[7]			±25			±25	ppm of FSR/°C
Total error over 0°C to +70°C[8]							
Unipolar		±0.08	±0.15		±0.08	±0.15	% of FSR
Bipolar		±0.06	±0.12		±0.06	±0.12	% of FSR
Gain		±15	±30		±15	±30	ppm/°C
Exclusive of internal reference			±10			±10	ppm/°C
Unipolar Offset		±1	±3		±1	±3	ppm of FSR/°C
Bipolar Offset		±7	±15		±7	±15	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	+1, -7/8		±1/2	+1, -7/8	LSB
Linearity Error 0°C to +70°C			±1/2			±1/2	LSB
CONVERSION SPEED/V models							
Settling Time to ±0.01% of FSR For FSR Change							
with 10kΩ Feedback[6]		5			5		μsec
with 5kΩ Feedback		3			3		μsec
For 1 LSB Change		1.5			1.5		μsec
Slew Rate	10	20		10	20		V/μsec
CONVERSION SPEED/I models - of FSR							
Settling Time to ±0.01% For FSR Change							
10 to 100Ω Load		300			300		nsec
1kΩ Load		1			1		μsec
ANALOG OUTPUT/V models							
Ranges[6]	±2.5, ±5, ±10, 0 to +5, 0 to +10				0 to +10		Volts
Output Current	±5			±5			mA
Output Impedance (DC)		0.05			0.05		ohms
Short Circuit Duration	Indefinite to Common						
ANALOG OUTPUT/I models							
Ranges		±1, 0 to -2			0 to -2		mA
Output Impedance - Bipolar		4.4			4.4		kΩ
Output Impedance - Unipolar		15			15		kΩ
Compliance			±2.5			±2.5	Volts
INTERNAL REFERENCE VOLTAGE		+6.3			+6.3		Volts
Maximum External Current[5]			±200			±200	μA
Tempco of Drift, max		±10	±20		±10	±20	ppm/°C
POWER SUPPLY SENSITIVITY							
+15V Supply		±0.02			±0.02		% of FSR/% V_S
-15 and +5V Supplies		±0.002			±0.002		% of FSR/% V_S
POWER SUPPLY REQUIREMENTS							
DAC80	±14, +4.75	±15, +5	±16, +16	±14, +4.75	±15, +5	±16, +16	VDC
DAC80Z[6]	±11.4, +4.75	±12, +5	±16, +16	±11.4, +4.75	±12, +5	±16, +16	VDC
Supply Drain							
±15/±12V (including 5mA load)		±25	±35		±25	±35	mA
+5V (logic supply)		+20	±30		+20	±30	mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Operating (double above specs)	-25		+85	-25		+85	°C
Storage	-55		+100	-55		+100	°C

TABLE I. Electrical Specifications

NOTES:
1. Adding external CMOS hex buffers CD 4009A will provide CMOS input compatibility. Approximate cost is $2.25 (1-24) to $1.50 (100's).
2. Adjustable to zero with external trim potentiometer.
3. FSR means "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc.
4. To maintain drift spec internal feedback resistors must be used for current output models.
5. Maximum with no degradation of specifications.
6. DAC80Z supply range is ±12.0V min to ±16.0V max for 0 to +10V and ±10V outputs.
7. See discussion on page 5-66.
8. With gain and offset errors adjusted to zero at 25°C. See discussion on page 5-67.

CONNECTION DIAGRAM

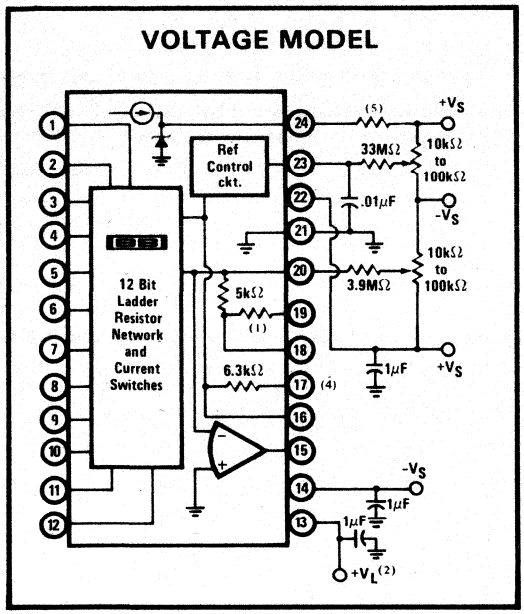


FIGURE 1. External Adjustment and Voltage Supply Connection Diagram, Voltage Model.

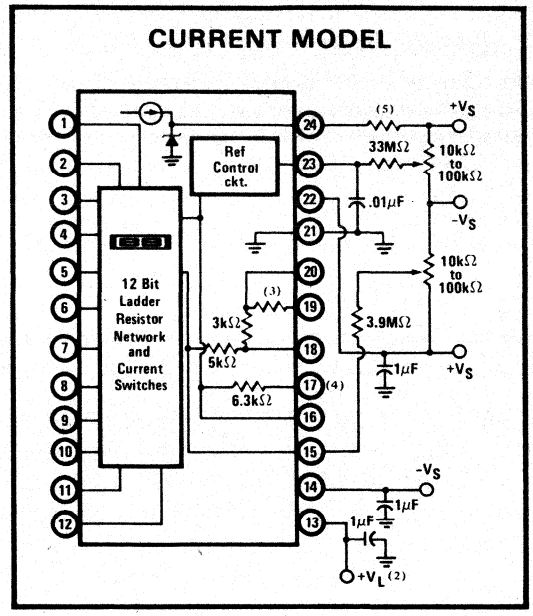


FIGURE 2. External Adjustment and Voltage Supply Connection Diagram, Current Model.

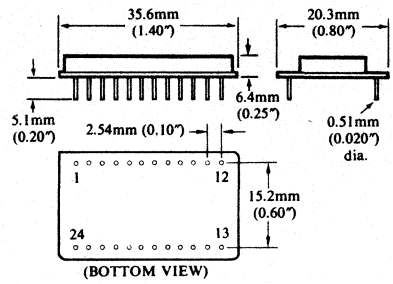
NOTES:

1. 3kΩ for CCD models, 5kΩ for CBI models.
2. If connected to $+V_S$, which is permissible, power dissipation increases 200mW.
3. CBI model, 2kΩ; CCD model,OΩ and pin 20 has no internal connection.
4. 6.3kΩ resistor internally grounded on CCD models.
5. Resistor required only for Z models, see **page 5-61.**

PIN ASSIGNMENTS

I Models	Pin #	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
(LSB) Bit 12	12	Bit 12 (LSB)
Logic Supply	13	Logic Supply
$-V_S$	14	$-V_S$
I_{OUT}	15	V_{OUT}
Ref. Input	16	Ref. Input
Bipolar Offset	17	Bipolar Offset
Scaling Network	18	10V Range
Scaling Network	19	20V Range
Scaling Network	20	Summing Junction
Common	21	Common
$+V_S$	22	$+V_S$
Gain Adjust	23	Gain Adjust
6.3V Ref. Out	24	6.3V Ref. Out

MECHANICAL



CASE: Black Ceramic
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to method 1014 Condition C Step 1 (fluorocarbon) of Mil-Std-883 (gross leak).

FIGURE 3. Mechanical Specifications

DISCUSSION

DIGITAL INPUT CODES

The DAC80 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The CBI model may be connected by the user for any one of three complementary codes: CSB, CTC or COB.

	DIGITAL INPUT	ANALOG OUTPUT		
	MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
CBI Models	000000000000	+Full Scale	+Full Scale	-LSB
	011111111111	+1/2 Full Scale	Zero	-Full Scale
	100000000000	Mid-scale -1LSB	-1 LSB	+Full Scale
	111111111111	Zero	-Full Scale	Zero
CCD Models	MSB LSB	CCD Complementary Coded Decimal - 3 Digits		
	0110 0110 0110	+Full Scale		
	1111 1111 1111	Zero		

* Invert the MSB of the COB code with an external inverter to obtain CTC code.

TABLE II. Digital Input Codes

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC80 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2 LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0 to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2 LSB means that the output voltage step sizes can range from 1/2 LSB to 3/2 LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0 to +70°C range is guaranteed in the DAC80 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each DAC80 model at 0°C, +25°C and +70°C; 2) calculating the gain error with respect to the 25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the specification table both with and without internal reference.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, +25°C and +70°C. The maximum change in OFFSET is referenced to the OFFSET at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC80 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input.

Voltage Output Models: Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1 LSB change. The 1 LSB change is measured at the major carry (0111 ... 11 to 1000 ... 00), the point at which the worst case settling time occurs.

Current Output Models: Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10 to 100 ohms and 1000 to 1875 ohms. Internal resistors are provided for connecting nominal load resistances of approximately 1000 to 1800 ohms for output voltage range of ±1V and 0 to -2V. See Table V.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is ±2.5V. Maximum safe voltage swing permitted without damage to the DAC80 is ±5V.

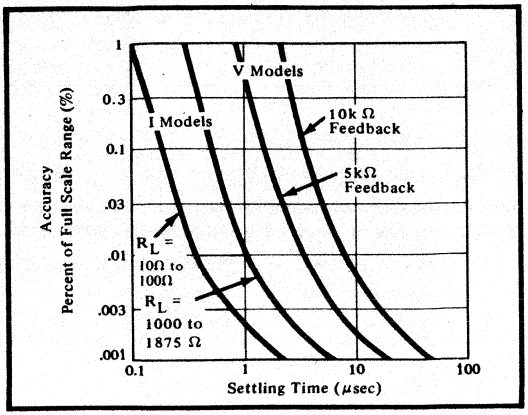


FIGURE 4. Full Scale Range Settling Time vs Accuracy

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a per cent of FSR per per cent of change in either the positive, negative, or logic supplies about the nominal power supply voltages. See Figure 5.

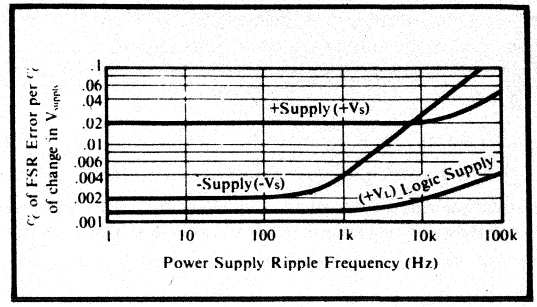


FIGURE 5. Power Supply Rejection vs Power Supply Ripple

REFERENCE SUPPLY

All DAC80 models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) has a tolerance of ±5% and must be connected to the Reference Input (pin 16) for specified operation. This reference may be used externally also, but external current drain is limited to 200μA. An external buffer amplifier is recommended if this reference will be used to drive other system components.

OPERATING INSTRUCTIONS

±12 VOLT SUPPLY OPERATION

The Z models will operate with supply voltages as low as ±11.4V. For operation with supplies less than ±14V an external resistor must be connected between the positive supply and pin 24. This provides additional current required by the internal reference. The required resistor value for supply voltages of ±11.4 to ±12.6V is 2.0kΩ and for supplies of ±12.6 to ±14V is 3.9kΩ.

It is recommended that output voltage ranges -10 to +10V and 0 to +10V not be used with the Z model if the supply voltages are ever less than the recommended ±12V. The output amplifier may saturate if $|V_{supply}| - |V_{out}\cdot max| <$ 2.0V. This applies to units with both CBI and CCD input codes. Except for operation at lower supply voltages, the DAC80Z and DAC80 operation is identical.

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the connection diagrams, Figures 1 and 2. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the DAC80. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers. If gain and offset adjust circuits are not used, pins 15, 20 and 23 should be connected as described in other sections herein. (Do not ground.) Connect the potentiometers as shown in Figure 1 and Figure 2 and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 33MΩ resistors (20% carbon or better) should be located close to the DAC80 to prevent noise pick-up. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 6, may be substituted in each case. The gain adjust (pin 23) is a high impedance point and a .001μF to .01μF ceramic capacitor should be connected from this pin to common to prevent noise pick-up. Refer to Figure 7 and 8 for relationship of OFFSET and GAIN adjustments to unipolar and bipolar D/A converters.

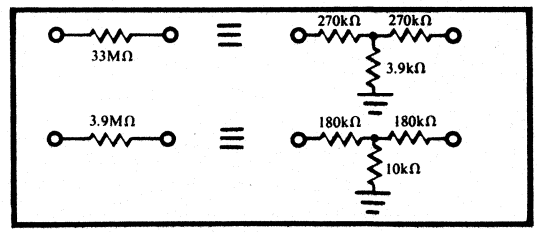


FIGURE 6. Equivalent Resistances.

Offset Adjustment: For unipolar (CSB, CCD) configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 volts, the maximum negative output voltage is -10V. See Table III for corresponding codes and the block diagrams on page 5-59 for offset adjustment connections.

Gain Adjustment: for either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. See Table III for positive full scale voltages and the block diagrams for gain adjustment connections.

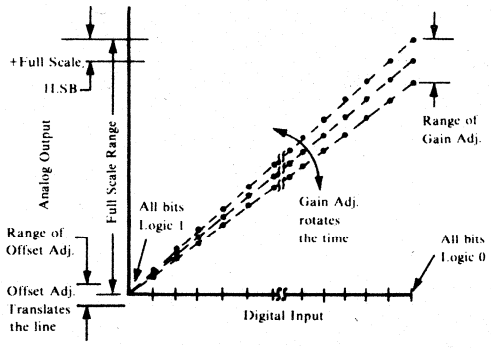


FIGURE 7. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter.

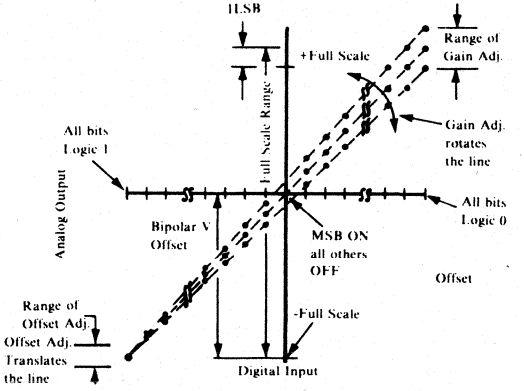


FIGURE 8. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A Converter

	DIGITAL INPUT	ANALOG OUTPUT			
		VOLTAGE*		CURRENT	
		0 to +10V	±10V	0 to -2mA	±1mA
CBI Models	12 Bit Resolution MSB LSB				
	000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
	011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
	100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
	111111111111	0.0000V	-10.0000V	0.0000mA	+1.000mA
	One LSB	2.44mV	4.88mV	0.488μA	0.488μV
CCD Models	3 Digital Resolution MSB LSB				
	0110 0110 0110	+9.990V**	N/A	-1.249mA	N/A
	0110 0110 1111	+9.900V	N/A	-1.238mA	N/A
	0110 1111 1111	+9.000V	N/A	-1.125mA	N/A
	1111 1111 1111	0.000V	N/A	0.000mA	N/A
	One LSB	10.00mV	N/A	1.25μA	N/A

** Normal full scale range with correct codes; output can go higher if illegal codes are applied.
* To obtain values for other binary (CBI) ranges: 0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

TABLE III. Digital Input/Analog Output

VOLTAGE OUTPUT MODELS

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC80 may be connected to produce bipolar output voltage ranges of ±10*, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5 or 0 to +10V.* See Figure 9.

*Refer to ±12V supply operation discussion, page 5-61.

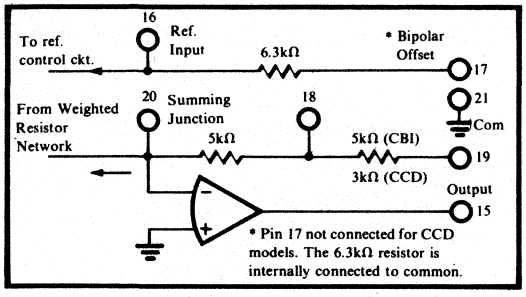


FIGURE 9. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized in the DAC80 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table IV. Settling time is specified for a full scale range change: 5 microseconds for 8kΩ or 10kΩ feedback resistors; 3 microseconds for a 5kΩ feedback resistor.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

TABLE IV. Output Voltage Range Connections - Voltage Model DAC80.

CURRENT OUTPUT MODELS

The equivalent output circuit and resistive scaling network of the current model differ from the voltage model and are shown in Figures 10 and 11. Instructions for using the DAC80-XXX-I with a resistor or an external op amp follow. External R_{LS} or R_{LP} resistors are required to produce exactly 0 to -2V or ±1V output. TCR of these resistors should be ±100 ppm/°C or less to maintain the DAC80 output specifications. If exact output ranges are not required, the external resistors are not needed.

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1V or 0 to -2V. These resistors (R_{LI}) are an integral part of the DAC80 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25 ppm/°C or less to minimize drift. This will typically add ±50 ppm/°C + the TCR of R_L (or R_F) to the total drift.

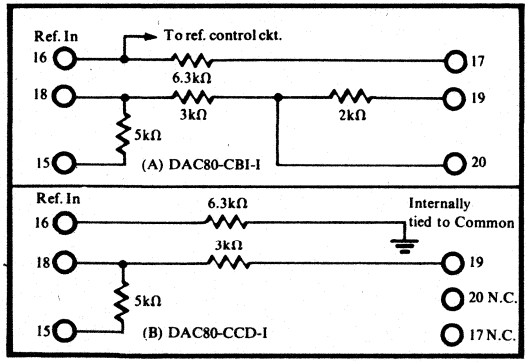


FIGURE 10. Internal Scaling Resistors

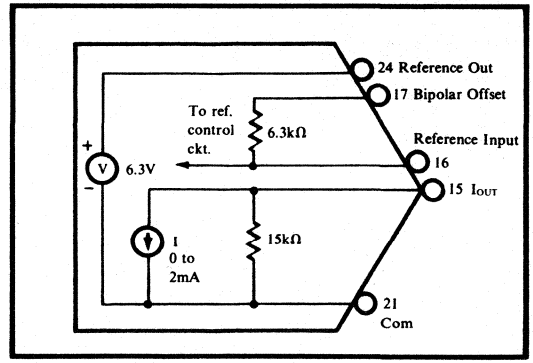


FIGURE 11. DAC80 Current Model Equivalent Output Circuit.

Digital Input Codes	Output Range	Internal Resistance R_{LI}	1% Metal Film External Resistance R_{LS}	1% Metal Film External Resistance R_{LP}	R_{LI} Connections: Connect Pin 15 to	R_{LI} Connections: Connect Pin 18 to	R_{LI} Connections: Connect Pin 20 to	Reference: Connect Pin 16 to	Bipolar Offset: Connect Pin 17 to	Bipolar Offset: R_{LS}	Bipolar Offset: R_{LP}
CSB	0 to -2V	0.968kΩ	105Ω	N/A	20	19 & R_{LS}	15	24	Com (21)	Between Pin 18 & Com (21)	N/A
CCD	0 to -2V	1.875kΩ	N/A	36.5kΩ	19	Com (21)	N.C.	24	N.C.	N/A	Between Pin 15 & 21
COB or CTC	±1V	1.2kΩ	90.9Ω	N/A	18	19	R_{LS}	24	15	Between Pin 20 & Com (21)	N/A

TABLE V. DAC80-XXX-I Resistive Load Connections.

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 12 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA \left(\frac{15k \times R_L}{15k + R_L}\right)$$

Where R_L max = 1.36kΩ
and V_{OUT} max = -2.5V

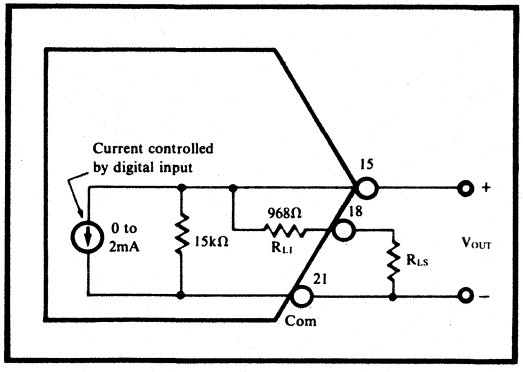


FIGURE 12. Equivalent Circuit DAC80-CBI-I connected for Unipolar Voltage Output with Resistive Load.

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown in Table V to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. With $R_{LS} = 0$, V_{OUT} = -1.82V.

CCD Input Code: Connect the internal scaling resistors as shown in Table V and add an external metal film resistor (R_{LP}) in parallel as shown in Figure 13 to obtain a 0 to -2 volt full scale output voltage range for CCD input codes.

$$\text{With } R_L = \frac{R_{LI} \times R_{LP}}{R_{LI} + R_{LP},}$$

$$V_{OUT} = -1.25mA \left(\frac{15.6k \times R_L}{15.6k + R_L}\right)$$

If $R_{LP} = \infty$, V_{OUT} = -2.08V

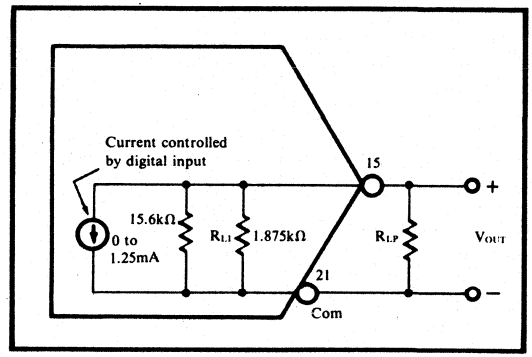


FIGURE 13. DAC80-CCD-I Connected for Voltage Output with Resistive Load

DRIVING A RESISTOR LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 14, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA \left(\frac{R_L \times 4.44k}{R_L + 4.44k}\right)$$

Where R_L max = 5.72kΩ
V_{OUT} max = ±2.5V

To achieve specified drift, connect the internal scaling resistors (R_{LI}) as shown in Table V for the COB or CTC codes and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V.

With $R_{LS} = 0$, $V_{OUT} = \pm 0.944V$.

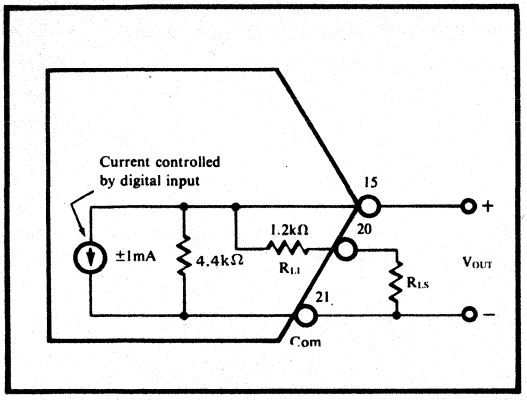


FIGURE 14. DAC80-CBI-I Connected for Bipolar Output Voltage with Resistive Load.

DRIVING AN EXTERNAL OP AMP

The current model DAC80 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. See Figure 15.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current model DAC80 provides output voltage ranges the same as the voltage model DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table VI.

Output Range	Digital Input Codes	Connect Ⓐ to	Connect Pin 17 to	Connect Pin 19 to	Conect Pin 16 to
±10V	COB or CTC	19	15	Ⓐ	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24
0 to +10V	CCD	19	N.C.	Ⓐ	24

TABLE VI. Voltage Range of Current Output DAC80.

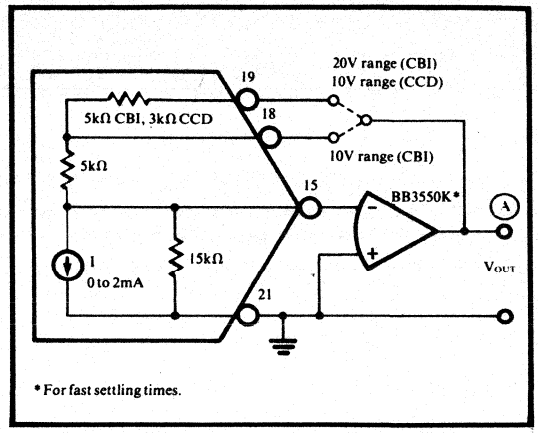


FIGURE 15. External Op Amp - Using Internal Feedback Resistors.

OUTPUT LARGER THAN 20V RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and -2mA for unipolar voltage ranges. See Figure 16. Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50 ppm/°C + R_F drift to total drift.

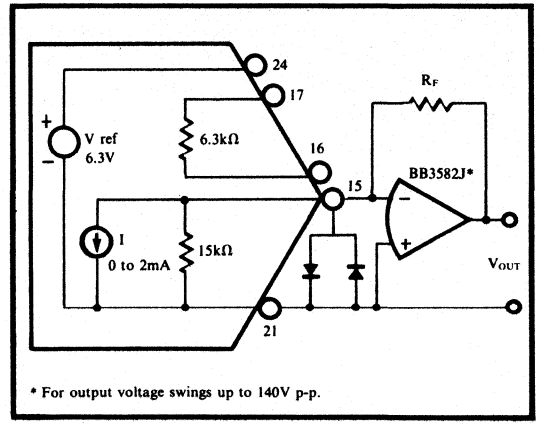


FIGURE 16. External Op Amp - Using External Feedback Resistors.

COMPUTING TOTAL ACCURACY OVER TEMPERATURE

The accuracy drift with temperature of a DAC80 consists of three primary components: Gain drift, unipolar or bipolar offset drift, and linearity drift. To obtain the worst case accuracy drift, most users would assume that all drift errors are random and would simply add them algebraically. However, the worst case accuracy drift for a DAC80 operating in the bipolar mode is about one-half of the algebraic sum of the individual drift errors.

To explain this fact, it is necessary to consider the unipolar and bipolar modes of operation separately. Note that the linearity drift of both modes is negligible. (Total linearity error is less than ±1/2 LSB over 0°C to +70°C.)

In the unipolar mode of operation, offset drift (±1 ppm/°C) is due primarily to voltage offset drift of the output op amp and, to a lesser extent, to the leakage current through the quad current switches. Gain drift consists of several components: 1) ±10 ppm/°C due to ratio drift of current weighting resistors to the reference resistor and current switch V_{BE} to the reference transistor (refer to Model 4550 data sheet); and 2) ±20 ppm/°C due to the zener reference. The sum of these two components, ±30 ppm/°C, is the maximum gain drift.

Because the parameters described could all drift in the same direction, the worst case accuracy drift in the unipolar mode is simply the sum of the components, or ±31 ppm/°C.

In the bipolar mode the major portion (67%) of gain drift is due to the zener reference. The gain and offset drifts caused by reference drift are always in opposite directions. Therefore, the accuracy drift will be the difference rather than the sum of these drifts.

First, consider the effect of reference variations on offset drift. Figure 17 shows a simplified circuit diagram of a DAC80 operating in the bipolar mode with all bits off. The current switch leakage current is negligible, so

$$V_{\text{-FULL SCALE}} = -\frac{R_F}{R_{BPO}} \cdot V_{REF}$$

$$= -\frac{10k}{6.3k} \cdot 6.3V = -10 \text{ volts}$$

This equation shows that if V_{REF} increases, the output voltage will decrease and vice versa. If the V_{REF} drift is

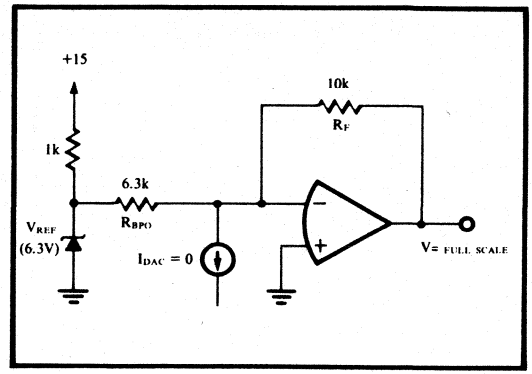


FIGURE 17. Simplified Diagram of DAC80 with "All Bits Off" Operating in Bipolar ±10V Range.

+20 ppm/°C, this is equivalent to (+20 ppm/°C) x (+6.3V) = +126μV/°C. This will result in a voltage drift at the amplifier output of

$$\frac{\Delta V_{\text{-FS}}}{\Delta T} = -\frac{R_F}{R_{BPO}} \cdot \frac{\Delta V_{REF}}{\Delta T}$$

$$= -\frac{10k}{6.3k} \cdot 126\mu V/^{o}C = -200\mu V/^{o}C.$$

Since the DAC80 is operating in the ±10V range this is equivalent to (-200μV/°C) ÷ (20V range) = -10 ppm of FSR/°C.

Now consider the effect of reference changes on gain drift. When all of the bits are turned on it can be shown that:

$$\frac{\Delta V_{\text{+FULL SCALE}}}{\Delta T} = +\frac{R_F}{R_{BPO}} \cdot \frac{V_{REF}}{\Delta T}$$

$$= +\frac{10k}{6.3k} \cdot 126\mu V/^{o}C = +200\mu V/^{o}C$$

$$\text{and } \frac{+200\mu V/^{o}C}{20V \text{ Range}} = +10 \text{ppm}/^{o}C \text{ of FSR.}$$

This result indicates that the drift of the minus full scale voltage will be equal in magnitude to, and in the opposite direction of, the drift of the plus full scale voltage and that

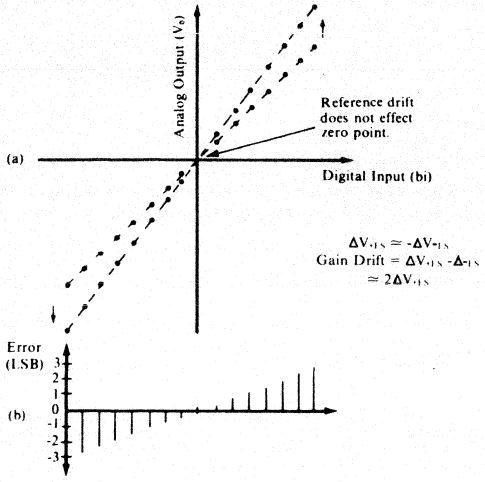


FIGURE 18. (a) Effect of a Positive Reference Drift on the Ideal D/A Transfer Function; (b) Error Distribution Due to Reference Voltage Drift in a DAC80.

zener reference variations have virtually no effect on the zero point. (See Figure 18) This equation also indicates that the gain drift is equal to the V_{REF} drift in ppm/°C, and the magnitude of the minus full scale drift and plus full scale drift is equal to one-half of the V_{REF} drift.

Using this relationship, the worst case accuracy drift for a bipolar DAC80 can be computed. The maximum TCR of the zener reference is ±20ppm/°C. The gain drift due to the reference then is also ±20ppm/°C. The full scale drift and bipolar offset drift are each half that amount or ±10ppm/°C. The maximum gain and offset drifts of the DAC80, exclusive of the reference, are ±10 and ±5ppm/°C respectively. Adding this to the full scale drift due to the reference gives a worst case total accuracy drift of ±25ppm/°C. (Random drifts, which these are, can be in the same direction, so they add directly.) This is much less that the total drift obtained by simply adding the maximum gain and bipolar offset drifts (±45ppm/°C). The maximum zero point drift is equal to one-half of the gain drift exclusive of the reference plus the offset drift exclusive of the reference, or ±10ppm of FSR/°C.

The DAC80 is specified over a 0°C to +70°C temperature range giving a maximum excursion from room temperature (+25°C) of 45°C. Assuming that gain and offset errors have been adjusted to zero at room temperature,

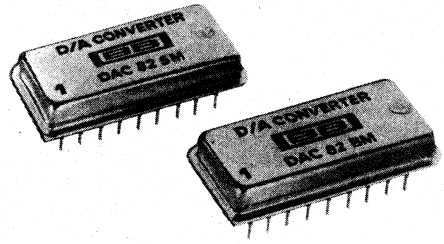
total worst case accuracy error
= Linearity error + Accuracy drift x ΔT
= ±0.01% + ±25ppm/°C (45°C) (100)
= ±0.12%;

total worst case bipolar zero point error
= Bipolar zero drift x ΔT
= ±10ppm of FSR% (45°C) (100)
= ±0.045%

ORDERING INFORMATION

DAC80	X	–	XXX	–	X
Low Cost 12 Bit D/A Converter Family Example: DAC80-CBI-V Binary DAC80 with voltage output	Z = Wide Supply Range Blank = Standard		INPUT CODE CBI = Complementary 12 bit binary CCD = Complementary 3 digit BCD		OUTPUT V = Voltage I = Current

BURR-BROWN



DAC82

8-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 8-BIT RESOLUTION/LINEARITY
- NO EXTERNAL ADJUSTMENTS REQUIRED FOR ±1LSB ACCURACY
- INTERNAL REFERENCE AND SCALING RESISTORS
- 2-QUADRANT MULTIPLYING WITH EXTERNAL REFERENCE
- HERMETIC, DUAL-IN-LINE PACKAGE
- OPERATION OVER -55°C/+125°C

DESCRIPTION

The DAC82 is an 8-bit digital-to-analog converter with voltage and current outputs. Packaged in an 18-pin metal DIP, it is complete with its own internal reference and scaling resistors. When used with a variable, external reference, the DAC82 will multiply in two quadrants. Two versions are available: the DAC82BM (-25°C to +85°C) and the DAC82SM (-55°C to +125°C). Both offer ±1LSB absolute accuracy at room temperature with no external adjustments required and nonlineaity is guaranteed to be within ±1/2LSB over the specified temperature ranges. The small size of the DAC82 makes it an ideal choice for applications where space or weight is at a premium such as aircraft instrumentation, portable instruments, or CRT displays.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-369A

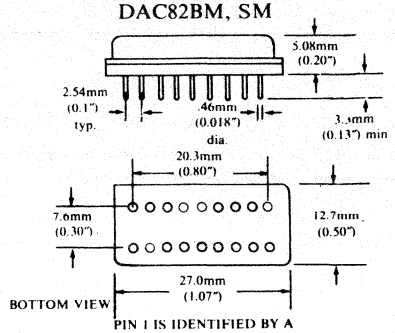
Printed in U.S.A. July, 1978

ELECTRICAL SPECIFICATIONS

MODEL	DAC82KG DAC82BM	DAC82SM	UNITS
DIGITAL INPUT			
Resolution	8	8	Bits
Logic Levels (TTL compatible)			
Logic "1"	$+2 < e_d < +5.5$ at $+40\mu A$		V
Logic "0"	$0 < e_d < +0.8$ at -1.0mA		V
TRANSFER CHARACTERISTICS			
ACCURACY			
Linearity Error at 25°C (max)	±0.16	±0.16	% of FSR
-25°C to +85°C (max)	±0.2		% of FSR
-55°C to +125°C (max)		±0.2	% of FSR
Differential Linearity Error	±0.5	±0.5	LSB
Gain Error	±0.1	±0.1	%
Offset Error	±0.05	±0.05	% of FSR
Total Accuracy Error (max)	±1	±1	LSB
Monotonicity Temp Range	-25 to +85	-55 to +125	°C
DRIFT			
Gain (max)			
-25°C to +85°C	±50		ppm/°C
-55°C to +125°C		±35	ppm/°C
Offset			
Unipolar			
-25°C to +85°C	±1		ppm of FSR/°C
-55°C to +125°C		±1	ppm of FSR/°C
Bipolar (max)			
-25°C to +85°C	±20		ppm of FSR/°C
-55°C to +125°C		±15	ppm of FSR/°C
CONVERSION SPEED			
Voltage Output			
Settling time to ±0.2% of FSR			
For FSR change			
with 10kΩ Feedback	2.5		µsec
with 5kΩ Feedback	2.0		µsec
For 1 LSB change	0.5		µsec
Slew Rate	20		V/µsec
Current Output			
Settling time to ±0.2%			
For FSR change			
10 to 100Ω load	250		nsec
1kΩ load	350		nsec
OUTPUT			
ANALOG OUTPUT			
Voltage Output			
Ranges	±2.5, ±5, ±10, +5, +10		Volts
Output Current, min	±5		mA
Output Impedance (DC)	0.05		Ω
Current Output			
Ranges	±0.8, 0 to -1.6		mA
Output Impedance - Bipolar	1.8		kΩ
Unipolar	2.0		kΩ
Compliance	±4.0V		Volts
INTERNAL REFERENCE VOLTAGE			
Magnitude	+6.3		Volts
Tempco of Drift, max	±20		ppm/°C
POWER SUPPLY SENSITIVITY			
+15V Supply	±0.02		% of FSR/%Vs
-15V Supply	±0.002		% of FSR/%Vs
POWER SUPPLY REQUIREMENTS			
Rated Voltage	±15		Volts
Range	±14.0 to ±16.0		Volts
Supply Drain (No load)			
+15V	15		mA
-15V	10		mA
TEMPERATURE RANGE			
Specification	-25 to +85	-55 to +125	°C
Operating (double above drift specs)	-55 to +125	-55 to +125	°C
Storage	-55 to +125	-55 to +125	°C

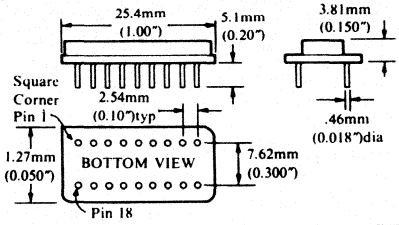
MECHANICAL

DAC82BM, SM

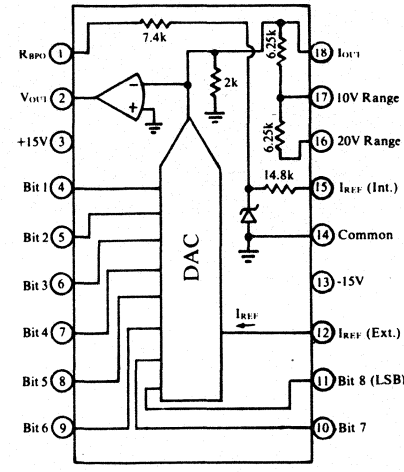


CONNECTOR: None
CASE: Kovar, Gold or Nickel plated (BM, SM) Ceramic (KG)
PIN: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
HERMETICITY: Conform to Mil-Std-883, Method 1014. Gross Leak (Condition C, Step 1, Fluorocarbon) Fine Leak (Condition A, Helium, 5×10^{-7} cc/sec) (BM, SM only)

DAC82KG



CONNECTION DIAGRAM



DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC82 accepts digital inputs in complementary binary (CBI) format and may be connected for complementary straight binary (CSB) or complementary offset binary (COB) operation. By using one external inverter, the user can operate the DAC82 in the complementary two's complement (CTC) mode.

DIGITAL INPUT CODES	OUTPUT RANGE			
	VOLTAGE*		CURRENT	
	0 to +10V	±10V	0 to 1.6mA	±0.8mA
MSB LSB				
0 0 0 0 0 0 0 0	+9.961V	+9.922V	-1.594mA	-0.794mA
0 1 1 1 1 1 1 1	+5.000V	0.000V	-0.800mA	0.000mA
1 0 0 0 0 0 0 0	+4.961V	-78.12mV	-0.792mA	+6.248μA
1 1 1 1 1 1 1 1	0.000V	-10.000V	0.000mA	+0.800mA
one LSB	39.06mV	78.12mV	6.248μA	6.248μA

* To obtain values for other binary (CBI) ranges:
0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

TABLE I. Digital Input and Analog Output Relationship.

ACCURACY

LINEARITY

The LINEARITY of a D/A converter is the true measure of its performance. The DAC82 analog output will not vary by more than ±1/2 LSB from an ideal straight line drawn between the end points (all 1's and all 0's) over the specified temperature range.

DIFFERENTIAL LINEARITY

The DIFFERENTIAL LINEARITY error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A DIFFERENTIAL LINEARITY error specification of ±1/2 LSB means that the output voltage can change anywhere from 1/2 LSB to 3/2 LSB when the input changes from one adjacent digital state to the next.

DRIFT

GAIN DRIFT

GAIN DRIFT is a measure of the change in the analog output over temperature expressed in parts per million per °C (ppm/°C). The GAIN DRIFT is determined by testing the end point differences at the high and low temperature extremes and at 25°C for each model, calculating the GAIN ERROR with respect to the 25°C value, and dividing by the temperature change.

OFFSET DRIFT

OFFSET DRIFT is a measure of the actual change in output voltage at zero volts output over the specified temperature range. The offset voltage is measured at the temperature extremes, and the maximum change referenced to 25°C is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time is the time required for the output to enter and remain in an error band equal to ±0.2% of full scale range measured from the time the digital input is changed. Typical settling time values for full scale changes are a function of the load resistor and are shown in the figure below.

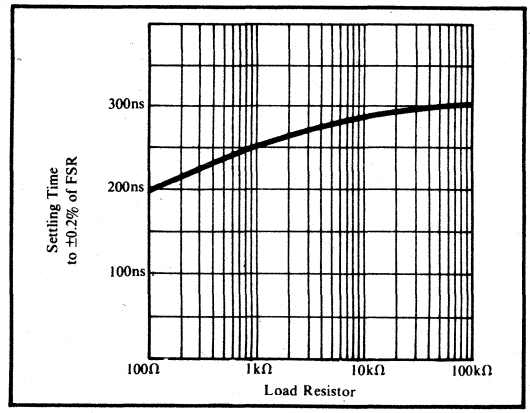


FIGURE 1. Settling Time for FSR Change vs Load.

COMPLIANCE

The COMPLIANCE VOLTAGE of the DAC82 is the maximum voltage swing allowed on the current output in order to maintain the specified accuracy. It is -4.0 to +4.0 volts for the unipolar and bipolar current ranges.

POWER SUPPLY SENSITIVITY

POWER SUPPLY SENSITIVITY is a measure of the effect of a power supply voltage change on the D/A converter output. It is defined as a percent of FSR/percent of change in either the +15 volt or -15 volt power supplies about the nominal power supply voltages. Figure 2 shows Power Supply Rejection vs Frequency.

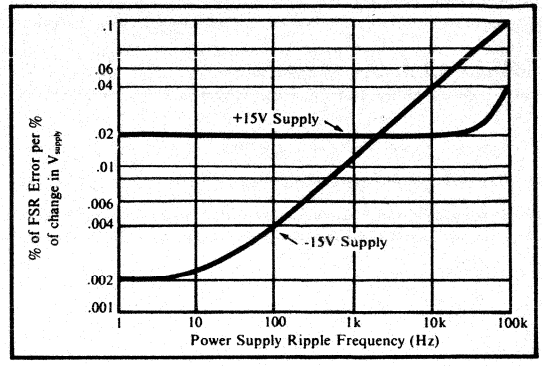


FIGURE 2. Power Supply Rejection vs. Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

DECOUPLING

For best performance and noise rejection, power supply decoupling capacitors should be connected as shown in Figure 3. These capacitors should be located close to the DAC82 and should be tantalum or electrolytic types bypassed with a 0.01 μF ceramic capacitor for best high frequency performance.

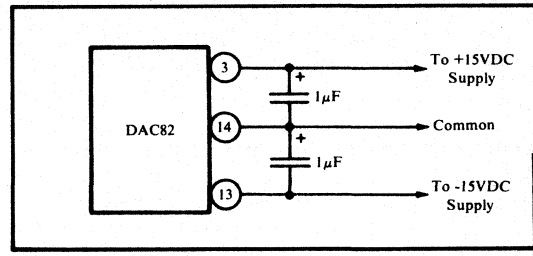


FIGURE 3. Recommended Power Supply Decoupling.

OPERATION IN THE CURRENT OUTPUT MODE

On the current output pin, the DAC82 provides a unipolar output current of 0 to -1.6mA and a bipolar output current of ±0.8mA. Refer to Figure 4 and Table II for proper connections. In applications requiring the use of the DAC82 in the current output mode, such as an A/D converter, the internal scaling resistors should be used to generate currents corresponding to analog input voltages.

OUTPUT RANGE	CONNECT PIN 1 TO:
0 to -1.6mA	N.C.
±0.8mA	Pin 18

TABLE II. Connections for Current Output Mode.

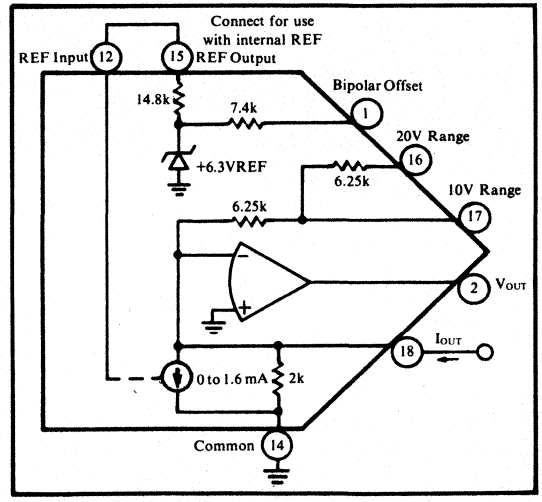


FIGURE 4. Current Output Mode Connection Diagram.

DRIVING AN EXTERNAL OP AMP

UNIPOLAR OR BIPOLAR - UP TO 20V OUTPUT RANGE

The DAC82 will drive the summing junction of an op amp (the op amp being used as a current to voltage converter) to produce an output voltage (see Figure 5).

$$V_{OUT} = -I_{OUT} \times R_F$$

where I_{OUT} is the DAC82 output current and R_F is the feedback resistor. The internal feedback resistors should be used to maintain the temperature drift specification. Refer to Table III and Figure 5 for proper connections.

OUTPUT RANGE	DIGITAL INPUT CODES	CONNECT Ⓐ TO	CONNECT PIN 1 TO	CONNECT PIN 16 TO
±10V	COB or CTC	16	18	Ⓐ
±5V	COB or CTC	17	18	N.C.
±2.5V	COB or CTC	17	18	18
0 to +10V	CSB	17	Common	N.C.
0 to +5V	CSB	17	Common	18

TABLE III. Voltage Ranges of Current Output DAC82 with External Op Amp.

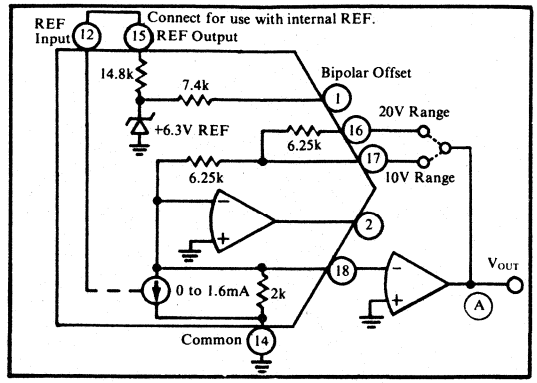


FIGURE 5. External Op Amp - Using Internal Feedback Resistors.

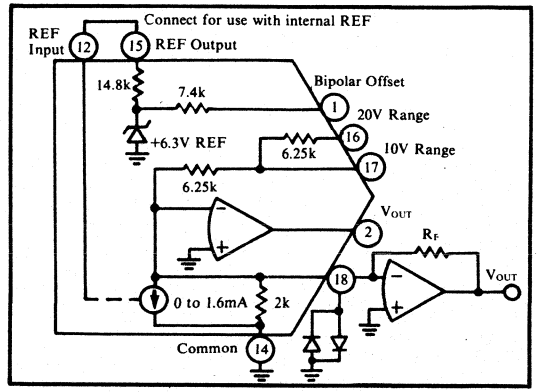


FIGURE 6. External Op Amp - Using External Feedback Resistors.

OUTPUTS LARGER THAN 20 VOLT RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±0.8mA for bipolar voltage ranges, and 0 to -1.6mA for unipolar voltage ranges (see Figure 6). Use protection diodes when a high voltage op amp is used.

VOLTAGE OUTPUT OPERATION USING INTERNAL AMPLIFIER

The DAC82 contains internal scaling resistors to provide a wide range of output voltage ranges. These resistors may be connected to provide 3 bipolar output ranges of ±10, ±5, or ±2.5 volts or two unipolar output voltage ranges of 0 to +5 or 0 to +10 volts. Gain and offset drift errors are minimized since these scaling resistors are an integral part of the DAC. Connections for DAC82 output voltage ranges are shown in Table IV and Figure 7 below.

OUTPUT RANGE	DIGITAL INPUT CODES	CONNECT PIN 2 TO	CONNECT PIN 1 TO	CONNECT PIN 16 TO
±10V	COB or CTC	16	18	2
±5V	COB or CTC	17	18	N.C.
±2.5V	COB or CTC	17	18	18
0 to +10V	CSB	17	Common	N.C.
0 to +5V	CSB	17	Common	18

TABLE IV. Voltage Ranges of Current Output DAC82 with External Op Amp.

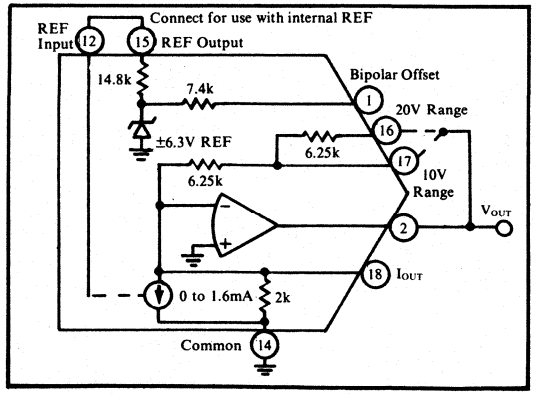


FIGURE 7. Voltage Output Using Internal Amplifier.

OPERATION AS MULTIPLYING DAC

By using an external voltage reference, the DAC82 can be connected as a multiplying DAC, such that the analog output represents the product of the digital input and the analog reference input. To operate the DAC82 as a two quadrant MDAC, connect the unit as shown in Figure 8. If R2, the bipolar offset resistor, is replaced with an open circuit, the DAC will operate in one quadrant. Table V below shows the digital input and analog output relationships for one quadrant and two quadrant multiplication and Figure 8 shows the connection for output voltage or output current. Since the absolute temperature coefficient of the internal feedback resistors (6.25k) is typically 30 ppm/°C, improved temperature stability can be achieved by using an external 13.5k resistor connected between pins 2 and pins 18, making no connection to pins 16 or 17.

DIGITAL INPUT CODES	OUTPUT RANGE			
	VOLTAGE*		CURRENT	
MSB LSB	0 to +10V	±10V	0 to -1.6mA	±0.8mA
00000000	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.9961)$	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.9922)$	$\frac{(4\ V_R)}{(R_1)}(0.9961)$	$\frac{(4\ V_R)}{(R_1)}(0.9922)$
0111111	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.5000)$	0.0000	$\frac{(4\ V_R)}{(R_1)}(0.5000)$	0.0000
10000000	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.4961)$	$\frac{(4\ V_R)(R_F)}{(R_1)}(-0.0078)$	$\frac{(4\ V_R)}{(R_1)}(0.4961)$	$\frac{(4\ V_R)}{(R_1)}(-0.0078)$
11111111	0.0000	$\frac{(4\ V_R)(R_F)}{(R_1)}(-1)$	0.0000	$\frac{(4\ V_R)}{(R_1)}(-1)$
1 LSB	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.0039)$	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.0078)$	$\frac{(4\ V_R)}{(R_1)}(0.0039)$	$\frac{(4\ V_R)}{(R_1)}(0.0078)$

TABLE V. Digital Input and Analog Output Relationship for Multiplying Configuration.

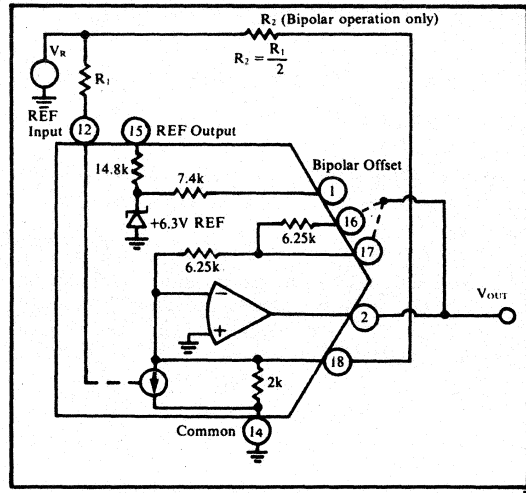


FIGURE 8. Connection for Multiplying Mode.

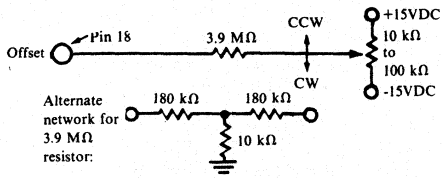
D/A DAC82

OPTIONAL EXTERNAL OFFSET AND GAIN ADJUSTMENTS

The DAC82 has been laser trimmed at the factory to insure absolute accuracy of 1 LSB at +25°C. However, externally connected offset and gain potentiometers may be used to null these error components to zero. If these adjustments are not used, simply leave the pins open. Adjustment networks should be located physically closed to the DAC82 to minimize signal pickup.

OFFSET ADJUSTMENT

For unipolar operation, apply the digital input code that should give zero volts output and adjust the OFFSET potentiometer for zero volts output. For bipolar operation, apply the digital input code that should give the maximum negative voltage output. Example: If the FULL SCALE RANGE is connected for 20 volts, then the maximum negative voltage output is -10 volts. See Table I for corresponding codes.



Range of adjustment: ±0.2% of FSR

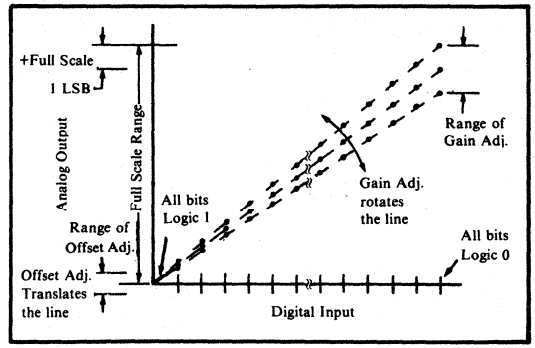
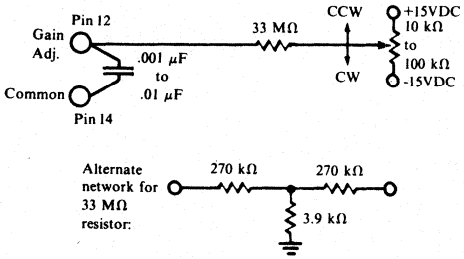


FIGURE 9. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter.

GAIN ADJUSTMENT

For either unipolar or bipolar D/A converters, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. The positive full scale voltages for the DAC82 are given in Table V.



Range of Offset Adjustment: ±0.2% of FSR

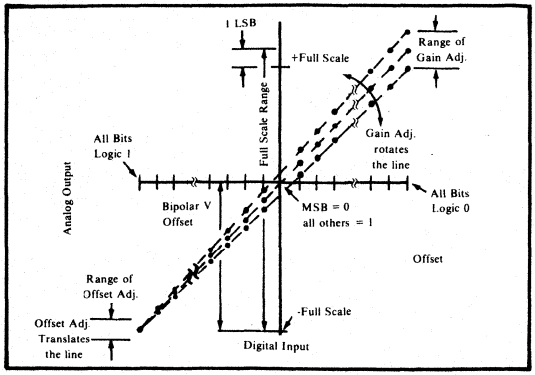


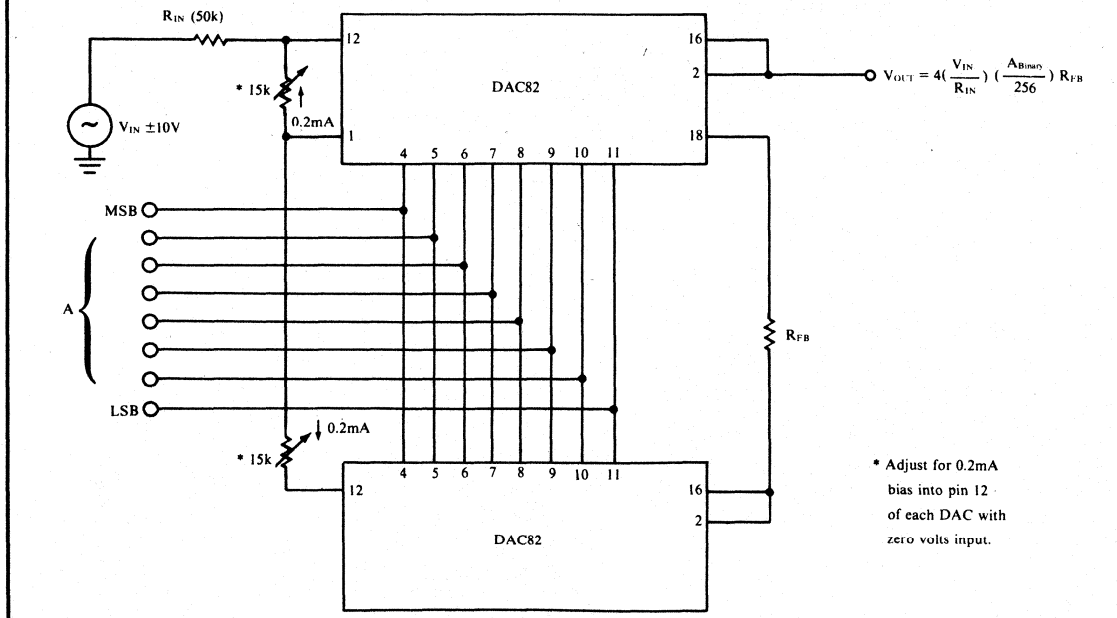
FIGURE 10. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A Converter.

APPLICATIONS

Two DAC82's can be connected as shown to construct a digitally-controlled attenuator which will accept bipolar input voltages. Since the input to the DAC is a summing junction (pin 12), input voltages greater than ±10V can be used if R_{IN} is increased proportionately. The transfer function is:

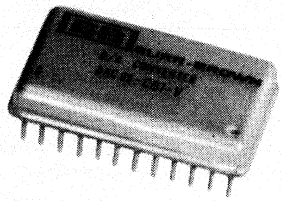
$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{4\,R_{FB}}{R_{IN}}\right)\left(\frac{A_{BINARY}}{256}\right)$$

To remove initial gain errors, the two 15k resistors should be adjusted such that 0.2 mA flows into pin 12 of each DAC82 when $V_{IN} = 0$.



DIGITALLY CONTROLLED ATTENUATOR WITH BIPOLAR INPUT

BURR-BROWN



DAC85

Hybrid Microcircuit DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 12-BIT RESOLUTION
- LASER-TRIMMED TO ±1/2LSB LINEARITY
- CURRENT OR VOLTAGE OUTPUT
- FAST SETTLING - 300nsec to ±.01% (Current Output Model)
- HERMETIC DUAL-IN-LINE PACKAGE
- LOW COST

DESCRIPTION

The DAC85 12-bit D/A converter offers quality performance usually found in larger modular units. Housed in a 24-pin dual-in-line metal case, this D/A converter is complete with internal reference and output amplifier and is engineered to preserve the performance normally found only in much larger, higher cost modular units, while providing sealed protection from rugged environments.

Highly stable laser-trimmed thin-film resistors and our Model 4550 quad current switches provide low nonlinearities of ±0.012% over 0°C to 70°C (DAC85C) and ±0.012% over -25°C to +85°C (DAC85 and DAC85LD) operating temperature ranges. Current output models settle to ±0.01% in 300nsec while voltage output models settle to ±0.01% in 5μsec, permitting throughput rates as high as 3MHz for full scale range changes.

The small size of the DAC85 makes it an ideal choice as the heart of your A/D converter design or for applications where space or weight is at a premium, such as CRT displays, aircraft instrumentation and portable instruments. The wide choice of performance models allows you to choose the right unit for your application and budget.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-300D

Printed in U.S.A. July, 1978

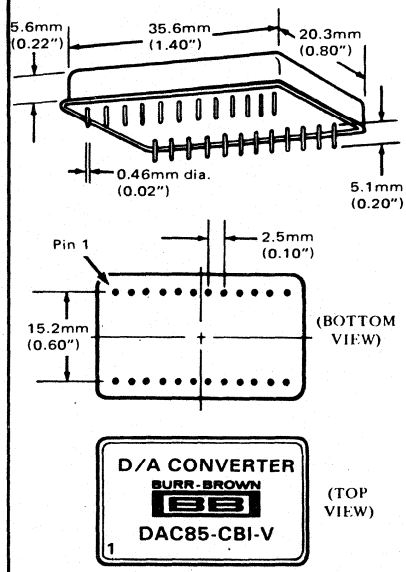
SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	DAC85C		DAC85		DAC85LD	Units
Binary	CBI		CBI		CBI	
Decimal		CCD		CCD		
INPUT						
DIGITAL INPUT						
Resolution	12	3	12	3	12	Bits / Digits
Logic Levels (TTL compatible)						
Logic "1"	+2 < e_d < +5.5 at +40 µA					V
Logic "0"	0 < e_d < +0.8 at -1.0 mA					V
TRANSFER CHARACTERISTICS						
ACCURACY						
Linearity Error @ 25°C (max)	±1/2	±1/4	±1/2	±1/4	±1/2	LSB
0°C to +70°C (max)	±1/2	±1/2				LSB
-25°C to +85°C (max)			±1/2	±1/2	±1/2	LSB
-55°C to +125°C (max)						LSB
Differential Linearity Error	±1/2					LSB
Gain Error(1)	±0.1					%
Offset Error(1)	±0.05					% of FSR(2)
Minimum Temperature Range for Guaranteed Monotonicity	0 to +70		-25 to +85			°C
DRIFT(3)						
Gain						
0°C to +70°C (max)	±20		±20		±10	ppm/°C
-25°C to +85°C (max)	—		±20		±10	ppm/°C
-55°C to +125°C (max)	—		—		—	ppm/°C
Offset						
Unipolar 0°C to +70°C	±1					ppm of FSR/°C
-25°C to +85°C			±1		±1	ppm of FSR/°C
-55°C to +125°C						ppm of FSR/°C
Bipolar 0°C to +70°C (max)	±10					ppm of FSR/°C
-25°C to +85°C(max)			±10		±5	ppm of FSR/°C
-55°C to +125°C(max)						ppm of FSR/°C
CONVERSION SPEED						
Voltage Models						
Settling time to ±0.01% of FSR for FSR change						
with 10 kΩ Feedback	5					µsec
with 5 kΩ Feedback	3					µsec
for 1 LSB change	1.5					µsec
Slew Rate	20					V/µsec
Current Models						
Settling time to ±0.01% of FSR for FSR change						
10 to 100 Ω load	300					nsec
1 kΩ load	1					µsec
OUTPUT						
ANALOG OUTPUT						
Voltage Models						
Ranges – CBI Units	±2.5, ±5, ±10, +5, +10					V
CCD Units	+10					V
Output Current (min)	±5					mA
Output Impedance (dc)	0.05					Ω
Current Models						
Ranges	±1, -2					mA
Output Impedance - Bipolar	4.4					kΩ
Unipolar	15					kΩ
Compliance	±2.5					V
Internal Reference Voltage (V_r)	6.3					V
Max. External Current(4)	200					µA
Tempco of Drift (max)	±10	±10	±10	±10	±5	ppm of V_r/°C
POWER SUPPLY SENSITIVITY						
+15V Supply	±0.02					%of FSR/%Vs
-15 and +5V Supplies	±0.002					%of FSR/%Vs
POWER SUPPLY REQUIREMENTS						
Rated Voltage	±15 and +5					V
Range	±14.5 to ±15.5 and +4.75 to +15.5(5)					V
Supply Drain						
±15 V (including 5 mA load)	±25					mA
+5 V	+20					mA
TEMPERATURE RANGE						
Specification	0 to +70		-25 to +85			°C
Operating(double above drift specs)	-25 to +85		-25 to +85			°C
Storage	-55 to +125		-55 to +125			°C

1. Adjustable to zero with external trim potentiometer.
2. FSR means "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc.
3. To maintain drift spec internal feedback resistors must be used for current output models.
4. With no degradation of specifications.
5. Operating logic supply at +15.5V increases power dissipation 200mW.

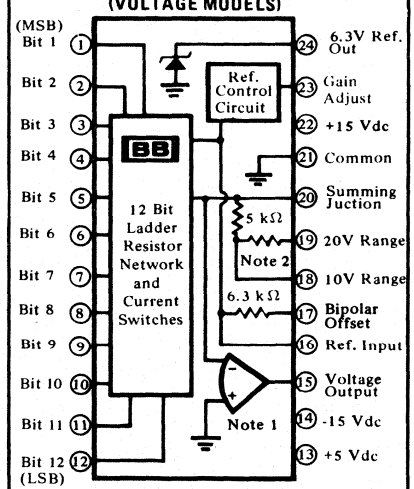
MECHANICAL



CASE: Kovar, Gold or Nickel Plated
Mating Connector 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
WEIGHT: 8.4 grams (0.3 oz.)

CONNECTION DIAGRAM

(VOLTAGE MODELS)



Note 1: Amplifier not included in current output models.
Note 2: 3 kΩ for CCD models
5 kΩ for CBI models

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC85 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The CBI model may be user connected for any one of three complementary binary codes: CSB, CTC, or COB.

	DIGITAL INPUT	ANALOG OUTPUT		
	MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
CBI Models	000000000000	+Full Scale	+Full Scale	-LSB
	011111111111	+1/2 Full Scale	Zero	-Full Scale
	100000000000	Mid Scale -1 LSB	-1 LSB	+Full Scale
	111111111111	Zero	-Full Scale	Zero
CCD Models	MSB LSB	CCD Complementary Coded Decimal - 3 Digits		
	0110 0110 0110	+Full Scale		
	1111 1111 1111	Zero		

* Invert the MSB of the COB code with an external inverter to obtain CTC code.

TABLE 1. Digital Input Codes.

ACCURACY

LINEARITY

The linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC85 and DAC-85C is specified over the entire specification temperature ranges. The definition of this specification means that the analog output will not vary by more than ±1/2 LSB (DAC85) or ±1 LSB (DAC85C) from an ideal straight line drawn between the end points (all bits ON and all bits OFF) over the specified operating temperature range.

DIFFERENTIAL LINEARITY

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2 LSB means that the output voltage can change anywhere from 1/2 LSB to 3/2 LSB when the input changes from one adjacent input state to the next.

DRIFT

GAIN DRIFT

GAIN DRIFT is a measure of the change in the full scale range analog output over temperature expressed in parts per million per °C (ppm/°C). The GAIN DRIFT is determined by testing the end point differences at -25°C or 0°C, +25°C and +70°C or +85°C for each model and calculating the GAIN ERROR with respect to the 25°C value and dividing by the temperature change. This specification is expressed in ppm/°C.

OFFSET DRIFT

OFFSET DRIFT is a measure of the actual change in the output with all bits OFF (V_{OUT}^{OFF}) over the specified temperature range. V_{OUT}^{OFF} is measured at -25°C or 0°C, +25°C and +70°C or +85°C. The maximum change in OFFSET is referenced to the OFFSET at 25°C divided by the temperature range. This drift is expressed in parts per million of full scale range per °C. (ppm of FSR/°C).

SETTLING TIME

The settling time for each model DAC85 is the total time (including slew time) for the output to settle to within an error band about its final value after a change in the input.

VOLTAGE OUTPUT MODELS

Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V and 10V and also for a 1 LSB change. The 1 LSB change is measured at the major carry (0111 ... 11 to 1000 ... 00) since this is the point where the worst case settling time occurs.

CURRENT OUTPUT MODELS

Two settling times are specified for current output models; each specified settling time to ±0.01% of FSR is given for the DAC85 current models connected with two different resistive loads – i.e., 10 to 100 ohms and 1000 to 1875 ohms. Internal resistors are provided for connecting nominal load resistances of approximately 1000 ohms to 1800 ohms for output voltage ranges of ±1 volt and 0 to -2 volts. (See Table 4)

COMPLIANCE

The compliance voltage of the DAC85 is the maximum voltage swing allowed on the current output mode in order to maintain the specified accuracy; it is ±2.5 volts for the bipolar current range of ±1.0 mA and is -2.5 volts for the unipolar current range of 0 to -2 mA. The maximum safe voltage swing allowed with no damage to the DAC85 output is ±5 volts for current output models.

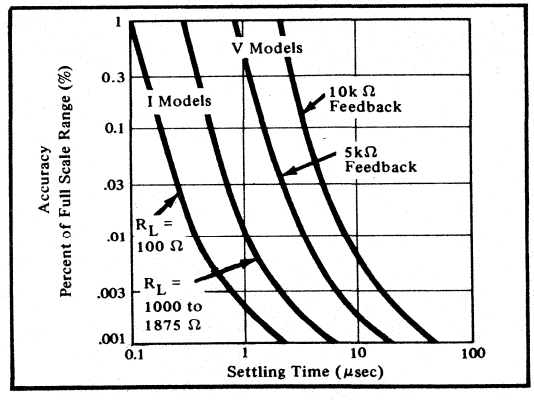


FIGURE 1. Full Scale Range Settling Time vs. Accuracy.

POWER SUPPLY SENSITIVITY

POWER SUPPLY SENSITIVITY is a measure of the effect of a power supply voltage change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the +15 volt or -15 volt and +5 power supplies about the nominal power supply voltages. Figure 2 shows Power Supply rejection vs. frequency.

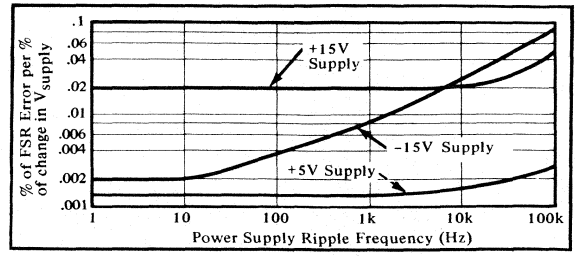


FIGURE 2. Power Supply Rejection vs. Power Supply Ripple Frequency.

REFERENCE SUPPLY

All DAC85 models are supplied with an internal 6.3 volt reference voltage supply. This reference voltage (pin 24) has a tolerance of ±5%, and must be connected to the Reference Input (pin 16) for specified operation.

This reference may also be used externally, but the current drain is limited to 200 μA. An external buffer amplifier is recommended if the DAC85 internal reference will be externally used in order to provide a constant load to the reference supply output.

ORDERING INFORMATION

DAC85 XX – XXX – X

- DAC85 XX: 12-Bit D/A Converter Family
  - Example: DAC85-CBI-V DAC85 with voltage output, Binary code and -25°C to +85°C temp. range.
- XX: C = 0 to +70°C Model; LD = Low drift -25°C to +85°C Model; Leave blank for -25°C to +85°C Model
- XXX: INPUT CODE; CBI = Complementary 12-bit binary; CCD = Complementary 3-digit BCD (not Available for DAC85LD)
- X: OUTPUT; V = Voltage; I = Current

OPERATING INSTRUCTIONS

DIGITAL INPUT AND ANALOG OUTPUT RELATIONSHIP

Digital Input Codes	Output Range			
	Voltage *		Current	
	0 to +10V	±10V	0 to -2mA	±1mA
Binary (CBI)				
12 bit resolution				
One LSB	+2.44mV	4.88mV	0.488μA	0.488μA
All bits ON	+9.9976V	+9.9951V	−1.9995mA	-0.9995mA
All bits OFF	Zero	−10.000V	Zero	+1.0000mA
Decimal (CCD)				
3 digit resolution				
One LSB	10 mV		1.25μA	
+ FS bits ON	+9.99V†	N/A	−1.249mA	N/A
All bits OFF	Zero		Zero	

TABLF 2. Ideal Output Voltage and Current.

†Normal full scale range with correct codes; output can go to +12 volts if illegal codes are applied.

*To obtain values for other binary (CBI) ranges:

0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

POWER SUPPLY CONNECTIONS

DECOUPLING

For best performance and noise rejection, power supply decoupling capacitors should be connected as shown in Figure 3. These capacitors should be located close to the DAC85 and should be tantalum or electrolytic types bypassed with a 0.01 μF ceramic capacitor for best high frequency performance.

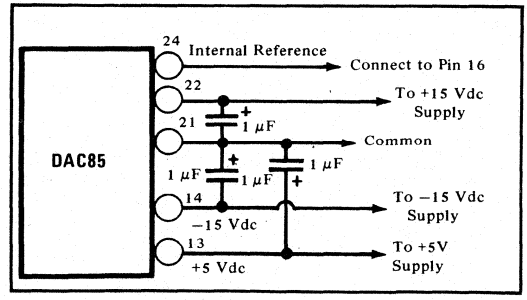


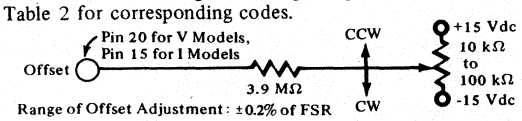
FIGURE 3. Recommended Power Supply Decoupling.

EXTERNAL OFFSET and GAIN ADJUSTMENT

Offset and gain may be trimmed externally by the user with externally connected OFFSET and GAIN potentiometers. If gain and offset adjust circuits are not used, pins 15, 20, and 23 should be connected as described in other sections herein. (Do not ground.) Connection of the potentiometers and the methods of adjutments is as outlined below. Potentiometer resistance values indicated are range of values. Potentiometers should have TCR of 100ppm/°C or less. The 3.9MΩ and 18MΩ resistors can be 20% carbon composition or better. These two resistors should be located close to the DAC85 to prevent signal pickup.

OFFSET ADJUSTMENT

For unipolar (CSB, CCD) D/A converters, apply the digital input code that should give zero volts output and adjust the OFFSET potentiometer for zero volts output. For bipolar (COB, CTC) D/A converters, apply the digital input code that should give the maximum negative voltage output. Example: If the FULL SCALE RANGE is connected for 20 volts, then the maximum negative voltage output is -10 volts. See Table 2 for corresponding codes.



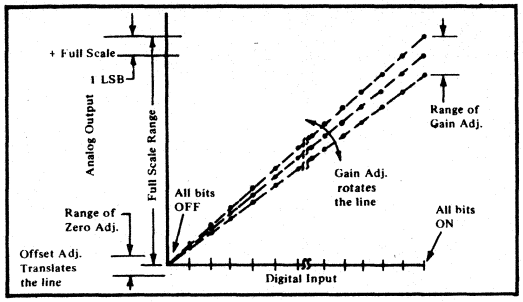
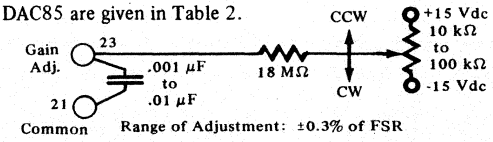


FIGURE 4. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter.

GAIN ADJUSTMENT

For either unipolar or bipolar D/A converters, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. The positive full scale voltages for the DAC85 are given in Table 2.



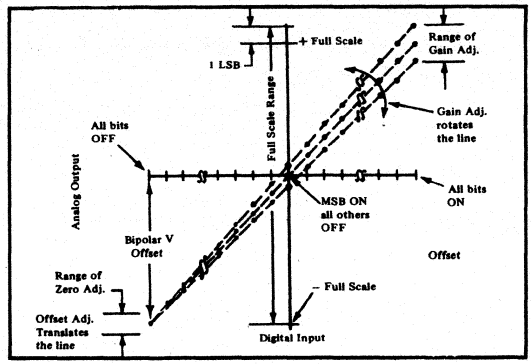


FIGURE 5. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A Converter.

VOLTAGE OUTPUT MODELS

OUTPUT RANGE CONNECTIONS

Internal scaling resistors are provided in the DAC85 to provide a wide range of output voltage range connections. These internal resistors may be connected to provide three bipolar output voltage ranges of ±10, ±5 or ±2.5 volts or two unipolar output voltage ranges of 0 to +5 or 0 to +10 volts. Since these internal scaling resistors are an integral part of the DAC85, gain and offset drift is minimized. Connections for DAC85 output voltage ranges are shown in Table 3.

Settling time for these voltage ranges is specified for a full scale range change, and is 5 microseconds for 8 kΩ or 10 kΩ and 3 microseconds for a 5 kΩ feedback resistor.

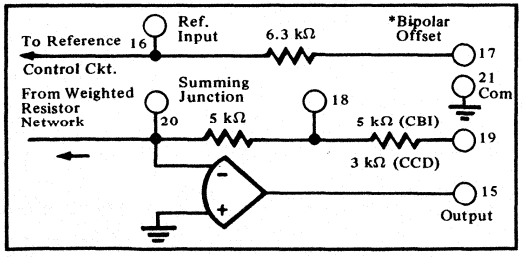


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

*pin 17 not connected for CCD models. The 6.3 kΩ resistor is internally connected to common.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

TABLE 3. Output Voltage Range Connections – Voltage Model DAC85.

CURRENT OUTPUT MODELS

Internal resistors are provided either for scaling an external op amp to the same voltage ranges as the voltage model DAC85 or for configuring a resistive load to provide two output voltage ranges of ±1 volt or 0 to -2 volts. These internal resistors (R_{LI}) are an integral part of the DAC85 design, and are required to maintain the gain and bipolar offset drift specifications of the DAC85. If the internal resistors are not used, external R_L or R_F resistors should have ±25 ppm/°C or less temperature coefficient to minimize drift.

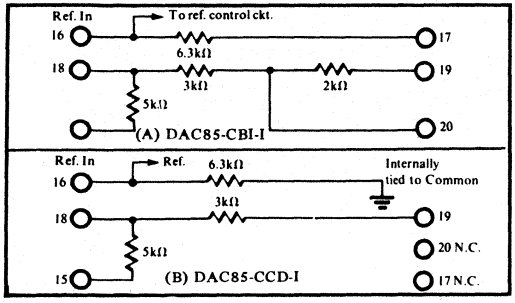


FIGURE 7. Internal Scaling Resistors.

The current model DAC85 equivalent output circuit and resistive scaling network is different from the voltage model DAC85, and is shown in Figure 7 and 8 for reference.

Instructions for using the DAC85-xxx-I with either a resistive load or an external op amp are on the following pages. External R_{LS} or R_{LP} resistors are required to give exactly 0 to -2V or ±1V output range. These resistors should have a TCR of ±100 ppm/°C or less. If these exact output ranges are not required, R_{LS} (or R_{LP}) need not be used as discussed below.

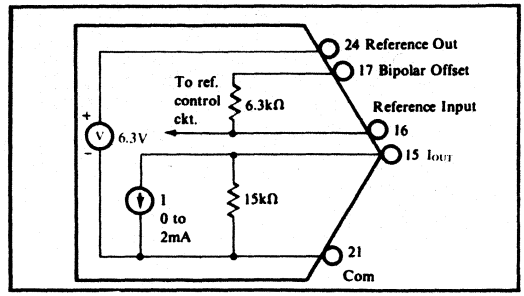


FIGURE 8. DAC85 Current Model Equivalent Output Circuit.

Voltage Output Using Resistive Load

UNIPOLAR

BINARY INPUT CODE (CSB)

A load resistance R_L connected to the output as shown in Figure 9, will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2\ mA \left(\frac{15\ k \times R_L}{15\ k + R_L} \right)$$

where R_L max = 1.36 kΩ
and V_{OUT} max = -2.5 volts

For minimum drift as specified, the internal scaling resistor (R_{LI}) should be connected as shown in Table 4 for the CSB code with a series connected external metal film full scale trim resistor (R_{LS}) to provide a full scale output voltage range of 0 to -2 volts. With R_{LS} = 0, V_{OUT} = -1.82V.

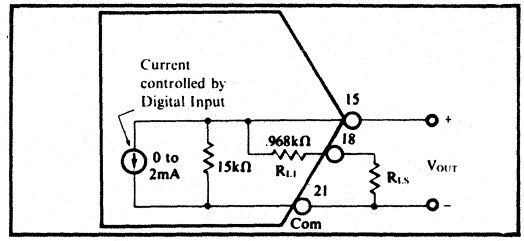


FIGURE 9. Equivalent Circuit DAC85-CBI-I connected for Unipolar Voltage Output with Resistive Load.

BCD INPUT CODE (CCD)

Connect the internal scaling resistors as shown in Table 4, and add an external parallel connected metal film resistor (R_{LP}) as shown in Figure 10 to obtain a 0 to -2 volt full scale output voltage range for CCD input codes. With R_{LP} = ∞, V_{OUT} = -2.08V.

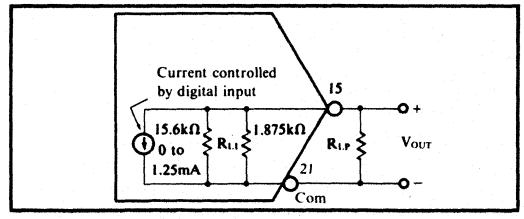


FIGURE 10. DAC85-CCD-I Connected for Voltage Output with Resistive Load.

Input Code	Output Voltage Range	Internal Resistance R_{LI}	1% Metal Film External Resistor R_{LS}	1% Metal Film External Resistor R_{LP}	R_{LI} Connections: Connect Pin 15 to	R_{LI} Connections: Connect Pin 18 to	R_{LI} Connections: Connect Pin 20 to	Reference: Connect Pin 16 to	Bipolar Offset: Connect Pin 17 to	Bipolar Offset R_{LS}	Bipolar Offset R_{LP}
CSB	0 to -2V	0.968 kΩ	105 Ω	N/A	20	19 & R_{LS}	15	24	21 (Com)	Between pin 18 & 21	N/A
CCD	0 to -2V	1.875 kΩ	N/A	36.5 kΩ	19	21 (Com)	N.C.	24	N.C.	N/A	Between pin 15 & 21
COB or CTC	±1V	1.2 kΩ	90.9 Ω	N/A	18	19	R_{LS}	24	15	Between pin 20 & 21	N/A

TABLE 4. DAC85X - XXX - I Resistive Load Connections.

BIPOLAR

COB and CTC INPUT CODES

The equivalent output circuit for a bipolar output voltage range is shown in Figure 11. V_{OUT} is determined by:

$$V_{OUT} = \pm 1\text{ mA} \times \left(\frac{R_L \times 4.44\text{ k}}{R_L + 4.44\text{ k}} \right)$$

where R_L max = 5.72 kΩ
V_{OUT} max = ±2.5 volts

For minimum drifts (as specified) the internal scaling resistors (R_{LI}) are connected as shown in Table 4 for the COB or CTC codes and an external series connected metal film resistor (R_{LS}) is added to obtain a full scale output voltage range of ±1 volt. With R_{LS} = 0, V_{OUT} = ±0.944V.

SETTLING TIME

The current output DAC85 models have a specified settling time of 300 nanoseconds with a 100 ohm load. Settling time increases as the load resistance increases due to the RC time constant of R_L and the summing junction capacitance.

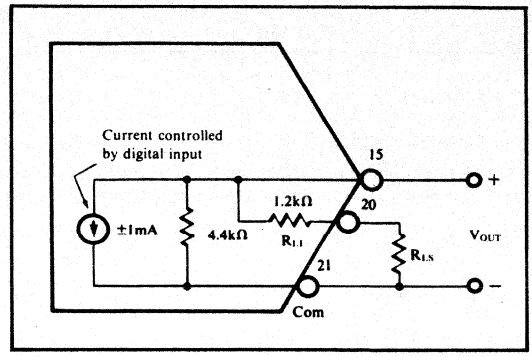


FIGURE 11. DAC85-CBI-I Connected for Bipolar Output Voltage with Resistive Load.

Driving an External Op Amp

UNIPOLAR or BIPOLAR – Up to 20V Output Range

The current model DAC85 will drive the summing junction of an op amp (the op amp being used as a current to voltage converter) to produce an output voltage (see Figure 12):

$$V_{OUT} = -I \times R_F$$

where I_{OUT} is the DAC85 output current and R_F is the feedback resistor. Use of the internal feedback resistors of the DAC85 will provide the same output voltage ranges as the voltage model DAC85. Table 5 must be used for connecting the external op amp to obtain the desired output voltage range.

Output Range	Digital Input Codes	Connect Ⓐ to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	Ⓐ	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24
0 to +10V	CCD	19	N.C.	Ⓐ	24

TABLE 5. Voltage Ranges of Current Output DAC85 with External Op Amp.

OUTPUTS LARGER THAN 20 VOLT RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1 mA for bipolar voltage ranges, and -2 mA for unipolar voltage ranges (see Figure 13). Use protection diodes when a high voltage op amp is used.

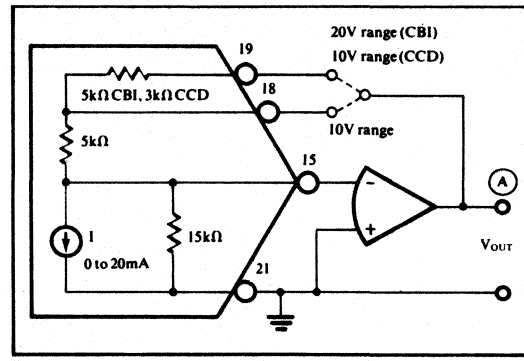


FIGURE 12. External Op Amp - Using Internal Feedback Resistors.

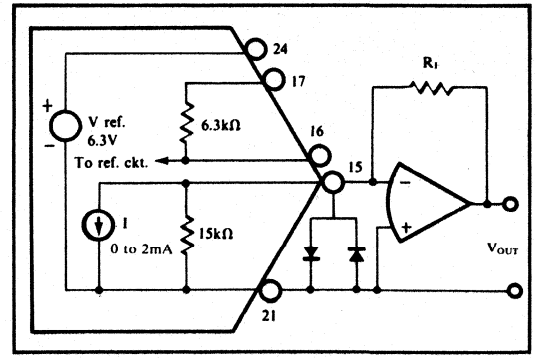


FIGURE 13. External Op Amp - Using External Feedback Resistors.

BUILDING AN A/D CONVERTER

The small size and good performance of the DAC85 makes it an excellent component for building A/D converters. The most popular medium speed (1 μsec/bit to 10 μsec/bit) A/D converter is the successive approximations type, in which the digital output equivalent of the analog input is formed by comparing a programmed D/A converter output with the analog input. The digital output is successively compared one bit at a time until the final comparison is within ± 1/2 bit of the resolution of the D/A converter.

The conversion speed of a successive approximation A/D converter constructed around a DAC85 is determined by the settling speed to ±1/2 LSB, the speed of the comparator, and the switching speed of the successive approximations logic. The A/D converter shown in Figure 14 will convert at speeds in excess of 60 kHz for 12 bits and near 80 kHz for 10 bits.

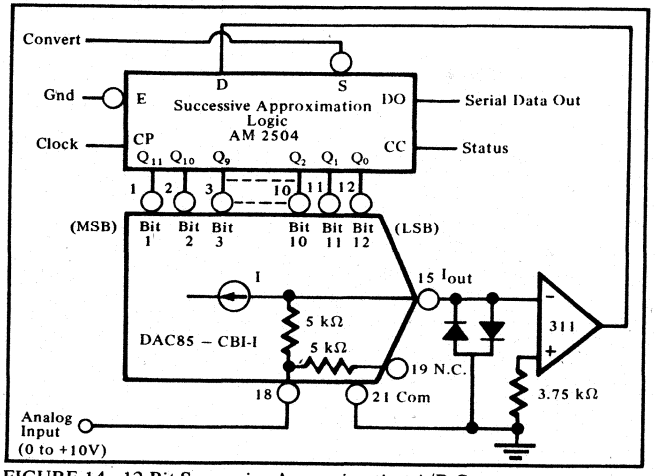
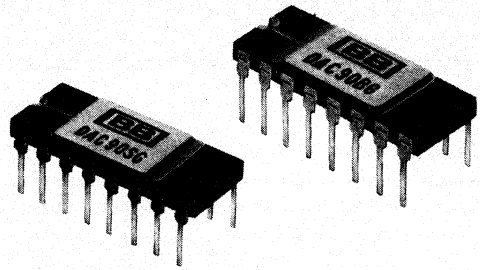


FIGURE 14. 12-Bit Successive Approximation A/D Converter.

BURR-BROWN



DAC90

Monolithic Microcircuit DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 8-BIT RESOLUTION
- CURRENT OUTPUT
- FAST SETTLING
  200nsec to ±0.2%
- HERMETIC DUAL-IN-LINE PACKAGE
- LOW COST
- INTERNAL REFERENCE AND SCALING RESISTORS

DESCRIPTION

The DAC90 is an 8-bit D/A Converter that offers performance usually found only in larger, modular units. Housed in a 16-pin ceramic dual-in-line package, the DAC90 is complete with its own internal reference and scaling resistors.

Two versions are available: the DAC90BG (-25°C to +85°C) and DAC90SG (-55°C to +125°C) both offer ±0.2% nonlinearity over their respective temperature ranges. Settling time to ±0.2% is typically 200nsec.

The small size of the DAC90 makes it an ideal choice as the heart of your A/D converter design or for applications where space or weight is at a premium, such as CRT displays, aircraft instrumentation, and portable instruments.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-347B

Printed in U.S.A. July, 1978

SPECIFICATIONS

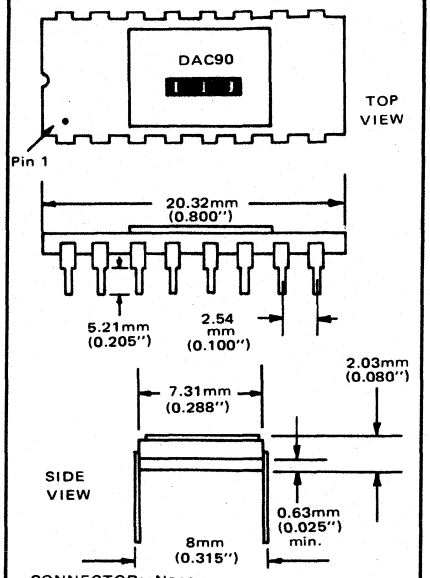
Typical at 25°C and rated power supplies unless otherwise noted.

ELECTRICAL

MODEL	DAC908G	DAC90SG	UNITS
DIGITAL INPUT			
Resolution	8	8	Bits
Logic Levels (TTL compatible)			
Logic "1"	+2 < e_d < +5.5 at +40μA		V
Logic "0"	0 < e_d < +0.8 at -1.0mA		V
TRANSFER CHARACTERISTICS			
ACCURACY			
Linearity Error @ 25°C (max)	±1/2	±1/2	LSB
-25°C to +85°C (max)	±1/2		LSB
-55°C to +125°C (max)		±1/2	LSB
Differential Linearity Error	±1/2	±1/2	LSB
Gain Error[1]	5	5	%
Offset Error[1]	1	1	% of FSR[2]
Minimum Temperature Range for Guaranteed Monotonicity	-25 to +85	-55 to +125	°C
DRIFT [3]			
Gain			
-25°C to +85°C	±50		ppm/°C
-55°C to +125°C		±50	ppm/°C
Offset			
Unipolar			
-25°C to +85°C	±1		ppm of FSR/°C
-55°C to +125°C		±1	ppm of FSR/°C
Bipolar			
-25°C to +85°C	±50		ppm of FSR/°C
-55°C to +125°C		±50	ppm of FSR/°C
CONVERSION SPEED			
Settling time to ±0.2% of FSR for FSR change			
10 to 100Ω load	200		nsec
1kΩ load	300		nsec
ANALOG OUTPUT			
Ranges	±1, 0 to -2		mA
Output Impedance – Bipolar	1.8		kΩ
Unipolar	2		kΩ
Compliance	-4 to +4		V
Internal Reference Voltage (V_r)	7.6		V
Tempco of Drift	±50	±50	ppm of V_r/°C
POWER SUPPLY SENSITIVITY			
+15V	±0.02		% of FSR/%Vs
-15V	±0.002		% of FSR/%Vs
POWER SUPPLY REQUIREMENTS			
Rated Voltage	±15		V
Range	±14.5 to ±15.5		V
Supply Drain ±15V	7		mA
TEMPERATURE RANGE			
Specification	-25 to +85	-55 to +125	°C
Operating	-55 to +125	-55 to +125	°C
Storage	-55 to +125	-55 to +125	°C

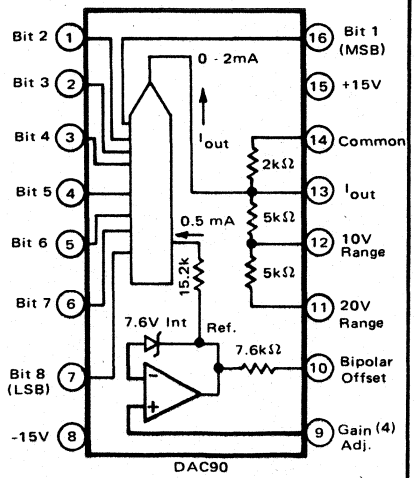
1. Adjustable to zero with external trim potentiometer.
2. FSR means "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc.
3. To maintain drift spec internal feedback resistors must be used.
4. Connect to ground if gain adjust circuit is not used.

MECHANICAL



CONNECTOR: None
CASE: Ceramic, with hermetic seal
PIN: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
HERMETICITY: Conforms to Mil-Std-883 Method 1014, Condition C, Step 1 (Flurocarbon) (Gross leak) and Condition A Helium), 5×10^{-7} cc/sec (fine leak).

CONNECTION DIAGRAM



DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC90 accepts digital inputs in complementary binary (CBI) format and may be connected for complementary straight binary (CSB) or complementary offset binary (COB) operation. By using one external inverter, the user can operate the DAC90 in the complementary two's complement (CTC) mode.

DIGITAL INPUT CODES	OUTPUT RANGE			
	VOLTAGE*		CURRENT	
	0 to +10V	±10V	0 to -2mA	±1mA
MSB LSB				
0 0 0 0 0 0 0 0	+9.961V	+9.922V	-1.992mA	-0.992mA
0 1 1 1 1 1 1 1	+5.000V	0.000V	-1.000mA	0.0000mA
1 0 0 0 0 0 0 0	+4.961V	-78.12mV	-0.99mA	+7.81μA
1 1 1 1 1 1 1 1	0.000V	-10.000V	0.000mA	+1.000mA
one LSB	39.06mV	78.12mV	7.81μA	7.81μA

* Requires external amplifier. To obtain values for other binary (CBI) ranges: 0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

TABLE I.Digital Input and Analog Output Relationship.

ACCURACY

LINEARITY

The LINEARITY of a D/A converter is the true measure of its performance. The DAC90 analog output will not vary by more than ±1/2 LSB from an ideal straight line drawn between the end points (all 1's and all 0's) over the specified temperature range.

DIFFERENTIAL LINEARITY

DIFFERENTIAL LINEARITY error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A DIFFERENTIAL LINEARITY error specification of ±1/2 LSB means that the output voltage can change anywhere from 1/2 LSB to 3/2 LSB when the input changes from one adjacent digital state to the next.

DRIFT

GAIN DRIFT

GAIN DRIFT is a measure of the change in the analog output over temperature expressed in parts per million per °C (ppm/°C). The GAIN DRIFT is determined by testing the end point differences at the high and low temperature extremes and at 25°C for each model, calculating the GAIN ERROR with respect to the 25°C value, and dividing by the temperature change.

OFFSET DRIFT

OFFSET DRIFT is a measure of the actual change in output voltage (using an external amplifier) at zero volts output over the specified temperature range. The offset voltage is measured at the temperature extremes, and the maximum change referenced to 25°C is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time is the time required for the output to enter and remain in an error band equal to ±0.2% of full scale range measured from the time the digital input is changed. Typical settling time values for full scale changes are a function of the load resistor and are shown in the figure below.

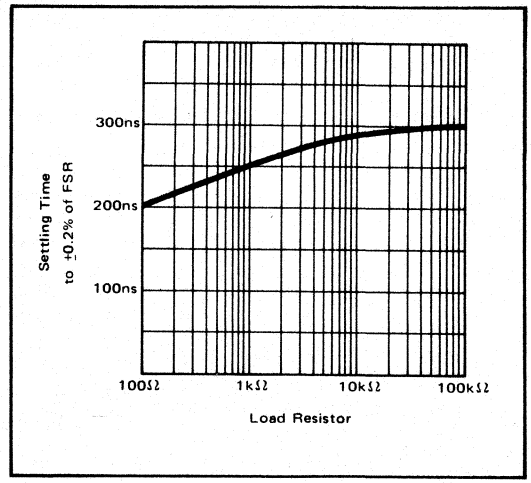


FIGURE 1. Settling Time for FSR Change vs Load.

COMPLIANCE

The COMPLIANCE VOLTAGE of the DAC90 is the maximum voltage swing allowed on the current output in order to maintain the specified accuracy; it is -4.0 to +4.0 volts for the unipolar and bipolar current ranges. The maximum safe voltage swing allowed with no damage to the DAC90 output is -4.0 to +15.0 volts.

POWER SUPPLY SENSITIVITY

POWER SUPPLY SENSITIVITY is a measure of the effect of a power supply voltage change on the D/A converter output. It is defined as a percent of FSR/percent of change in either the +15 volt or -15 volt power supplies about the nominal power supply voltages. Figure 2 shows Power Supply Rejection vs Frequency.

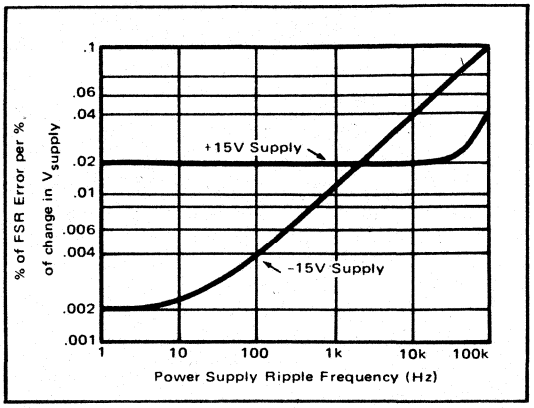


FIGURE 2. Power Supply Rejection vs. Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

DECOUPLING

For best performance and noise rejection, power supply decoupling capacitors should be connected as shown in Figure 3. These capacitors should be located close to the DAC90 and should be tantalum or electrolytic types bypassed with a 0.01 μF ceramic capacitor for best high frequency performance.

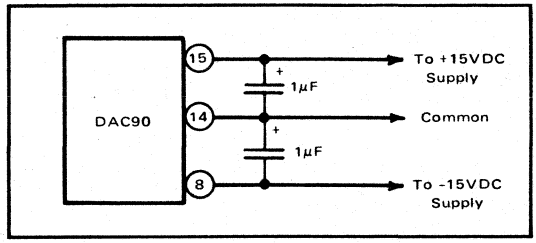


FIGURE 3. Recommended Power Supply Decoupling.

OPERATION IN THE CURRENT OUTPUT MODE

In the current output mode, the DAC90 provides a unipolar output current of 0 to -2mA and a bipolar output current of ±1mA. Refer to Figure 4 and Table II for proper connections. In applications requiring the use of the DAC90 in the current output mode, such as an A/D converter, the internal scaling resistors should be used to generate currents corresponding to analog input voltages.

Output Range	Connect Pin (13) to:
0 to -2mA	N.C.
±1mA	Pin 10

TABLE II. Connections for Current Output Mode.

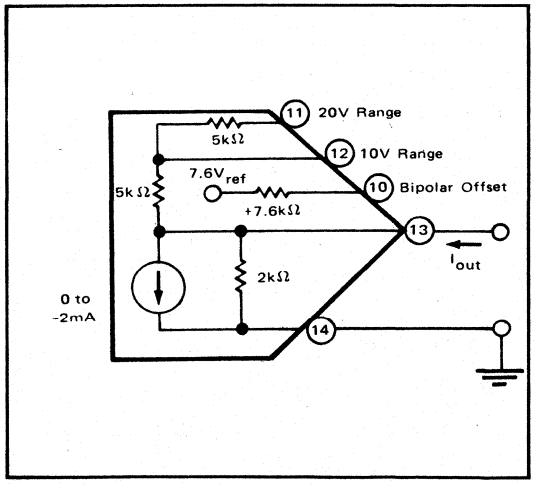


FIGURE 4. Current Output Mode Connection Diagram.

VOLTAGE OUTPUT using an EXTERNAL OP AMP

UNIPOLAR OR BIPOLAR OPERATION

The DAC90 wil drive the summing junction of an op amp (the op amp being used as a current-to-voltage converter) to produce an output voltage.

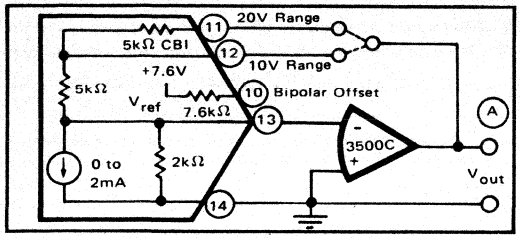


FIGURE 5. External Op Amp Using Internal Feedback Resistors.

$$V_{OUT} = -I \times R_F$$

where I_{OUT} is the DAC90 output current and R_F is the feedback resistor. Refer to Table III and Figure 5.

Output Range	Digital Input Codes	Connect (A) to	Connect Pin (13) to
±10V	COB	11	10
±5V	COB	12	10
±2.5V	COB	12	10,11
0 to +10V	CSB	12	N.C.
0 to +5V	CSB	12	11

TABLE III. Voltage Ranges of Current Output DAC90 With External Op Amp.

EXTERNAL OFFSET and GAIN ADJUSTMENT

Initial offset and gain errors may be trimmed by the user with externally connected OFFSET and GAIN potentiometers and an operational amplifier. Refer to Figures 5 and 6 for proper connections. The adjustment procedures are described below. Potentiometer resistances are shown as a range of values and should have a temperature drift coefficient of 100 ppm/°C or less. The trimming networks should be located as close to the DAC90 as possible to minimize noise pickup. The ceramic capacitor shown in Figure 6 will further reduce noise pickup at the gain adjust point.

OFFSET ADJUSTMENT

Offset adjustment should be made prior to gain adjustment. Connect the unit as shown in Figure 5 for the desired output range and add the offset adjust network shown in Figure 6. Offset adjustment is the same procedure for either bipolar or unipolar operation. Apply the digital input code which should give zero volts output and adjust the offset potentiometer for zero volts output. See Table I for the corresponding codes.

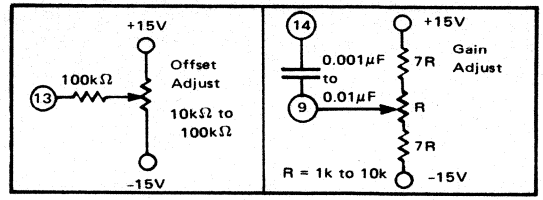


FIGURE 6. Connections for OFFSET and GAIN Adjustment.

GAIN ADJUSTMENT

The gain adjust procedure is the same for either bipolar or unipolar operation. An external amplifier should be connected as shown in Figure 5. Connect the unit for the desired output range and add the gain adjust network shown in Figure 6. Apply the digital input code which should give the maximum positive output voltage and adjust the gain potentiometer for the correct output. Refer to Table I for the corresponding codes.

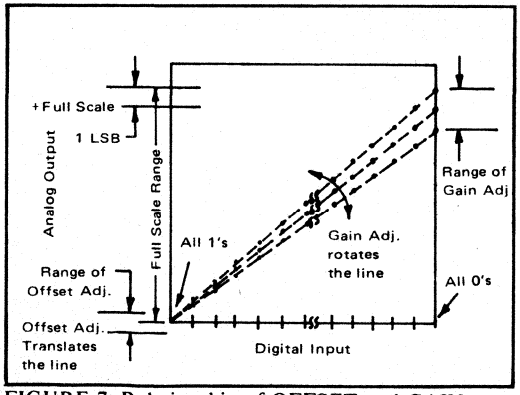


FIGURE 7. Relationship of OFFSET and GAIN Adjustment for a UNIPOLAR D/A Converter.

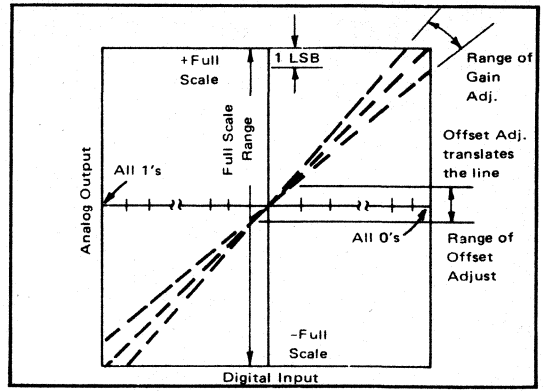
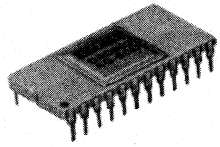


FIGURE 8. Relationship of OFFSET and GAIN Adjustments for BIPOLAR D/A Converter.

D/A DAC90

BURR-BROWN

DAC862



ADVANCE INFORMATION
Subject to Change

IC 12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 12-BIT ACCURACY
- 2-QUADRANT MULTIPLYING
- MONOTONIC OVER FULL TEMPERATURE RANGE
- LOW COST
- HERMETIC 24-PIN DIP
- PIN COMPATIBLE TO "562" CONVERTERS

DESCRIPTION

DAC862 is a 2-chip IC D/A converter. It is comprised of a stable, weighted current switch chip and a thin-film laser trimmed resistor chip. It produces a 12-bit accurate analog output current proportional to the product of the input reference voltage and the digital input word.

The digital input code is positive true logic and is compatible with TTL or CMOS logic without buffering.

DAC862 is packaged in a 24-pin hermetic ceramic package. Three temperature ranges are available: 0°C to 70°C (DAC862KG); -25°C to +85°C (DAC862BG); -55°C to +125°C (DAC862SG). Screening to the requirements of Mil-Std-883 is available.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-394 Printed in U.S.A. July, 1978

ELECTRICAL SPECIFICATIONS

Typical at +25°C, +10V reference, and rated supplies unless otherwise noted.

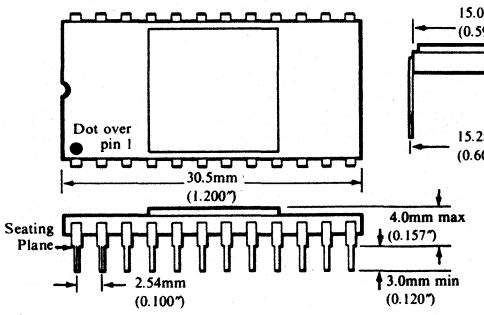
MODEL	DAC862KG-BIN			DAC862BG-BIN			DAC862SG-BIN			UNITS
DIGITAL INPUTS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution			12			12			12	Bits
TTL - Logic "1" at 100nA max	2.0			2.0			2.0			V
- Logic "0" at -100μA max			0.8			0.8			0.8	V
CMOS[7] - Logic "1" at 100nA max	70% V_{cc}			70% V_{cc}			70% V_{cc}			V
- Logic "0" at -100μA max			30% V_{cc}			30% V_{cc}			30% V_{cc}	V
REFERENCE INPUT										
Input Impedance		20 ±10%			20 ±10%			20 ±10%		kΩ
Voltage Range	0		+10.24	0		+10.24	0		+10.24	V
ACCURACY										
Linearity Error										
at +25°C		±1/4	±1/2		±1/8	±1/4		±1/8	±1/4	LSB
over rated temperature range		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB
Gain Error		0.05	0.15		0.05	0.15		0.05	0.15	%
Bipolar Offset Error		0.05	0.15		0.05	0.15		0.05	0.15	% of FSR
Leakage Current (all "0"s)			0.03			0.03			0.03	% of FSR
Monotonic Temp. Range	0		70	-25		+85	-55		+125	°C
Differential Linearity Error		±1 2	±1		±1/4	±1/2		±1/4	±1/2	LSB
POWER SUPPLY SENSITIVITY OF GAIN										
V_{cc} at +5VDC		1/2	1		1/2	1		1/2	1	ppm of FSR/%
V_{cc} at +15VDC		1/2	1		1/2	1		1/2	1	ppm of FSR/%
V_{EE} at -15VDC		1	2		1	2		1	2	ppm of FSR/%
DRIFT										
Gain (over temp. range)										
exclusive of reference drift		2	5		2	5		2	5	ppm of FSR/°C
Bipolar Offset		2	4		2	4		2	4	ppm of FSR/°C
Leakage Current		0.5	1		0.5	1		1	2	ppm of FSR/°C
Differential Linearity		2	3		1	2		1	2	ppm of FSR/°C
EXTERNAL ADJUSTMENTS										
Gain Adjust Range		0.25			0.25			0.25		% of FSR
Bipolar Offset Adjust Range		0.25			0.25			0.25		% of FSR
Unipolar Offset Adjust Range		0.25			0.25			0.25		% of FSR
CONVERSION SPEED										
Settling Time to 1 2LSB[1] (±FS change)			3.5			3.5			3.5	μsec
Major Carry Glitch Duration										
Duration (to 90% complete)		400			400			400		nsec
NOISE (0.1 to 10Hz, all "1"s)		20			20			20		μV p-p
OUTPUT										
Current - Unipolar (±10%)		0 to -2			0 to -2			0 to -2		mA
- Bipolar (±10%)		-1 to +1			-1 to +1			-1 to +1		mA
Selectable Ranges[6]		0 to +5, 0 to +10, -2.5 to +2.5, -5 to +5, -10 to +10								V
Resistance		6.6			6.6			6.6		kΩ
Capacitance		33			33			33		pF
Compliance Voltage	-2.5		+10	-2.5		+10	-2.5		+10	V
MULTIPLYING MODE PERFORMANCE										
Number of Quadrants[2]			2			2			2	
Reference Voltage Range	0		+10.24	0		+10.24	0		+10.24	V
Accuracy[3]	±0.05			±0.05			±0.05			% of FSR
Feedthrough[4]		±0.01			±0.01			±0.01		% of FSR
Output Slew Rate[5]		1			1			1		mA/μsec
Output Settling Time[5] (to 0.01% of FS)		5			5			5		μsec
Control Amplifier BW (small-signal, closed-loop)		1			1			1		MHz
POWER SUPPLIES										
Voltage - V_{cc}	+4.75		+15.75	+4.75		+15.75	+4.75		+15.75	VDC
- V_{EE}	-14.25	-15	-15.75	-14.25	-15	-15.75	-14.25	-15	-15.75	VDC
Current - V_{cc}		15			15			15		mA
- V_{EE}		20			20			20		mA
TEMPERATURE RANGE										
Specification	0		+70	-25		+85	-55		+125	°C
Operating (reduced specs)	-25		+85	-55		+125	-55		+125	°C
Storage	-55		+150	-55		+150	-55		+150	°C

TABLE I. Electrical Specifications

ELECTRICAL SPECIFICATIONS CONTINUED:

NOTES:
1. Current settling into short circuit.
2. Bipolar operation at digital inputs only.
3. For 1VDC reference voltage (see Figure 5). Full Scale range = 1V.
4. Voltage at reference input: 0 to +10V, 2kHz sine wave (see Figure 6).
5. All "1"s, 10V step on reference input.
6. Using internal scaling resistors.
7. +4.75V < V_{CC} < + 15.8V and pin 2 tied to pin 1.

MECHANICAL



CASE: Ceramic with hermetic seal
PIN: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)

PIN ASSIGNMENTS

1. V_{CC} +15/+5VDC	13. Bit 12 (LSB)
2. CMOS/TTL Logic Threshold	14. Bit 11
3. -Input, REF Amp	15. Bit 10
4. REF Amp Summing Junction	16. Bit 9
5. +Input REF Amp	17. Bit 8
6. V_{EE}, -15VDC	18. Bit 7
7. Bipolar Offset Resistor	19. Bit 6
8. Bipolar Offset Resistor	20. Bit 5
9. Current Output	21. Bit 4
10. 10V Range	22. Bit 3
11. 20V Range	23. Bit 2
12. Common	24. Bit 1 (MSB)

FIGURE 1. Mechanical and Pin Assignments

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

DAC862 accepts a positive-true straight binary (BIN) input code. Offset-binary code is created by offsetting the output amplifier with the DAC reference. Two's complement code is obtained from offset binary by inverting bit 1 (the most significant bit) externally. See Table II.

ACCURACY

LINEARITY of each DAC862 model is guaranteed to be within the specification over its respective temperature range. This is the measure of the deviation of the actual transfer curve from the ideal transfer curve. The ideal curve can be expressed graphically as a straight line drawn between the end-point values. For DAC862BG and DAC862SG the maximum deviation is ±1/4LSB. For DAC862KG it is ±1/2LSB.

DIFFERENTIAL LINEARITY error is the deviation from an ideal 1LSB output voltage change from one adjacent state to the next. An error specification of ±1/2LSB indicates that output voltage step size can range from 1/2LSB to 3/2LSB between adjacent states.

MONOTONICITY is an important property for a D/A converter, especially one used in a closed control loop. A converter is monotonic if the output signal increases or remains the same for an increase in digital input. A converter's differential linearity determines whether or

DIGITAL INPUT CODES				
	ANALOG OUTPUT			
LOGIC INPUTS	VOLTAGE**		CURRENT	
Binary	0 to +10V	-10 to +10V	0 to -2mA	-1 to +1mA
111111111111	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
100000000000	+5.0000V	0.0000V	-1.0000mA	0.0000mA
011111111111	+4.9976V	-0.0049V	-0.9995mA	-0.0005mA
000000000000	0.0000V	-10.0000V	0.0000mA	-1.0000mA
Binary Two's Complement*				
011111111111		+9.9951V		-0.9995mA
000000000000		0.0000V		0.0000mA
111111111111		-0.0049V		-0.0005mA
100000000000		-10.0000V		-1.0000mA
1 LSB (BIN)	2.44mV	4.88mV	0.488μA	0.488μA

TABLE II. Digital Input Codes

*MSB must be inverted externally for this code.

**To obtain values for other binary ranges:
0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5 range: divide ±10V range values by 4.

not it is monotonic. If differential linearity is $< \pm 1$LSB, the converter will be monotonic. Monotonicity is guaranteed over the entire specified temperature range for each DAC862 model.

LEAKAGE CURRENT is measured at the converter output with logic 0 on all digital inputs. It appears as part of offset error, both at room temperature and over the specified temperature range. In the unipolar configuration, virtually all offset error is due to leakage current.

DRIFT

GAIN DRIFT is a measure of the change in the full scale analog output due to a change in temperature and is expressed in parts per million per °C (ppm/°C). It is calculated by determining the full-scale output value at high temperature, then at low temperature. The difference in the two values is divided by the difference in the two temperatures.

OFFSET DRIFT is a measure of the actual change in output over the specified temperature range with logic 0 on all digital inputs. It is calculated by measuring offset voltage at the temperature extremes. The maximum change referred to the offset voltage at +25°C is divided by the temperature excursion from +25°C. Offset drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

DIFFERENTIAL LINEARITY DRIFT (the change in differential linearity over the specified temperature range) is calculated in a manner similar to offset drift and is expressed in ppm of FSR/°C.

CONVERSION SPEED

SETTLING TIME is the time required for the output to enter and remain within an error band of the final value measured from the time the digital input is changed. Figure 2 illustrates settling times for several conditions.

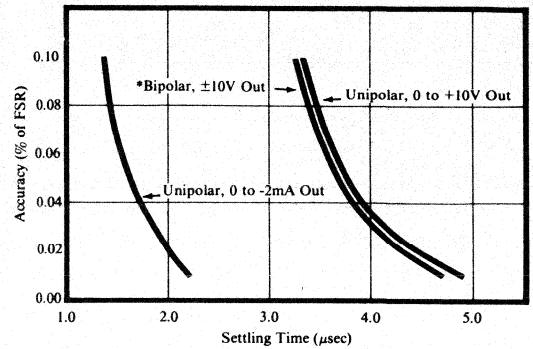
The settling time for a 1LSB change at the input is naturally less than for a full scale change. It is greatest at the major-carry point (the point at which the most significant bit changes states) due to non-uniform switching times of the internal current switches. For a 1LSB change at the major carry point, settling time to within .01% will typically be 1.8μsec. Settling time can be reduced as much as 50% by adding the compensation circuit shown in Figure 3.

COMPLIANCE VOLTAGE

This is the maximum voltage which can be impressed on the current output node, yet remain within the specified accuracy of the DAC862. These voltages are -2.5V and +10V. Maximum voltages of -5V and +18V can be sustained at the current output without damage.

POWER SUPPLY SENSITIVITY

This measure of the effect of a power supply voltage change on the D/A converter output is defined as a per cent of FSR/per cent of change in either the +5/+15 volt or -15 volt power supplies about the nominal supply voltages. Figure 4 shows power supply rejection vs frequency.



*With Schottky clamp diodes connected back-to-back from amplifier summing junction to ground.

FIGURE 2. Settling Time vs. Accuracy

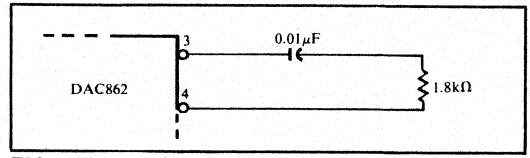


FIGURE 3. Settling Time Compensation Network

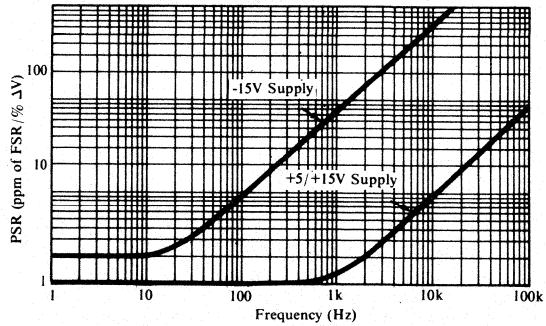


FIGURE 4. Power Supply Rejection vs Power Supply Ripple Frequency

MULTIPLYING MODE PERFORMANCE

The output of the DAC862 is the product of the reference input and digital input values. The reference may be an AC signal and can vary from 0 to +10 volts. This is useful in applications where digitally programmed attenuation of a signal is desired. Because the reference voltage input must be positive, the DAC862 multiplies in two quadrants only. For highest accuracy the input reference voltage should be as high as possible. See Figure 5.

Feedthrough of the DAC862 is the amount of reference signal that appears at the output when all digital inputs are logic 0. Expressed in % of FSR, it increases with increasing reference frequency. See Figure 6.

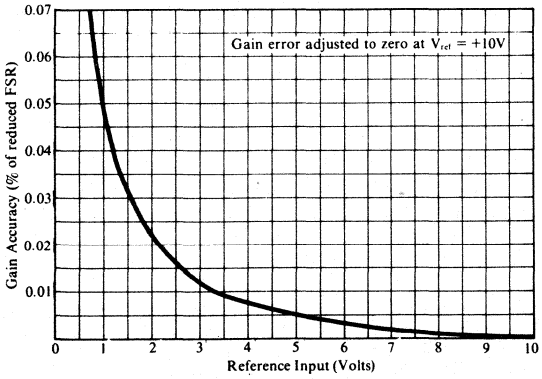


FIGURE 5. Gain Accuracy vs Reference Voltage

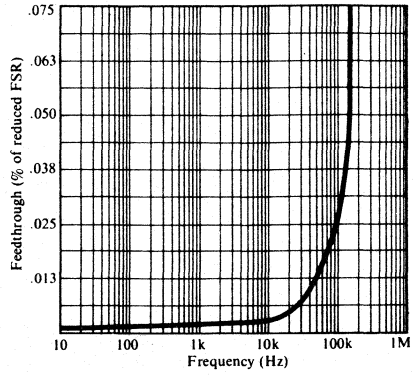


FIGURE 6. Feedthrough Voltage vs Frequency Unipolar Mode

OPERATING INSTRUCTIONS

INPUT LOGIC LEVELS

Inputs of the DAC862 can be either TTL or CMOS logic compatible. For TTL, connect +5 volts to pin 1 (pin 2 open). For +5V CMOS, connect +5 volts to pins 1 and 2. For +15V CMOS compatibility, connect +15 volts to pins 1 and 2.

In circuits where pin 2 is used to determine the digital threshold level, the following application tip may be helpful. If, for some reason, the analog system ground (to which the DAC862 is referred) differs from the digital driving logic ground, the threshold voltage input (at pin 2) may be driven from an external voltage source to keep the threshold at proper value. Threshold voltage will always be at 1/2 the voltage applied to pin 2 (< pin 2 voltage <15V).

POWER SUPPLIES

Each power supply should be bypassed to ground with a 0.1μF capacitor as shown in Figure 7. Locate the capacitors close to the power supply.

GAIN AND OFFSET ADJUSTMENTS

(Voltage Output Configuration)

Initial gain and offset errors of the DAC862 circuit may be trimmed out using the following procedures.

Unipolar configuration (Figure 7) - input all 0's and null offset error by adjusting R_3 until output voltage equals zero. Input all 1's and adjust R_1 until the output voltage is plus full scale minus 1LSB (+FS - 1LSB). See Table II for FS values.

Bipolar configuration (Figure 8) - input all 0's and null offset error by adjusting R_2 until the output voltage equals -FS. Input all 1's and adjust R_1 until the output voltage is +FS - 1LSB. See Table II for FS values.

SELECTING AN EXTERNAL REFERENCE

DAC862 is configured to use a +10V reference. An internal 20kΩ resistor in series with an external 100Ω adjust potentiometer sets the current into the reference input at 0.5mA. See Figure 9.

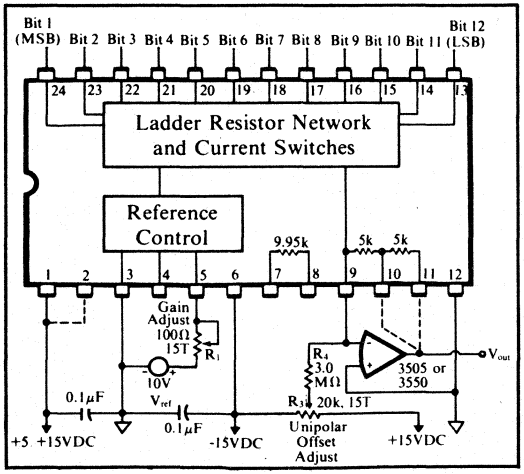


FIGURE 7. Connection Diagram, Unipolar

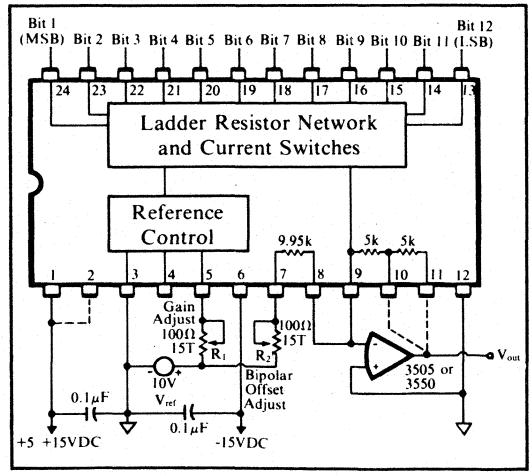


FIGURE 8. Connection Diagram, Bipolar

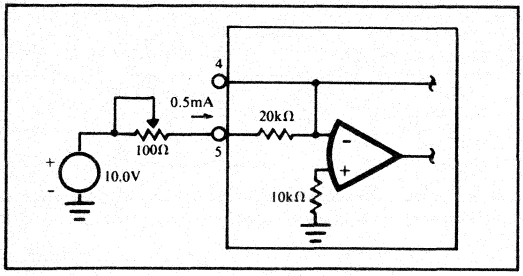


FIGURE 9. Using a +10V Reference

Temperature drift of the reference increases drift of the entire circuit. In unipolar configurations the drift specification adds directly to the total circuit drift. In the bipolar configuration some drift cancelling effects take place. One-half of the reference drift added to the total DAC drift will give total circuit drift.

If a reference voltage other than +10V is required, use the circuit shown in Figure 10.

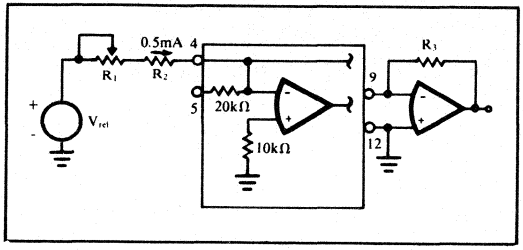


FIGURE 10. Using a Voltage Reference Other Than +10V

The equation $V_{ref}/(R_2+1/2R_1)=0$ 0.5mA should be used to select R_1 and R_2. The ratio of R_2 and R_1 should be approximately 200:1 for proper gain adjust range. To achieve good low drift performance over temperature with this method, R_2 and R_3 should track each other to within 5ppm/°C.

SELECTING AN OUTPUT AMPLIFIER

The most important characteristics of the output amplifier are input voltage offset drift, input bias (or difference) current drift and settling time. Initial input offset voltage and bias current effects will be trimmed out, but bias errors will be introduced as these parameters drift with temperature changes. Errors introduced will appear as offset in the D/A circuit output.

Table III provides the equations used to convert these amplifier errors to D/A output errors.

PARAMETER	UNIPOLAR CONFIGURATION	BIPOLAR CONFIGURATION
I_{Bias}	$\frac{I_B \times R_F}{FSR} \times 100$	$\frac{I_B \times R_F}{FSR} \times 100$
V_{os}	$\frac{V_{os}\left(1+\frac{R_F}{6.6k\Omega}\right)}{FSR} \times 100$	$\frac{V_{os}\left(1+\frac{R_F}{4.0k\Omega}\right)}{FSR} \times 100$

FSR = Full scale range (-2.5 to +2.5V is a 5V FSR, etc.) Results are in % of FSR; to get ppm of FSR, multiply by 10^4.

R_F is the value of the feedback resistor.

TABLE III. Computing DAC Error Contributed by External Amplifier (See Figure 11)

Example:

If V_{os} drift and I_{bias} drift of the output amplifier are 10 μV/°C and 0.5nA/°C, respectively, in a D/A converter with -10V to +10V output, the output drift due to these effects would be computed in this manner:

$$V_{os}: \frac{(10 \times 10^{-6})\left(1+\frac{10k\Omega}{4.0k\Omega}\right)}{20} \times 100 = 0.00018\% \text{ of FSR/°C}$$

or 1.8 ppm of FSR/°C

$$I_{Bias}: \frac{0.5 \times 10^{-9} \times (10k\Omega)}{20} \times 100 = 0.00003\% \text{ of FSR/°C}$$

or 0.3 ppm of FSR/°C

1.8 + 0.3 = 2.1 ppm of FSR/°C

Effects of input bias current drift may be reduced approximately by a factor of 5 by placing a resistor in series with the positive input lead of the amplifier as shown in Figure 11.

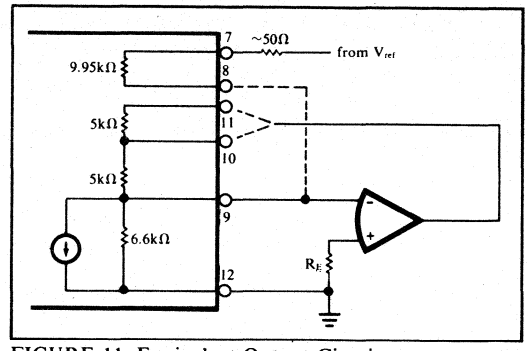


FIGURE 11. Equivalent Output Circuit

This balances the offset created and the error is reduced to the difference in bias currents in the positive and negative inputs. (Substitute I_{offset} for I_{bias} in equations in Table III.

The value of this resistor is shown in Table IV for different output ranges.

Output Range	±2.5V	±5V	±10V	0 to +5V	0 to +10V
R_E Value	1.5kΩ	2.2kΩ	2.8kΩ	1.8kΩ	2.8kΩ

TABLE IV. R_E Values

Settling time of the DAC862 is guaranteed to be < 3.5 μsec for a FSR change to within 0.01% of final value. The output amplifier's dynamic characteristics should be compatible with this performance. Burr-Brown's 3505J and 3550J fast settling amplifiers are recommended.

CURRENT OUTPUT OPERATION

DAC862 can be connected to produce a bipolar voltage output without the use of external components by connecting the internal resistors as shown in Figure 12. Output voltage range of this circuit is ±2.5V.

Gain and offset adjustments are made as described previously except that "+FS" and "-FS" are interchanged and "-FS + 1LSB" substituted for +FS - 1LSB. See page 5-92.

Unipolar and other bipolar ranges may be selected by using an external load resistor as long as the compliance voltage limits, -2.5 to +10V, are observed. To minimize temperature drift when using an external load resistor, (R_3 in Figure 13), an external reference-current-setting resistor should also be used. These two resistors should track over temperature as explained in the section on selecting an external reference on page 5-93.

MULTIPLYING MODE OPERATION

DAC862 can be used as a 2-quadrant multiplying D/A converter by applying the analog signal to be processed through a 100Ω potentiometer to the reference voltage input, pin 5. The analog signal must be between 0 and +10V. The output will be an analog signal equal to the product of the input analog signal and the input digital code. DC error of the output signal is guaranteed to be no more than 0.05% for a reference voltage range of +1V to +10V. For voltages near zero, the error can be quite large. See Figure 5.

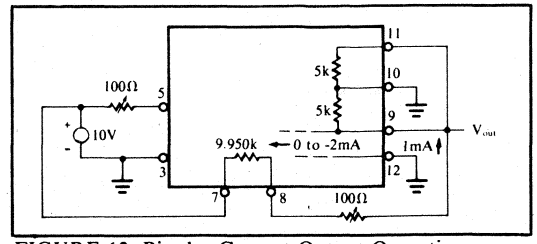


FIGURE 12. Bipolar Current Output Operation Utilizing Internal Resistors

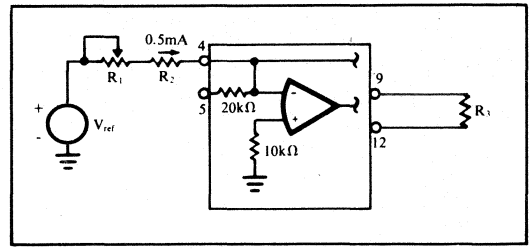
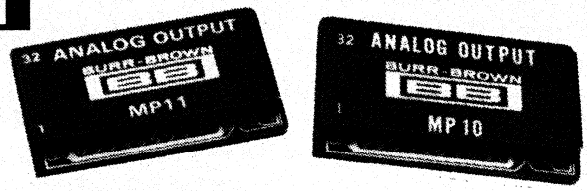


FIGURE 13. Using an External Load Resistor

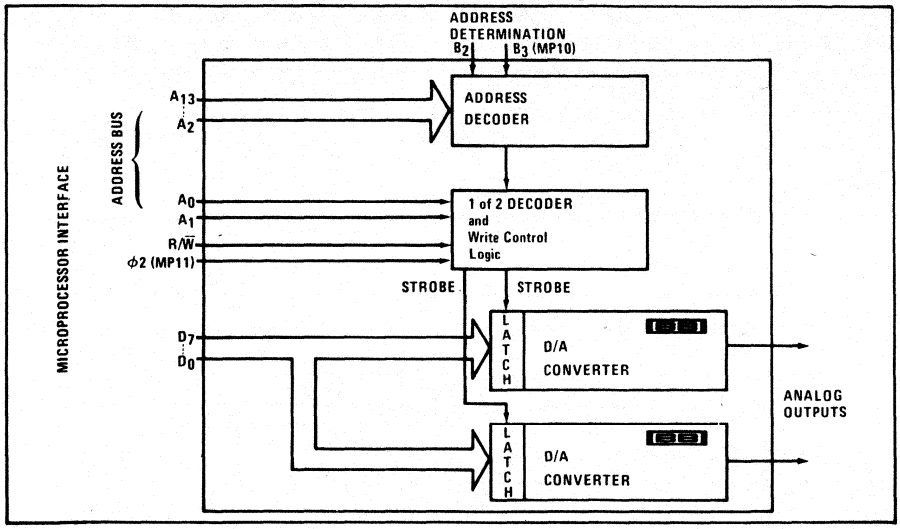
BURR-BROWN

MP10
MP11



8-BIT MICROPROCESSOR INTERFACED ANALOG INPUT SYSTEM

MP10, MP11 BLOCK DIAGRAM



FEATURES

- USE AS ANALOG INPUT AND OUTPUT
- EASY TO USE
  - Completely compatible with most microprocessors
  - No external logic required
  - Timing compatible
  - Memory-mapped
- SAVES DEVELOPMENT MONEY AND TIME
- COMPLETELY SELF-CONTAINED
- COMPATIBLE WITH:
  - 8080 (Intel)
  - 9080A (AMD)
  - Z-80 (Zilog)
  - 6800 (Motorola)
  - 8008 (Intel)
  - F-8 (Fairchild)
  - SC/MP (National)
  - 650X (MOS Technology)

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PDS-363A
Printed in U.S.A. July, 1978

DESCRIPTION

These microprocessor peripherals provide an analog interface compatible with most microprocessors. The MP10 and MP11 are electrically and functionally microprocessor compatible in static or dynamic situations.

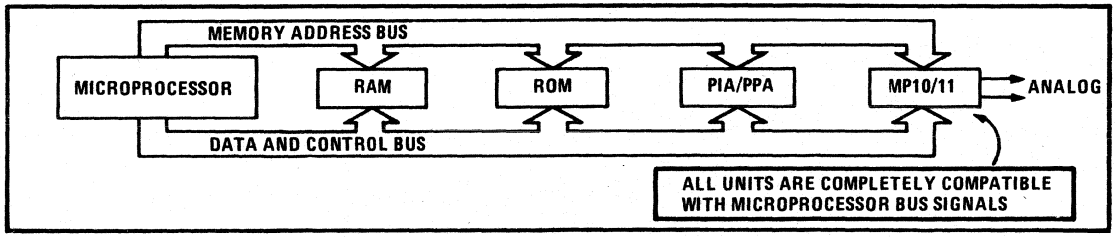
These units are complete analog systems packaged in 32 pin triple wide dual-in-line packages. They contain two 8 bit D/A converters which are internally trimmed for gain and offset so that no external trimming is required. All necessary interface, timing and address decoding logic is also included.

The MP10 is designed to be used with 8080A and 8008 type microprocessors. It can be used with SC/MP if pull-up resistors are added to the address bus, with the F-8 Dynamic or Static memory interface chip if the RAM WRITE signal is a minimum of 430nsec and with the Z-80 if t_w (ϕH) = t_w (ϕL) = 500ns. The MP11 is designed to be used with 6800 and 650X type microprocessors.

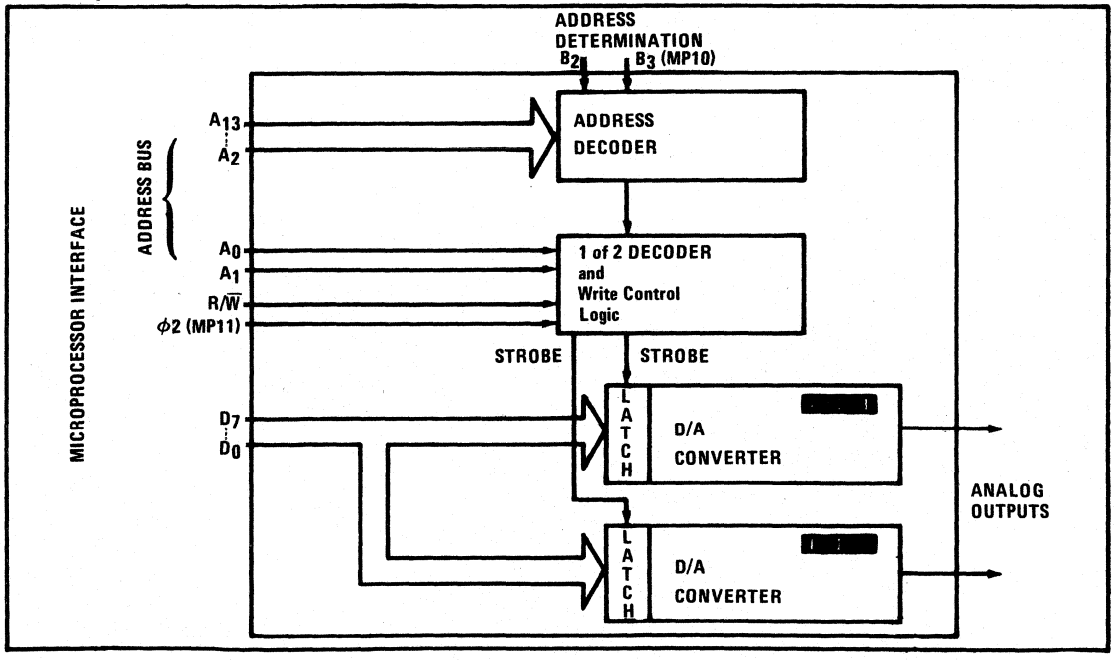
The address lines A_2 through A_{13}, B_2 and B_3 of the MP10 are CMOS compatible so that they can be directly connected to the address bus of an 8080 or 8008. All other input lines require standard TTL voltages. The address lines A_2 through A_{13} and B_2 of the MP11 are LSTTL compatible so they can be directly connected to the address bus of a 6800 or 650X. All other input lines require standard TTL voltages but are high impedance requiring only microamp drive currents.

THEORY OF OPERATION

When programming these peripherals, the user treats them as memory. Because the D/A converter input is an 8 bit word, one 8 bit memory location is required for each channel. Since these units are treated as memory, a single instruction is all that's needed to write to an output channel. For instance, when the MP10 is used with an 8080, a single instruction, SHLD, can be used to output data to both D/A converter channels from the H and L register pair. Likewise, when the MP11 is used with the 6800 or 650X, a single STX instruction can be used to output data to both D/A converter channels from the index register. The MP10 and the MP11 require an initialization as would any programmable peripheral.



MP10, MP11 BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

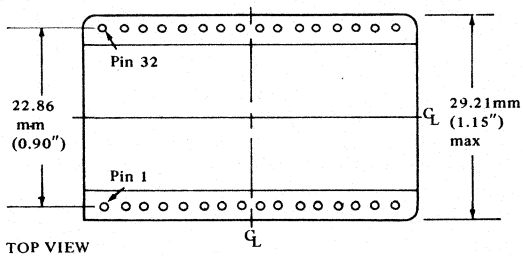
(Typical at 25°C and rated supplies unless otherwise noted.)

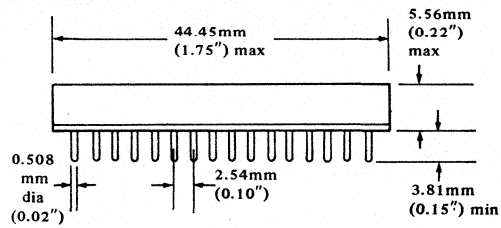
	MP10/MP11
ANALOG OUTPUT	
Number of analog outputs	2
Output voltage range	±10V
Output impedance	1Ω
Output settling time	25 μsec
TRANSFER CHARACTERISTICS	
Resolution	8 bit binary (complementary binary)
One LSB	78.1mV
Throughput accuracy (max)	±0.4% FSR[1,2]
Throughput accuracy (typical)	±0.25% FSR
Temperature coefficient of accuracy	±0.008% FSR/°C

	MP10/MP11
DIGITAL INPUT/OUTPUT	
All signals compatible with the microprocessor bus	
An analog output channel selected by:	A0
Input data bits read by:	D0 - D7
POWER REQUIREMENTS	
	+5VDC ±5% at 90 mA
	+15V ±3% at 30 mA
	-15V ±3% at 30 mA
TEMPERATURE RANGE	
Operating temperature range	0 - 70°C
Storage temperature range	-55°C to +85°C

1. FSR is Full Scale Range = 20V.
2. Accuracy components are: Linearity Error = ±0.2% FSR; Gain Error = ±0.1% FSR, Offset Error = ±0.1% FSR.

MECHANICAL SPECIFICATIONS



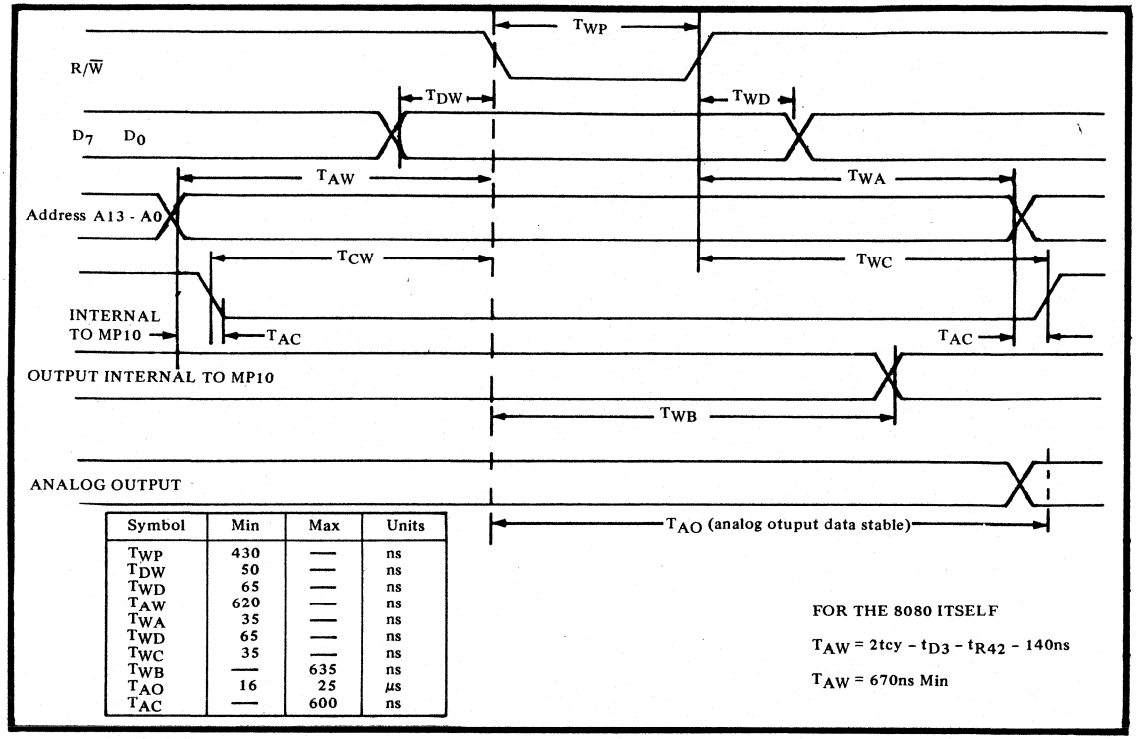


MATERIAL: Alumina
WEIGHT: 14 grams (0.5 oz)
PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
MATING CONNECTOR: 2302MC (Set of two, 16-pin strips)

PIN CONNECTIONS

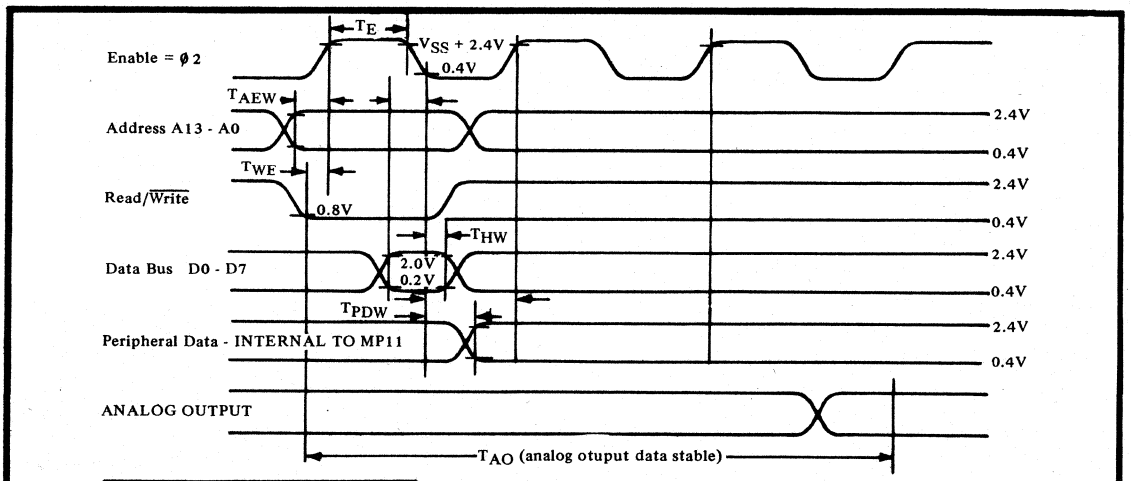
8080 Pin Connections					8080 Pin Connections
1	1	A10	A11	32	40
2	2	Common	A13	31	38
3	3	D4	A12	30	37
4	4	D5	A 9	29	35
5	5	D6	A 8	28	34
6	6	D7	A 7	27	33
7	7	D3	A 6	26	32
8	8	D2	A 5	25	31
9	9	D1 MP10	A 4	24	30
10	10	D0	A 3	23	29
12	11	Reset	A 2	22	27
18	12	R/$\overline{W}$	B 2	21	—
26	13	A1	B 3	20	—
25	14	A0	+5V	19	20
—	15	+15V	Out 1	18	—
—	16	-15V	Out 2	17	—

6800 Pin Connections					6800 Pin Connections
—	1	Output 1	-15V	32	—
—	2	Output 2	+15V	31	—
8	3	+5V	R/$\overline{W}$	30	34
37	4	Enable	$\overline{Reset}$	29	40
9	5	A0	D0	28	33
10	6	A1	D1	27	32
11	7	A2	D2	26	31
12	8	A3	D3	25	30
13	9	A4 MP11	D4	24	29
14	10	A5	D5	23	28
15	11	A6	D6	22	27
16	12	A7	D7	21	26
17	13	A8	Common	20	21
18	14	A9	B2	19	—
19	15	A10	A13	18	23
20	16	A11	A12	17	22



Symbol	Min	Max	Units
T_{WP}	430	—	ns
T_{DW}	50	—	ns
T_{WD}	65	—	ns
T_{AW}	620	—	ns
T_{WA}	35	—	ns
T_{WD}	65	—	ns
T_{WC}	35	—	ns
T_{WB}	—	635	ns
T_{AO}	16	25	μs
T_{AC}	—	600	ns

FIGURE 1. MP10 Timing Diagram.



Symbol	Min	Max	Unit
T_E	0.450	25	μs
T_{AEW}	180	—	ns
T_{DSU}	300	—	ns
T_{WE}	130	—	ns
T_{HW}	10	—	ns
T_{PDW}	—	1.0	μs
T_{AO}	17	25	μs

FIGURE 2. MP11 Timing Diagram.

PROGRAMMING

These units are easily programmed since all are treated as memory locations. They use any memory reference instruction that can write data from internal registers or the accumulator. A single instruction can be used to write data to one or both channels. When the MP10 is used with an 8080, a single SHLD instruction referenced to the lower of the two addresses will automatically transfer the data in the H register to DAC1 and the data in the L register to DAC2. An STA instruction will transfer the data in the accumulator to either DAC. When the MP11 is used with a 6800, a single STX instruction referenced to the lower of the two addresses will automatically transfer the eight upper bits of the index register to DAC1 and the eight lower bits to DAC2. An STAA instruction will transfer the contents of the accumulator to either DAC. Of course, if direct addressing is not desired, MOV instructions may be used to transfer data from internal registers to a specific DAC memory location. As with any programmable peripheral, the MP10 and MP11 must be initialized.

MP10 INITIALIZATION

The RESET input controls the status of the control register of the MP10. An active high on this line will reset the control register to all "zeros".

The MP10 will require initialization every time RESET is activated. If RESET is connected to ground, the MP10 must be initialized only once before output of the data.

MP10 INITIALIZATION SEQUENCE:

1. Load initialization address
2. Load initialization data

MP10 INITIALIZATION ADDRESS:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X	X	1	1	1	1	1	1	1	1	1	1	a	a	1	1
												User Defined			

X = don't care, not connected to MP10
1 = True

MP10 INITIALIZATION DATA

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1	0	0	0	0	0	0	0	$= 80_{16}$

For 8080 the sequence may look as follows:

LXI H, ADDR; ADDR = Initialization address
Loads H & L registers with initialization address

MVI M, DATA; DATA = 80
Loads initialization data (80_{16}) to initialization address

The initialization sequence assigns internal registers tc function as input registers for the D/A converters. Now data can be written into the MP10. This is accomplished by outputing the correct MP10 address:

A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	1	1	1	1	1	1	1	1	1	a	a	0	0	OUTPUT 1
										User Defined				
1	1	1	1	1	1	1	1	1	1	a	a	0	1	OUTPUT 2
										User Defined				

The B_2 and B_3 inputs determine the address to which the MP10 will respond. The four memory locations which are possible are outlined below:

B_2	B_3	A_2	A_3
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

At the time that the address appears on the address bus, data will appear on the data bus and a R/$\overline{W}$ pulse will be generated by the microprocessor. 25μs later, the analog voltage will be stable at the selected output. Timing requirements shown in Figure 1 must be satisfied in order for the MP10 to be initialized and operate correctly. These timing requirements are completely compatible with the 8080.

MP11 INITIALIZATION

The $\overline{\text{RESET}}$ input controls the status of the control and peripheral registers of the MP11. The initialization sequence will differ if $\overline{\text{RESET}}$ is connected to a master reset line of a microprocessor or if it is hard-wired to V_{cc}. The MP11 will require initialization every time the $\overline{\text{RESET}}$ line is activated low. If the $\overline{\text{RESET}}$ line is hard wired to V_{cc}, the MP11 must be initialized only once before output of the data is attempted.

MP11 ADDRESS STRUCTURE

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X	X	1	1	1	1	1	1	1	1	1	1	0	a	Y	Y

A_{15}, A_{14} - don't care, not connected to MP11
A_2 - Address is user selectable
A_0, A_1 - Addresses control the initialization sequence

Initialization sequence when $\overline{\text{RESET}}$ is hard wired to V_{cc}:

1. Load accumulator with "zeros"
2. Store accumulator at memory locations:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
X	X	1	1	1	1	1	1	1	1	1	1	0	a	1	0	Address of Control register A
X	X	1	1	1	1	1	1	1	1	1	1	0	a	1	1	Address of Control register B

3. Load accumulator with "ones"
4. Store accumulator at memory locations:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
X	X	1	1	1	1	1	1	1	1	1	1	0	a	0	0	Address of Peripheral register A
X	X	1	1	1	1	1	1	1	1	1	1	0	a	0	1	Address of Peripheral register B
X	X	1	1	1	1	1	1	1	1	1	1	0	a	1	0	Address of Control register A
X	X	1	1	1	1	1	1	1	1	1	1	0	a	1	1	Address of Control register B

For the 6800 this sequence can be written as follows:

	LDAA	"zeros"	Loads Zeros in accumulator
	STAA	Address of control register A	Stores zero's in C.R.A.
	STAA	Address of control register B	Stores zero's in C.R. B
	LDAA	"ones"	Loads one's in accumulator
	STAA	Address of peripheral register A	Stores one's in P.R.A
	STAA	Address of peripheral register B	Stores one's in P.R.B.
	STAA	Address of control register A	Stores one's in C.R.A
	STAA	Address of control register B	Stores one's in C.R.B
Or as:	LDX	# $0000	Loads zero's in index register
	STX	$ Address control register A	Stores zero's in C.R. A and B
	LDX	# $1111	Loads one's in index register
	STX	$ Address peripheral register A	Stores one's in P.R. A and B
	STX	$ Address control register A	Stores one's in C.R. A and B

Initialization sequence when $\overline{\text{RESET}}$ line is connected to master reset (control registers A and B are always set to zero after master reset and only ones need to be stored in the registers):

LDAA	"ones"
STAA	Address Peripheral register A
STAA	Address Peripheral register B
STAA	Address Control register A
STAA	Address Control register B

or as:

LDXX	# $1111
STX	$ Address Peripheral register A
STX	$ Address Control register A

Now data can be written into MP11. This is accomplished by outputing the correct MP11 address:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
X	X	1	1	1	1	1	1	1	1	1	1	0	a	0	0	OUTPUT 1
X	X	1	1	1	1	1	1	1	1	1	1	0	a	0	1	OUTPUT 2

At the time that the address appears on the address bus, data will appear on the data bus, and if the R/W and Enable pulses are correctly timed, 25μs from the true address the analog voltage will be stable at the selected output.

Timing requirements shown in Figure 1 must be satisfied for the MP11 to be initialized and operate correctly. All timing requirements are completely compatible with 6800 microprocessors. User definable address line A_2 used in conjunction with the B_2 input allows the user to place the MP11 in two different memory locations or use two different MP11's in order to expand the analog system to four outputs. When B_2 is wired to logical 1, the MP11 responds to an A_2 address of 0 and when B_2 is wired to a logical 0, the MP11 responds to an A_2 address of 1.

TEST PROGRAMS

The test circuit and test programs following allow the user to test the operation of the MP10 or MP11. The test may be conducted by setting up the MP10/MP11 as shown in Figure 3. The microprocessor system should have a teletype/CRT terminal interface. The programs will step through several output voltage levels for each DAC output (see Figure 4). Notice how the software is different for the two test programs to illustrate two software approaches.

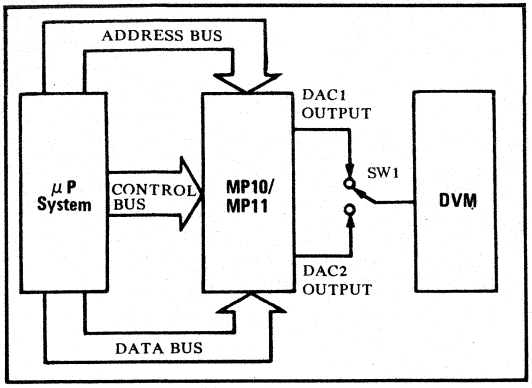


FIGURE 3. Test Circuit for MP10/MP11.

MP10 Test Program

```
                    Initialize MP10
        LXI H ADDR X        Address of the first
                            byte of data.
LOOP 1  MOV A, M            Load ACC with first byte
                            of data.
        STA ADDR2           Output to MP10 DAC1
        INX H               Increment ADDR1
        CALL CI  }          Call Input routine
        CPI      }          Wait for any character
        8D       }          except carriage return
        JNZ LOOP1
        LXI ADDR X
LOOP 2  MOV A, M
        STA ADDR3           Output to MP10 DAC2
        INX H               Increment ADDR1
        CALL CI  }
        CPI      }          Wait for any character
        8D       }          except carriage return
        JNZ LOOP2
        RET
```

The MP10 test program will output five different voltages from DAC1 and then from DAC2 (see Figure 4). DAC1 will initially output -10V. To step through the other values for DAC1 enter any character other than carriage return (CR). To transfer control to DAC2, enter CR. DAC2 will output -10V. To step through the other values for DAC2 enter any character except CR. To exit the test program, enter CR.

Store the following codes in memory beginning with location ADDR X:

ADDR X ← FF
ADDR X + 1 ← BF
ADDR X + 2 ← 7F
ADDR X + 3 ← 3F
ADDR X + 4 ← 00

ADDR 2 is the address of output 1, ADDR 3 is the address of output 2:

MP11 Test Program

```
                              Initialize MP11
        LDX   # $ FFFF;       Load index register
        STX   ADDR 1;         Store FF in each DAC
        JSR   INP
        LDX   # $ BFBF;       Load index register
        STX   ADDR 1;         Store BF in each DAC
        JSR   INP
        LDX   # $ 7F7F;       Load index register
        STX   ADDR 1;         Store 7F in each DAC
        JSR   INP
        LDX   # $ 3F3F;       Load index register
        STX   ADDR 1;         Store 3F in each DAC
        JSR   INP
        LDX   # $ 0000;       Load index register
        STX   ADDR 1;         Store 00 in each DAC
        JSR   INP
INP     LDAA  ADDR X          Load Status  }  Wait for
                              of ACIA      }  TTY
        Bit A #01                          }  input
        BEQ   INP                          }
        LDA A ADDR X + 1      Load Data    }
                              From ACIA    }
        CMP   A                            }  Jump back
        8D                                 }  to test
        BNE   Back                         }  program or
        JMP   Return                       }  return to
BACK RTS                                   }  main program
```

The MP11 test program will output -10V from both DAC1 and DAC2 then wait for an input from the TTY. Any character except CR will advance both DAC's of the MP11 to the next value as defined in Figure 4. CR terminates test program by jumping to RETURN.

ADDR 1 is the address of output 1, ADDR X is the address of the ACIA.

Step	Ideal Output	Actual Output Limits
1	-10V	-9.922V to -10.078V
2	-5.0V	-4.922 to -5.078
3	0.000V	-0.078 to +0.078
4	+5.0V	+4.972 to +5.078
5	+9.922V	+9.844 to +10.000

FIGURE 4. Output Voltages for Test Programs.

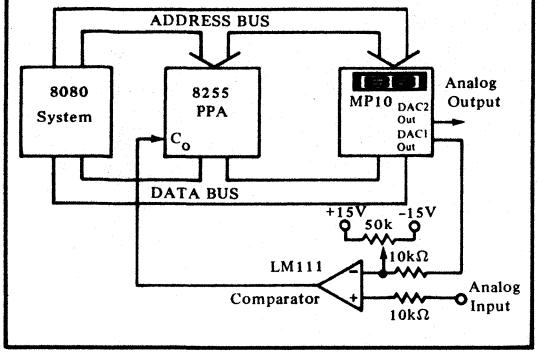
APPLICATIONS

ANALOG INPUT AND ANALOG OUTPUT

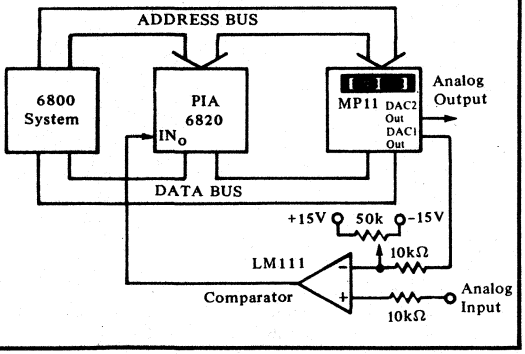
Although the MP10 and MP11 are analog output peripherals, they can be easily adapted to provide both analog inputs and outputs.

With the addition of a few external components, these units can each provide one analog input and one analog output for your system as shown below:

MP10 ANALOG INPUT/OUTPUT



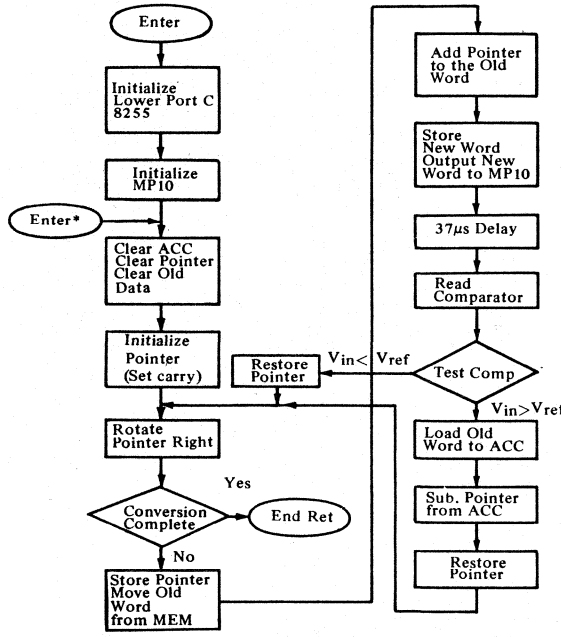
MP11 ANALOG INPUT/OUTPUT



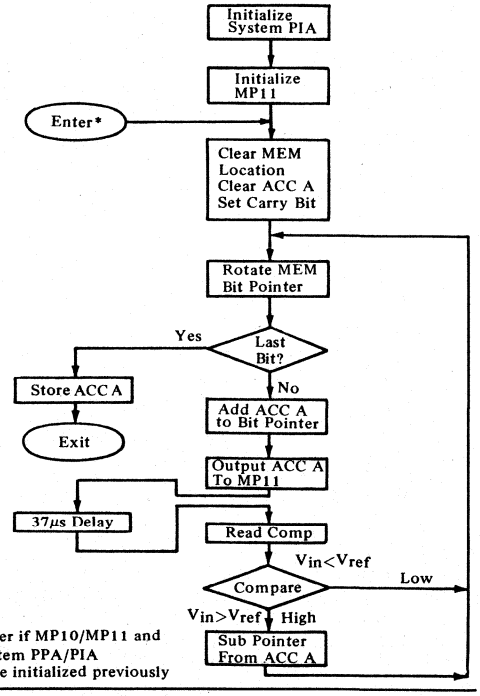
These systems use the microcomputer system to perform the logic of a successive approximation A/D converter, using one channel of the MP10 or MP11 to provide the D/A converter reference function required. In a successive approximation converter, the analog input is compared to known outputs of a D/A converter. First, the microcomputer turns the MSB on, waits for the settling time of the MP10 or MP11, and the switching time of the comparator, then reads the status. If the comparator indicates that the MSB voltage is smaller than the analog input, the MSB input to the MP10/MP11 stays "on" and the next most significant bit is turned on. If the comparator indicates that the MSB value is larger than the analog input, the microcomputer will turn the MSB "off" and turn "on" the next most significant bit. In this way all 8 bits of the D/A converter are tested. When the conversion is complete, the input of the D/A converter will be a digital representation of the analog input. This value will also be stored in the microprocessor's accumulator (complementary binary).

The A/D conversion will require approximately 900 microseconds when performed in this manner. Burr-Brown will shortly have available a detailed application note describing this process including all software required.

FLOWCHART USING 8080 and MP10



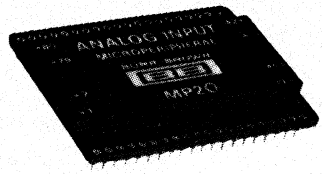
FLOWCHART USING 6800 and MP11



* Enter if MP10/MP11 and system PPA/PIA were initialized previously

BURR-BROWN

MP20



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FEATURES

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  - 8085
  - 8008
  - 8048
  - Z-80
  - SC/MP
- EASY TO PROGRAM
  - Choice of ways to interface:
    - Memory-mapped or I/O mapped
    - Only one instruction to acquire data
- EASY TO USE
  - Completely compatible with 8080A microprocessors
  - PPA is not needed
  - No external logic needed
  - No external adjustments
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PDS-371A
Printed in U.S.A. July, 1978

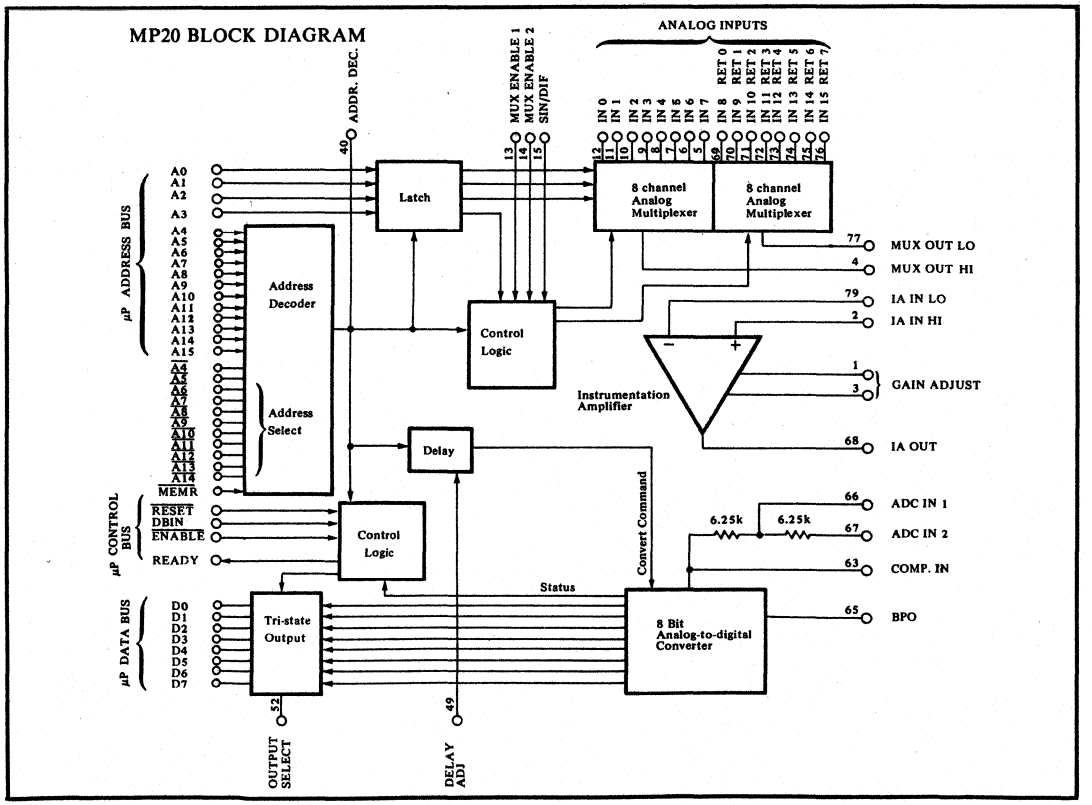
DESCRIPTION

The MP20 is a complete analog input system packaged in an 80-pin quad-in-line package. It is completely compatible with 8080A and 8008 microprocessors. It is also compatible with SC/MP and with the Z-80. The MP20 contains a high speed 8-bit A/D converter, an instrumentation amplifier, an input multiplexer that can accept up to 16 single-ended signals or 8 differential signals as well as interface, timing and address decoding logic. The gain and offset are internally laser trimmed so that no external adjustments are required on the ±5V or 0 to +5V input range to obtain an absolute accuracy of better than ±0.4% (1 LSB). The system can digitize low level or high level analog signals. The gain of the internal instrumentation amplifier can be programmed with a single external resistor to allow input signal ranges as low as ±10 mV. This means that the MP20 can be connected to low level sensors such as thermocouples and strain gauges without external signal amplification.

The address lines A0 through A15 are low power Schottky TTL compatible and can be connected directly to the address bus of an 8080A or 8008. All digital input lines require standard LSTTL voltages.

PROGRAMMING

When programming these peripherals, the user treats them as memory. Each analog input channel occupies one memory location. Any memory reference instruction can be used. Since most microprocessors have been optimized for memory usage, memory reference instructions are the most powerful instructions in a microprocessor's repertoire. The MP20 is treated as memory to simplify software and allow an almost unlimited number of systems to be connected to a single processor. Pins $\overline{A4}$ to $\overline{A14}$ are made available so that the microperipheral address can be hardwired for almost any possible memory location. Since these units are treated as memory, a single instruction is all that's needed to read an input channel. For instance, when the MP20 is used with an 8080A, a single instruction, LHLD, can be used to input data to the H and L registers from two consecutive analog inputs. Likewise, a single LDA or MOV instruction will input data from one channel to the CPU.



SPECIFICATIONS

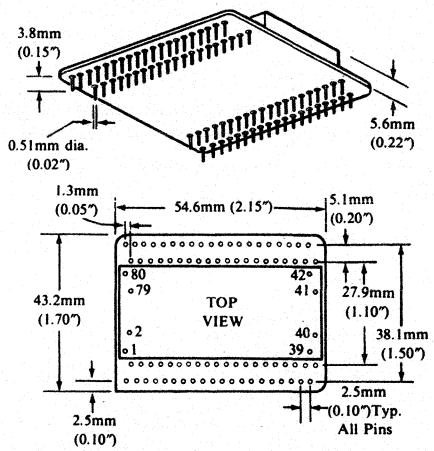
(Typical at 25°C unless otherwise noted.)

ELECTRICAL

TRANSFER CHARACTERISTICS	
Resolution	8 bits binary
Number of channels	16 single-ended/8 differential
Throughput rate[1] (max)	40 μsec/channel
ANALOG INPUTS	
ADC gain ranges	0-5V, 0-10V, ±2.5V, ±5V, ±10V
Amplifier gain range	2 to 250
Amplifier gain equation	$G = 2 + 50k\Omega/R_{EXT}$[2]
Max input voltage without damage[3]	±20 volts
Max input voltage for multiplexer operation	±6 volts
Input impedance	$5 \times 10^9\Omega$ || 10 pF - OFF channel $5 \times 10^9\Omega$ || 100 pF - ON channel
Bias current 25°C	100 nA
0 - 70°C	200 nA
Amplifier output noise	
Gain = 100, R_S = 500 Ω	400 μV rms (10 Hz to 10 kHz)
Amplifier input offset voltage (max)	±1 mV
Amplifier offset voltage drift	±(6 + 50/G) μV/°C
Amplifier settling time (to .1% FSR)	
G = 2	20 μs
G = 10	25 μs
G = 50	50 μs
G = 100	100 μs
G = 200	200 μs
CMRR (for differential inputs) G = 2	70 dB (DC to 60 Hz)
ACCURACY	
Throughput accuracy	
±5V range (max)[4]	±0.4% of FSR[5]
0-5V range (max)[4]	±0.4% of FSR
±50 mV range (max)[6]	±0.8% of FSR
0-50 mV range (max)[6]	±0.8% of FSR
Linearity (max)[4]	±0.2% of FSR
Differential linearity[4]	±0.2% of FSR
Quantizing error	±1/2 LSB
Gain error[4]	±0.1%
Offset error[4]	±0.1% of FSR
Power supply sensitivity	
±15V	$\pm 0.02\%/\%\Delta V_{CC}$
+5V	$\pm 0.002\%/\%\Delta V_{CC}$
STABILITY OVER TEMPERATURE	
System accuracy drift[7] (max)	±40 ppm/°C
Linearity (max)	±20 ppm/°C
Monotonicity (0°C to +70°C)	Guaranteed
DIGITAL INPUT/OUTPUT	
All signals are compatible with Microprocessor bus	
Output coding	Binary or Binary two's complement
Logic loading	All digital inputs are one LSTTL load
Output drive (D0 - D7)	5 TTL loads or 20 LSTTL loads
An analog input channel is selected by:	A0 - A3
The output data bits are read into:	D0 - D7
POWER REQUIREMENTS	
Rated voltages	±15V, +5V
Range for rated accuracy	4.75 to 5.25 and ±14.5 to ±15.5V
Supply drain ±15V	±30 mA
+5V	+90 mA
TEMPERATURE RANGE	0°C to +70°C

(1) Includes 35μsec for mux and amplifier settling time and 5μsec for ADC conversion time.
(2) R_{EXT} is the resistance between pins 1 and 3.
(3) With power applied.
(4) Gain = 2, with no external adjustments.
(5) FSR is Full Scale Range (FSR is 10V for ±5V range).
(6) Gain = 100 with external gain and offset trim.
(7) Includes gain drift, offset drift and linearity drift.

MECHANICAL



MATERIAL: Alumina
WEIGHT: 32 grams (1.2 oz)
PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
MATING CONNECTOR: 2350MC (Set of four 20 pin strips)

PIN CONNECTIONS

Pin		Pin	
1	IA GAIN ADJUST	41	A14
2	IA IN HI	42	$\overline{A14}$
3	IA GAIN ADJUST	43	A15
4	MUX OUT HI	44	$\overline{MEMR}$
5	IN 7	45	$\overline{DBIN}$
6	IN 6	46	$\overline{ENABLE}$
7	IN 5	47	$\overline{RESET}$
8	IN 4	48	READY
9	IN 3	49	DELAY ADJ
10	IN 2	50	+5V
11	IN 1	51	DIG. COM
12	IN 0	52	OUTPUT SELECT
13	MUX ENABLE 1	53	D7 (MSB)
14	MUX ENABLE 2	54	D6
15	SIN/DIF	55	D5
16	A0	56	D4
17	A1	57	D3
18	A2	58	D2
19	A3	59	D1
20	A4	60	D0 (LSB)
21	$\overline{A4}$	61	-15V
22	A5	62	+15V
23	$\overline{A5}$	63	COMP IN
24	A6	64	ANA. COM
25	$\overline{A6}$	65	BPO
26	A7	66	R2
27	$\overline{A7}$	67	R1
28	A8	68	IA OUT
29	$\overline{A8}$	69	IN 8 RET 0
30	A9	70	IN 9 RET 1
31	$\overline{A9}$	71	IN 10 RET 2
32	A10	72	IN 11 RET 3
33	$\overline{A10}$	73	IN 12 RET 4
34	A11	74	IN 13 RET 5
35	$\overline{A11}$	75	IN 14 RET 6
36	A12	76	IN 15 RET 7
37	$\overline{A12}$	77	MUX OUT LO
38	A13	78	OFFSET NULL
39	$\overline{A13}$	79	IA IN LO
40	ADDR DECODE OUT	80	OFFSET NULL

PIN FUNCTIONS

IA GAIN ADJUST (Optional). Pin 1 and Pin 3. By connecting a resistor between pin 1 and 3 the gain of the internal instrumentation amplifier can be varied as follows:

$$\text{Gain} = 2 + 50k\Omega/R$$

where R is the gain setting resistor. The IA is factory adjusted for a gain of 2 without any external resistor.

Important: If a gain greater than 10 is required an external capacitor must be connected from "DELAY" (pin 49) to +5V. This increases an internal delay to allow for the increased settling time of the instrumentation amplifier.

IA IN HI Pin 2. This is the positive input of the internal instrumentation amplifier. This should be connected to pin 4 (MUX OUT HI) for normal operation.

MUX OUT HI Pin 4. This is the high output of the analog input multiplexer. This is connected to pin 2 (IA IN HI) for differential operation. It is connected to pin 77 (MUX OUT LO) and pin 2 for single-ended input operation.

IN7 - IN0 Pins 5 - 12. The first 8 (of 16) analog inputs for single-ended operation or the 8 positive inputs for 8 channel differential input operation.

MUX ENABLE 1 Pin 13. Leave open for single-ended input operation. Connect to pin 14 (MUX ENABLE 2) for differential input operation.

MUX ENABLE 2 Pin 14. Connect to pin 15 (SIN/DIF) for single-ended input operation. Connect to pin 13 (MUX ENABLE 1) for differential input operation.

SIN/DIF Pin 15. Single/Differential input operation connect to pin 14 (MUX ENABLE 2) for single-ended operation. Leave open for differential input operation.

A0 - A3 Pin 16 - 19. Address lines that select one of 16 analog input signals (IN0 - IN15). 0000 selects channel 0 and 1111 selects channel 15 when the correct address is presented to the MP20. Connect A3 to ground for 8 channel differential operation.

A4 - A15 Address lines. Pins 20, 22, 24, 26, 28 30, 32, 34, 36, 38, 41, and 43. When the proper address is presented to the MP20 in addition to the $\overline{\text{MEMR}}$ (pin 44) pulse, the conversion is initiated.

$\overline{\text{A4}}$ - $\overline{\text{A14}}$ Address select lines. Pin 21, 23, 25, 27, 29, 31, 33, 35, 37, 39 and 42. By connecting these lines to DIG COM or +5 volts (through a 1kΩ resistor) almost any address can be assigned to the MP20. For example if $\overline{\text{A4}}$ is connected to GND., the correct (valid) address for A4 is a "1" (> + 2.0).

ADDR DEC Pin 40. A positive pulse will appear when a valid address appears on the MP20 address lines and $\overline{\text{MEMR}}$ (pin 44) is low. The rising edge of this pulse strobes the input channel select information (A0 - A3) into a latch. It can also be used for external purposes.

$\overline{\text{MEMR}}$ Pin 44. Memory read. A "Low" pulse on this line along with a correct address will enable D0 - D7 (data lines). Also used to initiate a conversion.

DBIN Pin 45. Connect to DBIN on 8080.

$\overline{\text{ENABLE}}$ Pin 46. Enables MP20 output. Connect to ground for normal operation (see figure 7).

$\overline{\text{RESET}}$ Pin 47. A "Low" on this line is required to RESET the MP20. Connect to RESIN input of the system's 8224 or invert 8080's RESET input.

READY Pin 48. When the MP20 is "Read" by the microprocessor, the READY line will go "Low" until conversion is complete. If the READY line is used to halt the CPU, the 8080 will enter a "Wait" state (T_w) until the multiplexer, instrument amp, and A/D converter have completed converting the analog data to a binary 8 bit code (40 μsec with gain ≤ 10). The READY line will then return to its "High" state which releases the processor from the T_w state. The output data appears on the data bus (D0 - D7) during the T_3 state.

DELAY ADJ Pin 49. When the MP20 is addressed, an internal delay of approximately 35μsec is initiated to allow for multiplexer and instrumentation amplifier settling time. When the IA is operated with gain > 10 this delay must be increased (see figure 4 and figure 5) to allow for the increased settling time of the IA.

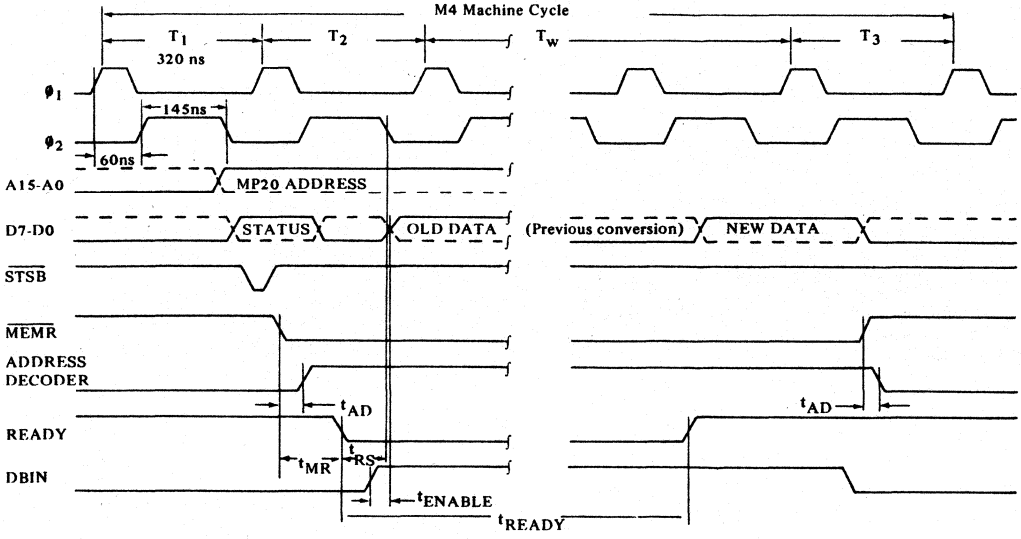
+5V Pin 50. +5 volt at 140 mA maximum, 90 mA typical.

DIG COM Pin 51. Digital common. This pin should be connected to analog common (pin 64) as close to the MP20 as possible for optimum performance.

OUTPUT SELECT Pin 52. This pin should be connected to DIG COM to obtain binary data at D0 - D7. To obtain two's complement data (bipolar mode) connect pin 52 to +5V through a 1kΩ resistor.

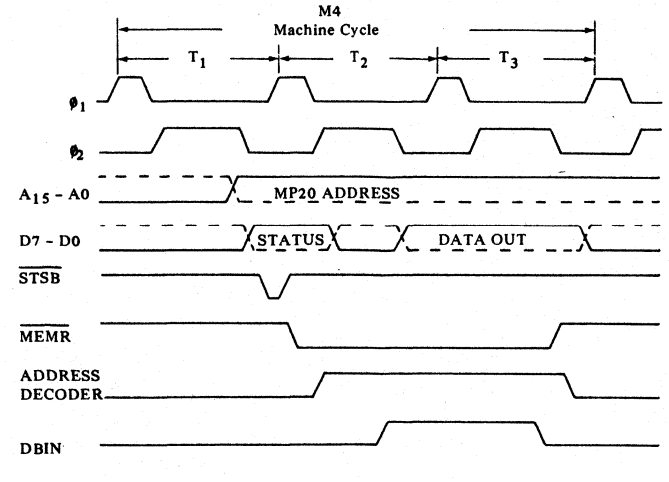
D7 - D0 Pin 53 - 60. 8 bit data bus. Tri-state low power Schottky TTL compatible.

-15V	Pin 61. -15 volt at 30 mA typical.
+15V	Pin 62. +15 volt at 30 mA typical.
COMP IN	Pin 63. Comparator input of 8 bit A/D converter (successive-approximation). Leave open for unipolar operation or connect to "BPO" (pin 65) for bipolar operation. NOTE: This point is extremely sensitive to noise. Any connection to this line should be as short as possible and shielded by ANA COM or ±15 volt supply patterns.
ANA COM	Pin 64. Analog common should be connected to digital common (pin 51) as close to the MP20 as possible for optimum performance.
BPO	Pin 65. A/D converter bipolar offset. It should be connected to ANA COM (pin 64) for unipolar operation of COMP IN (pin 63) for bipolar operation.
R2	Pin 66. A/D converter input resistor. Connect to IA OUT (pin 68) for 0 to +5V input unipolar operation or ±2.5V input bipolar operation. Leave open for ±5V input bipolar operation.
R1	Pin 67. A/D converter input resistor. Connect to IA OUT for ±5 volt operation.
IA OUT	Pin 68. Instrumentation amplifier output. Connect to R1 (pin 67) or R2 (pin 66) for normal operation.
IN8 - IN15 RET0-RET7	Pin 69 - 76. Analog inputs 8 through 15 for single-ended operation or analog returns 0 through 7 for differential input operation.
MUX OUT LO	Pin 77. Multiplexer output for IN8 – IN15 RET0 – RET7 Connect to "MUX OUT HI" (pin 4) and "IA IN HI" (pin 2) for single-ended input operation or connect to "IA IN LO" (pin 79) for differential input operation.
OFFSET NULL	Pin 78, 80. Optional instrumentation amplifier offset adjust (see figure 1).
IA IN LO	Pin 79. Negative input of instrumentation amplifier. Connect to ANA COM (pin 64) for single-ended input operation or "MUX OUT LO" (pin 77) for differential input operation.



All waveforms shown are for an 8080A – 1 microprocessor operating at:
CLOCK PERIOD (t_{CY}) = 320 ns
INSTRUCTION CYCLE = 1.3 μs
ϕ_1 and ϕ_2 clock signals are shown for reference only. They are not required for operation of MP20.

MP20 Timing Diagram Normal Operation (LDA Instruction using READY to stop microprocessor during conversion).



SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AD}	Delay from $\overline{MEMR}$ to ADDR. DEC.	-	25	ns
t_{MR}	Delay from $\overline{MEMR}$ and correct address to READY	-	100	ns
t_{RS}	Delay from READY to ϕ_2.	-	90	ns
t_{ENABLE}	Output Data Stable from DBIN	-	40	ns
t_{READY}	Conversion time (READY low)	-	40	μs

The LDA Instruction will READ the data from the previous conversion and start a new conversion. The new data can be read in 40 μs (max).
CAUTION: Do not read the MP20 while a conversion is in progress or an erroneous output may result.

MP20 Timing Diagram (LDA Instruction without stopping microprocessor during conversion).

OPERATING INSTRUCTIONS

PROGRAMMING

The MP20 is easily programmed since it is treated as memory. It uses any memory reference instruction that can read data. A single instruction can read data from one channel (LDA) or two adjacent channels (LHLD).

Example: MP20 used with an 8080. MP20 base address - FF70; acquire data from channels FF70 through FF72. Normal operation.

LHLD FF70	Acquires data and transfers channel 0 (FF70) data to L register and channel 1 (FF71) data to H register.
LDA FF72	Acquires data from channel 2 (FF72) and transfers to the accumulator.

The MP20 may be operated in several programming modes. The minimum software approach (i.e., one instruction to acquire data as described above) is to halt the CPU during conversion (40 μsec). This mode of operation is effected by connecting the READY line (pin 48) of the MP20 to the 8080's READY input. The MP20 may also be operated without halting the CPU. In this mode of operation conversion may be initiated by a memory read instruction referenced to the proper channel. When the conversion is complete, the data value may be acquired by another read instruction. The second read instruction can be referenced to any channel address of the MP20. This instruction should be addressed to the next channel to be acquired since it will start a conversion cycle.

Example: MP20 used with an 8080. MP20 base address - FF70; acquire data from channels FF70 through FF72. Do not halt CPU.

LDA FF70	Starts conversion of channel 0 (FF70).
⋮	At least 40 microseconds of software here to insure that conversion is complete.
LDA FF71	Transfers conversion data from channel 0 (FF70) to accumulator and starts conversion of channel 1 (FF71).
⋮	At least 40 microseconds of software.
LDA FF72	Transfers conversion data from channel 1 (FF71) to accumulator and starts conversion of channel 2 (FF72).
⋮	At least 40 microseconds of software.
LDS FF7X	Transfers conversion data from channel 2 (FF72) to accumulator and starts conversio of any other channel of data.

The time required for conversion may be between 40 and 200 microseconds depending upon the gain of the internal instrumentation amplifier. Therefore, the 40 microsecond time between LDA instructions shown above could be as long as 200 microseconds for a system used in the highest gain mode. If desired, the READY line may be polled to determine that conversion is complete and the data output valid. Of course, if direct addressing is not desired, MOV instructions may also be used.

Example: MP20 used with an 8080. MP20 base address FF70. Normal Operation. Read and Print the value of all 16 input channels and then stop.

```
CROUT   EQU 01F3H (01EEH)
NMOUT   EQU 02C2H (02C3H)
        LXI SP 3FFF H (13EDH)
        LXI H 0FF70 H     :Address for channel zero
BEG 1:  MOV D, M          :Read data from board
        CALL CROUT        :Print CR & LF
        MOV A, D
        CALL NMOUT        :Print data
```

```
        INX H           :Next channel
        MOV A, L
        CPI 10          :Have all 16 channels
                         been read?
        JZ WHOA
        JMP BEG 1
WHOA:   HLT
```

This program assumes that the system is under the control of the SBC80/10 prototype package monitor (M80P, version 1.0, March 1, 1976). The locations in parenthesis are used with the MCS-80 system design kit.

The base address of the MP20 is set by inputs $\overline{A4}$ through $\overline{A14}$. Address lines A4 through A14 respond to the inverse of inputs $\overline{A4}$ through $\overline{A14}$. For instance, if $\overline{A6}$ is grounded, A6 will respond to a "high" input. A15 is internally connected to respond to a "high" input.

ANALOG INPUT RANGE SELECTION

The MP20 may be set for any range between ±5V and ±10 mV. Table I shows the pin connections for the various high level ranges available.

MP20 Input Range	Gain	ADC Range	Pin Connections
±5V	2	±10V	65 to 63; 66 open; 67 to 68
±2.5V	2	±5V	65 to 63; 66 to 68; 67 open
±1.25V	2	±2.5V	65 to 63; 66 to 68; 63 to 67
0 - 5V	2	0 - 10V	65 to 64; 66 to 68; 67 open
0 - 2.5V	2	0 - 5V	65 to 64; 66 to 68; 63 to 67

Table I. Analog Input Range Pin Connections

The MP20 may be set to output data with straight binary coding (pin 52 grounded) or two's complement coding (pin 52 to +5VDC through a 1 kΩ resistor). Straight binary coding is typically used with unipolar input ranges and two's complement coding with bipolar input ranges. Table II describes the coding.

The internal instrumentation amplifier is factory set for a gain of 2. This gain can be increased to 250 by adding an external resistance (R_{ext}) between pins 1 and 3. R_{ext} should be a stable resistor (10 ppm/°C) since this temperature drift will add to the accuracy temperature coefficient. The gain of the amplifier can be determined by this formula:

$$\text{Gain} = 2 + \frac{50k}{R_{ext}}$$

With pins 1 and 3 open, the gain is 2.

Since the amplifier input offset will be multiplied by the amplifier gain, an offset adjust may be required (see figure 1b).

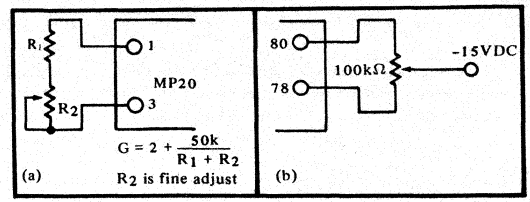


FIGURE 1. (a) MP20 Gain Adjust; (b) Offset Adjust

SINGLE ENDED VS. DIFFERENTIAL INPUTS

The MP20 analog inputs may be connected as single-ended, differential or pseudo-differential. Single-ended operation may be used for high level (over one volt full scale) signals in low noise environments (Figure 3). Differential operation will reject common-mode noise appearing on both inputs (Figure 2). It should be used in noisy environments or with any low level signal (less than one volt). In the pseudo-differential mode, the MP20 is connected as for the single-ended mode in Figure 3 except the I.A. low input, pin 79, is not grounded. Pin 79 is connected to an external ground that is common to all of the analog inputs. In cases with a noisy remote ground where little noise will be picked up between sensor and MP20, the pseudo-differential mode may be used.

The MP20 is set for single-ended operation when wired as shown in Figure 3. The microprocessor address lines are connected as indicated in the Pin Connections table on page 5-105. Differential operation occurs when the unit is connected as in Figure 2. However, address line A3 (Pin 19) should be grounded and A3 on the microprocessor connected to A4 on the MP20. The remainder of the higher ordered microprocessor address bits should be connected to the next higher bit on the MP20.

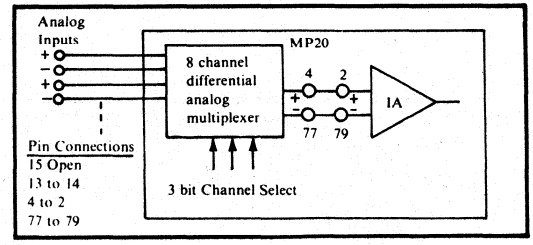


FIGURE 2. Differential Input Connections

	DIGITAL OUTPUT		ANALOG INPUT		
Straight Binary Code	Two's Complement Code		±5V	0 to +5V	±10mV
1111 1111 (FF_{in})	0111 1111 ($7F_{in}$)	+Full Scale	+4.961V	+4.980V	+9.92mV
1000 0000 (80_{in})	0000 0000 (00_{in})	Mid-Scale	0.000V	2.500V	0.000V
0000 0000 (00_{in})	1000 0000 (80_{in})	-Full Scale	-5.000V	0.000V	-10.00mV
		One LSB	39mV	19.5mV	78µV

TABLE II. Analog Input Values

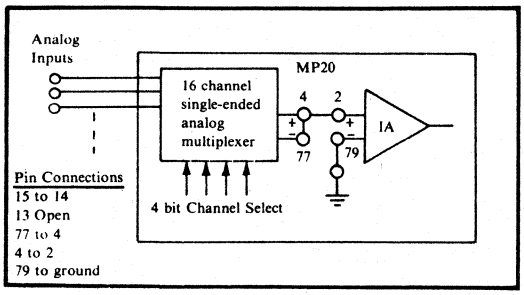


FIGURE 3. Single-ended Input Connections

DELAY TIMING

A delay time between channel selection and start of conversion is built into the MP20 to allow the analog multiplexer and instrumentation amplifier (I.A.) time to settle before starting the A/D converter. As the gain of the amplifier is increased, the settling time required increases. The factory set delay time (35 μsec) is sufficient for gains of up to 10. At higher gains, a capacitor must be added from pin 49 to the +5 VDC supply to increase the delay time. Figure 4 shows the settling time of the MP20 vs. gain. Figure 5 shows the value of capacitance required to increase the delay.

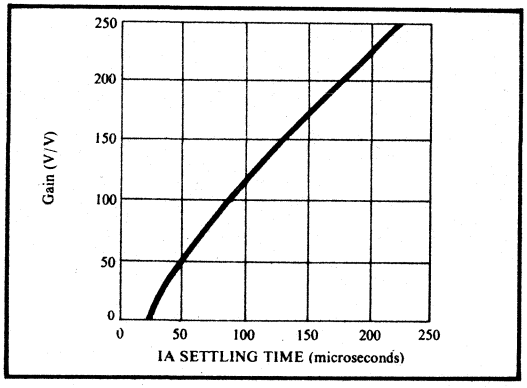


FIGURE 4. Typical IA Settling Time vs Gain (Output Settling to ±0.1%)

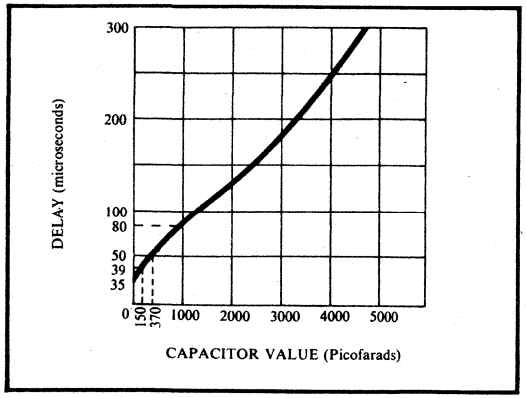


FIGURE 5. Typical Delay Time vs Capacitor Value

The only external factor, other than gain, that effects the MP20 settling time is the impedance of the source connected to a channel. Figure 6 shows a circuit model of an "ON" channel.

The signal at the output of the multiplier must be allowed to settle to ±0.1% (six time constants) to maintain the full accuracy of the system. The multiplexer time constant can be calculated with the formula: $\tau = (R_S + R_{ON})\,C_o$. For R_S = 1 kΩ and C_o = 50 pF, τ = (1.5 + 1) kΩ x 50 pF = 125ns. Thus 0.75 μs is needed to settle to ±0.1%. For high input impedances requiring more than 10 microseconds for mulitplexer settling time, the required delay time may be calculated with this formula: $T_D = \sqrt{T^2_{mux} + T^2_{IA}}$, where T_{mux} is the settling time of the multiplexer and T_{IA} is the settling time of the instrumentation amplifier as shown in Figure 4. If the source bandwidth can be limited, high impedance sources may be accurately handled by placing a large capacitance across the multiplexer input. An analysis of such a circuit shows that a capacitor of 0.5μF is sufficient. For such a capacitance the multiplexer time constant becomes 80 ns.

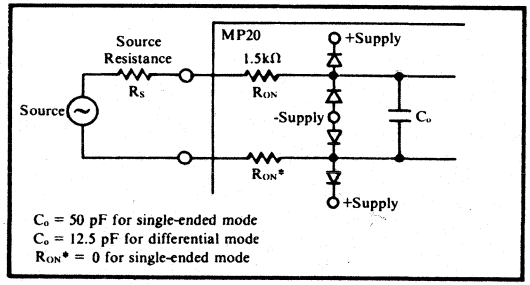


FIGURE 6. "ON" Channel Circuit Model

INPUT OVERVOLTAGE PROTECTION

As shown in Figure 6, the analog inputs have reverse biased diode circuits which protect from damage by overvoltage (such as static). It is still reasonable to take precautions against static discharge. The same circuitry protects the inputs from steady-state overvoltage damage during operation. The MP20's overvoltage protection can be increased by adding series resistors at each input. The input resistance must limit the current flowing through the input protection diodes to 10 mA. For instance, if 15 kΩ resistors are added to each input, the protection is increased to 165V (16.5kΩ x 10mA). Increased input resistance will, of course, increase the amount of time necessary for the multiplexer to settle as described in the previous section.

OUTPUT ENABLE

The circuitry used to enable the tristate output lines (D7 - D0) on the MP20 can be connected in such a way as to meet a wide variety of timing requirements. The output is enabled only when the address decoder output (pin 40) is high, DBIN (pin 45) is high, and $\overline{\text{ENABLE}}$ (pin 46) is low. Any other combination of digital signals on these lines will result in D7 - D0 being in a high impedance state (see Figure 7).

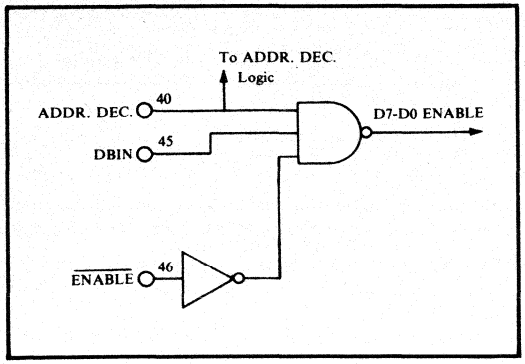


FIGURE 7. Output Enable Circuitry

The combination of a correct address and a memory read ($\overline{\text{MEMR}}$ - pin 44) command will cause the address decoder output to go high. If $\overline{\text{ENABLE}}$ is not used it should be connected to DIG COM. If DBIN is not used it should be connected to +5 volts through a 1kΩ resistor. Most applications will only require the use of one of these lines.

RESET

It is important to reset the MP20 on start up with a low pulse on the $\overline{\text{RESET}}$ line (pin 47) if the READY line (pin 48) is being used to halt the processor. The reset pulse simply clears an internal flip-flop and guarantees that on start up the READY line will go high thereby not halting CPU.

If the MP20 conversion cycle is being timed out by software control, a reset pulse is not necessary. If the $\overline{\text{RESET}}$ line is not used it should be connected to +5 volts.

HIGHER SPEED OPERATION

The MP20's internal instrumentation amplifier requires 35 microseconds to allow for settling time. If this internal amplifier is not used, substantial improvements in throughput rate can be obtained. This is easily done since neither the inputs or the output of the instrument amplifier are internally connected. For instance, Burr-Brown's 3622 high speed instrument amplifier (for differential inputs) or 3505J high speed op amp (for single-ended inputs) may be used, with a settling time of 1 μsec for gains of up to 100. The total delay time necessary may be calculated by this formula:

$$T_D = \sqrt{T^2_{MUX} + T^2_{IA}},$$

where T_{MUX} is the settling time of the multiplexer (750ns) and T_{IA} is the settling time of the instrument amplifier. For a T_{IA} of 1 μsec we have $T_D = 1.3$ μsec. Using 3μsec for the delay time to allow for unit to unit variation, the total throughput time will be 8 μsec (including 5 microseconds for ADC conversion time) or 125 kHz. A resistor between pin 49 and +5 VDC will reduce the delay time from the factory set value of 35 microseconds (see figure 8).

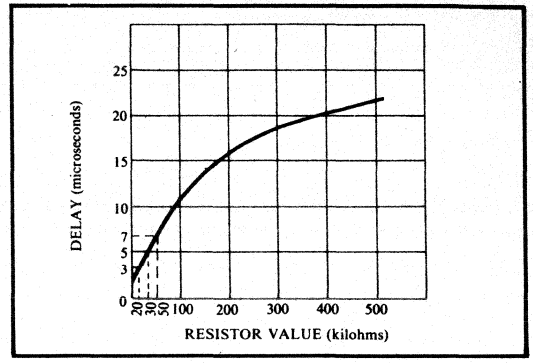


FIGURE 8. Typical Resistor Value to decrease Delay Time

CALIBRATION

The MP20 is laser trimmed at the factory to ±0.4% accuracy when using the ±5V or 0 to +5V ranges. If one of these ranges is used, no adjustments are required. If the ±2.5V, ±1.25V or 0 to +2.5V ranges are used, an offset adjust only is required. For other ranges, both the gain and offset must be adjusted. Figure 1 shows the adjustment connections. The gain adjustment should be made such that the transition to a full scale output (1111 1110 to 1111 1111 for straight binary) occurs with an input of positive full scale less 1 and 1/2 LSB's. One least significant bit (LSB) is the full scale range (FSR) divided by 2^n where n is the number of bits of the A/D converter. For the MP20, one LSB is $FSR/2^8 = FSR/256$. The offset adjustment should be made such that the transition to minus full scale output (0000 0001 to 0000 0000 for straight binary) occurs with an input of negative full scale plus one half LSB. For a range of ±50 mV, one LSB = 100 mV/256 = 0.39 mV. The gain adjustment should be made at +50 mV - (1.5)(0.39 mV) = +49.42 mV. The offset adjustment should be made at -50 mV + (0.5)(0.39mV) = 49.80 mV. Table III shows offset and gain calibration values for typical ranges.

MP20 Input Range	Instrument Amp Gain	ADC Range	Calibration Values	
			Offset	Gain
±5V	2	±10V	-4.980V	+4.941V
0 to +5V	2	0 to +10V	+9.8mV	+4.971V
±2.5V	2	±5V	-2.490V	+2.471V
0 to +2.5V	2	0 to +5V	+4.9mV	+2.485V
±1.25V	2	±2.5V	-1.245V	+1.235
0 - 50mV	100	0 to +5V	+98 μV	+49.7mV
±25mV	100	±2.5V	-24.9mV	+24.7mV
0 - 25mV	200	0 to +5V	+49 μV	+24.9mV

Table III. Calibration Values.

The following program may be used to adjust gain and offset.

```
REF     EQU  00H              Offset Ref =00H
                              Full Scale Ref = FFH

CO      EQU  01E8H(01E3H)     Monitor routines

CROUT   EQU  01F3H(01EEH)
```

```
NMOUT EQU     02C2H(02C3H)
      ;
      ORG     3C50H
      ;
      LX1     H, 0FF7ØH       Initialize
      LX1     SP,3FFFH(13EDH)
BEG1: MVI     E,10H
BEG2: LXI     B, 0
CLP:  MOV     A, M            ;Read data from
                              board
      SUI     REF             ;Increment data
                              count if data =
                              REF
      JNZ     NEQ
      INR     B
NEQ:  INR     C               ;Have 100
                              conversions
                              been made?
      MVI     A, 64H
      SUB     C
      JNZ     CLP
      MOV     A, B            ;Yes, Print data
                              count
      CALL    NMOUT
      MVI     C,20H           ;Print a space
      CALL    CO
      DCR     E               ;Full line been
                              printed?
      JNZ     BEG2
      CALL    CROUT           ;Yes, Print CR
                              & LF
      JMP     BEG1
      END
```

This program assumes that the system is under the control of the SBC80/10 prototype package monitor (M80P, version 1.0, March 1, 1976). The locations in parenthesis are used to allow the program to work with the MCS-80 system design kit. It may be used for both offset and gain calibration. The system offset should be adjusted first, followed by the gain adjustment.

The address of channel zero is assumed to be FF7Ø. If it is not, the LXI H instruction should reflect that change. The reference values on the first line assume straight binary coding. For offset binary coding, Offset Ref = 80 and Full Scale Ref = 7F.

A G3C50 monitor command will begin program execution. After 100 conversions have been made, the value (in hex) of the B register will be printed. This value represents the number of times the data read from the board was equal to "REF" (00 for offset; FF for gain).

Calibration is performed by connecting a voltage source capable of 0.01% accuracy to input channel zero (this could also be a DC voltage source of less absolute accuracy whose output is monitored by a 0.01% DVM).

The offset adjustment is made first by using the appropriate offset calibration voltage. Run the calibration program and adjust the on board offset potentiometer until the B register contains a value between $1E_{16}$ and 46_{16} (30_{10} and 70_{10}).

To perform the gain adjustment change the data labeled "REF" in the calibration program from 00 to FF, set the input voltage to the correct value as shown in Figure 8 and adjust the on board gain potentiometer in the same manner as described for offset.

If the SBC80 monitor is available, the substitute (S) command can be used to interrogate an input channel.

THERMOCOUPLE TEMPERATURE ACQUISITION

Thermocouples are often used as temperature sensors for process control systems. Thermocouples are characterized by temperature coefficients of 10 to 70 $\mu V/^{\circ}C$ and operating ranges of minus hundreds to plus thousands of degrees centigrade. When the MP20 is operated with an instrumentation amplifier gain of 100 or more, it may be connected directly to these devices. The wire runs from thermocouple to measuring device often pick up large common-mode noise signals of 60 Hz or higher frequencies. When the MP20 is used as an eight channel differential input system, the high common-mode rejection of the instrument amplifier will reject common-mode noise. To minimize differential mode noise, the signal wire should be twisted and if possible shielded. As a rule an unshielded twisted pair is better than a coax, and a shielded, twisted pair is still better. In applications where these wiring practices cannot always be observed, a differential RC filter may be used. Figure 9 shows such a system.

The 10 kΩ resistors and 10 μF capacitor provide low pass filtering (f_c = 0.8 Hz) while the optional 1 MΩ resistors supply bias current to the instrumentation amplifier. The remote sensor should be earth grounded to prevent common-mode voltages from exceeding the ±5 volt range of the multiplexer. If the sensor is earth grounded, the 1 MΩ resistors are not required. The 1 MΩ resistors do not enter into an error calculation for input errors because the low resistance of the sensor shorts any differential voltage that might be caused by the offset (difference current) of the amplifier. Offset or difference current is merely the difference between the bias current of each input. See the overvoltage protection section for a discussion of the effects of the 10 kΩ in the input filter. The 1 MΩ resistors could have been put on the output side of the multiplexer eliminating the need for repeating them for each input; however, this would have loaded the 10 k resistors of the filter causing a possible 1% error for static conditions.

To complete a thermocouple system it is necessary to terminate all thermocouple wire pairs at an isothermal box or connector strip of some type. An ordinary barrier strip may be monitored to allow the observed thermocouple emf to be cold junction compensated. Figure 9 shows an excellent circuit for this purpose. Its output is connected to one of the input channels to supply ambient temperature data to the system computer. Its output sensitivity is approximately 2 $mV/^{\circ}C$.

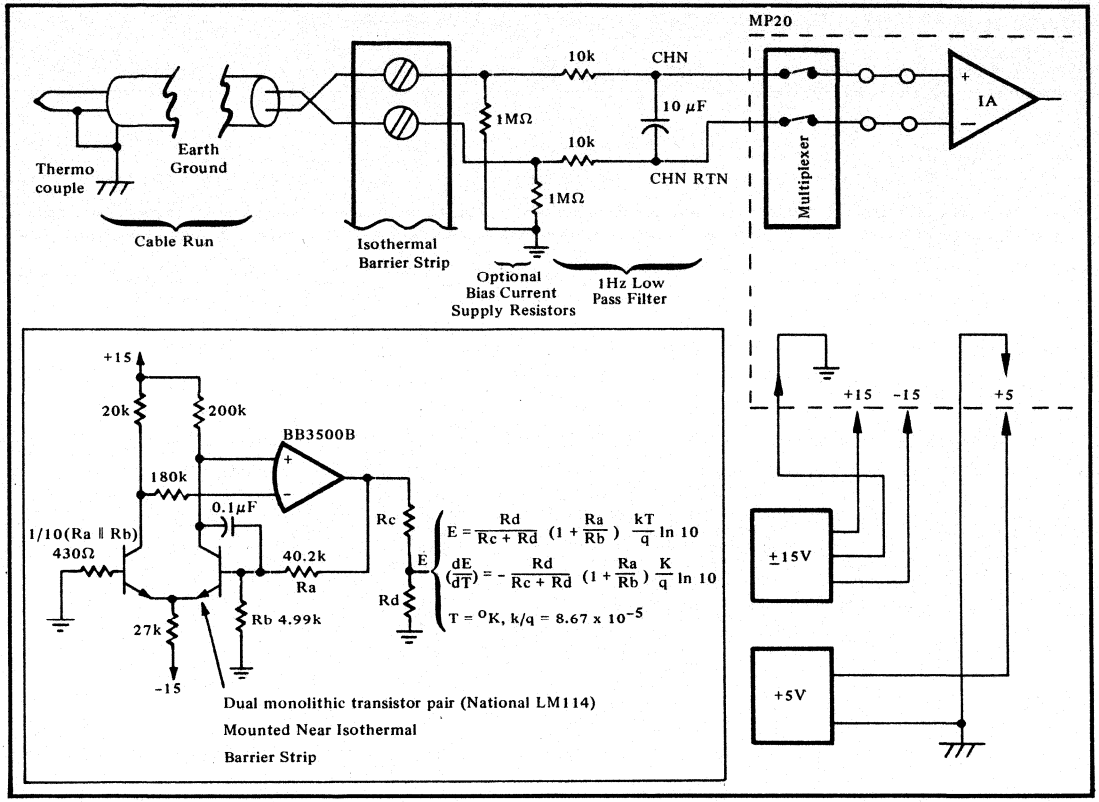


FIGURE 9. Thermocouple Input System Using MP20

PIN CONNECTION SUMMARY

	JUMPER		JUMPER
Single-ended Multiplexer	4 to 2; 4 to 77; 79 to 64; 15 to 14; 13 open	Address Bus (A0-A15)	Connect to 8080's address bus A0-A15
Differential Multiplexer	4 to 2; 77 to 79; 13 to 14; 15 open	Address Select ($\overline{A4}$-$\overline{A14}$)	Connect to +5V* or Ground
Amplifier	1 and 3 open for G = 2; R_{ext} between 1 and 3 for G≠2.	Control Bus	44 to 8228's $\overline{MEMR}$ output (pin 24) 45 to 8080's DBIN output (pin 17) 46 to ground 47 to 8224's $\overline{RESIN}$ input (pin 23) for normal operation 48 open for operation without halting CPU.
Input Range ±5V ±2.5V ±1.25V 0 - 5V 0 - 2.5V	 65 to 63; 66 open; 67 to 68 65 to 63; 66 to 68; 67 open 65 to 63; 66 to 68; 63 to 67 65 to 64; 66 to 68; 67 open 65 to 64; 66 to 68; 63 to 67		
Output Coding	52 to 51 for binary; 52 to 50* for two's complement.	Data Bus (D0 - D7)	Connect to 8080's data bus.
* Through a 1kΩ resistor			

MICROPROCESSOR INTERCONNECTION

The following diagrams show interconnections of the MP20 (described in this data sheet) and also of Burr-Brown's MP10 analog output microperipheral (PDS-363) with Intel's 8080, National's SC/MP and Zilog's Z-80.

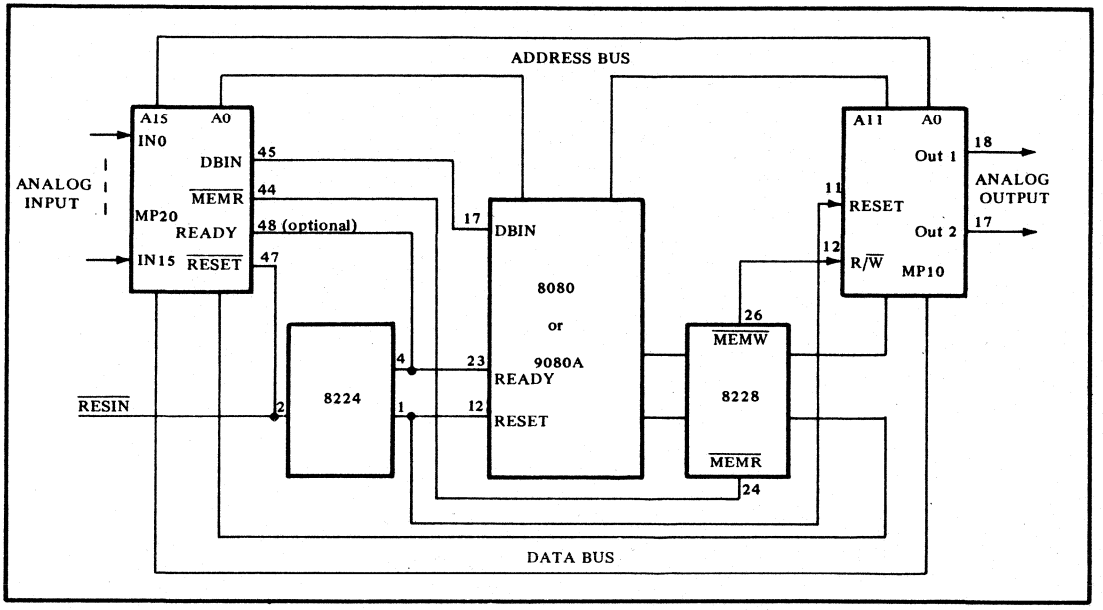


FIGURE 10. MP10 and MP20 Used With the 8080

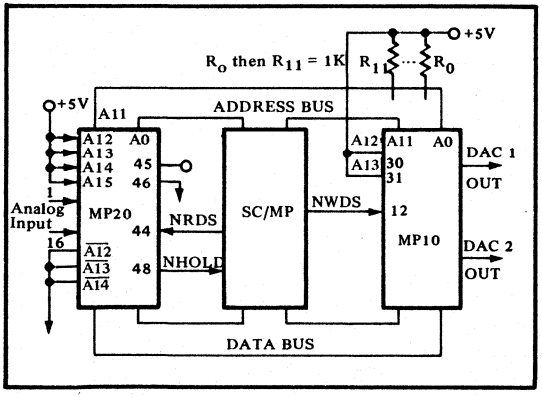


FIGURE 11. MP10 and MP20 Used With the SC/MP

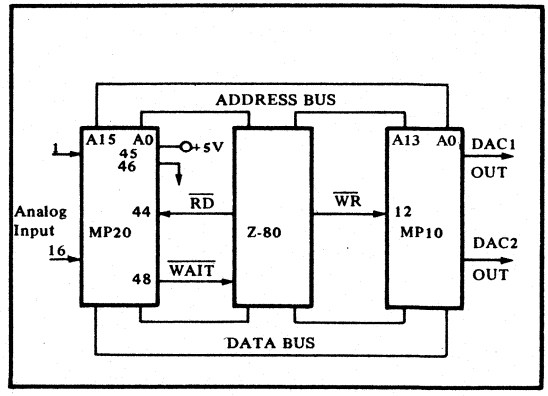
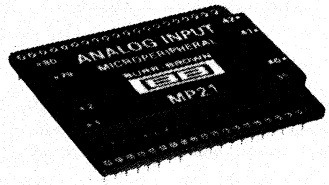


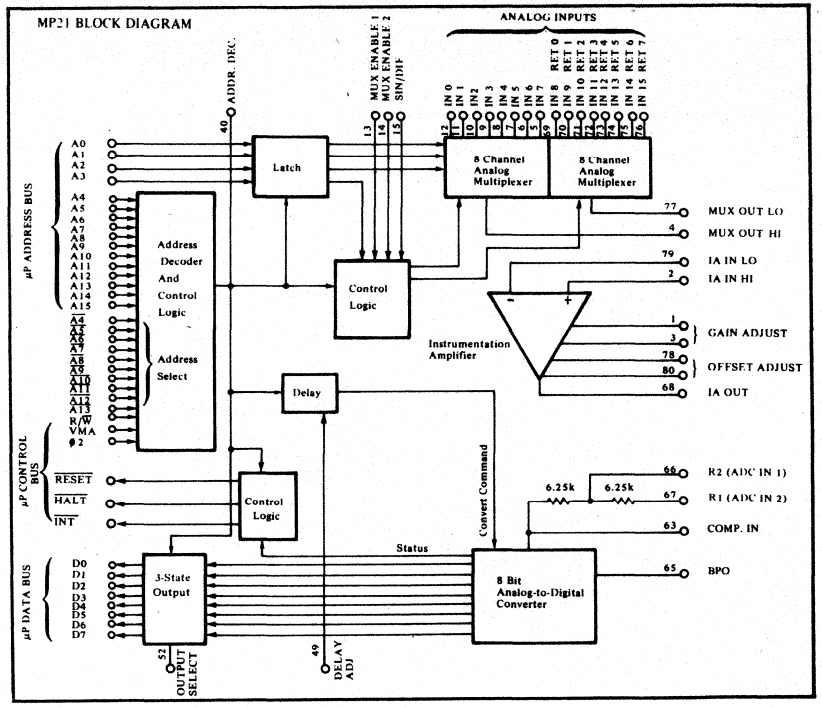
FIGURE 12. MP10 and MP20 Used With the Z-80

BURR-BROWN

MP21



8-BIT MICROPROCESSOR-INTERFACED ANALOG INPUT SYSTEM



FEATURES

- COMPATIBLE WITH:
  - 6800
  - 650X
  - F-8
- EASY TO PROGRAM
  - Choice of ways to interface:
    - Memory-mapped
    - Interrupt capability
- SAVES DEVELOPMENT TIME AND MONEY
- EASY TO USE
  - PIA is not needed
  - No external logic needed
  - No external adjustments
  - Low or high level analog inputs
  - Unlimited expansion
- COMPLETELY SELF-CONTAINED
- LOW COST

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PDS-375

Printed in U.S.A. July, 1978

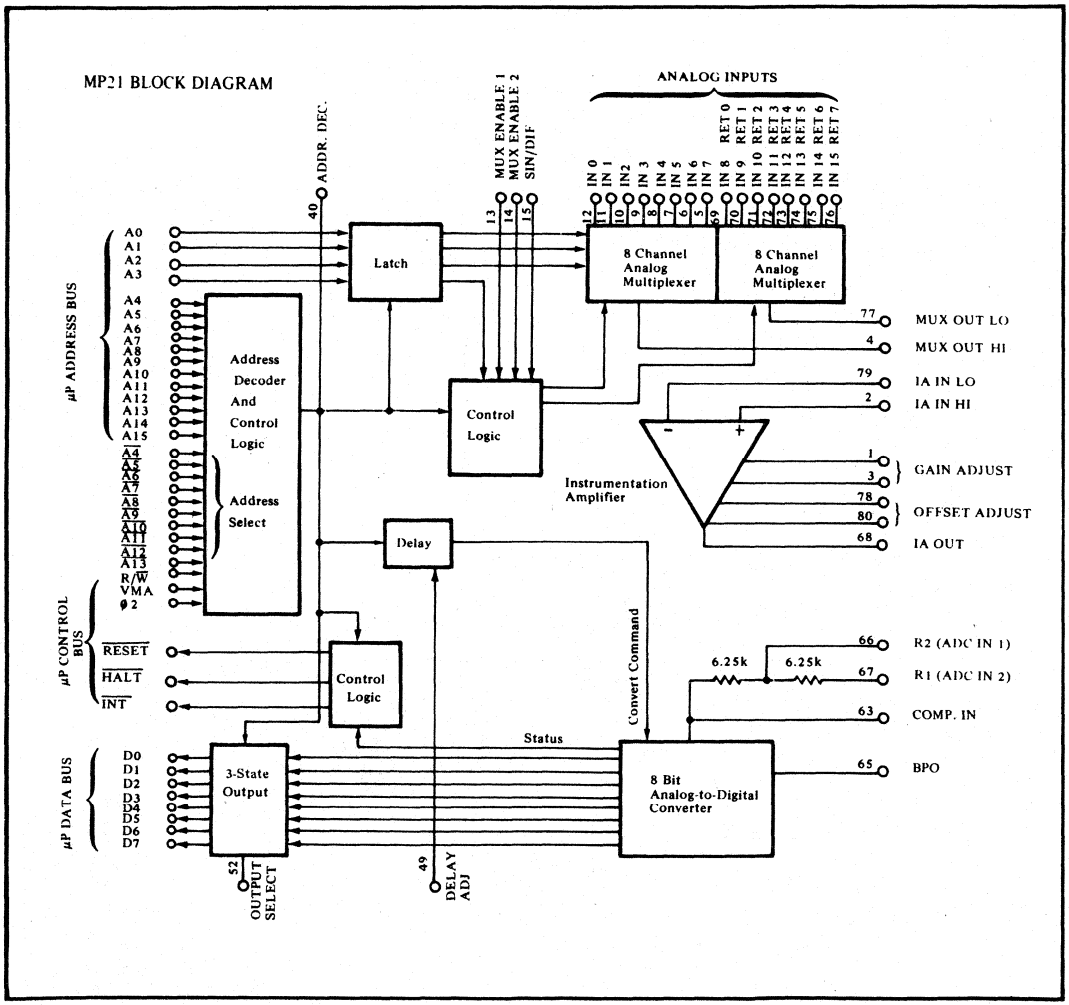
DESCRIPTION

The MP21 is a complete analog input system packaged in a 80-pin quad-in-line package. It is completely compatible with 6800 microprocessors. It is also compatible with the 650X and with the F-8. The MP21 contains a high speed 8-bit A/D converter, an instrumentation amplifier, an input multiplexer that can accept up to 16 single-ended signals or 8 differential signals as well as interface, timing and address decoding logic. The gain and offset are internally laser trimmed so that no external adjustments are required on the ±5V or 0 to +5V input range to obtain an absolute accuracy of better than ±0.4% (1 LSB). The system can digitize low level or high level analog signals. The gain of the internal instrumentation amplifier can be programmed with a single external resistor to allow input signal ranges as low as ±10 mV. This means that the MP21 can be connected to low level sensors such as thermocouples and strain gauges without external signal amplification.

All control lines are fully compatible with the microprocessor bus and operate at low power Schottky TTL levels. The MP21 input lines present one LS TTL load while all outputs can drive up to 20 LS TTL loads.

PROGRAMMING

When programming these peripherals, the user treats them as memory. Each analog input channel occupies one memory location. Any memory reference instruction can be used. Pins $\overline{A4}$ to $\overline{A13}$ are made available so that the microperipheral address can be hardwired for any of 1024 possible memory location bands. Since these units are treated as memory, a minimum of instructions are needed to read an input channel. The MP21's versatile memory mapped operation allows it to be used with or without halting the CPU or in the interrupt mode.



SPECIFICATIONS

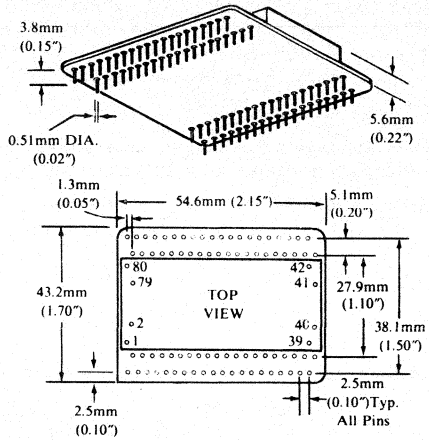
Typical at 25°C unless otherwise noted.

ELECTRICAL

TRANSFER CHARACTERISTICS	
Resolution	8 bits binary
Number of channels	16 single-ended/8 differential
Throughput rate[1] (max)	40μsec/channel
ANALOG INPUTS	
ADC gain ranges	0-5V, 0-10V, ±2.5V, ±5V, ±10V
Amplifier gain range	2 to 250
Amplifier gain equation	$G = 2 + 50k\Omega/R_{ext}$[2]
Max input voltage without damage[3]	±23 volts
Max input voltage for multiplexer operation	±6 volts
Input impedance	$5 \times 10^9\Omega$ || 10 pF - OFF channel $5 \times 10^9\Omega$ || 100 pF - ON channel
Bias current 25°C	100 nA
0 - 70°C	200 nA
Amplifier output noise	
Gain = 100, $R_S = 500\Omega$	400μV rms (10 Hz to 10 kHz)
Amplifier input offset voltage (max)	±1 mV
Amplifier offset voltage drift	±(6 + 50/G)μV/°C
Amplifier settling time (to .1% FSR)	
G = 2	20μs
G = 10	25μs
G = 50	50μs
G = 100	100μs
G = 200	200μs
CMRR (for differential inputs) (G = 2)	70 dB (DC to 60 Hz)
ACCURACY	
Throughput accuracy	
±5V, ±2.5V, ±1.25V range (max)[4]	±0.4% of FSR[5]
0-5V, 0-2.5V range (max)[4]	±0.4% of FSR
±50 mV range (max)[6]	±0.8% of FSR
0-50 mV range (max)[6]	±0.8% of FSR
Linearity (max)[4]	±0.2% of FSR
Differential linearity[4]	±0.2% of FSR
Quantizing error	±1/2 LSB
Gain error (max)[4]	±0.1%
Offset error (max)[4]	±0.1% of FSR
Power supply sensitivity	
±15V	$\pm 0.02\%/\%\Delta V_{CC}$
+5V	$\pm 0.002\%/\%\Delta V_{CC}$
STABILITY OVER TEMPERATURE	
System accuracy drift[7] (max)	±40 ppm/°C
Linearity (max)	±20 ppm/°C
Monotonicity (0°C to +70°C)	Guaranteed
DIGITAL INPUT/OUTPUT	
All signals are compatible with Microprocessor bus	
Output coding	Binary or Binary two's complement
Logic loading	All digital inputs are one LSTTL load
Output drive (D0 - D7)	5 TTL loads or 20 LSTTL loads
An analog input channel is selected by:	A0 - A3
The output data bus are read into:	D0 - D7
POWER REQUIREMENTS	
Rated voltages	±15V, +5V
Range for rated accuracy	4.75 to 5.25 and ±14.5 to ±15.5V
Supply drain ±15V	±30 mA
+5V	+90 mA
TEMPERATURE RANGE	0°C to +70°C

(1) Includes 35μsec for mux and amplifier time and 5μec for ADC conversion time.
(2) R_{ext} is an external resistor connected between pins 1 and 3.
(3) With power applied.
(4) With no external adjustments.
(5) FSR is Full Scale Range (FSR is 10V for ±5V range).
(6) Gain = 100 with external gain and offset trim.
(7) Includes gain drift, offset drift and linearity drift.

MECHANICAL



MATERIAL: Alumina
WEIGHT: 32 grams (1.2 oz.)
PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
MATING CONNECTOR: 2350MC (Set of four 20 pin strips)

PIN CONNECTIONS

Pin		Pin	
1	IA GAIN ADJUST	41	A14
2	IA IN HI	42	R/$\overline{W}$
3	IA GAIN ADJUST	43	A15
4	MUX OUT HI	44	$\overline{INT}$
5	IN 7	45	VMA
6	IN 6	46	ϕ2
7	IN 5	47	$\overline{RESET}$
8	IN 4	48	$\overline{HALT}$
9	IN 3	49	DELAY ADJ
10	IN 2	50	+5V
11	IN 1	51	DIG COM
12	IN 0	52	OUTPUT SELECT
13	MUX ENABLE 1	53	D7 (MSB)
14	MUX ENABLE 2	54	D6
15	SIN/DIF	55	D5
16	A0	56	D4
17	A1	57	D3
18	A2	58	D2
19	A3	59	D1
20	A4	60	D0 (LSB)
21	$\overline{A4}$	61	-15V
22	A5	62	+15V
23	$\overline{A5}$	63	COMP IN
24	A6	64	ANA. COM
25	$\overline{A6}$	65	BPO
26	A7	66	R2 (ADC IN 1)
27	$\overline{A7}$	67	R1 (ADC IN 2)
28	A8	68	IA OUT
29	$\overline{A8}$	69	IN 8 RET 0
30	A9	70	IN 9 RET 1
31	$\overline{A9}$	71	IN 10 RET 2
32	A10	72	IN 11 RET 3
33	$\overline{A10}$	73	IN 12 RET 4
34	A11	74	IN 13 RET 5
35	$\overline{A11}$	75	IN 14 RET 6
36	A12	76	IN 15 RET 7
37	$\overline{A12}$	77	MUX OUT LO
38	A13	78	OFFSET NULL
39	$\overline{A13}$	79	IA IN LO
40	ADDR DECODE OUT	80	OFFSET NULL

PIN FUNCTIONS

IA GAIN ADJUST (Optional). Pin 1 and Pin 3. By connecting a resistor between pin 1 and 3 the gain of the internal instrumentation amplifier can be set as follows:

$$\text{Gain} = 2 + 50k\Omega/R_{ext}$$

Where R_{ext} is the gain setting resistor. The IA is factory adjusted for a gain of 2 without any external resistor.

Important: If a gain greater than 10 is required an external capacitor must be connected from "DELAY" (pin 49) to +5V. This increases an internal delay to allow for the increased settling time of the instrumentation amplifier. (See page 5-122)

IA IN HI Pin 2. This is the positive input of the internal instrumentation amplifier. This should be connected to pin 4 (MUX OUT HI) for normal operation.

MUX OUT HI Pin 4. This is the output of the analog input multiplexer. This is connected to pin 2 (IA IN HI) for differential operation. It is connected to pin 77 (MUX OUT LO) and pin 2 for single-ended input operation.

IN7 - IN0 Pins 5 - 12. The first 8 (of 16) analog inputs for single-ended operation or the 8 positive inputs for 8 channel differential input operation.

MUX ENABLE 1 Pin 13. Leave open for single-ended input operation. Connect to pin 14 (MUX ENABLE 2) for differential input operation.

MUX ENABLE 2 Pin 14. Connect to pin 15 (SIN/DIF) for single-ended input operation. Connect to pin 13 (MUX ENABLE 1) for differential input operation.

SIN/DIF Pin 15. Single/Differential input operation connect to pin 14 (MUX ENABLE 2) for single-ended operation. Leave open for differential input operation.

A0 - A3 Pin 16 - 19. Address lines that select one of 16 analog input signals (IN0 - IN15). 0000 selects channel 0 and 1111 selects channel 15 when the correct address is presented to the MP21. Note: A3 should be connected to DIG COM for 8 channel differential input operation.

A4 - A15 Address lines. Pins 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 41, and 43. Connect to A4 - A15 of the 6800.

$\overline{A4}$ - $\overline{A13}$ Address select lines. Pin 21, 23, 25, 27, 29, 31, 33, 35, 37, and 39. By connecting these lines to DIG COM or +5 volts (through a 1kΩ resistor) any of 1024 address bands can be assigned to the MP21. For example, if $\overline{A4}$ is connected to GND., the correct (valid) address for A4 is a "1" (> + 2.4V).

ADDR DEC Pin 40. A positive pulse will appear when a valid address appears on the MP21 address lines and when R/$\overline{W}$ (pin 42), and ∅2 (pin 46) and VMA (pin 45) are high. The rising edge of this pulse strobes the input channel select information (A0 - A3) into a latch. It can also be used for external purposes.

R/$\overline{W}$ Pin 42. Read/Write control line. Connect to R/$\overline{W}$ of 6800.

$\overline{INT}$ Pin 44. Interrupt output. Connect to $\overline{IRQ}$ or $\overline{NMI}$ of the 6800 if interrupt operation is desired. When conversion has been completed, a 10μsec pulse (negative) is generated on this line. (Not an open collector output.)

VMA Pin 45. Connect to VMA on 6800.

∅2 Pin 46. Connect to ∅2 on 6800.

$\overline{RESET}$ Pin 47. A "Low" on this line is required to reset the MP21. Connect to the $\overline{RESET}$ input of the 6800.

$\overline{HALT}$ Pin 48. When the MP21 is "Read" by the microprocessor via any memory reference instruction the $\overline{HALT}$ line will go "Low" until conversion is complete. If the $\overline{HALT}$ line is used to halt the CPU, the 6800 will halt upon completion of the next instruction. When the multiplexer, instrument amp, and A/D converter have completed converting the analog data to a binary 8 bit code (40μsec with gain ≤ 10) the $\overline{HALT}$ line will then return to its "High" state which releases the processor. The output data can then be read with a second memory reference instruction. (Not an open collector output.)

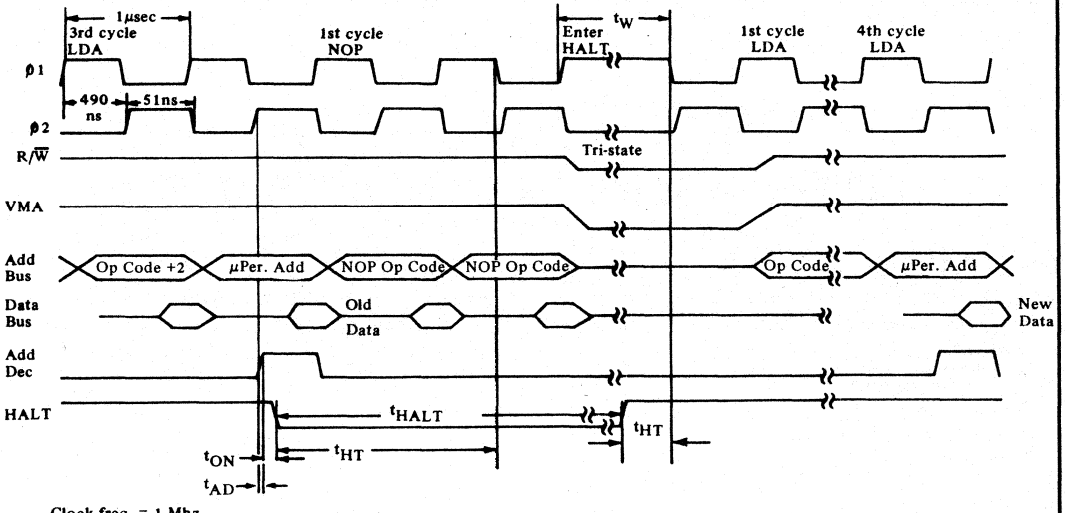
DELAY ADJ Pin 49. When the MP21 is addressed, an internal delay of approximately 35μsec is initiated to allow for multiplexer and instrumentation amplifier settling time. When the IA is operated with gain > 10 this delay must be increased (see Figure 4) to allow for the increased settling time of the IA. This is done by adding a capacitor between pin 49 and +5V. (See Figure 5)

+5V Pin 50. +5 volt at 140 mA maximum, 90 mA typical.

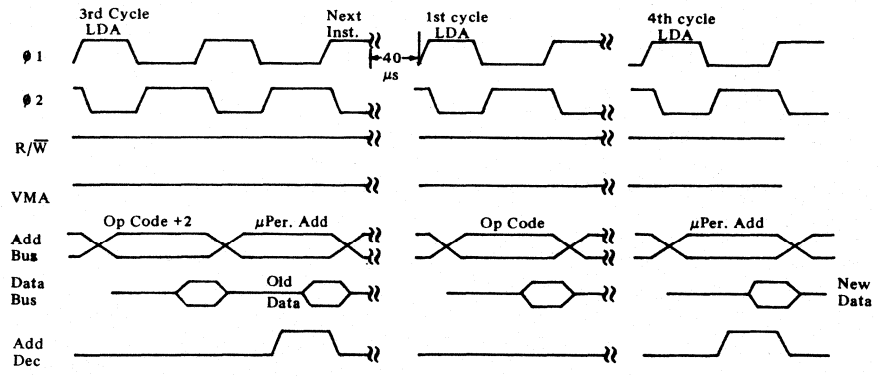
DIG COM Pin 51. Digital common. This pin should be connected to analog common (pin 64) as close to the MP21 as possible for optimum performance.

OUTPUT SELECT Pin 52. This pin should be connected to DIG COM to obtain binary data at D0 - D7. To obtain two's complement data (bipolar mode) connect pin 52 to +5V through a 1kΩ resistor.

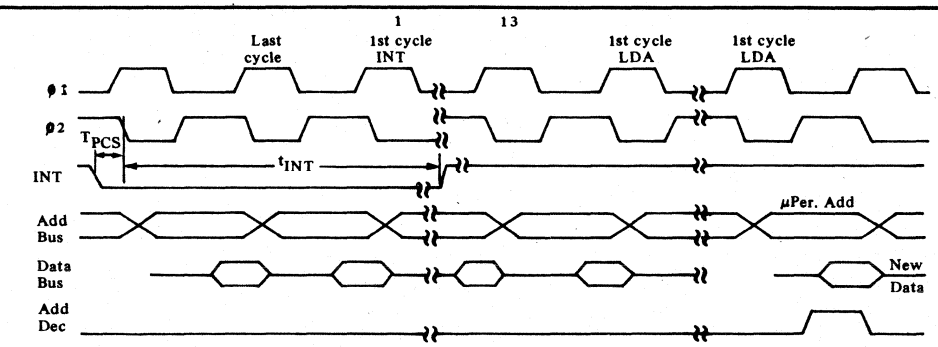
D7 - D0	Pin 53 - 60. 8 bit data bus. 3-state low power Schottky TTL compatible.
-15V	Pin 61. -15 volt at 30 mA typical.
+15V	Pin 62. +15 volt at 30 mA typical.
COMP IN	Pin 63. Comparator input of 8 bit A/D converter (successive-approximation). Leave open for unipolar operation or connect to "BPO" (pin 65) for bipolar operation. NOTE: This point is extremely sensitive to noise. Any connection to this line should be as short as possible and shielded by ANA COM or ±15 volt supply patterns.
ANA COM	Pin 64. Analog common should be connected to digital common (pin 51) as close to the MP21 as possible for optimum performance.
BPO	Pin 65. A/D converter bipolar offset. It should be connected to ANA COM (pin 64) for unipolar operation or COMP IN (pin 63) for bipolar operation.
R2	Pin 66. A/D converter input resistor. Connect to IA out (pin 68) for 0 to +5V input unipolar operation or ±2.5V input bipolar operation. Leave open for ±5V input bipolar operation.
R1	Pin 67. A/D converter input resistor. Connect to IA out for ±5 volt operation. Connect to Pin 63 for 0 to +2.5V and ±1.25V ranges.
IA OUT	Pin 68. Instrumentation amplifier output. Connect to R1 (pin 67) or R2 (pin 66) for normal operation.
IN8-IN15 RET0-RET7	Pin 69-76. Analog inputs 8 through 15 for single-ended operation or analog returns 0 through 7 for differential input operation.
MUX OUT LO	Pin 77. Multiplexer output for IN8-IN15 or RET0-RET7. Connect to "MUX OUT HI" (pin 4) and "IA IN HI" (pin 2) for single-ended input operation or connect to "IA IN LO" (pin 79) for differential input operation.
OFFSET NULL	Pin 78, 80. Optional instrumentation amplifier offset adjust (see Figure 1).
IA IN LO	Pin 79. Negative input of instrumentation amplifier. Connect to ANA COM (pin 64) for single-ended input operation or "MUX OUT LO" (pin 77) for differential input operation.



MP21 Timing Diagram (using HALT to stop microprocessor during conversion).



MP21 Timing Diagram (without stopping microprocessor during conversion).



t_{PCS} = 200ns min before falling edge of next to last φ2 clock pulse of instruction

t_{INT} = 12μsec (max)

MP21 Timing Diagram (using Interrupt).

OPERATING INSTRUCTIONS

PROGRAMMING

The MP21 is easily programmed since it is treated as memory. It uses any memory reference instruction that can read data.

The MP21 can be operated in four modes:

1) Start data conversion, halting the microprocessor for the 40μsec* conversion time. This is the simplest approach. It should be used if 40μsec of software time is available. (MP21's $\overline{\text{HALT}}$ line, pin 48, connected to the 6800's $\overline{\text{HALT}}$ input, pin 2.)

Example: LDA XXXX starts conversion of channel at location XXXX
NOP CPU halts at the end of this instruction
LDA XXXX transfers data from channel at location XXXX to accumulator

2) Start data conversion, then go to a different part of the program. When 40μsec* or more have passed, come back to the MP21 to read the converted data. This mode uses the least amount of time; it should be used when software time is at a minimum. (MP21's $\overline{\text{HALT}}$ line, pin 48, is open.)

Example: LDA XXXX starts conversion of the channel at location XXXX
•
•
• } at least 40μsec* of software here
LDA XXXX transfers data from channel at location XXXX to accumulator

* The conversion time of the MP21 may be between 40 and 200 microseconds depending upon the gain of the internal instrumentation amplifier. See Figure 4.

3) Start data conversion, then go to a different part of the program. Periodically, check the MP21's $\overline{\text{HALT}}$ line (pin 48) to detect if conversion is complete. This mode should

be used if a positive check of a complete conversion is needed. (MP21's $\overline{HALT}$ line, pin 48, could be interfaced to a 6820 PIA for instance.)

```
Example:  LDA $XXXX starts conversion of channel at
                    location XXXX
            •
            •       } other software
            •
          LDA $YYYY, loop to determine if conversion
                    is complete
AA ANDA $ZZ         YYYY is location of 6820 PIA
                    with HALT information
                    ZZ is mask used for determin-
                    ing if end of conversion bit
                    is set
          BEQ AA
          LDA $XXXX transfers data from channel at
                    location XXXX to accumulator
```

4) Start conversion, then go to a different part of the program. The MP21 will interrupt at the end of conversion. The interrupt mode is very useful when the MP21 is at high gains with conversion times longer than 40μsec, see Figure 4.(MP21's $\overline{INT}$ line, pin 44, connected to the 6800's $\overline{IRQ}$ line, pin 4.)

Example: MP21 used with a 6800. MP21 base address 92E0. Processor halted operation. Read and Print the value of all 16 input channels and then stop.

```
                        NAM   MP21
     E0BF    OUT2H      EQU   $E0BF
     F1D1    OUTEEE     EQU   $E1D1
     E1AC    INEEE      EQU   $E1AC
0100                    ORG   $100
0100 CE 92E0 START      LDX   #$92E0   Base address for MP21
0103 5F                 CLR B         Clear Counter
0104 A6 00   CONV       LDA A,X       Initiate Conversion
0106 01 01              NOP
0107 A6 00              LDA A, X      Read Data
0109 FF 0137            STX   STRE1   Store Index Reg.
010C F7 0139            STA B STRE2   Store Counter
010F B7 013B            STA A STRE3   Store Data
0112 CE 013B            LDX   #STRE3
0115 BD E0BF            JSR   OUT2H   Print Data
0118 86 0D              LDA A #$0D
011A BD E1D1            JSR   OUTEEE
011D 86 0A              LDA A #$0A
011F BD E1D1            JSR   OUTEEE
0122 F6 0139            LDA B STRE2
0125 FE 0137            LDX   STRE1
0128 5C                 INC B         Next Channel
0129 C1 10              CMP B #$10    Have 16 channels been
                                      read?
012B 27 04              BEQ   STOP    Yes
012D 08                 INX
012E 7E 0104            JMP   CONV    Do another conversion
0131 BD E1AC STOP       JSR   INEEE   Input character
                                      to begin again
0134 7E 0100            JMP   START
0137 0002    STRE1      RMB   2
0139 0001    STRE2      RMB   1
013A 0001    STRE3      RMB   1
                        END
```

This program assumes that the system is under the control of the MIK BUG monitor, Revision 9. To read and print the value of all 16 channels again, input any character from the keyboard.

ADDRESS SELECTION

The base address of the MP21 is set by inputs $\overline{A4}$ through $\overline{A13}$. Address lines A4 through A13 respond to the inverse of inputs $\overline{A4}$ through $\overline{A13}$. For instance, if $\overline{A6}$ is grounded, A6 will respond to a "High" input. A14 and A15 are internally connected to respond to a "High" input.

ANALOG INPUT RANGE SELECTION

The MP21 may be set for any range between ±5V and ±10 mV. Table I shows the pin connections for the various high level ranges available.

MP21 Input Range	Gain	ADC Range	Pin Connections
±5V	2	±10V	65 to 63; 66 open; 67 to 68
±2.5V	2	±5V	65 to 63; 66 to 68; 67 open
±1.25V	2	±2.5V	65 to 63; 66 to 68; 63 to 67
0 - 5V	2	0 - 10V	65 to 64; 66 to 68; 67 open
0 - 2.5V	2	0 - 5V	65 to 64; 66 to 68; 63 to 67

Table I. Analog Input Range Pin Connections

The MP21 may be set to output data with straight binary coding (pin 52 grounded) or two's complement coding (pin 52 to +5VDC through a 1kΩ resistor). Straight binary coding is typically used with unipolar input ranges and two's complement coding with bipolar input ranges. Table II describes the coding.

The internal instrumentation amplifier is factory set for a gain of 2. This gain can be increased to 250 by adding an external resistor (R_{ext}) between pins 1 and 3. R_{ext} should be a stable resistor (10 ppm/°C) since this temperature drift will add to the accuracy temperature coefficient. The gain of the amplifier can be determined by this formula: $\text{Gain} = 2 + \frac{50k\Omega}{R_{ext}}$. With pins 1 and 3 open, the gain is 2.

Since the amplifier input offset will be multiplied by the amplifier gain, an offset adjust may be required at high gains (see Figure 1b).

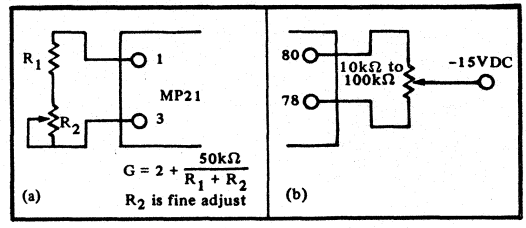


FIGURE 1. (a) MP21 Gain Adjust; (b) Offset Adjust

SINGLE-ENDED VS. DIFFERENTIAL INPUTS

The MP21 analog inputs may be connected as single-ended, differential or pseudo-differential. Single-ended operation may be used for high level (over one volt full scale) signals in low noise environments (Figure 3). Differential operation will reject common-mode noise appearing on both inputs (Figure 2). It should be used in noisy environments or with any low level signal (less than one volt). In the pseudo-differential mode, the MP21 is

	DIGITAL OUTPUT		ANALOG INPUT		
Straight Binary Code	Two's Complement Code		±5V	0 to +5V	±10mV
1111 1111 (FF_{16})	0111 1111 ($7F_{16}$)	+Full Scale	+4.961V	+4.980V	+9.92mV
1000 0000 (80_{16})	0000 0000 (00_{16})	Mid-Scale	0.000V	2.500V	0.000V
0000 0000 (00_{16})	1000 0000 (80_{16})	-Full Scale	-5.000V	0.000V	-10.00mV
		One LSB	39mV	19.5mV	78μV

TABLE II. Analog Input Values

connected as for the single-ended mode in Figure 3 except the IA low input, pin 79, is not grounded. Pin 79 is connected to an external ground that is common to all of the analog inputs. In cases with a noisy remote ground where little noise will be picked up between sensor and MP21, the pseudo-differential mode may be used.

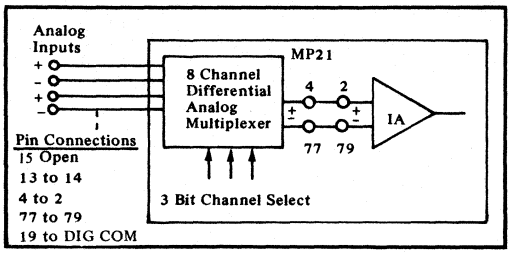


FIGURE 2. Differential Input Connections

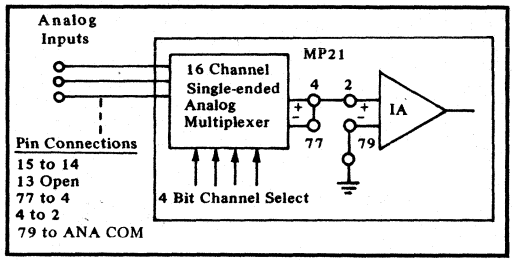


FIGURE 3. Single-ended Input Connections

DELAY TIMING

A delay time between channel selection and start of conversion is built into the MP21 to allow the analog multiplexer and instrumentation amplifier (IA) time to settle before starting the A/D converter. As the gain of the amplifier is increased, the settling time required increases. The factory set delay time (35μsec) is sufficient for gains of up to 10. At higher gains, a capacitor must be added from pin 49 to the +5 VDC supply to increase the delay time. Figure 4 shows the settling time of the MP21 vs. gain. Figure 5 shows the value of capacitance required to increase the delay.

The only external factor, other than gain, that affects the MP21 settling time is the impedance of the source connected to a channel. Figure 6 shows a circuit model of an "ON" channel.

The signal at the output of the multiplexer must be allowed to settle to ±0.1% (six time constants) to maintain the full accuracy of the system. The multiplexer time constant can be calculated with the formula: $\tau = (R_s + R_{on} + R_{on}^*)C_o$. For $R_s = 1k\Omega$ and $C_o = 50pF$, $\tau = (1.5 + 1)$ kΩ x 50pF = 125ns (single-ended operation). Thus 0.75μs is needed to settle to ±0.1%. For high input impedances requiring more than 10 microseconds for multiplexer settling time, the required delay time may be calculated with this formula: $T_D = \sqrt{T^2_{mux} + T^2_{IA}}$, where T_{mux} is the settling time of the multiplexer and T_{IA} is the settling time of the instrumentation amplifier as shown in Figure 4. If the source bandwidth can be limited, high impedance sources may be accurately handled by placing a large capacitance across the multiplexer input. An analysis of such a circuit shows that a capacitor of 0.5μF is sufficient. For such a capacitance the multiplexer time constant becomes 80ns.

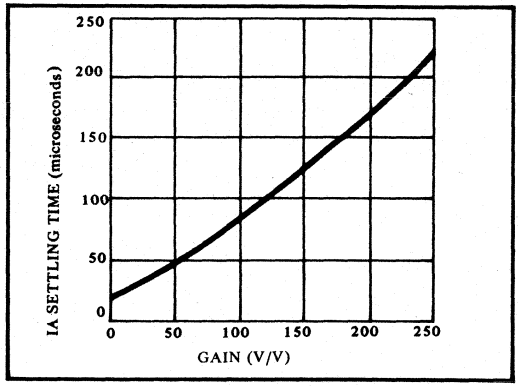


FIGURE 4. Typical IA Settling Time vs. Gain (Output Settling to ±0.1%).

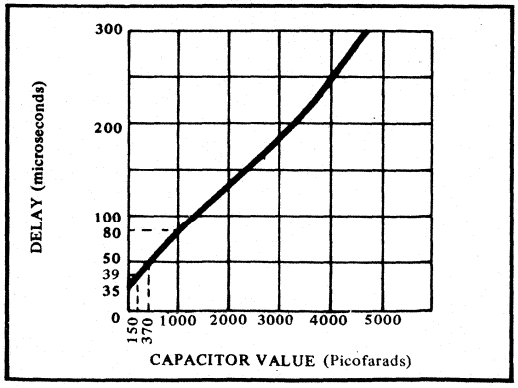


FIGURE 5. Typical Delay Time vs. Capacitor Value.

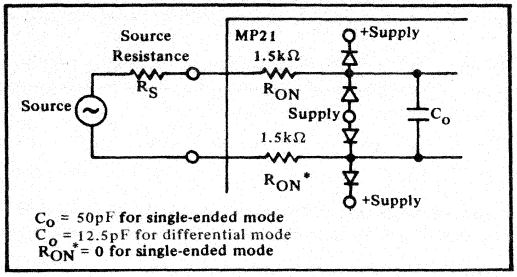


FIGURE 6. "ON" Channel Circuit Model.

INPUT OVERVOLTAGE PROTECTION

As shown in Figure 6, the analog inputs have reverse biased diode circuits which protect from damage by overvoltage (such as static). It is still advisable to take precautions against static discharge. The same circuitry protects the inputs from steady-state overvoltage damage during operation. The MP21's overvoltage protection can be increased by adding series resistors at each input. The input resistance must limit the current flowing through the input protection diodes to 10mA. For instance, if 15kΩ resistors are added to each input, the protection is increased to 165V (16.5kΩ x 10mA). Increased input resistance will, of course, increase the amount of time necessary for the multiplexer to settle as described in the previous section and increase the offset voltage by the drop caused when the bias current passes through this resistance.

NON 6800 OPERATION

The circuitry used to enable the 3-state output lines (D7 - D0) and begin conversion on the MP21 can be connected in such a way as to meet a wide variety of timing requirements. The output is enabled only when a valid address appears on the address inputs and when VMA (pin 45), R/$\overline{W}$ (pin 42), and ϕ2 (pin 46) are high. Any other combination of digital signals on these lines will result in D7 - D0 being in a high impedance state (see Figure 7).

All that is required to use the MP21 with a system other than a 6800, is that these signals be brought to their active levels. When this occurs, operation begins as previously described. Applications using the MP21 with other processors are shown in Figure 10 and 11.

RESET

It is important to reset the MP21 on startup with a low pulse on the $\overline{\text{RESET}}$ line (pin 47). The reset pulse clears an internal flip-flop and guarantees that the next read instruction to the unit will start a conversion. Thereafter, every other read instruction will initiate a conversion as previously described.

HIGHER SPEED OPERATION

The MP21's internal instrumentation amplifier requires 35 microseconds to allow for settling time. If this internal amplifier is not used, substantial improvements in throughput rate can be obtained. This is easily done since neither the inputs nor the output of the instrument amplifier are internally connected. For instance, Burr-Brown's 3622 high speed instrument amplifier (for differential inputs) or 3505J high speed op amp (for single-ended inputs) may be used, with a settling time of 1μsec for gains of up to 100. The total delay time necessary may be calculated by this formula:

$$T_D = \sqrt{T^2_{MUX} + T^2_{IA}},$$

where T_{MUX} is the settling time of the multiplexer (750ns) and T_{IA} is the settling time of the instrument amplifier. For a T_{IA} of 1μsec we have T_D = 1.3μsec. Using 3μsec for the delay time to allow for unit to unit variation, the total throughput time will be 8μsec (including 5 microseconds for ADC conversion time) or 125 kHz. A resistor between pin 49 and +5 VDC will reduce the delay time from the factory set value of 35 microseconds (see Figure 8).

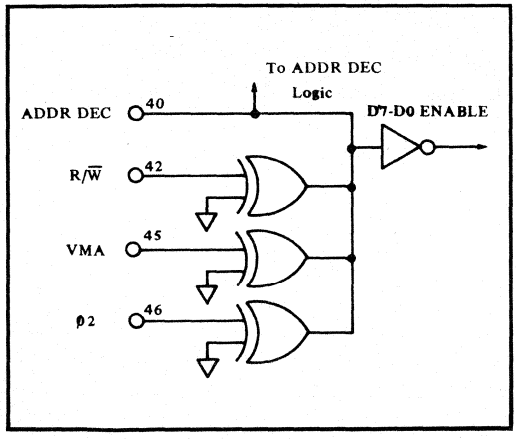


FIGURE 7. Output Enable Circuitry

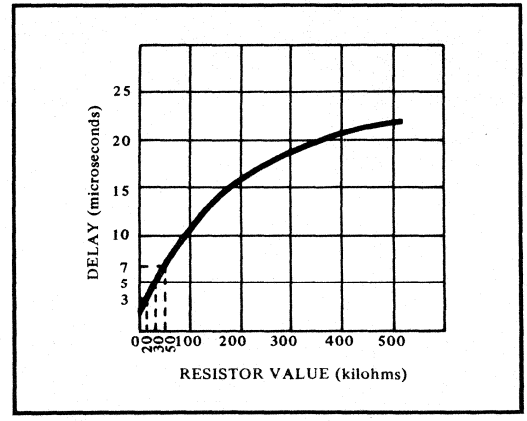


FIGURE 8. Typical Resistor Value to Decrease Delay Time.

CALIBRATION

The MP21 is laser trimmed at the factory to ±0.4% accuracy when using the ±5V, ±2.5V, ±1.25V, 0 to +2.5V or 0 to +5V ranges. If one of these ranges is used, no adjustments are required. For other ranges ($G \neq 2$), both the gain and offset must be adjusted. Figure 1 shows the adjustment connections. The offset adjustment should be made such that the transition to minus full scale output (0000 0001 to 0000 0000 for straight binary) occurs with an input of negative full scale plus 1/2 LSB. One least significant bit (LSB) is equal to the full scale range (FSR) divided by 2^n where n is the number of bits of the A/D converter. For the MP21, 1 LSB is $FSR/2^8 = FSR/256$. The gain adjustment should be made such that the transition to a full scale output (1111 1110 to 1111 1111 for straight binary) occurs with an input of positive full scale less 1/2 LSB. Since 128 states are used for negative inputs and one state is used for zero, only 127 states are available for the remaining positive range. Thus the positive full scale voltage is 1 LSB less than nominal full scale. For a range of ±50 mV, 1 LSB = 100 mV/256 = 0.39 mV. The gain adjustment should be made at +49.61mV* -(0.5)(0.39 mV) = +49.42 mV. The offset adjustment should be made at -50 mV + (0.5)(0.39mV) = -49.80 mV. Table III shows offset and gain calibration values for typical ranges.

* (50mV - 1 LSB = 49.61mV)

MP21 Input Range	Instrument Amp Gain	ADC Range	Calibration Values	
			Offset	Gain
±5V	2	±10V	-4.980V	+4.941V
0 to +5V	2	0 to +10V	+9.8mV	+4.971V
±2.5V	2	±5V	-2.490V	+2.471V
0 to +2.5V	2	0 to +5V	+4.9mV	+2.485V
±1.25V	2	±2.5V	-1.245V	+1.235
0 - 50mV	100	0 to +5V	+98μV	+49.7mV
±25mV	100	±2.5V	-24.9mV	+24.7mV
0 - 25mV	200	0 to +5V	+49μV	+24.9mV

Table III. Calibration Values.

The following program may be used to adjust gain and offset.

```
                        ORG  $100
START   0100    86      LDA A #$64
                64
        0102    B7      STA A COUNT
                01
                1A
        0105    4F      CLR A           Clear Accumulators.
        0106    5F      CLR B
CONV    0107    B6      LDA A $92 E0    Begin Conversion.
                92
                E0
        010A    01      NOP
        010B    B6      LDA A $92 E0    Read Data.
                92
                E0
        010E    81      CMP A #REF      I_S Data = REF?
                REF
        0110    26      BNE AA          No. Do not count.
                01
        0112    5C      INC B           Yes. Do count.
AA      0113    7A      DEC COUNT       Have 100 conversions
                                        been done.
                01
                1A
        0116    26      BNE CONV        No. Do another.
                EF
        0118    20      BRA START       Yes. Begin next run.
                E6
COUNT   011A            RMB  1
                        END
```

This program assumes that the program is under control of the Motorola EXORciser EXbug monitor. If the Mikbug monitor is available, the following printout software may be added by using it to replace all codes starting from location 0118. In addition the references to count at 0104 and 0115 must be replaced with 2E.

```
OUT 2H  EQU  $E0   BF
OUT EEE EQU  $E1   D1

0118 F7    STA  B  STR0
     01
     2E
011B    CE    LDX  #STR0
        01
        2E
011E    BD    JSR  OUT 2H  Print no. of true conversions.
        E0
        BF
0121    86    LDA A  #0D
        0D
0123    BD    JSR  OUTEEE
        E1
        D1
012E          RMB  1          COUNT
012F          RMB  1          STR0
              END
```

This program may be used for both offset and gain calibration. The system offset should be adjusted first, followed by the gain adjustment.

The address of channel zero is assumed to be 92EO. If it is not, the LDA instructions should reflect that change. The reference values for Ref assume straight binary coding, Offset Ref = 00 and Gain Full Scale Ref = FF. For two's complement binary coding, Offset Ref = 80 and Gain Full Scale Ref = 7F.

A 100;G command to Exbug will begin program execution. For Mikbug the user's stack must be loaded with 1ØØ and then a G command executed to begin program execution. For those applications not using the printer portion of the program insert a breakpoint via a 118;V command. After 100 conversions have been made, the value (in hex) of the B accumulator will be printed if using Mikbug program. This value represents the number of times the data read from the board was equal to "REF" (00 for offset; FF for gain).

Calibration is performed by connecting a voltage source capable of 0.01% accuracy to input channel zero (this could also be a DC voltage source of less absolute accuracy whose output is monitored by a 0.01% DVM).

The offset adjustment is made first by using the appropriate offset calibration voltage and REF value. Run the calibration program and adjust the offset potentiometer until the B register contains a value between $1E_{16}$ and 46_{16} (30_{10} and 70_{10}).

To perform the gain adjustment, change the data labeled "REF" in the calibration program to its correct gain value. Set the input voltage to the correct value as shown in Figure 8 and adjust the gain potentiometer in the same manner as described for offset.

If EXbug is used the program will halt and the B accumulator can be examined from the program register display produced by the breakpoint.

THERMOCOUPLE TEMPERATURE ACQUISITION

Thermocouples are often used as temperature sensors for process control systems. Thermocouples are characterized by temperature coefficients of 10 to 70μV/°C and operating ranges of minus hundreds to plus thousands of degrees centrigrade. When the MP21 is operated with an instrumentation amplifier gain of 100 or more, it may be connected directly to these devices. The wire runs from thermocouple to measuring device often pick up large common-mode noise signals of 60 Hz or higher frequencies. When the MP21 is used as an eight channel differential input system, the high common-mode rejection of the instrument amplifier will reject common-mode noise. To minimize differential mode noise, the signal wire should be twisted and if possible shielded. As a rule, an unshielded twisted pair is better than a coax, and a shielded, twisted pair is still better. In applications where these wiring practices cannot always be observed, a differential RC filter may be used. Figure 9 shows such a system.

The 10 kΩ resistors and 10μF capacitor provide low pass filtering (f_c = 0.8 Hz) while the optional 1 MΩ resistors supply bias current to the instrumentation amplifier. The remote sensor should be earth grounded to prevent common-mode voltages from exceeding the ±5 volt range of the multiplexer. If the sensor is earth grounded, the 1MΩ resistors are not required. The 1 MΩ resistors do not enter into an error calculation for input errors because the low resistance of the sensor shorts any differential voltage that might be caused by the offset (difference current) of the amplifier. Offset or difference current is merely the difference between the bias current of each input. See the overvoltage protection section for a discussion of the effects of the 10kΩ resistors in the input filter. The 1MΩ resistors could have been put on the output side of the multiplexer eliminating the need for repeating them for each input; however, this would have loaded the 10kΩ resistors of the filter causing a possible 1% error for static conditions.

To complete a thermocouple system it is necessary to terminate all thermocouple wire pairs at an isothermal box or connector strip of some type. An ordinary barrier strip may be monitored to allow the observed thermocouple emf to be cold junction compensated. Figure 9 shows an excellent circuit for this purpose. Its output is connected to one of the input channels to supply ambient temperature data to the system computer. Its output sensitivity is approximately 2 mV/°C.

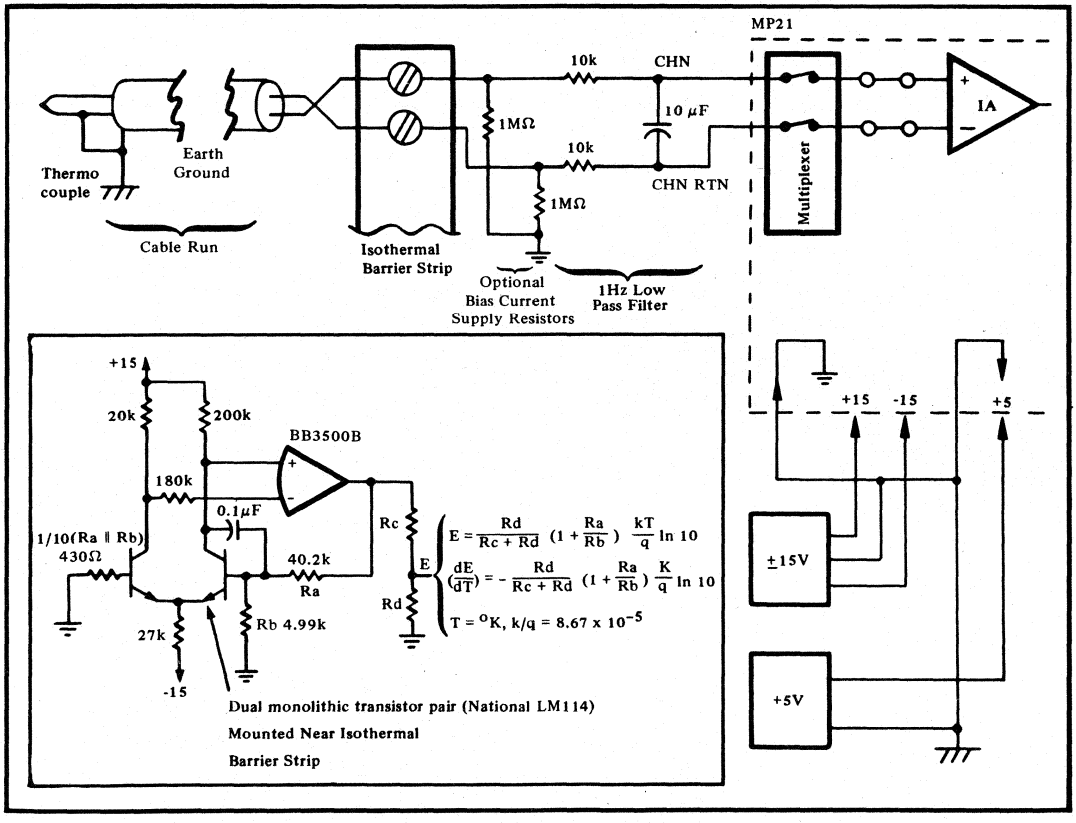


FIGURE 9. Thermocouple Input System Using MP21.

PIN CONNECTION SUMMARY

	JUMPER		JUMPER
Single-ended Multiplexer	4 to 2; 4 to 77; 79 to 64; 15 to 14; 13 open	Address Bus (A0 - A15)	Connect to 6800's address bus A0 - A15
Differential Multiplexer	4 to 2; 77 to 79; 13 to 14; 15 open	Address Select ($\overline{A4}$ - $\overline{A13}$)	Connect to +5V* or Ground
Amplifier	1 and 3 open for G = 2; R_{ext} between 1 and 3 for G ≠ 2.	Control Bus	42 to 6800's R/$\overline{W}$ (pin 39) 44 optionally to 6800's IRQ (pin 4) 45 to 6800's VMA (pin 5) 46 to 6800's Ø2 (pin 37) 47 to 6800's $\overline{RESET}$ (pin 40) 48 to 6800's $\overline{HALT}$ (pin 2) open for operation without halting CPU.
Input Range ±5V ±2.5V ±1.25V 0 - 5V 0 - 2.5V	 65 to 63; 66 open; 67 to 68 66 to 63; 66 to 68; 67 open 65 to 63; 66 to 68; 63 to 67 65 to 64; 66 to 68; 67 open 65 to 64; 66 to 68; 63 to 67		
Output Coding	52 to 51 for binary; 52 to 50* for two's complement.	Data Bus (D0 - D7)	Connect to 6800's data bus.
* Through a 1kΩ resistor.			

MICROPROCESSOR INTERCONNECTION

The following diagrams show interconnections of the MP21 (described in this data sheet) and also of Burr-Brown's MP10 and MP11 analog output microperipherals (PDS-363) with Motorola's 6800, MOS Technology's 650X, and Fairchild's F-8. Although Burr-Brown's analog microperipherals are optimized for 8 bit microprocessors, with the addition of a few external components, they can be used with any 4 through 16 bit microprocessors.

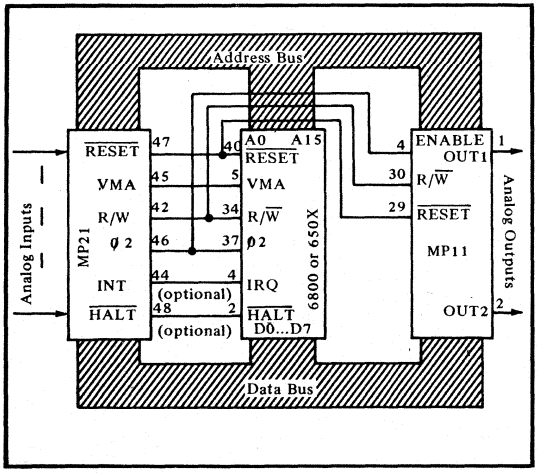


FIGURE 10. MP21 and MP11 Used With the 6800 or 650X.

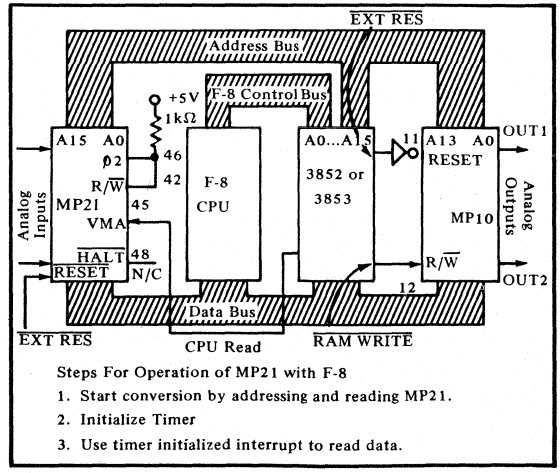
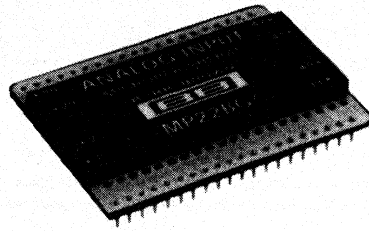


FIGURE 11. MP21 and MP10 Used With the F-8.

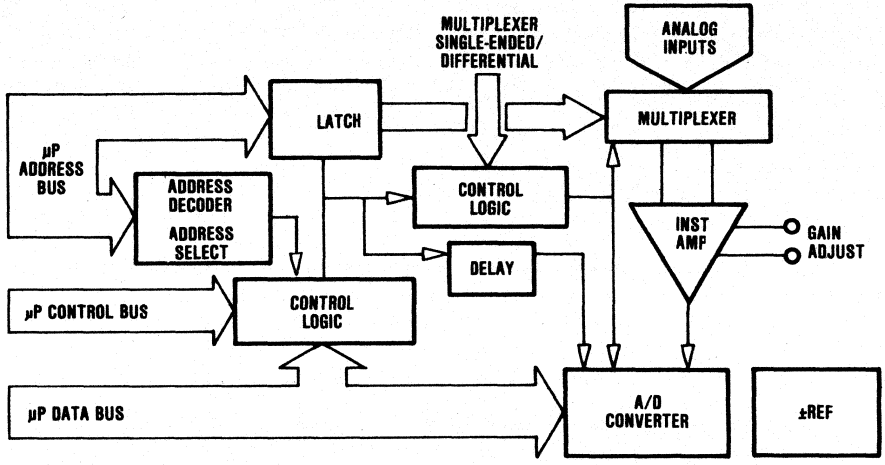
BURR-BROWN



MP22BG

ADVANCE INFORMATION
Subject to Change

12 Bit Microprocessor - Interfaced DATA ACQUISITION SYSTEM



FEATURES

- **INTERFACES WITH 8080A, 8048, Z-80, SC/MP MICROPROCESSORS WITHOUT ADDITIONAL COMPONENTS**
- **INTERFACES WITH 6800, 650X, F8, 8085 MICROPROCESSORS WITH MINIMAL EXTERNAL LOGIC**
- **EASY TO PROGRAM**
  One instruction acquires data as a memory mapped device
  Two instructions acquire data as an accumulator I/O device
- **COMPATIBLE WITH PDP-8, PDP-11, NOVA, ECLIPSE MINICOMPUTERS**

DESCRIPTION

A complete analog input system, the MP22 interfaces to most microprocessors without requiring additional external components. Contained in an 80-pin quad-in-line package, it includes a 12-bit CMOS A/D converter, instrumentation amplifier, input multiplexer that accepts up to 16 single-ended signals or 8 differential signals, an address decoder and control logic. Logic to generate interrupt, halt and direct memory access request signals are also included.

The system can digitize low level or high level analog signals. Gain of the internal instrumentation amplifier can be programmed with a single external resistor allowing input ranges as low as ±5mV/.

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PDS-387A

Printed in U.S.A. July, 1978

ANALOG MULTIPLEXERS

Two 8-channel CMOS analog multiplexers are used on the input which permits selection of 16 single-ended or 8 differential inputs. A pseudo 16 channel differential mode of operation can also be achieved by connecting the amplifier's inverting input to a common, remote signal ground. Channels are addressed by the address decoder which is connected directly to the microprocessor address bus. The number of input channels can be expanded without limit using external multiplexers.

INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is a low drift, differential amplifier featuring high speed at gains above unity and gain programming with an external resistor. Gain may be selected from unity to 54dB.

ANALOG-TO-DIGITAL CONVERTER

The 12-bit A/D converter is a CMOS, successive approximation device with 45μsec conversion time and three-state outputs. Laser-trimmed, compatible thin-film networks are used to assure linearity and stability over wide temperature ranges.

ADDRESS DECODER

Typical microprocessor systems have several thousand memory locations, teletype or CRT terminals, and possibly several MP22s. By using 12 address lines the microprocessor can communicate with as many as 2^{12} or 4096 memory locations or peripheral devices, with each having its own unique address.

The MP22's address decoder is made up of exclusive-or gates which have open collector outputs so that the outputs of several gates may be connected together through a single pull-up resistor. The address of the MP22 is determined by wiring the address select lines to either ground or +5 volts. Only when all of the address lines (A inputs) are in opposite states of their respective address select lines ($\overline{A}$ inputs) will the address decoder output go high.

DELAY TIMER

A time delay between channel selection and start of conversion is built into the MP22. This allows the analog multiplexer and the instrumentation amplifier time to settle before starting the A/D converter. As amplifier gain increases, settling time increases. See Figure 8. Factory set delay time (15μsec) is sufficient for gains from unity to 50. At higher gains a capacitor must be added between pins 49 and 50 to increase delay. Figure 7 indicates the capacitance required to increase delay time.

CONTROL LOGIC

The control logic generates signals to halt or interrupt the CPU while conversion takes place and to signal the CPU when conversion is complete and data can be read. Enable signals are also generated to gate the data onto the data bus.

REFERENCE

The internal voltage reference of the MP22 has been optimized for stable outputs with respect to temperature. Output current up to 2mA can be drawn externally from the reference outputs.

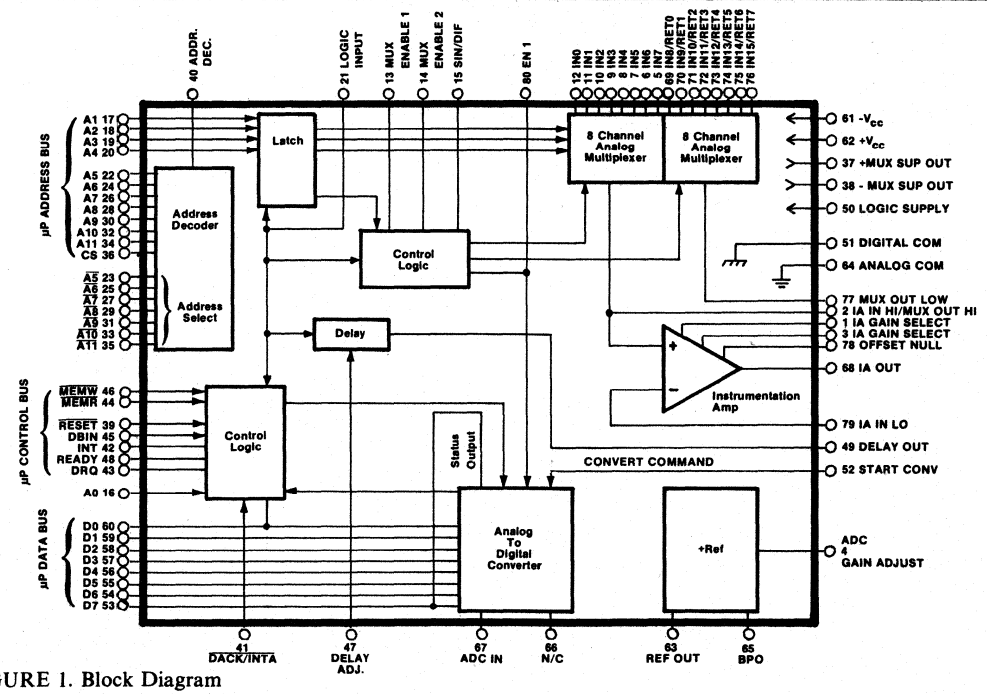
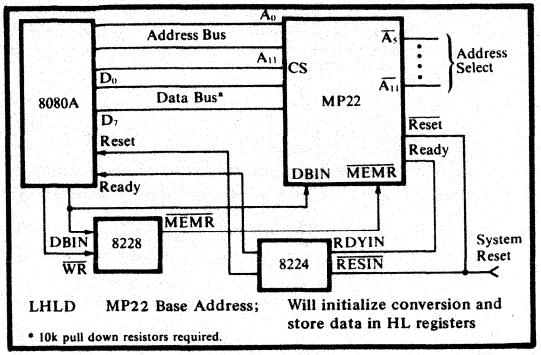


FIGURE 1. Block Diagram

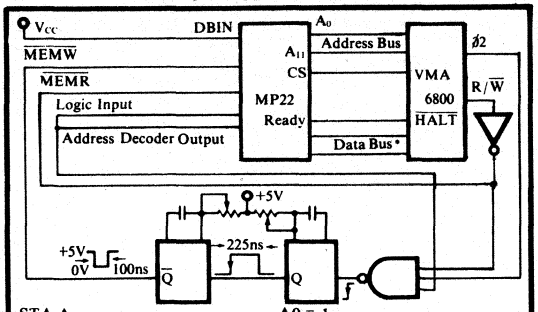
MICROPROCESSOR CONNECTION DIAGRAMS



LHLD MP22 Base Address; Will initialize conversion and store data in HL registers

* 10k pull down resistors required.

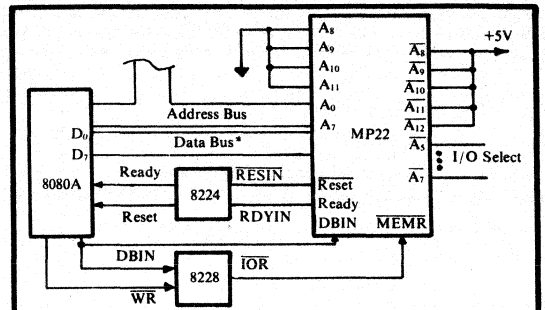
FIGURE 2. MP22 Used with 8080 Halt Mode Memory Mapped



STA A	A0 = 1	
Destination Address	D0 = 0	Starts conversion
NOP		Halt
LDA		
Destination Address	A0 = 0	8 LSB's, Resets MP22
LDA		
Destination Address	A0 = 1	4 MSB's

* 10k pull down resistors required.

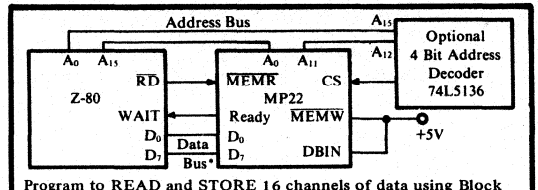
FIGURE 3. MP22 Used with 6800



IN	MP22 Base Address;	$A_0 = 0$ A_1 - A_4 channel select A_5 - A_7 I/O select initializes conversion and reads 8 LSB's
MOV C, A		Store 8 LSB's in REG C
IN	MP22 Base Address;	$A_0 = 1$ A_5 - A_7 I/O select reads 4 MSB's

* 10k pull down resistors required.

FIGURE 4. MP22 Used with 8080 Halt Mode Accumulator I/O



Program to READ and STORE 16 channels of data using Block Transfer Instruction.

LD HL, NN	NN points to channel 0 MP22
LD DE, MM	MM points to the first location of the destination
LD BC, 0100_H	byte counter (2 bytes/channel x 16) = 32_{10}
LDI	Load and increment

Total Execution Time with tcy = .4μs and conversion rate 40μs is T = 3 (4μs) + 16 (6.4 + 40μs) = 754.4μs.

* 10k pull down resistors required.

FIGURE 5. MP22 Used with Z-80 (Halt Mode)

DELAY TIME COMPONENT SELECTION CURVES

FIGURE 6. Typical Resistor Value to Decrease Delay Time

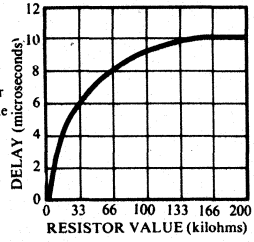
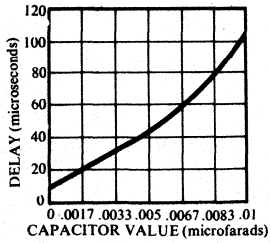


FIGURE 7. Typical Delay Time vs Capacitor Value



TYPICAL PERFORMANCE CURVES

FIGURE 8. Differential Amplifier Settling Time vs Gain

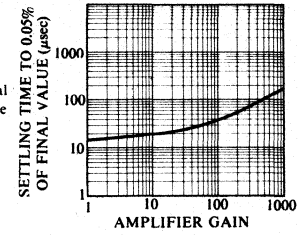
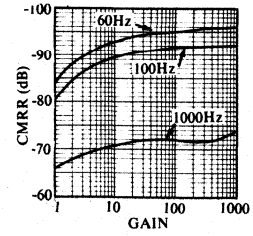


FIGURE 9. Differential Amplifier Common-mode Rejection vs Gain



μC I/O MP22BG

ELECTRICAL SPECIFICATIONS

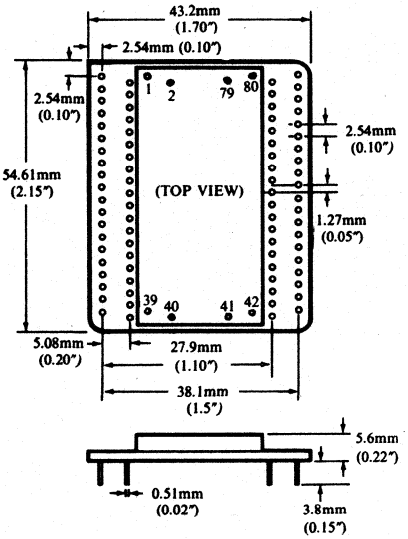
Typical at +25°C and rated supplies unless otherwise noted.

MODEL	MP22BG Min	MP22BG Typ	MP22BG Max	Units
TRANSFER CHARACTERISTICS				
Resolution[1]	12	12	12	Bits
Number of Channels		16 Single-Ended/8 Differential		
Throughput Rate[1] at G = 1	40	45	55	μs/Channel
ANALOG INPUTS				
ADC Gain Ranges				
Bipolar[3]		±5		Volts
Unipolar[1]		0-5		Volts
Amplifier Gain Range		1 to 500		
Gain Equation		$\left(1+\frac{25k\Omega}{R_{EXT}}\right)$		
Input Voltage Without Damage			±16	Volts
Input Voltage for Multiplexer Operation			±6.0	Volts
Input Impedance				
Off Channel		$5 \times 10^9\Omega \parallel 10pF$		
On Channel		$5 \times 10^9\Omega \parallel 100pF$		
Bias Current				
25°C			300	nA
0°C to +70°C			400	nA
Amplifier Output Noise G = 100, R_S = 150Ω		1.2		mV, rms
		7.0		mV, p-p
Amplifier Input Offset		±0.5	±7.0	mV
Amplifier Offset Drift (R_{max} = 1.5k)		±(7 + 90/G)	±(26 +190/G)	μV/°C
Amplifier Gain Drift, (R_{EXT} ≤10 ppm/°C)				
G = 1			10	ppm/°C
G = 10			110	ppm/°C
G = 100			120	ppm/°C
G = 1000			120	ppm/°C
Amplifier Settling Time to ±0.05% of FSR				
G = 1[1]			15	μs
G = 10		20		μs
G = 100		25		μs
G = 500		100		μs
CMRR for Differential Inputs Dc to 60Hz	74	84		dB
ACCURACY				
System RSS Accuracy[2] at 25kHz Throughput				
G = 1			±0.1	% FSR
Linearity			±0.05	% FSR
Differential Linearity		±0.05		% FSR
Gain Error		Adjustable to Zero		
Offset Error		Adjustable to Zero		
System RSS Accuracy at Gain = 500 and 1kHz Throughput			±0.39	% FSR
ADC Accuracy Drift				
Linearity			±3	ppm/°C
Gain			±10	ppm/°C
Reference Drift				
Ref Out (Pin 63)			±15	ppm/°C
BPO (Pin 65)			±25	ppm/°C
System Accuracy Drift (Excluding I.A.)				
Unipolar			±25	ppm/°C
Bipolar			±60	ppm/°C
Monotonicity (-25 to +85°C)		Guaranteed		
No Missing Codes (-25 to +85°C) (10 bits only)		Guaranteed		
Power Supply Sensitivity (Excluding I.A.)				
$\pm V_{CC}$			±0.008	% FSR/%ΔV
Logic Supply			±0.0002	% FSR/%ΔV
Instrumentation amplifier				
Power Supply Sensitivity			$(1+2/G)10^{-4}$	% FSR/%ΔV

MODEL	MP22BG Min	MP22BG Typ	MP22BG Max	Units
DIGITAL INPUT/OUTPUT				
Bipolar Code		Bipolar Offset Binary		
Unipolar Code		Unipolar Straight Binary		
Logic Loading Pin (21)			3LSTTL	
Pin (60)			2LSTTL	
Output Drive	1 TTL Load			
Analog Input Channels Selected By:		A1-A4		
Output Data:		D0-D7		
POWER REQUIREMENTS				
Rated Voltages[1]		±15, +5		Volts
Range for Rated Accuracy (Logic Supply, $\pm V_{cc}$)		4.75 to 5.25 and ±11.4 to ±15.75		Volts
$\pm V_{cc}$ Operating Range	±10		±18	Volts
Supply Drain				
$+V_{cc}$		10	20	mA
$-V_{cc}$		15	20	mA
Logic Supply		80	160	mA
Power Dissipation ($\pm V_{CC}$ = ±12V)		700	1300	MW
TEMPERATURE RANGE				
Specification	-25		+85	°C
Operating	-40		+100	°C
Storage	-55		+125	°C

NOTES: 1. These parameters are 100% tested.
2. Gain and offset adjusted to zero.
3. External amplifier required.

MECHANICAL



MATERIAL: Alumina
WEIGHT: 32 grams (1.2 oz.)
PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
MATING CONNECTOR: 2350MC (Set of four 20 pin strips)
HERMETICITY: Conforms to Method 1014 Condition C, Step 1 (fluorocarbon) of Mil-Std-883 (Gross Leak)

PIN CONNECTIONS

Pin 1	IA GAIN SELECT	Pin 41	$\overline{\text{DACK/INTA}}$
2	IA IN HI/MUX OUT HIGH	42	INT
3	IA GAIN SELECT	43	DRQ
4	ADC GAIN ADJUST	44	$\overline{\text{MEMR}}$
5	IN7	45	$\overline{\text{DBIN}}$
6	IN6	46	$\overline{\text{MEMW}}$
7	IN5	47	DELAY ADJ.
8	IN4	48	READY
9	IN3	49	DELAY OUTPUT
10	IN2	50	+5V LOGIC SUPPLY
11	IN1	51	DIG. COMMON
12	IN0	52	START CONV.
13	MUX ENABLE 1	53	D7 (MSB)
14	MUX ENABLE 2	54	D6
15	SIN/DIF	55	D5
16	A0	56	D4
17	A1	57	D3
18	A2	58	D2
19	A3	59	D1
20	A4	60	D0 (LSB)
21	LOGIC INPUT	61	-Vcc
22	A5	62	+Vcc
23	$\overline{\text{A5}}$	63	REF OUT
24	A6	64	ANA. COMMON
25	$\overline{\text{A6}}$	65	BPO
26	A7	66	NO CONNECTION
27	$\overline{\text{A7}}$	67	ADC IN
28	A8	68	IA OUT
29	$\overline{\text{A8}}$	69	IN8 RET0
30	A9	70	IN9 RET1
31	$\overline{\text{A9}}$	71	IN10 RET2
32	A10	72	IN11 RET3
33	$\overline{\text{A10}}$	73	IN12 RET4
34	A11	74	IN13 RET5
35	$\overline{\text{A11}}$	75	IN14 RET6
36	CHIP SELECT (CS)	76	IN15 RET7
37	+MUX SUPPLY OUTPUT	77	MUX OUT LOW
38	-MUX SUPPLY OUTPUT	78	OFFSET NULL
39	$\overline{\text{RESET}}$	79	IA IN LO
40	ADDR DECODE	80	EN1

OPERATING INSTRUCTIONS

The MP22 is designed to be used as a memory-mapped or an accumulator I/O. Since there are many powerful memory reference instructions, the MP22 is used most efficiently as a memory-mapped device. Pins $\overline{A5}$ through $\overline{A11}$ are provided so that the microperipheral can be hardwired for any base address within a 4096 word block of the memory field. The address decoder output is available and can be easily expanded to 16 bits.

If used as a memory-mapped microperipheral, the MP22 can provide three modes of operation: HALT Mode, INTERRUPT Mode and DMA Mode.

More detailed application instructions are given in the operating manual, available upon request.

HALT MODE

After power up (or manual) reset, the MP22 is automatically set for operation in the HALT Mode. This mode requires minimum software to acquire data. To use the MP22 in the HALT Mode connect the MP22 READY line to the 8080 READY input (see Figure 2). When a memory reference instruction such as LHLD is executed, the READY line goes low, halting the CPU for the duration of the data conversion (45 μsec, gain = 1). When the conversion is complete the READY line goes high, signaling the CPU exit the wait state and enter the T_3 state to read the 8 LSB's. After reading the 8 LSB's, the CPU increments the memory address register and reads the 4 MSB's. When the most significant data byte has been read, the internal logic resets and the MP22 is ready for the next conversion.

Example:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
X	X	X	1	1	1	1	1	0	1	1	1	0	0	1	0

MP22 Base Address — Channel Select

MP22 used with 8080; read MP22 base address: $1F72_H$ channel 10.
LHLD $1F72_H$ acquires and transfers data to CPU from channel 10.
The 8 LSB's (at location $1F72_H$) are transferred to register L and the 4 MSB's (at location $1F73_H$) are transferred to register H.
Total time: 16 tcy + 40μsec = 47.8μsec (for tcy = 488 nsec [8080A]).

INTERRUPT MODE

To use the MP22 in the INTERRUPT Mode connect the INT and $\overline{DACK}$/$\overline{INTA}$ lines to the 8080's INT input and INTA output respectively. Conversion is initiated by writing D0 = 0 into the MP22. When the conversion is complete the MP22 generates an INT signal which will remain low until INTA is received from the 8080.

Example: MP22 base address $1F72_H$.

```
MVIA   00H
                        START conversion
STA    1F72H
 .
 .                      Continue with program. INT will
 .                      arrive 40 μsec after start of conversion.
INCA
                        INT arrives here
CPIA                    User will jam RST instruction which
                        will provide address of an interrupt hand-
                        ling routine and store program counter.
INTERRUPT Subroutine:
        PUSH PSW        Store Acc. and Flags
        PUSH H  }
        PUSH D  }       Store reg. if necessary
        PUSH B  }
        EI              Enable interrupt
        LHLD 1F72H      READ DATA from MP22
                        Channel 10 L = 8 LSB's
                                   H = 4 MSB's
                        Process data
        POP B   }
        POP D   }       Restore registers and flags
        POP H   }
        POP PSW         Restore program counter
        RET
```

The user must supply an instruction op code to the processor during the next DBIN time after the $\overline{INTA}$ status appears. This is usually done through use of an RST instruction.

DIRECT MEMORY ACCESS MODE

To use the MP22 in the DMA Mode connect the MP22 to the DMA controller. The controller is initialized by the CPU before reading data from the MP22. To accomplish a block move the CPU loads the 8257 with the starting address of the source block (the MP22 location) with A0 = 0 and the length of the block (L = 1) into channel 0. Channel 1 is programmed with the starting location of the destination block and the length (L = 1).

Next, start conversion by writing D0 = 0 into the MP22. When the conversion is complete, the MP22 will generate a DRQ request on channels 0 and 1. The 8257 is initialized to the rotating priority mode, therefore the first DMA cycle is from channel 0 which latches data from the first location of the source block into the 8212. The second cycle will be from channel 1 which will store the latched data in the first location of the destination block. The next cycle will return to channel 0 and the sequence will start over again until the terminal count is reached. When the terminal count for channel 1 is reached, $\overline{\text{DACK1}}$ and TC signals are generated and MP22 DRQ line is reset.

ANALOG INPUT RANGE SELECTION

The MP22 may be set for any range between ±5V and ±10mV. Pin connections for the high level ranges available are shown in Table I.

MP22 Input Range	Gain	ADC Range	Pin Connections
±5V	1	±5V	See bipolar operation
0 - 5V	1	0-5V	65, 63 open; connect 67 to 68

TABLE I. Analog Input Range Pin Connections

In the unipolar mode the MP22 output data is straight binary. In the bipolar mode it is bipolar offset binary. If two's complement output is needed an external three-state inverting buffer is required.

Gain of the internal instrumentation amplifier (without external gain adjust) is 1.0. This gain can be increased to any value between 1.0 and 500 by adding an external resistor between pins 1 and 3. This external resistor (R) should be stable (10 ppm/°C or better) because its drift will add to the system accuracy temperature coefficient. Gain of the amplifier is determined by this formula:

External resistor R_{ext} connected: Gain = $1 + 25k\Omega/R_{ext}$

Pins 1 and 3 open: Gain = 1.0 ±0.02%

OPERATION WITH BIPOLAR INPUT VOLTAGES

To operate the MP22 with bipolar input voltages of ±5V, connect the unit as shown in Figure 10. Amplifier A1 divides the magnitude of the input by two, and the connection of a 12.5kΩ resistor between pin 63 (ref out) and pin 78 (offset null) offsets the signal such that the A/D converter sees a unipolar voltage from 0 to +5V.

To null the gain and offset errors of this circuit, follow this procedure:

1. Input - 5.0000V to any MP22 channel.
2. Adjust R1 until a digital output of all zeros is obtained.
3. Input +4.99817V to that MP22 channel.
4. Adjust R2 until a digital output of $0FFF_H$ is obtained.

POWER SUPPLY CONSIDERATIONS

For best performance and noise rejection, power supplies should be decoupled with 1.0μf tantalum or electrolytic capacitors in parallel with 0.01μF ceramic capacitors. To insure proper power supply sequencing, a diode should be connected between the pins 50 and 62 with the anode connected to pin 50.

A 0.1μF ceramic capacitor is required on each of the lines +MUX SUPPLY OUT (pin 37) and -MUX SUPPLY OUT (pin 38).

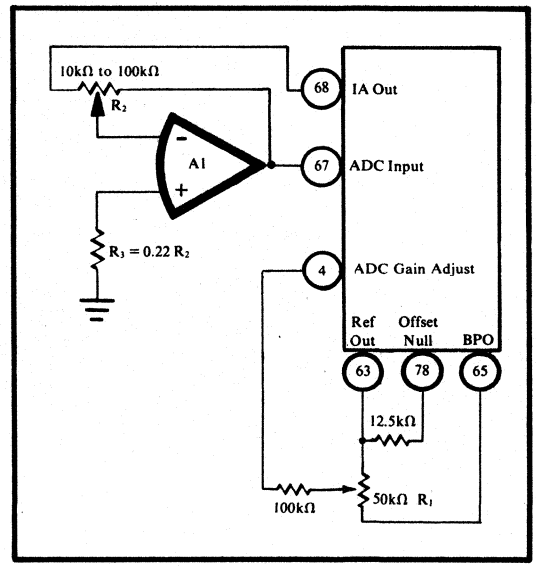


FIGURE 10. Connection for ±5V Input

	ANALOG INPUT			DIGITAL OUTPUT		
	±5V	0 to +5V	±5mV	OFFSET BINARY	STRAIGHT BINARY	TWO'S COMPLEMENT
+Full Scale	4.9975V	4.9988 V	4.9975 mV	FFF_H	FFF_H	$7FF_H$
Mid Scale	0.0000V	2.5000 V	0.0000	800_H	800_H	000_H
-Full Scale	-5.0000V	0.0000 V	-5.0000 mV	000_H	000_H	800_H
One LSB	2.44mV	1.22mV	2.44μV			

TABLE II. Analog Input, Digital Output Relationship

APPLICATIONS

DATA ACQUISITION FROM THERMOCOUPLE INPUTS

Thermocouples are often used as temperature sensors for process control systems. Thermocouples are characterized by temperature coefficients of 10 to 70μV/°C and operating ranges of minus hundreds to plus thousands of degrees centrigrade. When the MP22 is operated with an instrumentation amplifier gain of 100 or more, it may be connected directly to these devices. The wire runs from thermocouple to measuring device often pick up large common-mode noise signals of 60 Hz or higher frequencies. When the MP22 is used as an eight channel differential input system, the high common-mode rejection of the instrument amplifier will reject common-mode noise. To minimize differential mode noise, the signal wire should be twisted and if possible shielded. As a rule, an unshielded twisted pair is better than a coax, and a shielded, twisted pair is still better. In applications where these wiring practices cannot always be observed, a differential RC filter may be used. Figure 11 shows such a system.

The 10 kΩ resistors and 10μF capacitor provide low pass filtering (f_c = 0.8 Hz) while the optional 1 MΩ resistors supply bias current to the instrumentation amplifier. The remote sensor should be earth grounded to prevent common-mode voltages from exceeding the ±5 volt range of the multiplexer. If the sensor is earth grounded, the 1MΩ resistors are not required. The 1 MΩ resistors do not enter into an error calculation for input errors because the low resistance of the sensor shorts any differential voltage that might be caused by the offset (difference current) of the amplifier. Offset or difference current is merely the difference between the bias currents of the two inputs. The 1MΩ resistors could have been put on the output side of the multiplexer eliminating the need for repeating them for each input; however, this would have loaded the 10kΩ resistors of the filter causing a possible 1% error for static conditions.

To complete a thermocouple system it is necessary to terminate all thermocouple wire pairs at an isothermal box or connector strip of some type. An ordinary barrier strip may be monitored to allow the observed thermocouple emf to be cold junction compensated. Figure 11 shows an excellent circuit for this purpose. Its output is connected to one of the input channels to supply ambient temperature data to the system computer. Its output sensitivity is approximately 2 mV/°C.

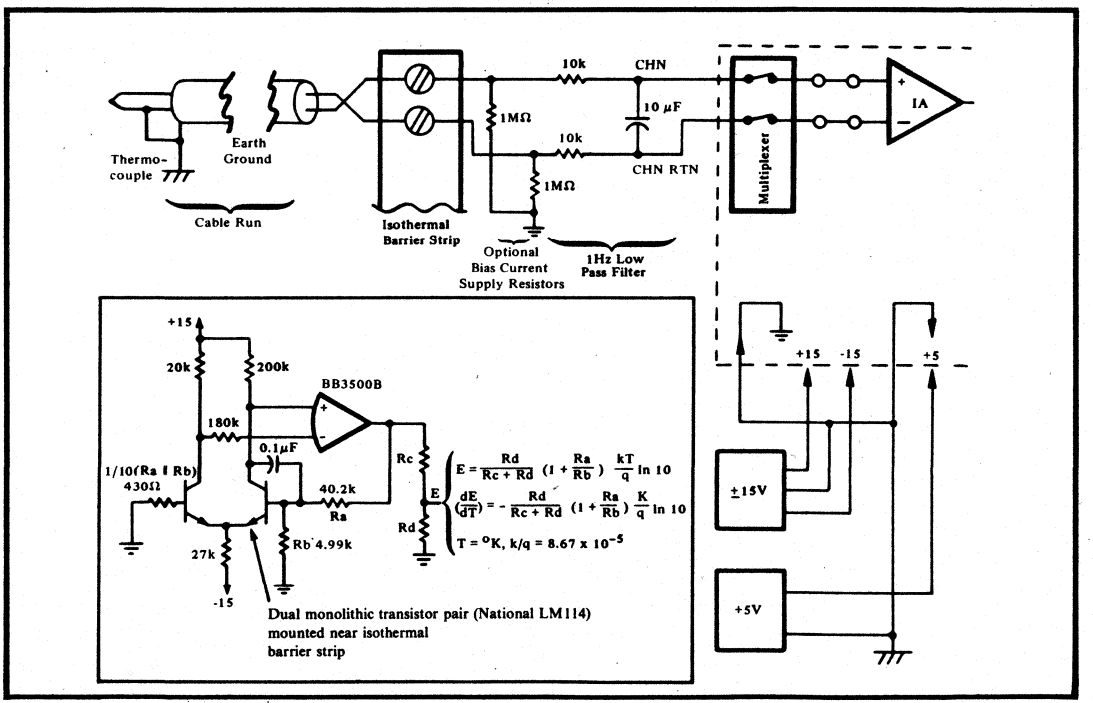
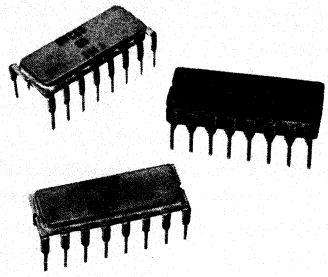


FIGURE 11. Thermocouple Input System Using MP22

BURR-BROWN



MPC4D
MPC8S

CMOS ANALOG MULTIPLEXERS

FEATURES

- LOW POWER CONSUMPTION
  CMOS analog switches
  15mW at 100kHz
- PROTECTS SIGNAL SOURCES
  Break-before-make switching
- HIGH THROUGHPUT RATE
- RELIABLE MONOLITHIC CONSTRUCTION

DESCRIPTION

The MPC8S is a single-ended monolithic 8-channel analog multiplexer and the MPC4D is a monolithic 4-channel differential input/output multiplexer. The digital and analog inputs are protected from overvoltage inputs that exceed either power supply. These CMOS devices feature self-contained binary channel address decoding and are compatible with DTL, TTL, or CMOS input levels. Channel interaction is eliminated during overvoltage conditions and also in the event of a power loss. They are packaged in a 16-pin DIP and dissipate typically 7.5mW.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-356 Printed in U.S.A. July, 1978

DESCRIPTION

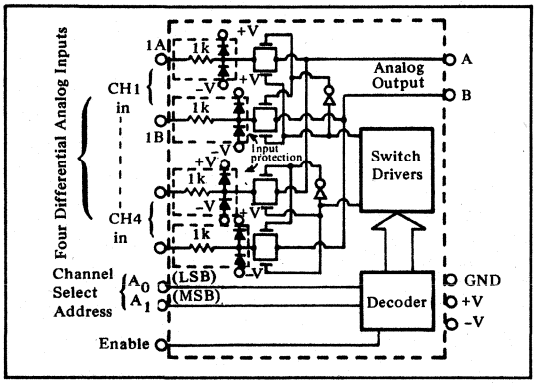
The MPC8S is a single-ended monolithic 8 channel analog multiplexer and the MPC4D is a monolithic differential input/output channel analog multiplexer constructed with failure protected CMOS devices. Transfer accuracies of better than 0.01% can be achieved at sampling rates up to 200 kHz from signal sources of up to ±10 volts amplitude.

These DTL/TTL/CMOS compatible devices feature self-contained binary channel address decoding. An ENABLE line is also made available which allows the user to individually enable an 8 channel group (MPC8S) or a 4 channel group (MPC4D) facilitating channel expansion in either single-mode or multi-tiered matrix configurations.

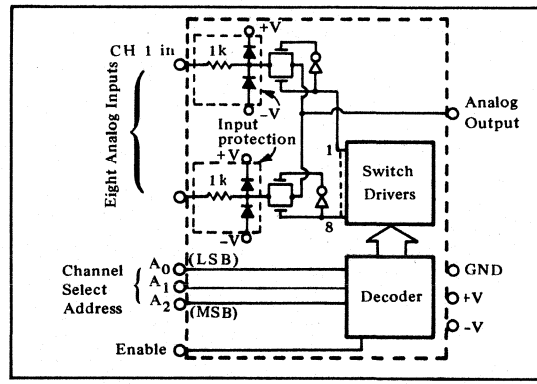
Digital and analog inputs are failure protected from either overvoltages that exceed the power supplies or from the loss of power.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, high OFF resistance, low feedthrough capacitance and fast settling time.

These devices are housed in compact 16 pin dual-in-line packages, and are specified for operation over a 0°C to +75°C temperature range. They are in pin and package compatible with the 508/509 series.



FUNCTIONAL BLOCK DIAGRAM – MPC4D



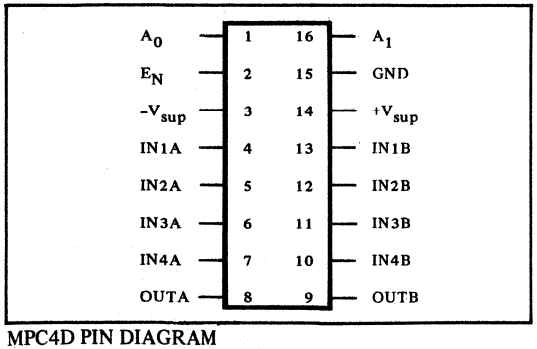
FUNCTIONAL BLOCK DIAGRAM – MPC8S

A_1	A_0	E_N	"On" Switch Pair
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

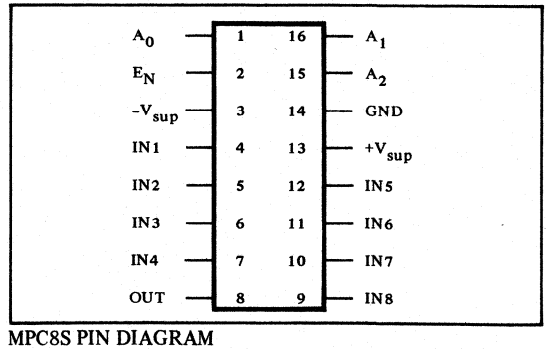
TRUTH TABLE –MPC4D

A_2	A_1	A_0	E_N	On Switch
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

TRUTH TABLE – MPC8S



MPC4D PIN DIAGRAM



MPC8S PIN DIAGRAM

SPECIFICATIONS

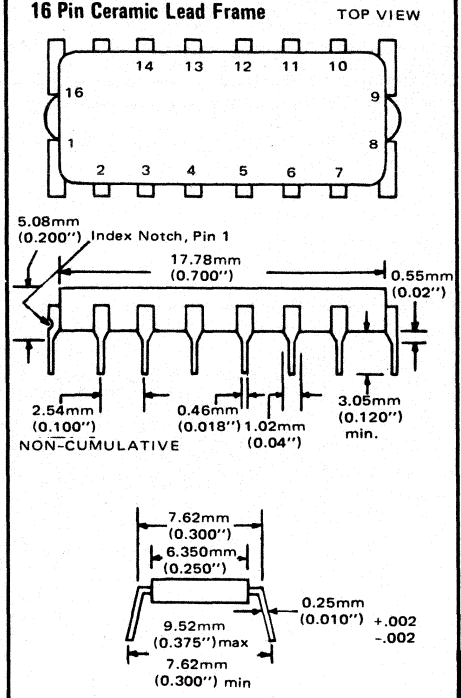
Typical for following conditions: V + = +15V, V - = -15V, $R_{source} \leq 1000\ \Omega$, $T_A = 25°C$ unless otherwise noted.

ELECTRICAL

MODELS	MPC8S	MPC4D	Units
INPUT			
ANALOG INPUT			
Voltage Range	±15		V
Maximum Overvoltage	+V supply +20		V
	-V supply -20		V
Current at Maximum Overvoltage per channel[1]	±18		mA
Number of Input Channels			
Single-ended	8		
Differential		4	
ON Characteristics			
ON Resistance (R_{ON})			
Typical	1.5		kΩ
Maximum	1.8		kΩ
R_{ON} Drift vs. Temperature (0°C to +75°C)	0.25		%/°C
R_{ON} Mismatch			
Channel-to-channel	50	50	Ω
Differential	N/A	50	Ω
Input Leakage (I_L)	0.1		nA
Input Leakage Drift	See Figure 9		
OFF Characteristics			
OFF Resistance	10^{11}		Ω
Output Leakage (All channels disabled)	0.2		nA
Input Leakage[6]	0.02		nA
Leakage Drift	See Figure 9		
Output Leakage with Input Overvoltage			
of +35V	1		nA
of -35V	1		μA
DIGITAL INPUTS			
Logic "0" (V_L)[1][2]	-V supply ≤ V_L < 0.8 at 1 nA		V
Logic "1" (V_H)[1][2]	+4V ≤ V_H ≤ + V supply at 1 nA		V
Channel Select	3 bit binary code - one of eight	2 bit binary code - one of four	
Enable	Logic "0" (low) disables all channels. Logic "1" (high) enables channel select to turn on selected channel.		
POWER REQUIREMENTS			
Rated Power Supply Voltages	±15		V
Supply Range			
+Supply	+5 to +20		V
-Supply	-5 to -20		V
Supply Drain			
At 1 MHz Switching Speed	+4, -2		mA
AT 100 kHz Switching Speed	±0.5		mA
Typical Power Consumption DC to 10 kHz	7.5		mW
DYNAMIC CHARACTERISTICS			
Gain Error (20 MΩ load) maximum	0.01		%
Crosstalk[3]	0.005		% of OFF channel signal
Settling Time[4]			
To ±2mV ±(0.01%)	5		μs
To ±20mV ±(0.10%)	2		μs
Common-mode Rejection (minimum)	N/A	120	dB
Switching Time			
Turn ON	0.5		μs
Turn OFF	0.3		μs
Recovery Time from Input Overvoltage Pulse of 35V for 100 μsec			
To 0.01%	150		μs
To 0.10%	15		μs
OUTPUT			
Voltage Range	±15		V
Capacitance to Ground	25	12[5]	pF
Capacitance Mismatch	N/A	±10	%
TEMPERATURE			
Specification	0 to +75		°C
Storage	-65 to +150		°C

MPC4D AND MPC8S

16 Pin Ceramic Lead Frame



NOTES:

1. Total power dissipation due to input overvoltage current flowing in the input protection circuitry must be limited to 0.75 watt for both (a) normal operation with power supplies turned on or (b) during a fault condition when the supplies are shorted to ground.
2. Maximum overvoltage is ±Vsupply ±4 volts at ±15 mA.
3. 20 volt peak-to-peak 1000 Hz sinewave; $R_{SOURCE} = 1000\Omega$, same signal on all unused channels.
4. For 20 volts between switched channels, $R_{SOURCE} = 1000\Omega$. See Figure 5 for settling time vs. source impedance (R_S).
5. From each side of MPC4D to ground.
6. Leakage measurement made with all OFF channel inputs fed in parallel to +20 volts.

DISCUSSION OF PERFORMANCE

Static Transfer Accuracy

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

SINGLE-ENDED MULTIPLEXER STATIC ACCURACY

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of 10^8 ohms or greater will keep resistive loading errors to 0.002% or less for 1000 ohm source impedances. A 10^6 ohm load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000 ohm source resistance will present less than 0.001% loading error and 10,000 ohm source resistance will increase source loading error to 0.01% with a 10^8 ohm load impedance.

Input resistive loading errors are determined by the following relationship: (see Figure 1)

Source and Multiplexer Resistive Loading Error

$$\in_{(R_S + R_{ON})} = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where R_S = source resistance
R_L = load resistance
R_{ON} = multiplexer ON resistance

INPUT OFFSET VOLTAGE

Bias current generates an input OFFSET voltage as result of the IR drop across the multiplexer ON resistance and source resistance. A load bias current of 10 nanoamperes will generate an offset voltage of 20μV if a 1000 ohm source is used, and 200μV if a 10,000 ohm source is used. In general, for the MPC8S, the OFFSET voltage at the output is determined by:

$$V_{OFFSET} = (I_b + I_L)(R_{ON} + R_S)$$

where I_b = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{SOURCE} = Source resistance

DIFFERENTIAL MULTIPLEXER STATIC ACCURACY

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full scale ranges of 10 to 100 millivolts.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

The effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications. Refer to Figure 2.

LOAD (OUTPUT DEVICE) CHARACTERISTICS

- Use devices with very low bias current. Generaly, FET input amplifiers should be used for low level signals less than 50mV RSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be 10^{10} ohms or higher.

SOURCE CHARACTERISTICS

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC4D is used for multiplexing high-level signals of ±1 volt to ±10 volts full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

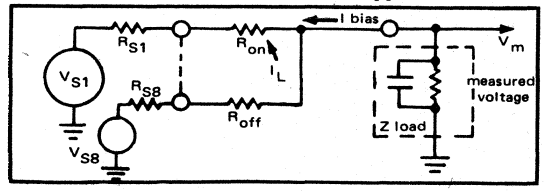


FIGURE 1: MPC8S Static Accuracy Equivalent Circuit.

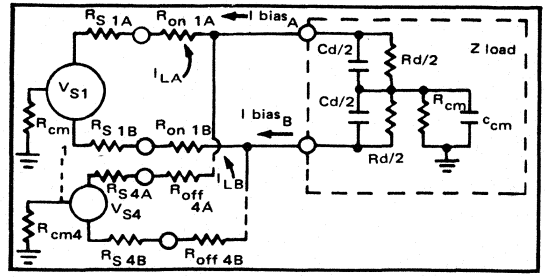


FIGURE 2: MPC4D Static Accuracy Equivalent Circuit.

SETTLING TIME

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation $i = C\frac{dV}{dt}$, the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figure 3 and 4. Using this relationship, one can see that the amplitude of the switching transients seen at the source and load decrease proportionally as the capacitance of the load and source increase. The tradeoff for reduced switching transient amplitude is increased settling time. If effect, the amplitude of the transients seen at the source and load are:

$$dV_{load} = \frac{i}{C}\,dt$$

where $i = C\frac{dV}{dt}$ of the CMOS FET switches

C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in Figure 5. This graph shows the settling time for a 20 volt step change on the input. The settling time for smaller step changes on the input will be less than that shown in Figure 5.

SWITCHING TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10 volt signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the three (MPC4D) or seven (MPC8S) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel OFF resistance and junction capacitances in series with the R_{ON} and R_{SOURCE} impedances of the ON channel. Crosstalk is measured with a 20 volt pk-pk 1000 Hertz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in Figure 6.

COMMON-MODE REJECTION (MPC4D ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the MPC4D, protection is provided for common-mode signals of ±20 volts above the power supply voltages with no damage to the analog switches.

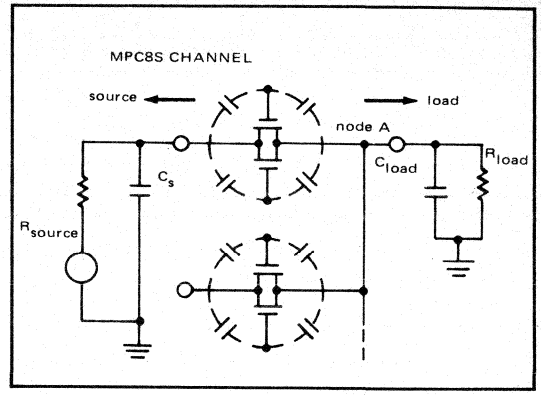


FIGURE 3: Settling Time Effects – MPC8S

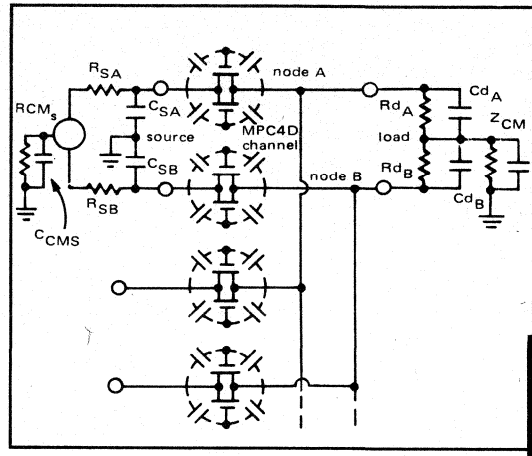


FIGURE 4: Settling & Common-Mode Effects – MPC4D.

The CMR of the MPC4D and Burr-Brown's model 3660 Instrumentation Amplifier is 120 dB at DC to 1 Hz with a 6 dB/octave rolloff to 70 dB at 1000 Hz. This measurement of CMR is shown in Figure 8 and is made with a Burr-Brown model 3660 Instrumentation Amplifier connected for a gain of 1000 and with source unbalance of 1kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

TYPICAL PERFORMANCE CURVES

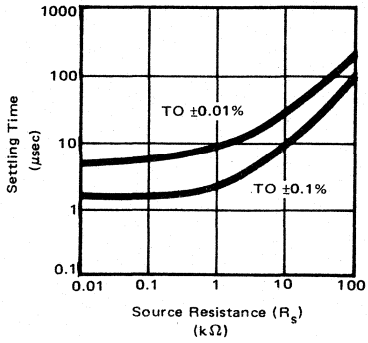


FIGURE 5. Settling time vs source resistance for 20 volt step change.

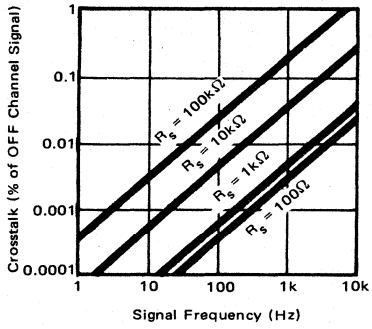


FIGURE 6. Crosstalk vs signal frequency.

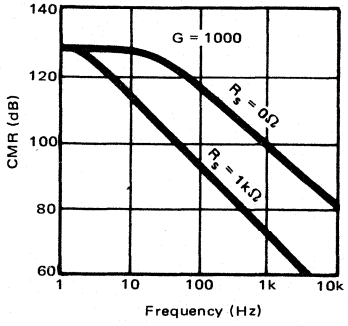


FIGURE 7. CMR vs frequency for Model 3660 IA and MPC4D (G = 1000).

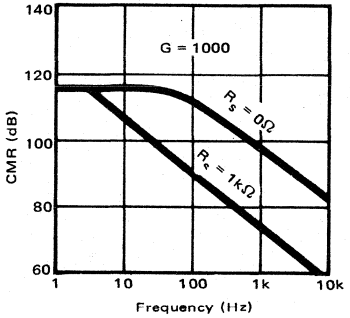


FIGURE 8. Combined CMR vs frequency for Model 3670 IA (G = 1000) and MPC4D.

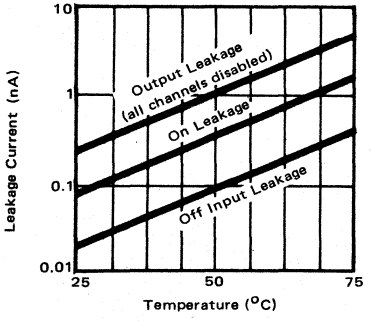


FIGURE 9. Leakage current vs temperature.

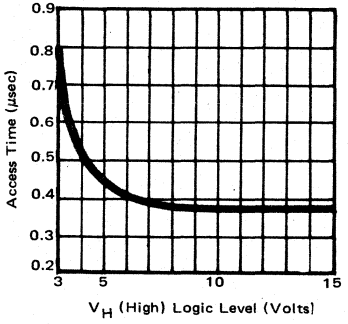


FIGURE 10. Access time vs logic level (high).

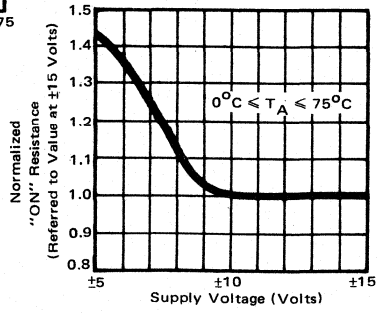


FIGURE 11. Normalized "ON" resistance vs supply voltage.

OPERATION & INSTALLATION INSTRUCTIONS

The ENABLE input, pin 2, is included for expansion of the number of channels on a single node as illustrated in Figure 12. With ENABLE line at a logic 1, the channel is selected by the 2 bit (MPC4D) or 3 bit (MPC8S) Channel Select Address (see the Truth Tables on page 5-136) If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to +V supply.

If the +15 volt and/or -15 volt supply voltage is absent or shorted to ground, the MPC4D and MPC8S multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded (see Footnote 1, page 5-137).

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull-up resistors are recommended. See Figure 10 (access time).

To preserve common-mode rejection of the MPC4D, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as closely as possible to system analog common or to the common-mode guard driver.

CHANNEL EXPANSION

SINGLE-ENDED MULTIPLEXER (MPC8S)

Up to 32 channels (4 multiplexers) can be connected to a single node, or up to 64 channels using 9 MPC8S multiplexers on a two-tiered structure as shown in Figure 12 and 13.

DIFFERENTIAL MULTIPLEXER (MPC4D)

Single or multi-tiered configurations can be used to expand multiplexer channel capacity up to 32 channels using a 32 x 1 or 16 channels using a 4 x 4 configuration.

SINGLE NODE EXPANSION

The 32 x 1 configuration is simply eight MPC4D units tied to a single node. Programming is accomplished with a 5 bit counter, using the 2 LSB's of the counter to control Channel Address inputs A_0 and A_1 and the 3 MSB's of the counter to drive a 1 of 8 decoder. The 1 of 8 decoder then is used to drive the ENABLE inputs (pin 2) of the MPC4D multiplexers.

TWO TIER EXPANSION

Using a 4 x 4 2-tier structure for expansion to 16 channels, the programming is simplified A 4-bit counter output does not require a 1 of 8 decoder. The 2 LSB's of the counter drive the A_0 and A_1 inputs of the four first tier multiplexers and the 2 MSB's of the counter are applied to the A_0 and A_1 inputs of the second tier multiplexer.

Single vs. Multi-Tiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single node expansion of reduced OFF channel current leakage (reduced OFFSET), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single node configuration, data cannot be taken from any channel, where as only one channel group is failed (4 or 8) in the multi-tiered configuration.

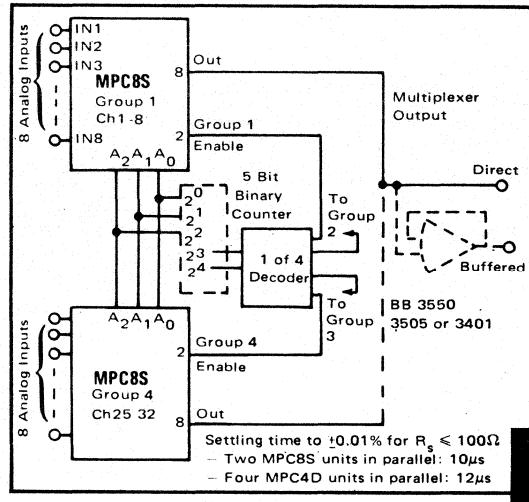


FIGURE 12. 32 Channel, Single-Tier Expansion.

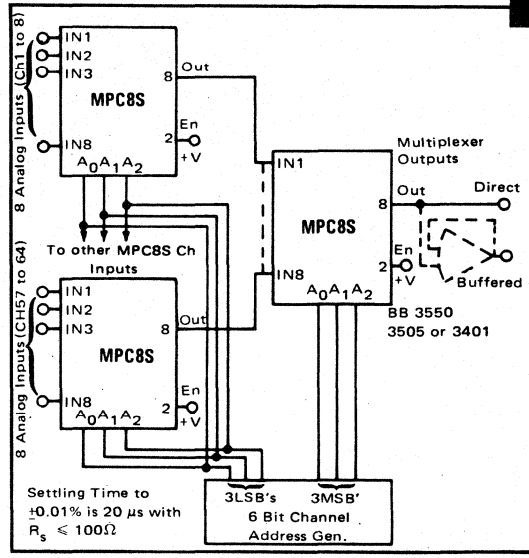
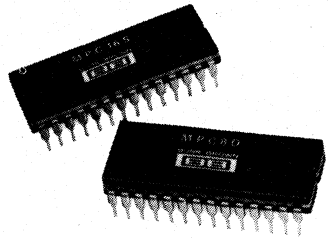


FIGURE 13. Channel Expansion Up to 64 Channels Using 8X8 Two-Tiered Expansion.

BURR-BROWN



MPC8D
MPC16S

CMOS ANALOG MULTIPLEXERS

FEATURES

- LOW POWER CONSUMPTION
  - CMOS analog switches
  - 15mW at 100kHz
  - 7.5mW standby power
- COMPACT DESIGN
  - Self-contained with internal channel address decoder
  - 8-channel dual (MPC8D) for differential inputs or
  - 16-channel (MPC16S) for single-ended inputs
  - 28-pin 0.600 inch-wide space-saving package
- WILL NOT SHORT SIGNAL SOURCES
  - Break-before-make switching
- FAST SWITCHING SPEEDS PROVIDE HIGH THROUGHPUT RATES
  - 7μsec settling to 0.01%
  - 3μsec settling to 0.1%
- WIDE SUPPLY RANGE
  - ±7VDC to ±20VDC

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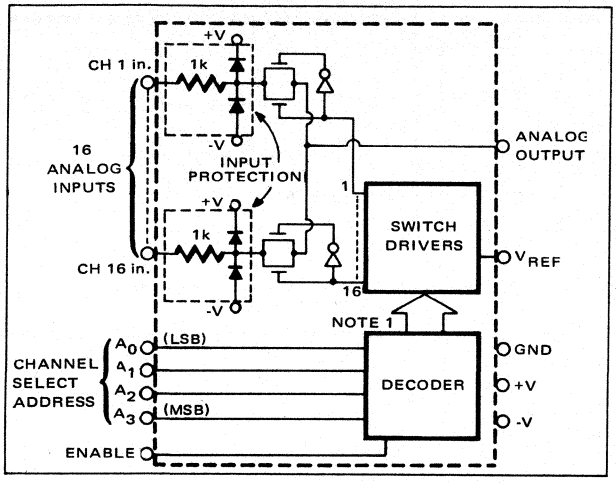
DESCRIPTION

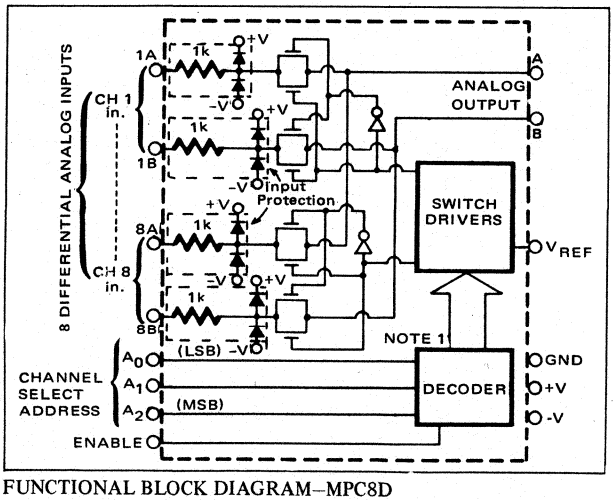
The MPC16S is single-ended monolithic 16 channel analog multiplexer and the MPC8D is a monolithic dual 8 channel analog multiplexer constructed with failure protected CMOS devices. Transfer accuracies of better than 0.01% can be achieved at sampling rates up to 200 kHz from signal sources of up to ± 10 volts amplitude.

These DTL/TTL/CMOS compatible devices feature self-contained binary channel address decoding. An ENABLE line is also made available which allows the user to individually enable a 16 channel group (MPC16S) or an 8 channel group (MPC8D) facilitating channel expansion in either single-node or multi-tiered matrix configurations.

Digital and analog inputs are failure protected from either overvoltages that exceed the power supplies or from the loss of power.



FUNCTIONAL BLOCK DIAGRAM–MPC16S

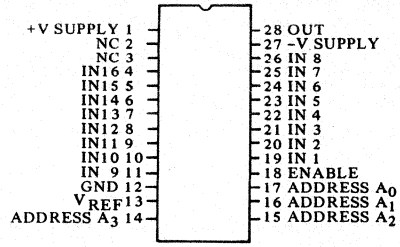


FUNCTIONAL BLOCK DIAGRAM–MPC8D

NOTE: 1 Inputs protected.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, high OFF resistance, low feedthrough capacitance and fast settling time.

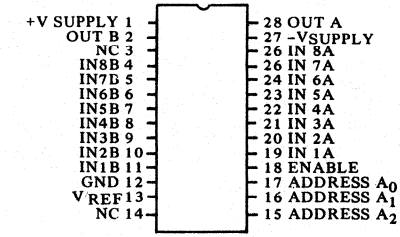
These devices are housed in compact 28 pin dual-in-line packages, and are specified for operation over a 0°C to +75°C temperature range. They are pin and package compatible with the 506/507 series.



MPC16S PIN DIAGRAM

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

TRUTH TABLE–MPC16S



MPC8D PIN DIAGRAM

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

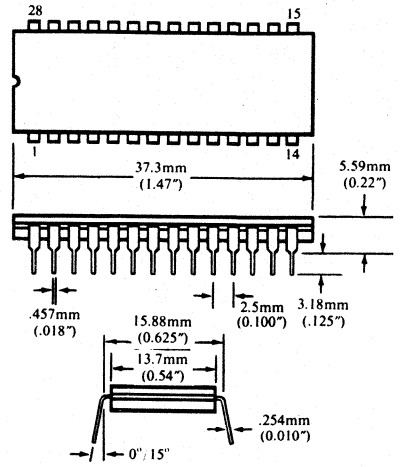
TRUTH TABLE–MPC8D

ELECTRICAL SPECIFICATIONS

Typical for following conditions:
$V+ = +15$ V, $V- = -15$ V, $R_{source} \leq 1000\ \Omega$, $T_A = 25^{\circ}C$ unless otherwise noted.

MODELS	MPC16S	MPC8D	Units
INPUT			
ANALOG INPUT			
Voltage Range	±15		V
Maximum Overvoltage	+V supply +20		V
	-V supply -20		V
Current at Maximum Overvoltage per Channel (1)	±18		mA
Number of Input Channels			
Single-Ended	16		
Differential		8	
Reference Voltage Range(2)	+6 to +10		V
ON Characteristics			
ON Resistance (R_{ON})			
Typical	1.3		kΩ
Maximum	1.8		kΩ
R_{ON} Drift vs. Temperature (0°C to +75°C)	0.25		%/°C
R_{ON} Mismatch			
Channel-to-channel	50	50	Ω
Differential	N/A	50	Ω
Input Leakage (I_L)	1.0		nA
Input Leakage Drift	See Figure 9		
OFF Characteristics			
OFF Resistance	10^{11}		Ω
Output Leakage (all channels disabled)	0.2		nA
Input Leakage (7)	0.02		nA
Leakage Drift	See Figure 9		
Output Leakage with Input Overvoltage			
of +35 V	1		nA
of -35 V	1		μA
DIGITAL INPUTS			
Logic "0" (V_L)(1)(3)	$-V$ supply $\leq V_L < 0.8$ @ 1 nA		V
Logic "1" (V_H)(1)(3)	$+4 \leq V_H \leq +V_{supply}$ @ 1 nA		V
Channel Select	4 bit binary code - one of sixteen	3 bit binary code – one of eight	
Enable	Logic "0" (low) disables all channels. Logic "1" (high) enables channel select to turn on selected channel.		
POWER REQUIREMENTS			
Rated Power Supply Voltages	±15		V
Supply Range			
+ Supply	+7 to +20		V
- Supply	-7 to -20		V
Supply Drain			
At 1 MHz Switching Speed	+4, -2		mA
At 100 kHz Switching Speed	±0.5		mA
Typical Power Consumption DC to 10 kHz	7.5		mW
DYNAMIC CHARACTERISTICS			
Gain Error (20 MΩ load) maximum	0.01		%
Crosstalk (4)	0.005		% of OFF channel signal
Settling Time(5)			
To 2 mV (0.01%)	7		μs
To 20 mV (0.10%)	3		μs
Common-Mode Rejection (minimum)	N/A	120	dB
Switching Time			
Turn ON	0.5		μs
Turn OFF	0.3		μs
Recovery Time from Input Overvoltage Pulse of 35 V for 100 μsec			
To 0.01%	150		μs
To 0.10%	15		μs
OUTPUT			
Voltage Range	±15		V
Capacitance to Ground	50	30(6)	pF
Capacitance Mismatch	N/A	±10	%
TEMPERATURE			
Specification	0 to +75		°C
Storage	-65 to +150		°C

MECHANICAL SPECIFICATIONS



NOTES:

1. Total power dissipation due to input overvoltage current flowing in the input protection circuitry must be limited to one watt for both (a) normal operation with power supplies turned on or (b) during a fault condition when the supplies are shorted to ground.
2. Reference voltage controls noise immunity level. Normally not used (pin 13 left open).
3. Maximum overvoltage is $\pm V_{supply}$ ±4 volts @ ±15 mA. Logic levels specified are for V_{REF} (pin 13) open. For V_{REF} = +10 V, $V_{H\ MIN}$ = +6 V.
4. 20 volt peak-peak 1000 Hz sinewave; R_{source} = 1000 Ω, same signal on all unused channels.
5. For 20 volts between switched channels, R_{source} = 1000 Ω. See Figure 5 for settling time vs. source impedance (R_S).
6. From each side of MPC8D to ground.
7. Leakage measurement made with all OFF channel inputs fed in parallel to +20 volts.

DISCUSSION OF PEFORMANCE

STATIC TRANSFER ACCURACY

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

SINGLE-ENDED MULTIPLEXER STATIC ACCURACY

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of 10^8 ohms or greater will keep resistive loading errors to 0.002% or less for 1000 ohm source impedances. A 10^6 ohm load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000 ohm source resistance will present less than 0.001% loading error and 10,000 ohm source resistance will increase source loading error to 0.01% with a 10^8 ohm load impedance.

Input resistive loading errors are determined by the following relationship: (see Figure 1)

Source and Multiplexer Resistive Loading Error

$$\in_{(R_S + R_{ON})} = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\% \text{ where}$$

$R_S = R_{source}$
R_L = load resistance
R_{ON} = multiplexer ON resistance.

INPUT OFFSET VOLTAGE

Bias current generates an input OFFSET voltage as a result of the I_R drop across the multiplexer ON resistance and source resistance. A load bias current of 10 nanoamperes will generate an offset voltage of 20μVolts if a 1000 ohm source is used, and 200μVolts if a 10,000 ohm source is used. In general, for the MPC16S, the OFFSET voltage at the output is determined by:

$$V_{OFFSET} = (I_b + I_L)(R_{ON} + R_{SOURCE})$$

where I_b = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{SOURCE} = Source resistance

DIFFERENTIAL MULTIPLEXER STATIC ACCURACY

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full scale ranges of 10 to 100 millivolts.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications.

LOAD (OUTPUT DEVICE) CHARACTERISTICS

- Use devices with very low bias current. Generally, FET input amplifiers should be used for low level signals less than 50 mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50 mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be 10^{10} ohms or higher.

SOURCE CHARACTERISTICS

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC8D is used for multiplexing high-level signals of 1 volt to 10 volts full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

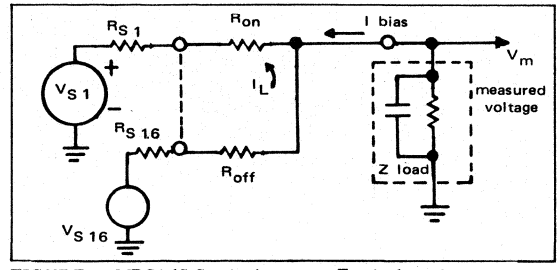


FIGURE 1: MPC16S Static Accuracy Equivalent Circuit.

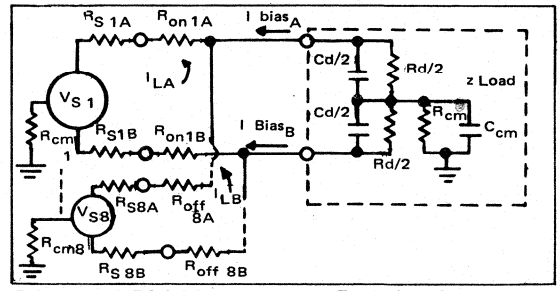


FIGURE 2: MPC-8D Static Accuracy Equivalent Circuit.

SETTLING TIME

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation $i = C\frac{dV}{dt}$, the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figure 3 and 4. Using this relationship, one can see that the amplitude of the switching transients seen at the source and load decrease proportionally as the capacitance of the load and source increase. The tradeoff for reduced switching transient amplitude is increased settling time. In effect, the amplitude of the transients seen at the source and load are:

$$dV_{load} = \frac{i}{C}\,dt$$

where $i = C\frac{dV}{dt}$ of the CMOS FET switches

C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in Figure 5. This graph shows the settling time for a 20 volt step change on the input. The settling time for smaller step changes on the input will be less than that shown in Figure 5.

SWITCHING TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10 volt signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the seven (MPC8D) or fifteen (MPC16S) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel OFF resistance and junction capacitances in series with the R_{ON} and R_{SOURCE} impedances of the ON channel. Crosstalk is measured with a 20 volt pk-pk 1000 Hertz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in Figure 6.

COMMON-MODE REJECTION (MPC8D ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the MPC8D, protection is provided for common-mode signals of ±20 volts above the power supply voltages with no damage to the analog switches.

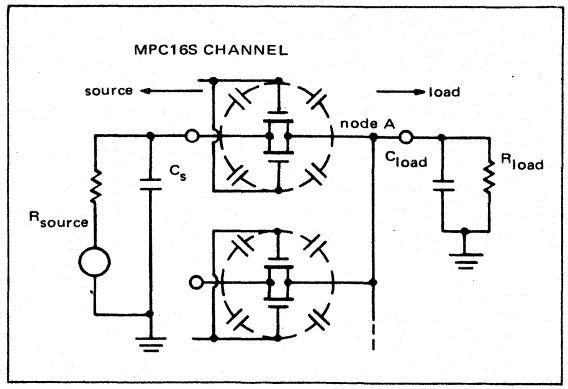


FIGURE 3: Settling Time Effects–MPC16S.

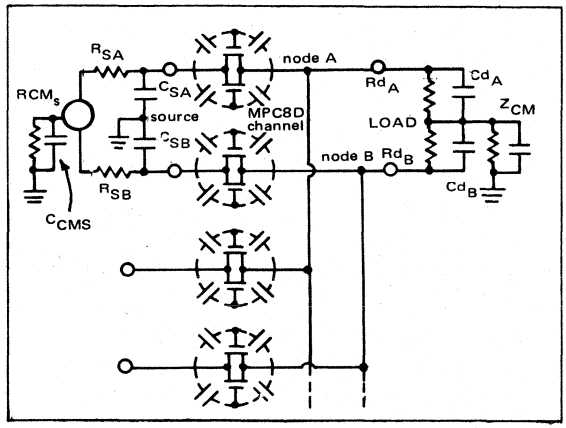


FIGURE 4: Settling & Common-Mode Effects–MPC-8D.

The CMR of the MPC8D and Burr-Brown's model 3660 Instrumentation Amplifier is 110 dB at DC to 1k Hz with a 6 dB/octave rolloff to 70 dB at 1000 Hz. This measurement of CMR is shown in Figure 8 and is made with a Burr-Brown model 3660 instrumentation amplifier connected for a gain of 1000 and with source unbalances of 10 k, 1 kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

TYPICAL PERFORMANCE CURVES

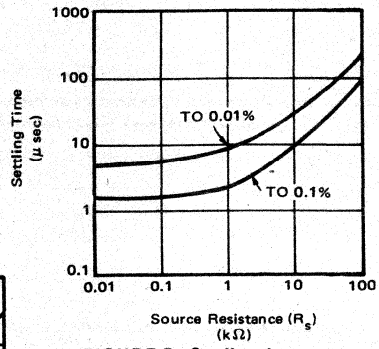


FIGURE 5. Settling time vs source resistance for 20 volt step change.

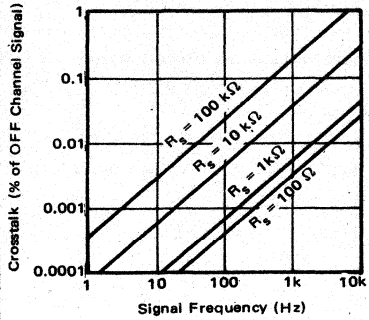


FIGURE 6. Crosstalk vs signal frequency.

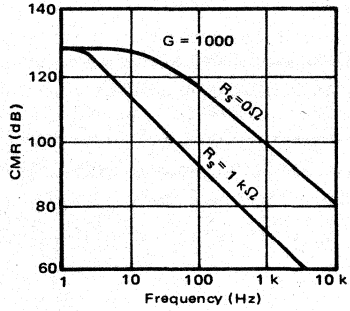


FIGURE 7. CMR vs. frequency for Model 3660 IA and MPC8D (G = 1000).

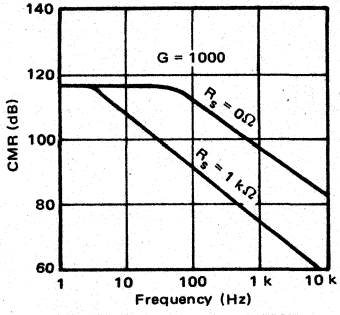


FIGURE 8. Combined CMR vs. frequency for Model 3670 IA and MPC8D (G = 1000).

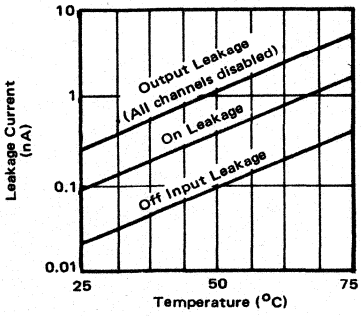


FIGURE 9. Leakage current vs temperature.

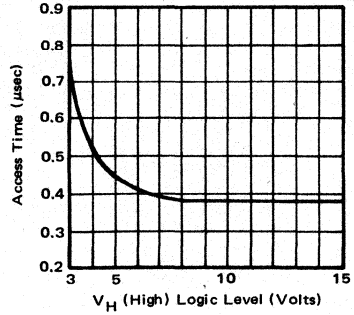


FIGURE 10. Access time vs logic level (high).

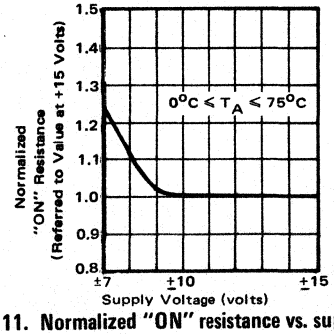


FIGURE 11. Normalized "ON" resistance vs. supply voltage.

OPERATION & INSTALLATION INSTRUCTIONS

The ENABLE input, pin 18, is included for expansion of the number of channels on a single node as illustrated in Figure 12. With the ENABLE line at a logic 1, the channel is selected by the 3 bit (MPC8D) or 4 bit (MPC16S) Channel Select Address (see the Truth Tables on page 5-143). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to +V supply.

If the +15 volt and/or -15 volt supply voltage is absent or shorted to ground, the MPC8D and MPC16S multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded (see Footnote 1, page 5-144).

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull-up resistors are recommended. See Figure 10 (access time).

To preserve common-mode rejection of the MPC8D, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as closely as possible to system analog common or to the common-mode guard driver.

CHANNEL EXPANSION

SINGLE ENDED MULTIPLEXER (MPC16S)

Up to 64 channels (4 multiplexers) can be connected to a single node, or up to 256 channels using 17 MPC16S multiplexers on a two-tiered structure as shown in Figures 12 and 13.

DIFFERENTIAL MULTIPLEXER (MPC8D)

Single or multi-tiered configurations can be used to expand multiplexer channel capacity up to 64 channels using a 64 x 1 or 8 x 8 configuration.

SINGLE NODE EXPANSION

The 64 x 1 configuration is simply eight MPC8D units tied to a single node. Programming is accomplished with a 6 bit counter, using the 3 LSB's of the counter to control Channel Address inputs A_0, A_1 and A_2 and the 3 MSB's of the counter to drive an 8 or 1 decoder. The 8 of 1 decoder then is used to drive the ENABLE inputs (pin 18) of the MPC8D multiplexers.

TWO TIER EXPANSION

Using an 8 x 8 2-tier structure for expansion to 64 channels, the programming is simplified. The 6 bit counter output does not require an 8 of 1 decoder. The 3 LSB's of the counter drive the A_0, A_1 and A_2 inputs of the eight first tier multiplexers and the 3 MSB's of the counter are applied to the A_0, A_1 and A_2 inputs of the second tier multiplexer.

Single vs. Multi-Tiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single node expansion of reduced OFF channel current leakage (reduced OFFSET), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single node configuration, data cannot be taken from any channel, whereas only one channel group is failed (8 or 16) in the multi-tiered configuration.

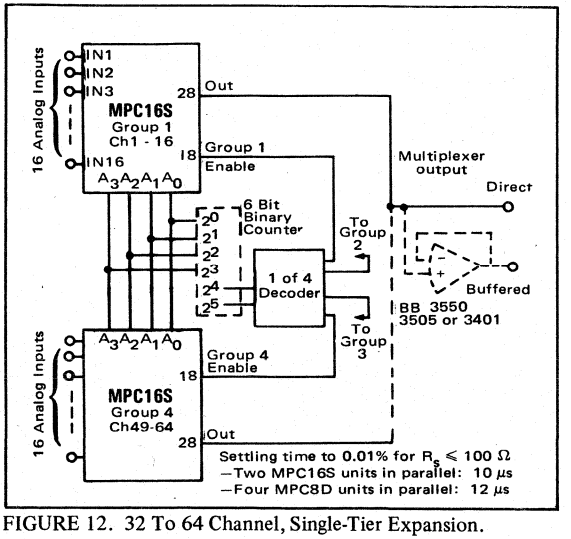


FIGURE 12. 32 To 64 Channel, Single-Tier Expansion.

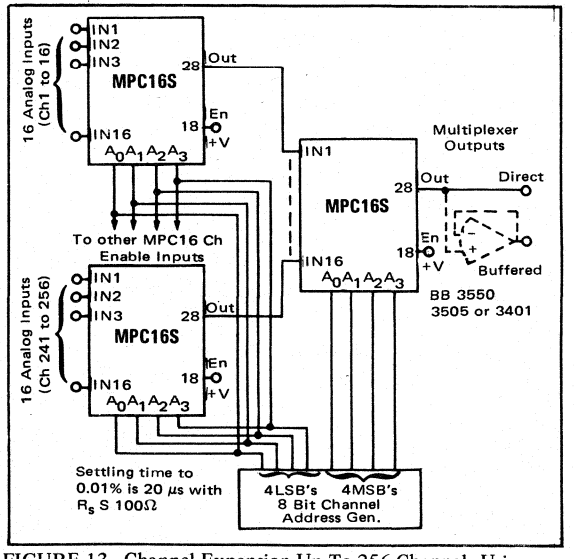
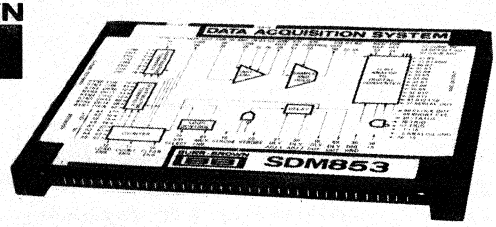


FIGURE 13. Channel Expansion Up To 256 Channels Using 16 x 16 Two Tiered Expansion.

BURR-BROWN



SDM853

DATA ACQUISITION SYSTEM

FEATURES

- SAVES DESIGN TIME
- RELIABLE - 168 hour bake
- LOW LEVEL OR HIGH LEVEL INPUTS
- SAVES SPACE
- FLEXIBLE - Up to four modes of operation
- LOW COST

DESCRIPTION

The SDM853 is a complete 8- or 16-channel data acquisition system in a compact 4.6″ x 3.0″ x 0.375″ metal case. This system differs from most in that it can acquire and digitize low level or high level analog signals. A built-in high quality instrumentation amplifier allows input signal ranges of ±10mV to ±10V. This means that the SDM853 can be connected to low level sensors such as thermocouples and strain gauges without external signal conditioning.

This expandable module accepts either 16 single-ended or 8 differential inputs and converts the multiplexed data signals into 12-bit digial words with an accuracy of ±0.025% at throughput rates of up to 33,000 samples per second.

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PDS-354A
Printed in U.S.A. July, 1978

DISCUSSION OF PERFORMANCE

The SDM853 is a complete modular "off the shelf" data acquisition system. With this system it is possible to configure complete data acquisition systems in one-fourth the space for a fraction of the cost previously possible.

These systems contain all the components necessary to multiplex and convert ±10mV to ±10V analog data into equivalent digital outputs yielding resolutions of 2.4μV to 2.4mV. The minimum throughput sampling rates are up to 30 kHz for 12 bit and up to 43 kHz for 8 bit resolution. The model SDM853 contains an analog multiplexer which can be connected in a 16 channel single ended or 8 channel differential mode, instrumentation amplifier, sample/hold, 12 bit successive approximation A/D converter and programming logic. The amplifier and sample/hold are not internally interconnected. This allows maximum application flexibility. These systems can be expanded without limit using Burr-Brown's MPC-16S and MPC-8D monolithic multiplexers. Figure 1 shows the components of the SDM853. The system is designed to be mounted on a printed circuit card. The only requirement for system operation are input signals, power and the interconnection of the system components into the desired operating configuration.

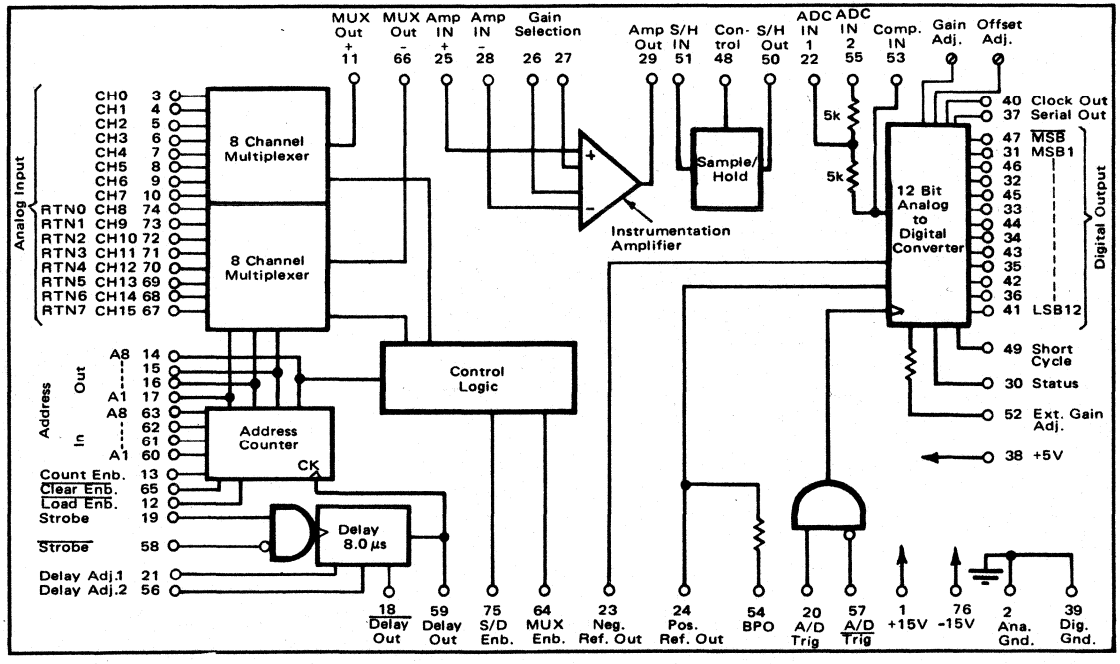


FIGURE 1. SDM853 Block Diagram.

ANALOG MULTIPLEXER

Two one of eight CMOS analog multiplexers are used to allow user selection by external jumpers of 16 single ended channel or 8 double ended channel operation. In 16 channel operation the multiplexer may be used in a pseudo differential mode by connecting the amplifier inverting input to a common, remote, signal ground. Channel selection is by a 3 or 4 bit binary word stored in a presettable address counter. Channel capacity is expandable without limit.

INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is a low drift, differential amplifier featuring high speed at gains above unity, and external gain programming with an external resistor. With the gain programming pins open, the gain is unity. Gain may be selected from unity to 60 dB.

SAMPLE AND HOLD AMPLIFIERS

The sample and hold amplifier is a complete, stand alone, sample and hold circuit featuring buffered output, 7μs acquisition time, and 30ns aperture time. Input, output and mode control functions are brought to separate connector pins. This allows maximum system flexability for performing such functions as automatic gain ranging with no loss of aperture time.

ANALOG-TO-DIGITAL CONVERTER

The ADC is a ceramic packaged, 12 bit converter featuring 24 μs conversion time and 0.01% accuracy. Thin-film networks and current switching are used to assure linearity over wide temperature ranges.

ADDRESS COUNTER

A four bit binary address counter is connected to the multiplexer. This counter may be externally loaded, cleared, clocked or enabled. The address outputs are brought to connector pins for convenient system control.

DELAY TIMER

The delay timer is provided to allow for the settling time of the multiplexer, amplifier, and sample and hold circuits. The delay time is adjustable over a wide range by an external potentiometer and/or external capacitor. This allows for the longer settling time of the instrument amplifier at high gains.

CONTROL LOGIC

Delay and ADC trigger functions are edge triggered and gated. Counter control functions are synchronous with the counter clock which is internally connected to the delay timer output.

CHANNEL EXPANSION

The number of analog input channels of these systems can easily be increased using Burr-Brown's MPC8D and MPC16S CMOS multiplexers. The MPC8D is an 8 channel differential model and the MPC16S is a 16 channel single-ended model. These are latch-free devices which contain internal binary decoding, TTL or MOS logic levels, and may be integrated into a system with minimum external logic.

SYSTEM PERFORMANCE

The SDM853 can be configured to continuously sequence through all analog channels, to accept random addresses or to sequence through all analog channels on command from an external trigger.

The status signal, pin 30, is connected to the strobe not input of the delay timer, pin 58, for normal program sequencing with a minimum throughput sampling rate of 30 kHz for 12 bit resolution.

By using "overlap" programming, the settling time effects of the analog multiplexer and instrumentation amplifier can be reduced, extending throughput sampling rates up to 32 kHz for 12 bit and 43 kHz to 8 bit resolution. This mode of operation is most useful when converting low level inputs to accommodate the increased settling time of the instrumentation amplifier. Overlap programming is accomplished by connecting the status signal, pin 30, to the strobe input of the delay timer, pin 19, and extending the delay time. The internal logic will then select analog channel (n + 1) while channel n is being converted.

SYSTEM PERFORMANCE

(Typical at 25°C and rated supplies)

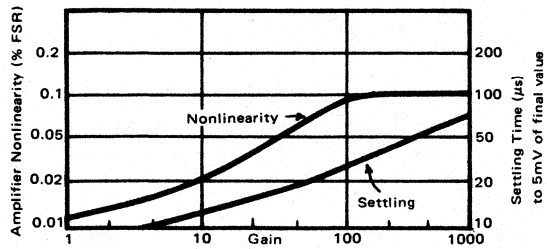


FIGURE 2. Nonlinearity and Settling Time vs. Amplifier Gain.

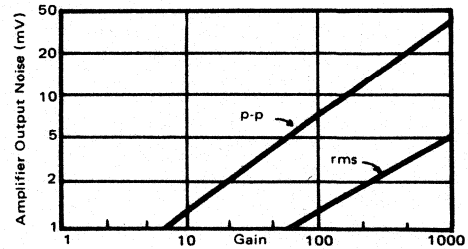


FIGURE 3. Output Noise vs. Amplifier Gain.

System Gain	System Accuracy	Throughput Rate (Channels/sec)		Delay Time (μs)	
V/V		Normal	Overlap	Normal	Overlap
1	±0.025% FSR	30k	32k	9	31
10	±0.035% FSR	25k	32k	18	31
100	±0.08% FSR	20k	32k	25	31
1000	±0.1% FSR	10k	14k	70	70

TABLE I. Throughput Rate vs. Gain. For normal and overlap modes.

FSR	ADC Range	Amplifier Gain	Resolution	Delay for Settling to ±0.2% (μsec)	Delay for Settling to ±0.05% (μsec)	Delay for Settling to 0.01% (μsec)
20V	±10V	1	4.88mV	7	8	9
1V	0 to 10V	10	244μV	10	15	18
0.1V	0 to 10V	100	24.4μV	20	25	30
10mV	0 to 10V	1000	2.44μV*	60	70	-

TABLE II. This table shows the delay timer setting required to allow for the settling time of the instrumentation amplifier to the accuracies specified. Add the 24μsec conversion time of the A/D converter to the above delay times to obtain channel conversion times. * Depends on desired S/N ratio.

SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	SDM853
TRANSFER CHARACTERISTICS	
Throughput Rate (min)	30 kHz, 33 μsec/channel
Resolution	12 Bits
Number of Channels	16 single-ended/8 differential
ANALOG INPUTS	
ADC gain ranges	0-5V, 0-10V, ±2.5V, ±5V, ±10V
Amplifier gain range	1 to 1000
Amplifier gain equation	$G = 1 + 20\ k\Omega / R_{EXT}$ [1]
Max. input voltage without damage	±16 volts
Max. input voltage for multiplexer operation	±10.24 volts
Input impedance	100 MΩ, 10 pF OFF Channel 100 MΩ, 100 pF ON Channel
Bias current	
25°C	20 nA
0°C to 70°C	50 nA
Differential Bias Current (25°C)	10 nA
Differential Bias Current Drift	0.1 nA/°C
Amplifier output noise (Gain = 100, R_s = 500Ω)	1.2 mV, rms; 7 mV, p-p
Amplifier input offset voltage (max)	400 μV
Amplifier voltage offset drift	$2 + \frac{20}{G}$ μV/°C
ACCURACY [2]	
System RSS accuracy @ 25°C (Gain = 1)	±0.025% FSR [3] @ 30 kHz throughput
Linearity (Gain = 1)	±1/2 LSB, @ 30 kHz throughput
Differential linearity (Gain = 1)	±1/2 LSB, @ 30 kHz throughput
Quantizing error	±1/2 LSB
Gain error	Adjustable to Zero
Offset error	Adjustable to Zero
Power supply sensitivity	±0.005% FSR/% Change of supply voltage
STABILITY OVER TEMPERATURE	
System accuracy drift (max)	±30 ppm/°C of Reading
Linearity drift	±3 ppm of FSR/°C
DYNAMIC ACCURACY	
Sample & Hold aperture time	30 ns
Aperture time uncertainty	±5 ns
Error for full scale transition between successively addressed channels	1 LSB @ 30 kHz
Differential amplifier CMRR (Gain = 1)	74 dB @ 1kHz 65 dB @ 3kHz (100 dB @ 60 Hz Gain = 1000)
Channel cross talk	80 dB down @ 2 kHz, for OFF channel to ON channel
Sample & Hold feedthrough	80 dB down @ 5 kHz
Sample & Hold decay rate	10 μV/μs
OUTPUT	
Output Coding (Complementary)	Unipolar Straight Binary, Bipolar Offset, Binary Two's Complement
Gain trim [4]	Adjustable to zero error
Offset trim [4]	Adjustable to zero error
A/D Conversion Time	24 μsec
Delay	9 μs nominal, externally adjustable from 5.5 μs to 14 μs [5]
POWER REQUIREMENTS	±15V ±3% @ +50 mA, 5 mV rms ripple -15V ±3% @ -75 mA, 5 mV rms ripple +5V ±5% @ +300 mA, 25 mV rms ripple
ENVIRONMENTAL	
Operating temperature	0°C to 70°C
Storage temperature	-25°C to +85°C
Relative humidity	95% noncondensing

(1) With R_{EXT} between pins 26 and 27.
(2) No missing codes guaranteed.
(3) FSR means Full Scale Range.
(4) Gain and Offset controls are located in the module. The adjustment ranges are ±0.1% FSR for Gain and ±0.1% FSR for Offset.
(5) Adjustable to 10 seconds with external capacitor.

DIGITAL INPUT SPECIFICATIONS

Address inputs	One standard TTL load, positive true
Coding	4 bit binary
Load Enable	One standard TTL load, negative true, address loaded with strobe inputs.
Clear Enable	One standard TTL load, negative true, address loaded with strobe inputs.
Strobe & Strobe	One standard TTL load, STROBE and STROBE edge trigger the delay timer and clock the address counter. STROBE must be high to enable STROBE and STROBE must be low to enable STROBE.
Count Enable	Two standard TTL loads, positive true, logic "0" allows the Strobe inputs to trigger the delay timer, but prevents the MUX address counter from being clocked.
ADC trigger	One standard TTL load, a positive going edge at TRIG initiates conversion, a negative going edge at TRIG initiates conversion; TRIG must be "0" to enable TRIG; TRIG must be "1" to enable TRIG.
Short cycle	One standard TTL load, logical 1 for 12 bit resolution, connected to the N + 1 bit output for N bit resolution.
Multiplexer Enable	
Multiplexer Enable	Two standard TTL loads, logical 1 enable multiplexer output and logical 0 turns off all channels.
S/D select	Two standard TTL loads, logical 1 enables 16 channel single-ended operation and logical 0 enable 8 channel differential operation.

DIGITAL OUTPUT SPECIFICATIONS

Data outputs	
Parallel B1, B1 . . . B12	2 Standard TTL loads, negative true.
Serial out	2 Standard TTL loads, negative true, time serial data output beginning with B1, (see timing diagram).
Address outputs	5 Standard TTL loads, positive true, 4 bit binary code, internal 2kΩ pull-up resistors.
Delay out (Delay Out)	5 Standard TTL loads high (low) during the delay period, triggered by Strobe and Strobe inputs.
Clock	5 Standard TTL loads for synchronizing serial out data (see timing diagram).
Status	5 Standard TTL loads, high during the A/D converison.

SYSTEM TIMING DIAGRAMS

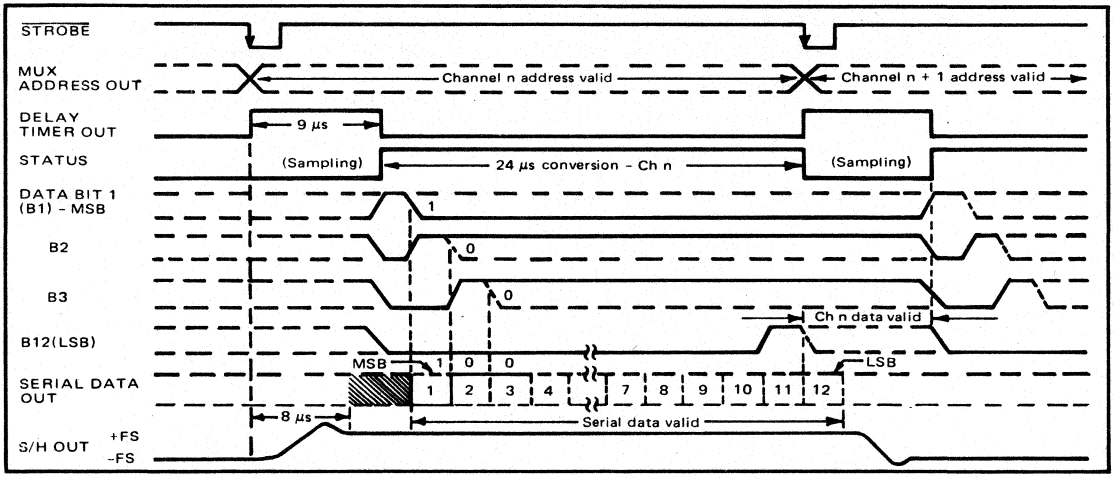


FIGURE 4. Timing Diagram for sequential addressing normal programming mode.

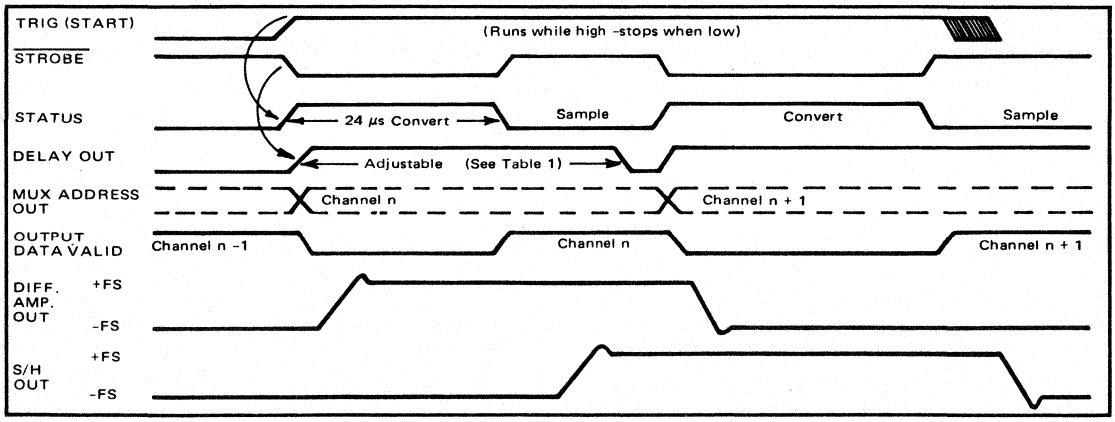
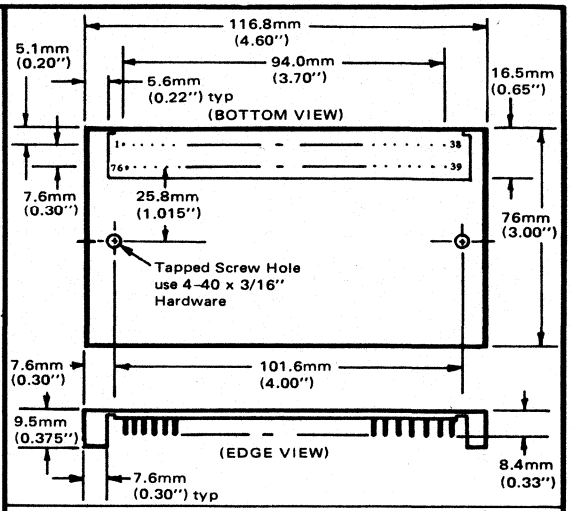


FIGURE 5. Timing Diagram for sequential overlap programming mode. (Delay must be adjusted to status pulse.)

PACKAGE AND PIN CONFIGURATION

SDM853 CONNECTOR PIN DIAGRAM

+15V	1	76	-15V
ANA. GND.	2	75	S/D ENB
CH 0 IN	3	74	CH 8 IN (0 RTN)
CH 1 IN	4	73	CH 9 IN (1 RTN)
CH 2 IN	5	72	CH 10 IN (2 RTN)
CH 3 IN	6	71	CH 11 IN (3 RTN)
CH 4 IN	7	70	CH 12 IN (4 RTN)
CH 5 IN	8	69	CH 13 IN (5 RTN)
CH 6 IN	9	68	CH 14 IN (6 RTN)
CH 7 IN	10	67	CH 15 IN (7 RTN)
MUX OUT HI	11	66	MUX OUT LO
$\overline{\text{LOAD ENB}}$	12	65	$\overline{\text{CLR ENB}}$
COUNT ENB	13	64	MUX ENB
A8 OUT	14	63	A8 IN
A4 OUT	15	62	A4 IN
A2 OUT	16	61	A2 IN
A1 OUT	17	60	A1 IN
$\overline{\text{DLY.}}$	18	59	DLY.
STROBE	19	58	$\overline{\text{STROBE}}$
ADC TRIG	20	57	ADC $\overline{\text{TRIG}}$
DLY. ADJ. 1	21	56	DLY. ADJ. 2
R1	22	55	R2
NEG REF OUT	23	54	BPO
POS. REF OUT	24	53	COMP IN
AMP IN HI	25	52	GAIN ADJ.
G2	26	51	S/H IN
G1	27	50	S/H OUT
AMP IN LO	28	49	SHT. CYC.
AMP OUT	29	48	S/H CONTROL
STATUS	30	47	$\overline{\text{B1}}$
B1 MSB	31	46	B2
B3	32	45	B4
B5	33	44	B6
B7	34	43	B8
B9	35	42	B10
B11	36	41	B12 LSB
SER OUT	37	40	CLK. OUT
+5	38	39	DIG RTN



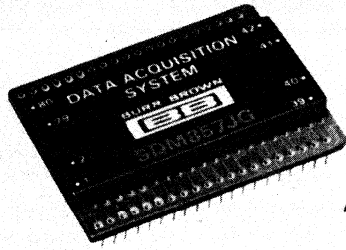
CASE MATERIAL: Insulated Steel
CONNECTOR PINS: Gold Flashed
WEIGHT: 145 grams (5 oz.)

MOUNTING INSTRUCTIONS:

MOUNTING FLUSH ON PC CARD

1. Use strip connectors or two 14 pin and three 16 pin low profile IC sockets (shipped with each unit).
2. Use 4-40 x 3/16" (4.8mm) LG Pan HD Hardware to secure the SDM853 to PC Card.

BURR-BROWN



SDM856
SDM857

ADVANCE INFORMATION
Subject to Change

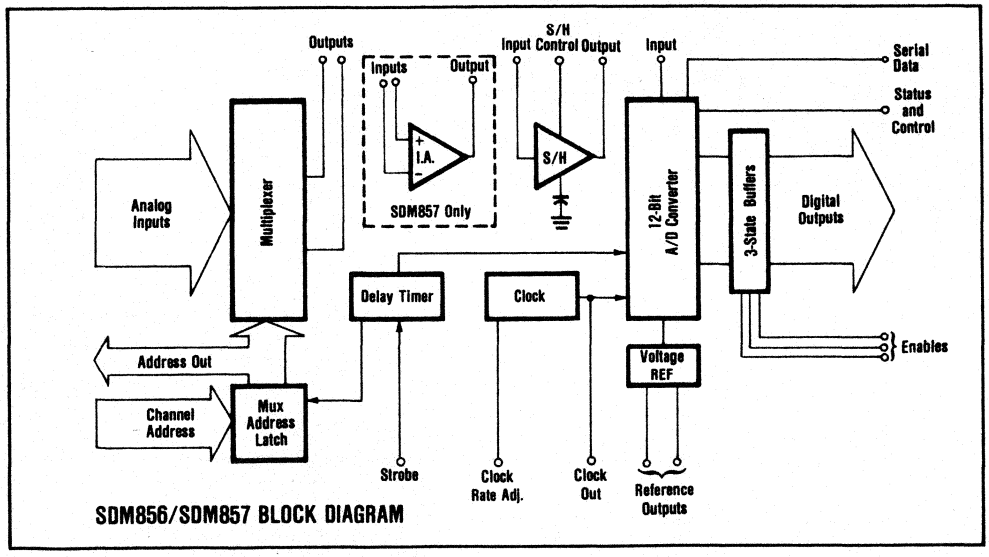
HYBRID DATA ACQUISITION SYSTEM

FEATURES

- MINIATURE SIZE
- LOW COST
- 12-BIT, 0.024% ACCURACY
- INSTRUMENT AMP OPTION
- LOW LEVEL INPUTS (SDM857)
- SELECTABLE 16 SINGLE, 8 DIFFERENTIAL INPUTS
- THREE-STATE OUTPUT BUFFERS
- 60kHz THROUGHPUT RATE WITH 8-BIT ACCURACY

DESCRIPTION

The SDM856 and SDM857 are complete data acquisition systems contained in a miniature 2.2" x 1.7" x 0.22" (55 x 43 x 5.6mm) ceramic package. These systems offer all the functions available in large modular data acquisition systems and are available with an optional internal instrumentation amplifier (SDM857). Inputs as low as ±50mV can be accepted by the SDM857; thermocouples, strain gages, and other low level signal sensors don't require external signal conditioning. Both models are fully expandable from the basic 16 channel single-ended or 8 channel differential input capability. Digital resolution is 12 bits with accuracy of ±0.024% at a throughput rate of 25kHz (SDM856KG).



SDM856/SDM857 BLOCK DIAGRAM

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DISCUSSION OF PERFORMANCE

INTRODUCTION

SDM857 contains all components necessary to multiplex and convert analog signals as small as 0 to +50mV and as high as ±5V into equivalent digital outputs. Throughput sampling rates are from 18kHz (12 bit resolution) to 40kHz (8 bit resolution). A complete low drift instrumentation amplifier allows selection of gains from 2 to 1000 with one external resistor. SDM856 is identical to SDM857, but does not include the instrumentation amplifier. This provides the option of adding an external instrumentation amplifier for specific requirements such as high speed, digital programming, etc. Throughput sampling rates as high as 60kHz (8 bit resolution) can be obtained with the SDM856. Both models can be configured to accept either 8 channel differential or 16 channel single-ended signals and can be expanded almost without limit with external multiplexers. Three-state outputs are provided for easy interface to microprocessor systems. Figure 1 illustrates all system components.

ANALOG MULTIPLEXER

The analog multiplexer consists of two CMOS integrated circuits. Pin interconnects are used to select 16 channel single-ended or 8 channel differential operation. In single-ended operation the multiplexer can be used in a pseudo-differential mode by connecting the amplifier inverting input to common remote signal ground. Channel selection is made by an internally latched 3 or 4 bit binary word, for differential or single-ended operation respectively.

INSTRUMENTATION AMPLIFIER (SDM857 only)

Offering low drift and high accuracy, the internal instrumentation amplifier may be programmed by a single external resistor for gains from 2 to 1000. With gain programming pins open, the gain is two.

SAMPLE AND HOLD

A complete stand alone circuit, the sample and hold amplifier features buffered output, 10μsec acquisition time, and 100nsec aperture time.

Input, output, and mode control lines are brought out to separate pins. This allows maximum system flexibility for performing functions, such as automatic gain ranging, with no loss of aperture time.

ANALOG TO DIGITAL CONVERTER

The ADC is a 12-bit, 25μsec converter with 0.01% linearity error. Its features include positive and negative reference voltage outputs, external gain and offset adjustments, straight binary or two's complement output, serial data and clock outputs, status output, a short cycle feature, and a clock rate control for higher throughput rates at lower resolution.

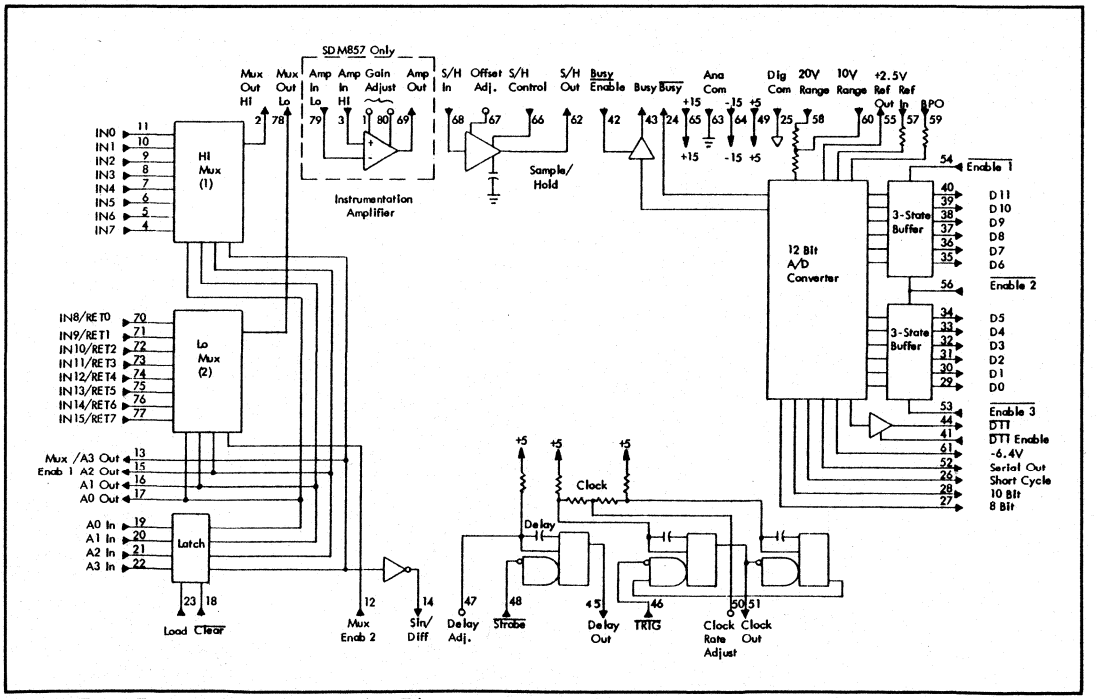


FIGURE 1. SDM856/SDM857 Function Diagram.

DISCUSSION OF PERFORMANCE (CONTINUED)

THREE-STATE OUTPUT BUFFERS

Digital outputs of the ADC are internally buffered by LSTTL three-state buffers. Three separate enable lines are brought out for easy interfacing to 4, 8 or 16 bit data buses. $\overline{D11}$ ($\overline{MSB}$) and BUSY are also buffered by separate three-state devices, each with its own enable line.

ADDRESS LATCH

Outputs of the 4-bit TTL register latch are connected to the address inputs of the multiplexer. This latch serves as an address storage register for the selected analog input. It may be loaded through 4 address inputs. Other inputs are LOAD and $\overline{CLEAR}$. The 3 least significant bits are used for 8 channel differential mode addressing.

DELAY TIMER

A delay timer allows settling time for the multiplexer, amplifier and sample/hold circuits before conversion begins. The delay is adjustable over a wide range by use of an external resistor or capacitor. This allows for longer settling time of the instrumentation amplifier when operating at high gains, or shorter settling time for lower resolution operation.

CHANNEL EXPANSION

The number of analog input channels of the SDM856 and SDM857 can be easily increased by using Burr-Brown's MPC8D (8 channel differential) and MPC16S (16 channel single-ended) multiplexers. These are latch-free devices which contain internal binary decoding at TTL or MOS levels and may be integrated into a system with minimal external logic.

SYSTEM PERFORMANCE

SDM856 and SDM857 are configured for random channel selection. With the addition of an external counter they can be configured to a) continuously sequence through all analog channels or b) sequence through all analog channels on command from an external trigger.

With the appropriate 4-bit (single-ended) or 3-bit (differential) channel address on the latch inputs, and DELAY OUT, pin 45, tied to the LOAD input, pin 23, a negative going edge is applied to the $\overline{STROBE}$ input, pin 48. This starts the delay timer, latches the multiplexer address, and allows the input signal to pass through the multiplexer, instrumentation amplifier and sample/hold and settle to its final value before starting the A/D conversion. The DELAY OUT signal (pin 45) is also connected to the $\overline{TRIG}$ input (pin 46) and the A/D conversion is initiated on the negative-going edge. The S/H CONTROL input (pin 66) is connected to $\overline{BUSY}$ (pin 24) so that the sample/hold is in the HOLD mode during the A/D conversion.

By using overlap programming the settling time effects of the analog multiplexer and instrumentation amplifier can be reduced, extending throughput sampling rates up to 29kHz for 12-bit and 67kHz for 8-bit resolution (ADC short-cycled). This mode of operation is most useful when converting low level inputs to accommodate the increased settling time of the instrumentation amplifier. Overlap programming is accomplished by connecting $\overline{BUSY}$ to $\overline{STROBE}$ and S/H CONTROL and DELAY OUT to LOAD and $\overline{TRIG}$. In this mode of operation the address of the next channel to be converted is latched and the output of the instrumentation amplifier allowed to settle to a new value during the present conversion.

SYSTEM TIMING DIAGRAMS

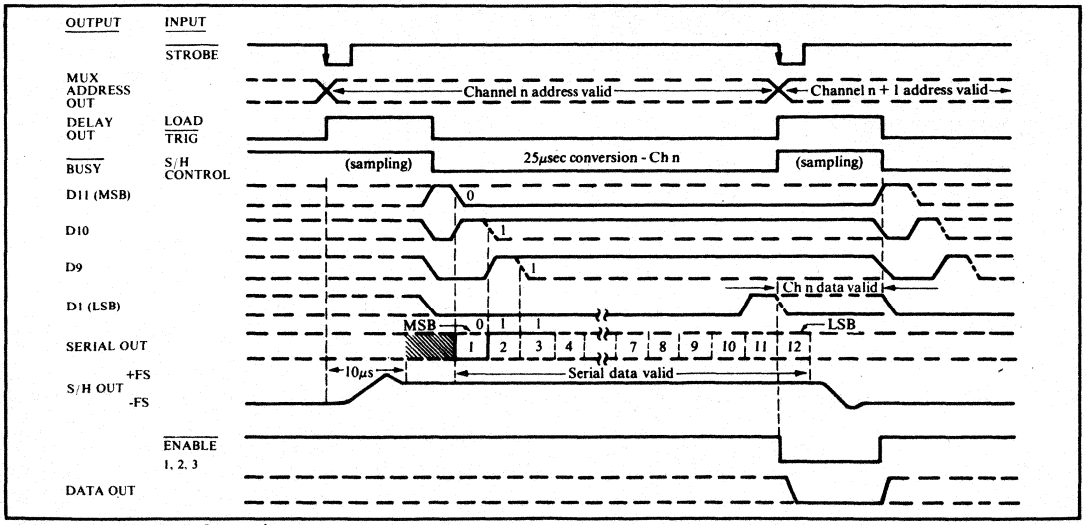


FIGURE 2. Normal Operation

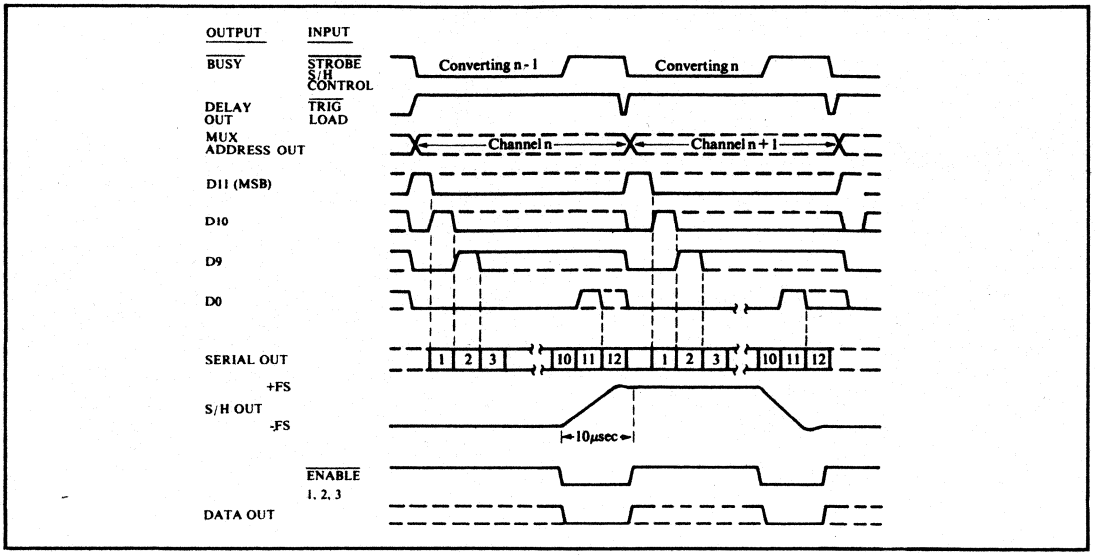


FIGURE 3. Overlap Operation

ELECTRICAL SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	SDM856/SDM857			
TRANSFER CHARACTERISTICS	MIN	TYP	MAX	UNITS
Resolution	12			Bits
Number of Channels	16 single-ended/8 differential			
Throughput Rate				
SDM856JG	25			kHz
SDM856KG	25			kHz
SDM857JG	18			kHz
SDM857KG	18			kHz
ANALOG INPUTS				
ADC Gain Ranges		0 to +5, ±5, ±10		V
Input Voltage Range				
Absolute max without damage			±20	V
For linear operation			±6	V
Input Impedance, OFF Channel		5 x 10⁹‖10		Ω‖pF
Input Impedance, ON Channel		5 x 10⁹‖100		Ω‖pF
Amplifier Characteristics (SDM857 only)				
Gain Range	2		1000	
Gain Equation		G = 2 + 20kΩ/R_{ext}[1]		
Input Bias Current at +25°C			±50	nA
0 to +70°C		±1.1		nA/°C
Offset Current at +25°C			±20	nA
0 to +70°C		±0.6		nA/°C
Input Offset Voltage		±0.1		mV
Input Offset Voltage Drift (G > 100)		±4		μV/°C
Output Noise (10Hz - 10kHz)				
G = 100, R_S = 500Ω		400		μVrms
Common-mode Rejection (DC) G = 2		90		dB
G = 1000		97		dB
Sample/Hold DC Characteristics				
Input Impedance		10^{10}		Ω
Bias Current		50		nA
Output Offset Voltage		7		mV
REFERENCE VOLTAGES				
Positive Output	+2.490	+2.500	+2.510	V
Positive Output Drift		±5		ppm/°C
Negative Output	-6.0	-6.4	-6.8	V
Negative Output Drift		±5		ppm/°C
ACCURACY				
Throughput Accuracy				
0 to +5V, ±5V ranges JG			±0.048	% of FSR[2]
0 to +5V, ±5V ranges KG			±0.024	% of FSR
0 to +50mV, ±50mV JG (SDM857 only)			±0.11	% of FSR
0 to +50mV, ±50mV KG (SDM857 only)			±0.08	% of FSR
Linearity (G = 1)				
JG			±0.024	% of FSR
KG			±0.012	% of FSR
Differential Linearity (G = 1)				
JG		±0.024		% of FSR
KG		±0.012		% of FSR
Quantizing Error			±0.012	% of FSR
System Gain Error[3]		±0.1		%
System Offset Error[3]		±0.1		% of FSR
Power Supply Sensitivity +15V		±0.0007		%/%ΔV
Power Supply Sensitivity -15V		±0.0007		%/%ΔV
Power Supply Sensitivity +5V		±0.001		%/%ΔV
TEMPERATURE STABILITY				
System Accuracy Drift[4] Unipolar			±25	ppm/°C
System Accuracy Drift[4] Bipolar			±20	ppm/°C
Linearity Drift			±2	ppm of FSR/°C
DYNAMIC ACCURACY				
Sample/Hold Characteristics				
Aperture Time		100		nsec
Feedthrough (10V step)		±1.4		mV
Amplifier CMRR at 60Hz G = 2		90		dB
Amplifier CMRR at 60Hz G = 1000		95		dB
Amplifier Overload Recovery Time		200		μs
OUTPUTS				
Digital Output Coding		Binary, Offset Binary, Two's Complement		
Serial Output Coding		Non-return to zero (NRZ)		
ADC Conversion Time[5]		25	30	μsec
Clock Frequency[5]		520		kHz
Delay[6] SDM856		15		μsec
Delay[6] SDM857		30		μsec
POWER REQUIREMENTS				
Rated Voltage for Specified Accuracy	±14.5, +4.75	±15, +5	+15.5, +5.25	V
Quiescent Current				
SDM856 +15		+10		mA
SDM856 -15		-35		mA
SDM856 +5		+120		mA
SDM857 +15		+15		mA
SDM857 -15		-40		mA
SDM857 +5		+120		mA
Power Dissipation SDM856		1300		mW
Power Dissipation SDM857		1400		mW
ENVIRONMENTAL				
Specification Temperature Range	0		+70	°C
Storage Temperature Range	-25		+85	°C

TABLE I. Electrical Specifications

NOTES:
1. R_{EXT} is the external gain-setting resistor. (Connect between pins 1 and 80.)
2. FSR means Full Scale Range, e.g., FSR is 10V for ±5V range.
3. Adjustable to zero.
4. Includes gain, offset, and linearity drifts.
5. Conversion time and clock frequency can be externally adjusted between 13μsec (f = 1.0MHz) to 110μsec (f = 118kHz). (Conv. times are for 12-bit resolution.)
6. Can be externally adjusted from 3μsec to 300μsec.

DIGITAL INPUT SPECIFICATIONS

Address Inputs (A0 - A3)	One standard LSTTL load, positive true
Address Coding	4-bit binary
Load	One standard LSTTL load, positive true, address loaded on positive edge.
$\overline{\text{Clear}}$	One standard LSTTL load, negative true, low level clears latch.
$\overline{\text{Strobe}}$	One standard LSTTL load, high-to-low transition triggers the delay timer.
$\overline{\text{TRIG}}$	One standard LSTTL load, a negative going edge initiates the A/D conversion.
Short Cycle	One standard LSTTL load, logical 1 for 12-bit resolution connect to "8-bit" or "10-bit" for 8- or 10-bit resolution.
$\overline{\text{Enable 1}}$, $\overline{\text{Enable 2}}$, $\overline{\text{Enable 3}}$, $\overline{\text{D11 Enable}}$, $\overline{\text{Busy Enable}}$	One standard LSTTL load, a low level enables the 3-state output.
S/H Control	TTL compatible, 10μA maximum input current. Logic 0 = Hold mode, Logic 1 = Sample (track) mode.
Mux Enable 2	TTL compatible, 2μA input current, Logic 0 enables multiplexer 2 (channels 8-15).

DIGITAL OUTPUT SPECIFICATIONS

Parallel Data Outputs	5 standard TTL loads, positive true, 3-state.
Serial Output	2 standard TTL loads, positive true, NRZ, time serial data output beginning with D11 (see Timing Diagram).
$\overline{\text{D11}}$	5 standard TTL loads, positive true, 3-state.
$\overline{\text{Busy}}$	5 standard TTL loads, low during A/D conversion.
Busy	5 standard TTL loads, high during A/D conversion, 3-state
Clock Out	5 standard TTL loads, for synchronizing serial out data (see Timing Diagram).
Address Outputs (A0 - A3)	5 standard TTL loads, positive true
Delay Out	5 standard TTL loads, high during delay period, triggered by $\overline{\text{Strobe}}$ input.
Sin Diff	5 standard TTL loads, high while addressing channels 0-7, low while addressing channels 8-15.

TYPICAL PERFORMANCE CURVES

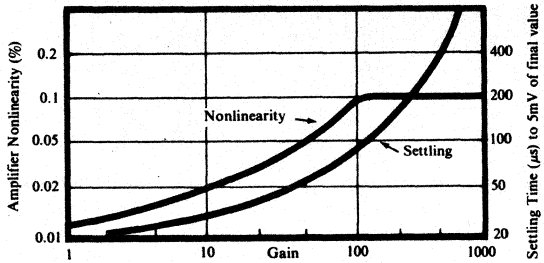


FIGURE 4. Nonlinearity and Settling Time vs. Amplifier Gain

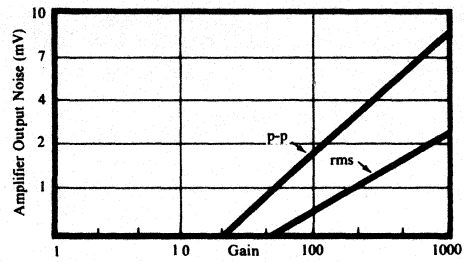


FIGURE 5. Output Noise vs. Amplifier Gain

THROUGHPUT ACCURACY AND TIMING RELATIONSHIPS

System Gain		System Accuracy		Throughput Rate (Channels/sec)		Delay Time (μsec)	
V/V		KG	JG	Normal	Overlap	Normal	Overlap
1	856 only	±0.024%	±0.048%	25k	29k	15	35
2	857 only	±0.024%	±0.048%	18k	29k	30	35
10	857 only	±0.035%	±0.06%	18k	29k	30	35
100	857 only	±0.08%	±0.11%	9k	11k	90	90
500	857 only	±0.1%	±0.15%	2.4k	2.6k	390	390

TABLE II. Throughput rate and delay time vs gain for normal and overlap modes.

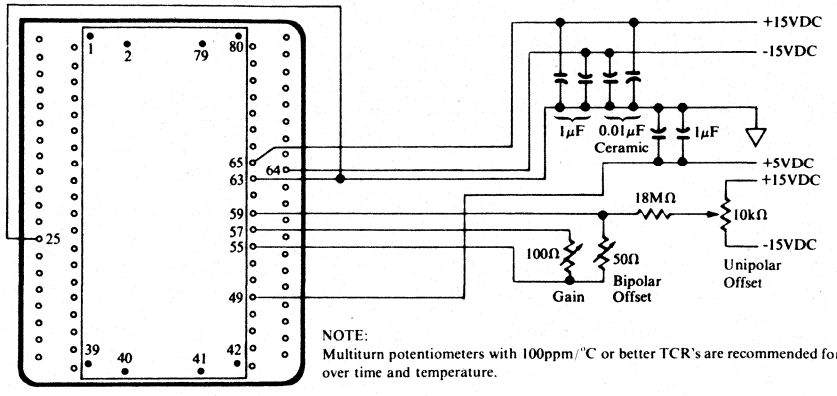
Full Scale Input Range	ADC Range	Amplifier Gain	Resolution	Amplifier/Multiplexer Settling Time (μsec)		
				To ±0.2%	To ±0.05%	To ±0.01%
10V	-10 to +10	2	2.44mV*	8	10	20
1V	0 to +10	10	244μV	12	14	24
0.1V	0 to +10	100	24.4μV	65	80	90
20mV	0 to +10	500	4.88μV*	320	390	450

TABLE III. This table shows the delay timer setting required to allow for the settling time of the instrumentation amplifier to the accuracies specified.

*Depends on desired S/N ratio.

In overlap, when the Amplifier/Multiplexer settling time is less than the ADC conversion time, set the delay timer for the ADC conversion time plus the sample and hold acquisition time (10μs). When the Amplifier/Multiplexer settling time exceeds the ADC conversion time plus the S/H acquisition time, set the delay timer for the Amplifier/Multiplexer settling time.

CONNECTION DIAGRAM



NOTE:
Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over time and temperature.

FIGURE 6. Connection Diagram for power supply decoupling and gain and offset adjustment.

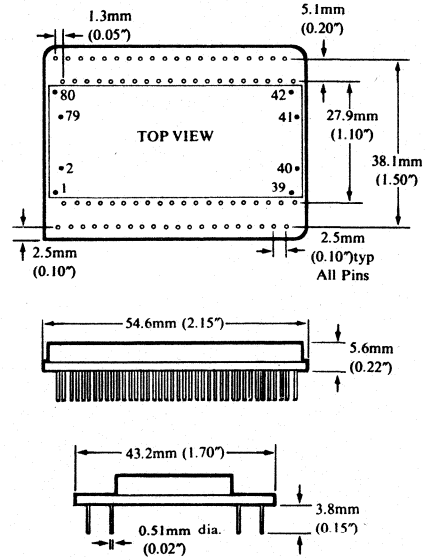
PACKAGE AND PIN CONFIGURATION

PIN CONNECTIONS

Pin		Pin	
*1	IA Gain Adjust	41	$\overline{\text{D11 Enable}}$
2	Mux Out High	42	Busy Enable
*3	Amp In High	43	Busy
4	CH7	44	$\overline{\text{D11}}$
5	CH6	45	Delay Out
6	CH5	46	$\overline{\text{TRIG}}$
7	CH4	47	Delay Adjust
8	CH3	48	$\overline{\text{Strobe}}$
9	CH2	49	+5V Supply
10	CH1	50	Clock Rate Adjust
11	CH0	51	Clock Out
12	Mux Enable 2	52	$\overline{\text{Serial Out}}$
13	A3 Out	53	$\overline{\text{Enable 3}}$
14	Single/Differential	54	$\overline{\text{Enable 1}}$
15	A2 Out	55	+2.5V Ref Out
16	A1 Out	56	$\overline{\text{Enable 2}}$
17	A0 Out	57	+2.5V Ref In
18	$\overline{\text{Clear}}$	58	20V Range
19	A0 In	59	BPO
20	A1 In	60	10V Range
21	A2 In	61	-6.4 Ref Out
22	A3 In	62	S/H Out
23	$\overline{\text{Load}}$	63	Analog Common
24	$\overline{\text{Busy}}$	64	-15V Supply
25	Dig. Common	65	+15V Supply
26	Short Cycle	66	S/H Control
27	10-bit Resolution	67	S/H Offset Adjust
28	8-bit Resolution	68	S/H Input
29	D0 (LSB)	*69	IA Out
30	D1	70	CH8/RET0
31	D2	71	CH9/RET1
32	D3	72	CH10/RET2
33	D4	73	CH11/RET3
34	D5	74	CH12/RET4
35	D6	75	CH13/RET5
36	D7	76	CH14/RET6
37	D8	77	CH15/RET7
38	D9	78	Mux Out Low
39	D10	*79	Amp In Low
40	D11 (MSB)	*80	IA Gain Adjust

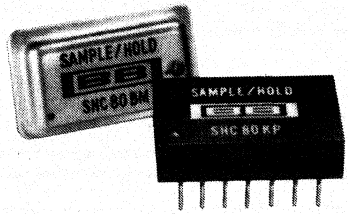
*For SDM857 only. Make no connection in SDM856.

MECHANICAL SPECIFICATIONS



MATERIAL: Alumina
WEIGHT: 32 grams (1.2 oz.)
PINS: Pin material and plating composition comform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
MATING CONNECTOR: 2350MC (Set of four 20 pin strips)

BURR-BROWN



SHC80

Fast IC SAMPLE/HOLD AMPLIFIERS

FEATURES

- 14-PIN DIP PACKAGE
- 10μsec ACQUISITION TIME
- COMPLETE WITH HOLDING CAPACITOR
- ±0.01% ACCURACY
- -25°C TO +85°C TEMPERATURE RANGE (SHC80BM)

DESCRIPTION

Ultra-linear performance and fast acquisition speeds - that's the combination that makes the SHC80 models ideal for your demanding data acquisition and control applications.

The SHC80 acquires and holds up to ±10V analog signals to an accuracy of ±0.01% of full scale. Acquisition time is 12μsec for a 20V step of 10μsec for a 10V step. High performance results from the use of internally compensated circuits normally found only in larger, more expensive sample/holds.

Two models give you a choice of operating temperature range: the SHC80KP (0°C to +70°C) in an epoxy package, also the SHC80BM (-25°C to +85°C) in a hermetic metal case. You'll find these units well suited for:

Data Acquisition Systems
Data Distribution Systems
Analog Delay Circuits
Pulse Amplitude Modulation Circuits
Waveform Amplitude Measurement

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-348 Printed in U.S.A. July, 1978

SPECIFICATIONS

Typical at 25°C with rated supply and 1000pF internal capacitor unless otherwise noted.

ELECTRICAL

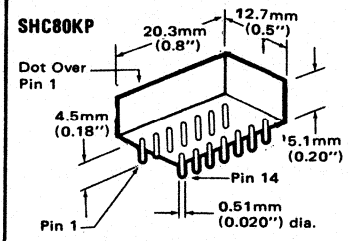
MODELS	SHC80KP	SHC80BM	Units
INPUT			
ANALOG INPUT			
Voltage Range	±10	±10	V
Maximum Safe Input Signal	±15	±15	V
Impedance	$10^8 \parallel 5$	$10^8 \parallel 5$	Ω/pF
Bias Current	400	400	nA
DIGITAL INPUT			
(TTL/MOS Compatible)	Voltage +5V	Voltage +15V	current
Mode Control	Logic Supply	Logic Supply	
"Sample" - Logic "1"	2 < e < 8V	5.5 < e < 15V	+50nA
"Hold" - Logic "0"	0 < e < 0.8V	0 < e < 3.5V	-50μA
TRANSFER CHARACTERISTICS			
ACCURACY (25°C)			
Dynamic Nonlinearity (max)	±0.01(3)	±0.01	% of 20V
@ min "Hold" time	1000	1000	μs
Gain	+1.0	+1.0	V/V
Gain Error	0.01	0.01	% of 20V
Throughput Offset (max) (adj. to zero)	2	2	mV
Droop Rate (max)	0.5	0.5	mV/mS
Droop Rate (typ)	0.2	0.2	mV/mS
Throughput Nonlinearity	±0.005	±0.005	% of 20V
Noise (RMS) (10Hz to 100kHz)	100	100	μV RMS
Supply Rejection (0 to 50kHz)	200	200	μV/V
ACCURACY DRIFT			
Gain Drift	2	2	ppm of 20V/°C
Offset Drift	20	20	μV/°C
Droop Rate(1)			
@ 70°C (max)	10	10	mV/mS
@ 85°C (max)	–	25	mV/mS
DYNAMIC CHARACTERISTICS			
Full Power Bandwidth(2)	75	75	kHz
Output Slew Rate	5	5	V/μs
Aperature Time	40	40	ns
Aperature Time Jitter	1	1	ns
Acquisition Time to 0.01%			
10V Step (max)	10	10	μs
20V Step (max)	12	12	μs
Feedthrough in Hold Mode	±0.02	±0.005	% of Input Step
Charge Offset (max)	2	2	mV
Sample to Hold Transient			
Peak Amplitude	150	150	mV
Settling to 1mV	1	1	μs
OUTPUT			
ANALOG OUTPUT			
Voltage Range (min)	±10	±10	V
Current Range (min)	±5	±5	mA
Impedance	0.5	0.5	Ω
TEMPERATURE			
Specification	0 to +70	-25 to +85	°C
Storage	-25 to +85	-55 to +125	°C
POWER SUPPLY			
Rated Voltage	±15	±15	V
Range	±14.5 to ±15.5	±14.5 to ±15.5	V
Current	±20	±20	mA
LOGIC SUPPLY			
Rated Voltage	+5	+5	V
Range	+4.75 to +15.5	+4.75 to +15.5	V
Current	1	1	mA

(1) May double every 10°C over temperature. (2) Small signal bandwidth 750kHz.

(3) ±0.015 including feedthrough for SHC80KP.

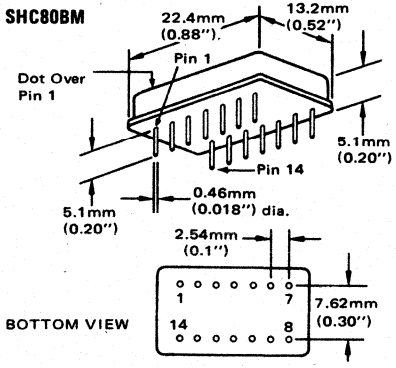
MECHANICAL

EPOXY PACKAGE



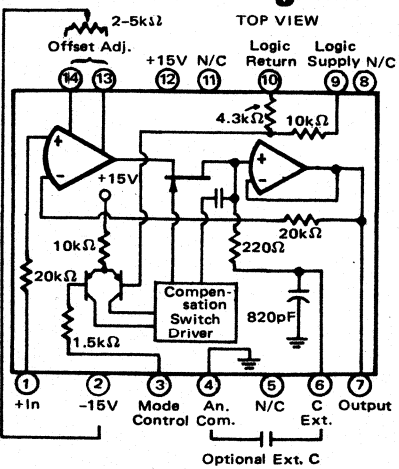
Pin Spacing: 2.54mm (0.1")
Row Spacing: 7.62mm (0.30")
Mating Connector: 145MC

METAL PACKAGE



Case: Kovar
Pin Material and plating Composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)

Connection Diagram



Note: No connection should be made to pins 11 & 5. Pin 8 is not internally connected.

DEFINITION OF SPECIFICATIONS

DYNAMIC NONLINEARITY

This is the total nonadjustable input-to-output error. It includes errors due to throughput nonlinearity, droop, thermal transients and feedthrough; in short, all errors that cannot be adjusted to zero for a 10 volt input change after a 10μsec acquisition time and a one millisecond hold time. Offset errors may be adjusted to zero by the offset control, but gain errors must be removed by a gain adjustment elsewhere in the system. (Gain adjust not included in SHC80.)

GAIN ACCURACY

The difference due to amplifier gain errors between INPUT and OUTPUT voltage when in the "sample" mode.

DROOP RATE

The voltage decay at the output during the "hold" mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH

The amount of input voltage change that appears at the output when the amplifier is in the "hold" mode.

THROUGHPUT – NONLINEARITY

The total charge offset and gain nonlinearity, i.e., the inaccuracy due to these two errors that cannot be corrected by gain and offset adjustments. Throughput – nonlinearity is specified over the 20 volt input range.

THROUGHPUT OFFSET

The sum of sample offset and charge offset.

CHARGE OFFSET

The offset that results from charge transferred from the holding capacitor to the gate capacitance of the switching FET. This charge is partially restored by a special compensation circuit when the unit goes into the "hold" mode.

ACQUISITION TIME

The time required for the output to settle to its final value within a given error band when the Mode control is switched from "hold" to "sample". See Figure 2.

APERTURE TIME

The time required to switch from "sample" to "hold". It is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

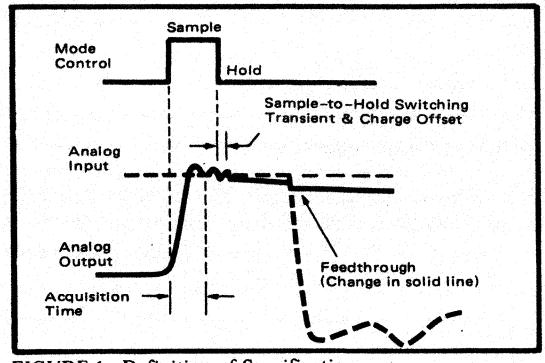


FIGURE 1. Definition of Specifications.

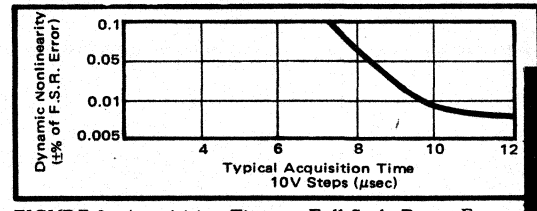


FIGURE 2. Acquisition Time vs. Full Scale Range Error.

OPERATING INSTRUCTIONS

OPTIONAL EXTERNAL CAPACITOR SELECTION

The value of the external capacitor determines the droop, charge offset, and acquisition time of the sample/hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table.

Figure 3 shows the behavior of acquisition time with added external capacitance. The behavior of droop with external C is determined by:

$$\text{Droop} = \frac{dv}{dt} = \left(\frac{0.5 \times 10^{-9}}{800\ \text{pF} + C_{ext\ \text{pF}}}\right) \frac{\text{mV}}{\text{mS}}$$

Capacitors with high insulation resistance and low dielectric absorption, such as teflon or polystyrene should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize leakage currents from the capacitor to minimize droop errors.

OFFSET ADJUSTMENT

Connect a 2k ohm to 5k ohm multi-turn potentiometer with a max TCR or 150 ppm/°C as shown in the Connection Diagram, and adjust the offset with the input grounded. During the adjustment, the sample/hold should be switching continuously between the "sample" and the "hold" mode. Adjust the error to zero when the unit is in the "hold" mode. This procedure insures that charge offset as well as amplifier offset error will be removed.

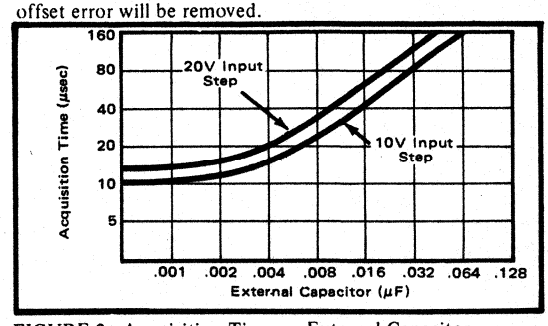


FIGURE 3. Acquisition Time vs. External Capacitor.

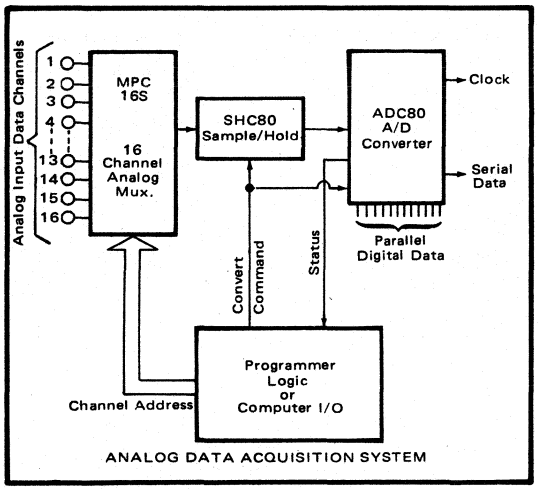
LOGIC THRESHOLD PROGRAMMING

Pin 10 is normally connected to the logic return and pin 9 to a positive logic supply. The logic threshold is determined by the 4.3kΩ and 10kΩ resistors shown in the connection diagram. The threshold is 1.5V for logic operated on a +5V supply and 4.5V for a +15V logic supply. If it is not convenient to connect a logic return and supply to the SHC80, pin 10 may be connected to the analog return and pin 9 to +15V for 15V logic or to +15V, through a 27kΩ resistor for 5V logic. The mode control switching transistors have sufficient current gain to allow the mode control pin to be driven from MOS logic. The mode control polarity may be reversed by connecting an externally-derived threshold voltage to pin 3 and by connecting pins 9 and 10 to the mode control source.

APPLICATIONS

DATA ACQUISITION SYSTEM

The SHC80 makes an excellent device for reducing aperture time and eliminating conversion noise from high gain circuitry in data acquisition systems. When it is combined with Burr-Brown's 16 channel MPC-16S Analog Multiplexer and ADC80 A/D Converter, you have a compact 16 channel data acquisition system with 25 kHz throughput sampling rates and ±0.02% (RSS) system accuracy.



ANALOG DATA ACQUISITION SYSTEM

SIMULTANEOUS SAMPLE/HOLD

Time correlation of sampled data signals may be implemented by using one sample/hold for each analog signal prior to input to an analog multiplexer. The SHC80's low aperture time of 40 nanoseconds practically eliminates channel-to-channel time slew. The throughput sampling rate and the number of data channels will determine the maximum "hold" time and hence, the worst case droop error of the sample/hold in the last channel to be sampled prior to the next "refresh" or sample/hold command. This droop error may be minimized by adding external capacitance to the SHC80 as shown in Figure 3.

The droop error is computed by:

MAX DROOP ERROR (CHANNEL N) = (T x n)(Droop rate)

Where $T = \frac{1}{\text{System Sampling Rate}}$ and

n = number of multiplexer data channels.

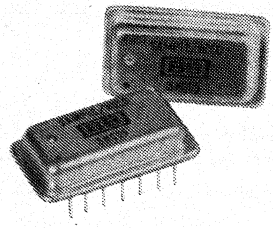
EXAMPLE:

For a 10 bit, 32 channel system with throughput sample rate of 25 kHz, assuming no external capacitance, the droop error of channel N is:

Droop Error $(E_D) = (\frac{1}{25k} \times 32)(500 \times 10^{-3}) = 640\mu V$.

For ±10 volt input signal range and 10-bit resolution, the resolution of ±½ LSB is ±9.77 mV. This droop error is less than 0.032 LSB (negligible), and no external C is needed to reduce the droop of the SHC80.

BURR-BROWN



SHC85
SHC85ET

Fast IC
SAMPLE/HOLD AMPLIFIERS

FEATURES

- 14-PIN DIP PACKAGE
- 5μsec ACQUISITION TIME
- COMPLETE WITH HOLDING CAPACITOR
- ±0.01% ACCURACY
- -55°C TO +125°C TEMPERATURE RANGE (SHC85ET)

DESCRIPTION

The SHC85 is designed to acquire and hold up to ±10VDC analog signals to an accuracy of ±0.01% of full scale range in 5μsec for a 20-volt step or 4.5μsec for a 10VDC step. Featuring internally compensated circuits normally found only in more expensive and larger sample/holds, the SHC85 offers ultra-liner performance and fast acquisition speeds for the most demanding data acquisition and control applications.

Two models are available: the SHC85 is specified for 0°C to 70°C operation, and the SHC85ET is specified for -55°C to +125°C operation.

The SHC85/SHC85ET are well suited for use in:

Data Acquisition Systems
Data Distribution Systems
Analog Delay Circuits
Pulse Amplitude Modulation Circuits
Waveform Amplitude Measurement

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PDS-321 Printed in U.S.A. July, 1978

SPECIFICATIONS

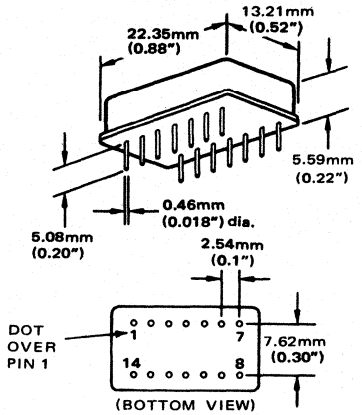
Typical at 25°C with rated supply and a 1000 pF internal capacitor unless otherwise noted.

ELECTRICAL

MODELS	SHC85	SHC85ET	UNITS
INPUT			
ANALOG INPUT			
Voltage Range	±10	±10	V
Maximum Safe Input Signal	±15	±15	V
Resistance	10^8	10^8	Ω
Bias Current	50	50	nA
DIGITAL INPUT (TTL Compatible)			
Mode Control	Voltage	Current	
"Sample" - Logic "1"	+2.0V < e < +8V	50 nA	
"Hold" - Logic "0"	0V < e < +0.8V	-50 μA	
TRANSFER CHARACTERISTICS			
ACCURACY (25°C)			
Dynamic Nonlinearity (max)	±0.01	±0.01	% of 20V
@ min. "Hold" Time	1000	1000	μs
Gain	+1.0	+1.0	V/V
Gain Error	±0.01	±0.01	% of 20V
Throughput Offset (max)(adj to zero)	2	2	mV
Droop Rate (max)	0.5	0.5	mV/ms
Droop Rate (typical)	0.125	0.125	mV/ms
Throughput Nonlinearity	±0.005	±0.005	% of 20V
Noise (rms) (10 Hz to 100 kHz)	100	100	μV
Supply Rejection (0 to 50 kHz)	100	100	μV/V
ACCURACY DRIFT			
Gain Drift	±2	±2	ppm of 20V/°C
Offset Drift	±25	±25	μV/°C
Droop Rate			
@ 70°C (max)	10	10	mV/ms
@ +125°C (max)	---	200	mV/ms
DYNAMIC CHARACTERISTICS			
Bandwidth (Full Power)(1)	200	200	kHz
Output Slew Rate	20	20	V/μs
Aperture Time	30	30	ns
Acquisition Time (to ±0.01%)			
10 V Step (max)	4.5	4.5	μs
20 V Step (max)	5.0	5.0	μs
Feedthrough in Hold Mode	±0.005	±0.005	% of step change
Charge Offset (max) @ 0V Input	±2	±2	mV
Sample-to-Hold Transient			
Peak Amplitude	50	50	mV
Settling to 1 mV	0.5	0.5	μs
OUTPUT			
ANALOG OUTPUT			
Voltage Range	±10	±10	V
Current Range	±10	±10	mA
Impedance	0.1	0.1	Ω
TEMPERATURE			
Specification	0 to +70	-55 to +125	°C
Storage	-55 to +125	-55 to +125	°C
POWER SUPPLY			
Rated Voltage	±15	±15	VDC
Range	±14.5 to ±15.5	±14.5 to ±15.5	VDC
Current	±13	±13	mA

(1) Small signal bandwidth is 3MHz.

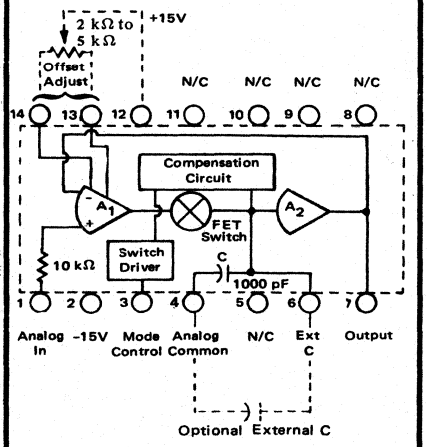
MECHANICAL



Case: Kovar
Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883, (except paragraph 3.2)

Mating Connector: 0145 MC

CONNECTION DIAGRAM



NOTE: Pins 5, 8, 9, 10 and 11 are not internally connected.

DEFINITION OF SPECIFICATIONS

DYNAMIC NONLINEARITY
This is the total nonadjustable input to output error. This specification includes throughput nonlinearity and errors due to droop, thermal transients and feedthrough, in short, all errors that cannot be adjusted to zero for a 10 volt input change after a 5 μsecond acquisition time and a one millisecond hold time. Offset errors must be adjusted to zero by the offset control and gain errors must be adjusted to zero by a gain adjustment elsewhere in the system (gain adjust not included in SHC85).

GAIN ACCURACY
The difference due to amplifier gain errors between INPUT and OUTPUT voltage when in the "sample" mode.

DROOP RATE
The voltage decay at the output when in the "hold" mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH
The amount of the input voltage change that appears at the output when the amplifier is in the "hold" mode.

THROUGHPUT - NONLINEARITY
The total charge offset and gain nonlinearity. That is, the inaccuracy due to these two errors that cannot be corrected by gain and offset adjustments. Throughput - nonlinearity is specified over the 20 volt input range.

THROUGHPUT OFFSET
The sum of sample offset and charge offset.

CHARGE OFFSET
The offset that results from charge transferred from the holding capacitor to the gate capacitance of the switching FET. This charge is partially restored by a special compensation circuit when the unit goes into the "hold" mode.

ACQUISITION TIME
The time required for the output to settle to its final value within a given error band, when the Mode control is switched from "hold" to "sample". See Figure 2.

APERTURE TIME
The time required to switch from "sample" to "hold". The time is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

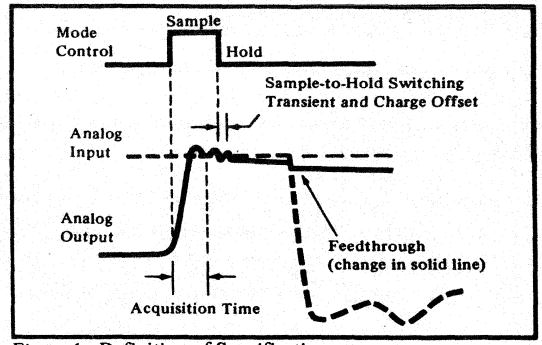


Figure 1. Definition of Specifications.

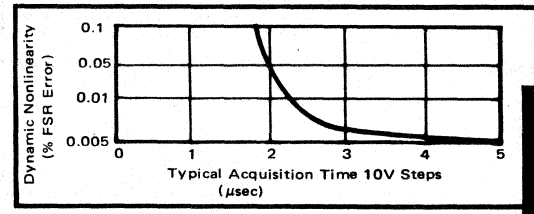


Figure 2. Acquisition Time vs. Full Scale Range Error.

OPERATING INSTRUCTIONS

OPTIONAL EXTERNAL CAPACITOR SELECTION
The value of the external capacitor determines the droop, charge offset and acquisition time of the sample/hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table.

Fig.3 shows the behavior of acquisition time with added external capacitance. The behavior of droop with external C is determined by:

$$\text{Droop} = \frac{dv}{dt} = \frac{0.5 \times 10^{-9}}{1000\ \text{pF} + C_{ext}}$$

Capacitors with high insulation resistance and low dielectric absorption, such as teflon or polystyrene should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize leakage currents from the capacitor; this will minimize droop errors.

OFFSET ADJUSTMENT
Connect a 2k to 5k ohm multi-turn potentiometer with a TCR of 150 ppm/°C or less as shown in the Connection Diagram. The offset should be adjusted with the input grounded. During the adjustment, the sample/hold should be switching continuously between the "sample" and the "hold" mode. The error should then be adjusted to zero where the unit is in the "hold" mode. In this way, charge offset as well as amplifier offset will be adjusted.

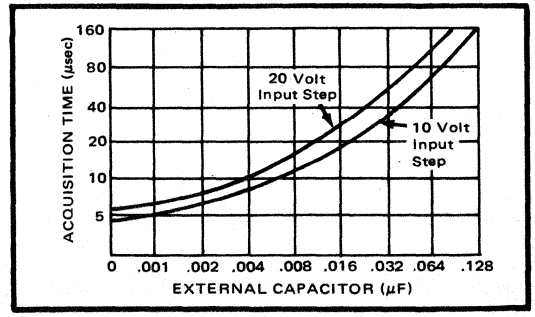
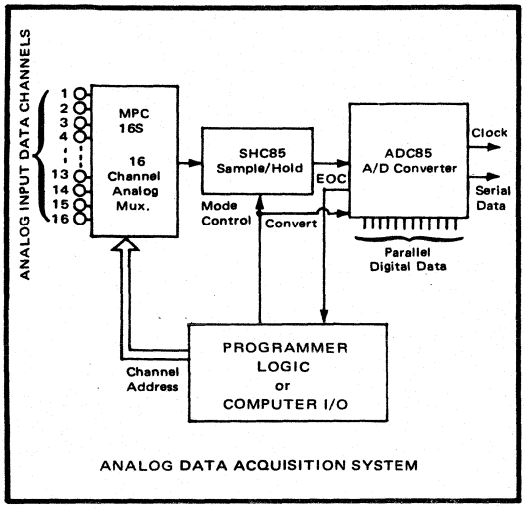


Figure 3. Acquisition Time vs. External Capacitor.

APPLICATIONS

DATA ACQUISITION SYSTEM

The SHC85 makes an excellent device for reducing aperture time in a data acquisition system. When combined with Burr-Brown's 16 channel MPC-16S Analog Multiplexer and ADC85 10 or 12 bit A/D Converter, you can have a compact 16 channel data acquisition system with 50 kHz to 65 kHz throughput sampling rates and 0.02 percent (RSS) system accuracy.



ANALOG DATA ACQUISITION SYSTEM

SIMULTANEOUS SAMPLE/HOLD

Time correlation of sampled data signals may be implemented by using one sample/hold for each analog signal prior to input to an analog multiplexer. The SHC85 low aperture time of 30 nanoseconds practically eliminates channel-to-channel time slew. The throughput sampling rate and the number of data channels will determine the maximum HOLD time and hence, the worst case droop error of the sample/hold in the last channel to be sampled prior to the next "refresh" or sample/hold command. This droop error may be minimized by adding external capacitance to the SHC85 as shown in Figure 3.

The droop error is computed by:

MAX DROOP ERROR (CHANNEL N)=(T x n)(Droop rate)

Where $T = \frac{1}{\text{System Sampling Rate}}$ and

n = number of multiplexer data channels

EXAMPLE:

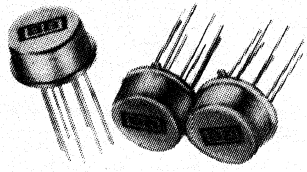
For a 10 bit, 32 channel system with throughput sample rate of 50 kHz, assuming no external capacitance, the droop error of channel N is:

$$\text{Droop Error}(E_D) = \left(\frac{1}{50k} \times 32\right)(500 \times 10^{-3}) = 320\ \mu V$$

For ±10 volt input signal range and 10 bit resolution, the resolution of ±½ LSB is ±9.77 mV. This droop error is less than 0.016 LSB (negligible), and no external C need be added to reduce the droop of the SHC85.

BURR-BROWN

SHC298AM



Low Cost Monolithic SAMPLE/HOLD AMPLIFIER

FEATURES

- 12-BIT THROUGHPUT ACCURACY
- LESS THAN 10μsec ACQUISITION TIME
- WIDEBAND NOISE LESS THAN 20μV, RMS
- RELIABLE MONOLITHIC CONSTRUCTION
- $10^{10}\,\Omega$ INPUT RESISTANCE
- TTL/PMOS/CMOS-COMPATIBLE LOGIC INPUT

DESCRIPTION

The SHC298AM is a high performance monolithic sample/hold circuit which features very high DC accuracy with fast acquisition times and a low droop rate. With the addition of one external holding capacitor, 12-bit accuracy can be achieved with a 6msec acquisition time. Droop rates less than 5mV/min can be achieved with a one microfarad holding capacitor.

The fully differential logic inputs have low input current, and are compatible with TTL, PMOS, and CMOS logic families. The input offset adjustment can be made using a single external potentiometer and resistor, and the adjustment does not degrade input offset drift.

The SHC298AM will operate with power supplies ranging from ±5DC to ±18VDC. It is available in a hermetically sealed 8 lead low profile package, and is specified for a temperature range from -25°C to +85°C. The SHC298AM is the best price/performance bargain in its class. It is well suited for use in data acquisition systems, data distribution systems, analog delay circuits, and pulse amplitude modulation circuits.

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PDS-373

Printed in U.S.A. July, 1978

SPECIFICATIONS

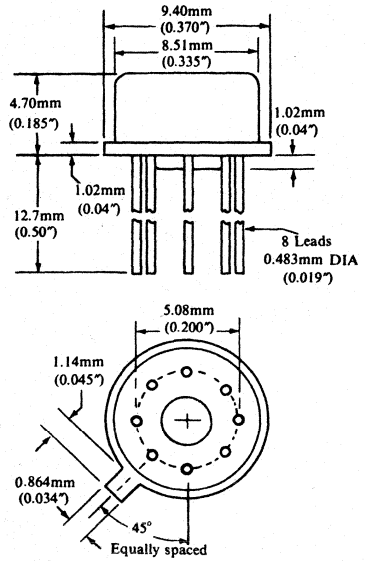
Specifications at T_A = +25°C with rated supplies with 1000 pF holding capacitor unless otherwise noted.

ELECTRICAL

MODELS	SHC298AM MIN	SHC298AM TYP	SHC298AM MAX	UNITS
INPUT				
ANALOG INPUT				
Voltage Range	±(V_{CC}-2.5)			Volts
Maximum Safe Input Signal		±V_{CC}		Volts
Resistance		10^{10}		Ohms
Bias Current		10	50	nA
DIGITAL INPUT	Pin 7	Pin 8	Circuit State	
Mode Control Truth Table	0V	+2.4V	Sample (Track)	
	0V	+0.8V	Hold	
	+2.4V	+2.8V	Hold	
	+0.8V	+2.8V	Sample (Track)	
Mode Control and Mode Control Reference Input Current			10	µA
Differential Logic Threshold		1.4		Volts
TRANSFER CHARACTERISTICS				
ACCURACY (25°)				
Throughput Nonlinearity for Hold Time < 1ms		±0.010	±0.015	% of 20V
Gain		+1.0		V/V
Gain Error		±0.004	±0.010	%
Input Voltage Offset (adj to zero)		±2	±7	mV
Droop Rate		±25	±125	µV/ms
Charge Offset		±15	±25	mV
Noise (rms) 10 Hz to 100 kHz		10	20	µV
Power Supply Rejection		±25	±50	µV/V
ACCURACY DRIFT				
Gain Drift		3	4	ppm/°C
Input Offset Drift		15	45	µV/°C
Charge Offset Drift C = 1000 pF		50	150	µV/°C
C = 10,000 pF		20	50	µV/°C
Droop Rate at T_A = +85°C		1	10	mV/ms
DYNAMIC CHARACTERISTICS				
Full Power Bandwidth, C = 1000 pF	75	125		kHz
C = 10,000 pF	10	16		kHz
Output Slew Rate, C = 1000 pF	7	10		V/µs
C = 10,000 pF	1.4	2		V/µs
Aperture Time				
Negative Input Step		125	200	ns
Positive Input Step		30	45	ns
Acquisition Time (C = 1000 pF)				
to ±0.01%, 10V step		6	10	µs
to ±0.01%, 20V step		8	12	µs
to ± 0.1%, 10V step		5	9	µs
to ±0.1%, 20V step		7	11	µs
Sample-to-Hold Transient				
Peak Amplitude		160		mV
Settling to 1 mV		1.0	1.5	µs
Feedthrough (Response to 10V Input Step)		±0.007	±0.015	% of 20V
OUTPUT				
ANALOG OUTPUT				
Voltage Range	±(V_{cc}-2.5)			Volts
Current Range	±2			mA
Impedance		0.5	4	Ohms
TEMPERATURE				
Specification		-25 to +85		°C
Operating		-55 to +125		°C
Storage		-55 to +150		°C
POWER SUPPLY				
Rated Voltage		±15		VDC
Range[1]	±4.75		±18	VDC
Current		±4.5	±6.5	mA

(1) Logic voltage on pin 8 should not exceed V_{cc} - 1 volt.

MECHANICAL

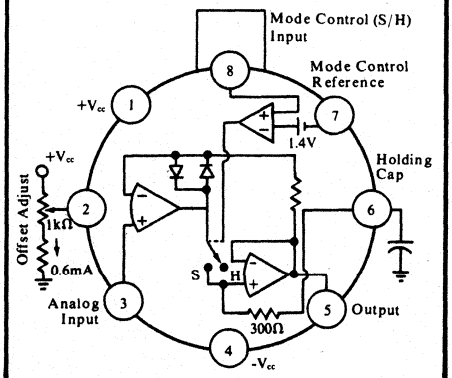


Pin Material and Plating Composition: Conforms to Mil-Std-883 Method 2003 (solderability)

Hermeticity: Conforms to Mil-Std-883, method 1014, Condition C, Step 1, Fluorocarbon (gross leak) and method 1014, Condition A, Heluim, 5 x 10^{-8} cc/sec (fine leak)

Connector: None

PIN CONFIGURATION



(TOP VIEW)

TYPICAL PERFORMANCE CURVES

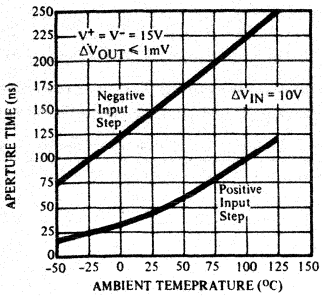


FIGURE 1. Aperture Time

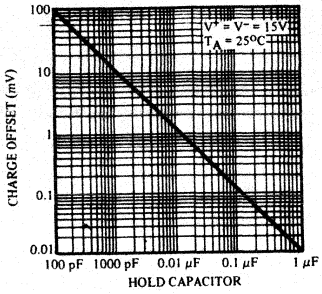


FIGURE 2. Charge Offset

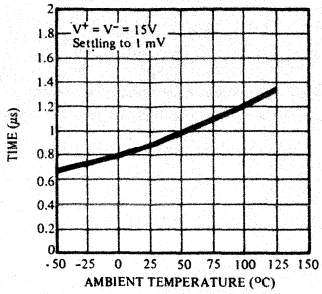


FIGURE 3. Sample-to-Hold Transient Settling Time

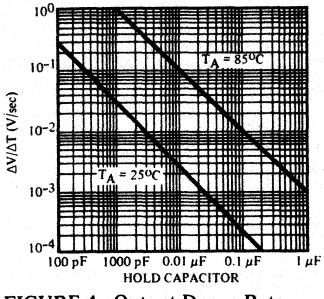


FIGURE 4. Output Droop Rate

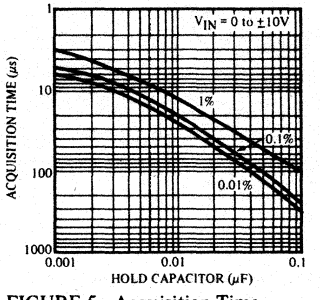


FIGURE 5. Acquisition Time

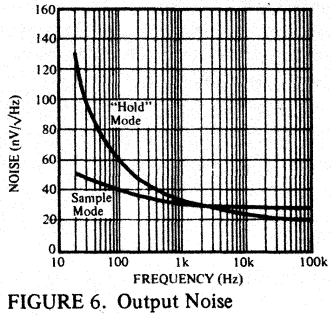


FIGURE 6. Output Noise

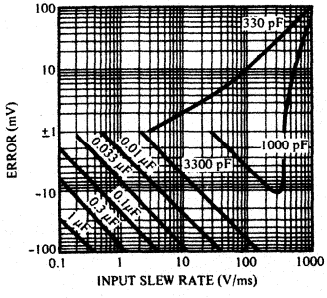


FIGURE 7. Dynamic Sampling Error

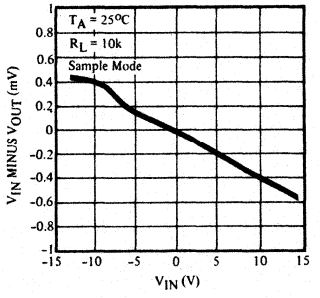


FIGURE 8. Gain Error

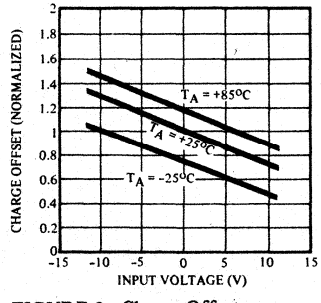


FIGURE 9. Charge Offset

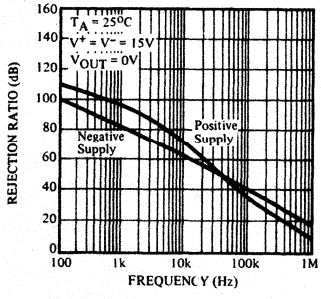


FIGURE 10. Power Supply Rejection

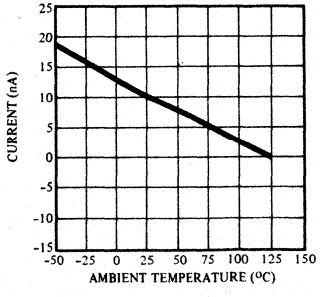


FIGURE 11. Input Bias Current

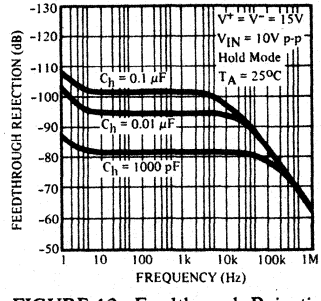


FIGURE 12. Feedthrough Rejection (Hold Mode)

DISCUSSION OF SPECIFICATIONS

THROUGHPUT-NONLINEARITY is defined as total Hold mode, non-adjustable, input to output error caused by charge offset, gain non-linearity, one millisecond of droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by offset and gain adjustments. Throughput nonlinearity is tested with a 1000 pF holding capacitor, 10 volt input changes, 10μsec acquisition time, and one millisecond Hold time.

GAIN ACCURACY is the difference between INPUT and OUTPUT voltage (when in the Sample mode) due to amplifier gain errors.

DROOP RATE is the voltage decay at the output when in the Hold mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH is the amount of the input voltage change that appears at the output when the amplifier is in the Hold mode.

APERTURE TIME is the time required to switch from Sample to Hold. The time is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

ACQUISITION TIME is the time required for the Sample and Hold output to settle within a given error band of its final value when the mode control is switched from Hold to Sample.

CHARGE OFFSET is the offset that results from the charge coupled through the gate capacitance of the switching FET. This charge is coupled into the storage capacitor when the FET is switched to the "hold" mode.

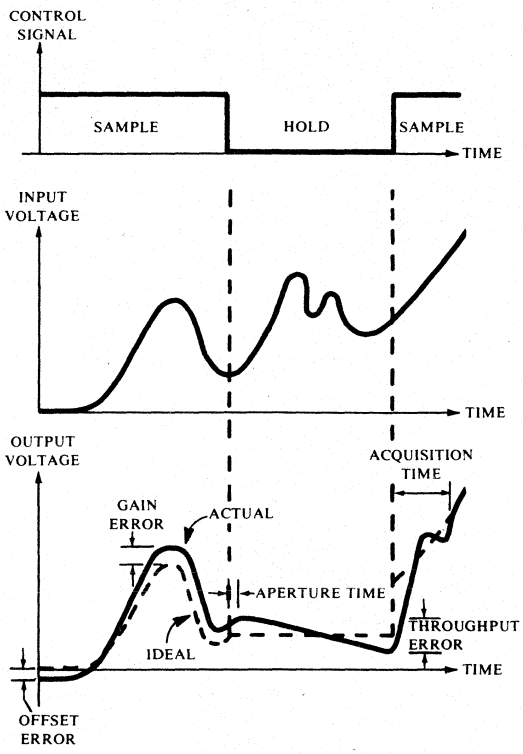


FIGURE 13. Sample-Hold Errors

OPERATING INSTRUCTIONS

EXTERNAL CAPACITOR SELECTION

Capacitors with high insulation resistance and low dielectric absorption, such as teflon, polystyrene or polypropylene units, should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize AC and DC leakage currents from the capacitor to reduce charge offset and droop errors.

The value of the external capacitor determines the droop, charge offset and acquisition time of the Sample/Hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table for a 0.001μF capacitor. With a capacitor of 0.01μF the droop will reduce to approximately 2.5μV/ms and the charge offset to approximately 1.5mV. Figure 5 shows the behavior of acquisition time with changes in external capacitance.

OFFSET ADJUSTMENT

The offset should be adjusted with the input grounded. During the adjustment, the Sample/Hold should be switching continuously between the Sample and the Hold mode. The error should then be adjusted to zero when the unit is in the Hold mode. In this way, charge offset as well as amplifier offset will be adjusted. When a 0.001μF capacitor is used, it will not be possible to adjust the full offset error at the Sample Hold. It should be adjusted elsewhere in the system.

APPLICATIONS

DATA ACQUISITION

The SHC298AM may be used to hold data for conversion with an analog to digital converter or used to provide Pulse Amplitude Modulation (PAM) data output.

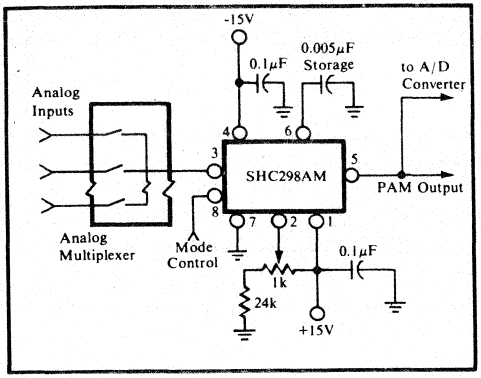


FIGURE 14. Data Acquisition

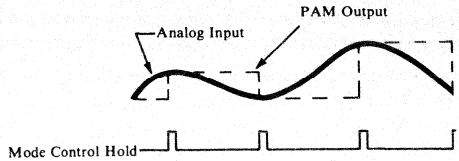


FIGURE 15. PAM Output

DATA DISTRIBUTION

The SHC298AM may be used to hold the output of a digital to analog converter whose digital inputs are multiplexed.

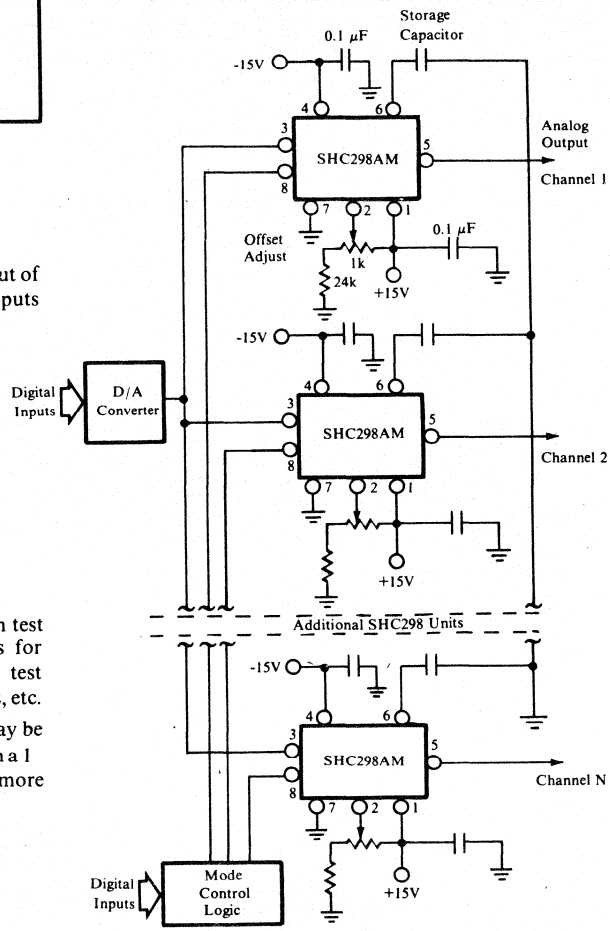


FIGURE 16. Data Distribution

TEST SYSTEMS

The SHC298AM is also well suited for use in test systems to acquire and hold data transients for human operators or for other parts of the test system such as comparators, digital voltmeters, etc.

With a 0.1 μF storage capacitor, the output may be held 10 seconds with less than 0.1% error. With a 1 μF storage capacitor, the output may be held more than 15 minutes with less than 1% error.

HIGH SPEED DATA ACQUISITION

The minimum sample time for one channel in a data acquisition system is usually considered to be the acquisition time of the Sample and Hold plus the conversion time of the analog to digital converter. If two or more Sample and Holds are used with a high speed multiplexer, the acquisition time of the Sample and Hold can be virtually eliminated. While the first channel is in hold and switched on to the ADC, the multiplexer may be addressed to the next channel. The second Sample and Hold will have acquired this data by the time the conversion is complete. Then, the Sample and Holds reverse roles and another channel is addressed. For low level systems, an instrumentation amplifier and double-ended multiplexer may be connected to the Sample and Hold inputs. The settling time of the multiplexer, instrumentation amplifier, and Sample and Hold can be eliminated from the channel conversion time as before.

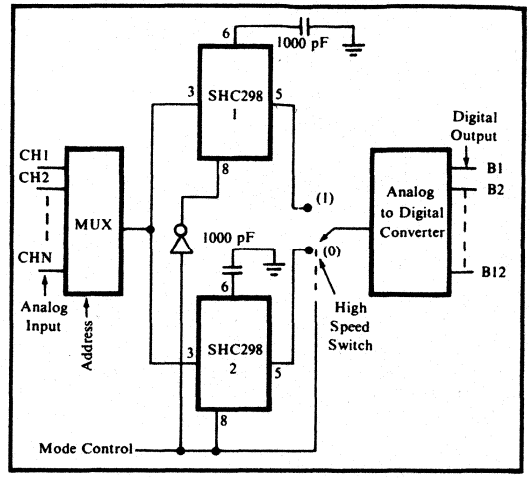
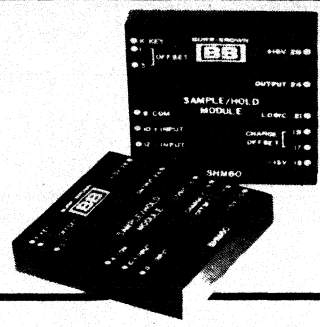


FIGURE 17. "Ping-Pong" Sample/Holds

BURR-BROWN

SHM60



High Speed SAMPLE/HOLD

FEATURES

- 1μsec ACQUISITION
- .01% ACCURACY
- SELECTABLE GAINS - ±1 to ±1000
- 12nsec APERTURE TIME
- LOW FEEDTHROUGH - 0.005%

DESCRIPTION

Designed for use with fast A/D and D/A converters and analog multiplexers, the Burr-Brown Model SHM60 high-speed sample/hold acquires analog signals of up to ±10V amplitude and settles to 0.01% in less than 1.5μsec for a 20V input step, and in less than 1μsec for a 10V input step. Both analog input terminals are available for user selection of gains from unity to 1000.

Internal compensation of charge storage effects and dielectric absorption are provided to assure accurate and fast operation. The SHM60 dynamic nonlinearity of 0.01% is specified for hold periods of up to 15μsec to simplify the user's task of computing system throughput error for specific operating conditions.

The 2" x 2" x 0.4" encapsulated modular package operates from ±15VDC power and is compatible with Burr-Brown's line of fast A/D and D/A converters such as Models ADC85 and ADC80 and ADC84 A/D converters, and DAC85, DAC80 and DAC85 D/A converters.

A few of the more popular applications for the SHM60 are:

A/D converter aperture error reduction
Time correlation of sampled signals
i.e., simultaneous sample/hold
Multiplexing D/A converter outputs
Generation of pulse-amplitude-modulation (PAM) telemetry signals
Analog memory for analog computations

... and many more.

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PDS-310A

Printed in U.S.A. July, 1978

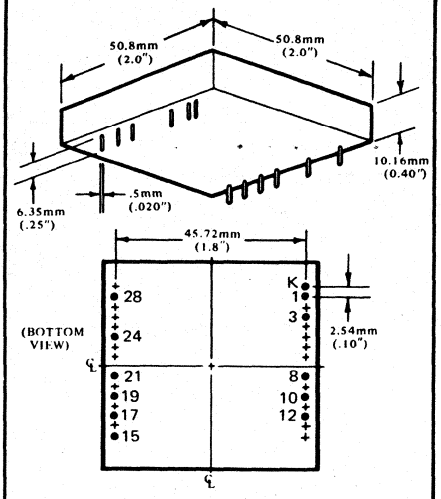
SPECIFICATIONS

Typical at 25°C and rated supplies unless otherwise noted.

ELECTRICAL

MODEL	SHM60			
	Min	Typ	Max	Units
INPUT				
ANALOG INPUT				
Signal Voltage	-10		+10	V
Maximum Safe Input[1]	-15		+15	V
Impedance		10^{11}		Ω
Bias Current		50		pA
DIGITAL INPUT (Mode Control)[2]				
Sample Mode (Logic 1)				
at 100 μA Source	+2.4		+5.0	V
Hold Mode (Logic 0)				
at 50 nA Sink	0.0		+0.8	V
Rise Time for Specified Performance			5	nsec
INPUT POWER				
+15V Supply Voltage Range	+14.55	+15	+15.45	Vdc
-15V Supply Voltage Range	-14.55	-15	-15.45	Vdc
Quiescent Current				
+15V Supply - Sample Mode		25		mA
- Hold Mode		17		mA
-15V Supply - Sample Mode		15		mA
- Hold Mold		15		mA
TRANSFER CHARACTERISTICS				
ACCURACY at Gain of 1 V/V[3]		±0.005	±0.01	% of 20V
Dynamic Nonlinearity[4]		±0.005	±0.01	% of 20V
Gain Error		3		mV
Throughput Offset (Adj. to Zero)[5]		1	5	μV/μsec
Droop Rate		±0.005		% of ΔV
Dielectric Absorption[4]		100		μV rms
Noise				V/V
Common Mode Rejection Ratio	10^{-4}			ppm/%
Power Supply Rejection		10	30	
ACCURACY DRIFT (0°C to +70°C)				
Throughput Drift		±2		ppm of 20V/°C
Droop Rate		doubles every 10°C		
DYNAMIC CHARACTERISTICS				
Bandwidth (Full Power)		400		kHz
Output Slew Rate		25		V/μsec
Acquisition Time (to ±0.01%)				
10V Step		0.8	1	μsec
20V Step		1.2	1.5	μsec
Aperture Time		12		nsec
Sample-to-Hold Transient				
Peak Amplitude		50		mV
Settling to .01%			200	nsec
Feedthrough in Hold Mode			±0.005	% of Step Change at input
OUTPUT				
Voltage Range	±10			V
Current Range	±20			mA
Impedance (Short Circuit Protected)			1.0	Ω
TEMPERATURE				
Specification		0 to +70		°C
Storage		-55 to +125		°C

MECHANICAL

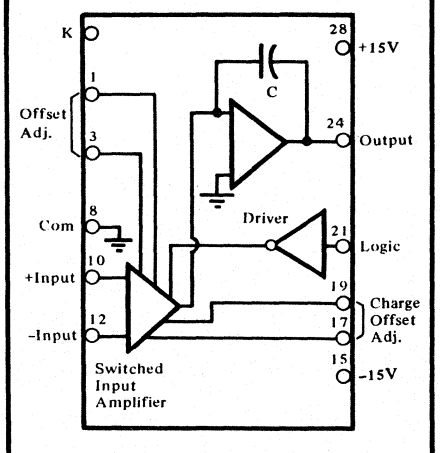


Dimensions in parentheses are in inches.

WEIGHT: 56.7 grams (2 oz)
MATING CONNECTORS:
2300 - P.C. Card and Terminals
2301 - Set of 2 - 16 Pin Connector Strips
PINS: Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

CONNECTION DIAGRAM

(TOP VIEW)



NOTES:

1. Input should never exceed supply by more than 0.6 volts.
2. Shottky TTL compatible.
3. Gain is user selectable.
4. For 1 μsec SAMPLE and 15 μsec HOLD times.
5. Includes voltage and charge offsets.

DISCUSSION OF SPECIFICATIONS

ACCURACY

All SHM60 sample/hold units are tested for accuracy and are factory trimmed to assure that all units meet critical specifications.

DYNAMIC NONLINEARITY

This is the unadjustable throughput error from input to output for a 1 microsecond SAMPLE period and a 15 microsecond HOLD period. Errors included in this specification are throughput nonlinearity, dielectric absorption, droop, thermal transients and feedthrough. Offset errors must be adjusted to zero with an offset trim control and gain errors must be adjusted to zero with a gain trim control elsewhere in the system.

ACCURACY – UNITY GAIN OPERATION

The initial accuracy of the SHM60 is ±0.01% maximum of full scale range when operated as a unity gain voltage follower.

GAIN and OFFSET ERRORS - GAINS OTHER THAN UNITY

The SHM60 should be treated in the same manner as an operational amplifier when gains other than unity are employed. The gain setting resistor parameters such as absolute accuracy and tracking ratio must be considered when computing error effects for gains other than unity.

THROUGHPUT DRIFT

The input to output accuracy drift over a 0°C to +70°C temperature range is the throughput drift - it is ±2 ppm/°C or ±0.0002% of 20 volts.

THROUGHPUT OFFSET

The output offset voltage encountered in the HOLD mode after sampling a grounded input is throughput offset. This error includes charge offset at zero volts input as well as amplifier d.c. voltage offsets.

ACQUISITION TIME

The acquisition time of the SHM60 is defined as shown in Figure 1. This is the time required for the SHM60 to turn on, slew and settle to 0.01% of the input voltage when the mode is changed from HOLD to SAMPLE.

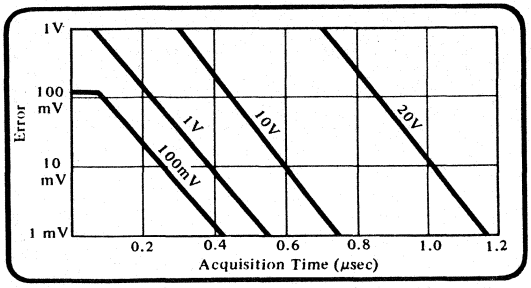


FIGURE 1. Error vs. Acquisition Time (Unity Gain Follower).

SAMPLE-TO-HOLD SWITCHING TRANSIENT

When the mode control is changed from SAMPLE -to-HOLD, the switching transient that appears on the output is the sample-to-hold switching transient.

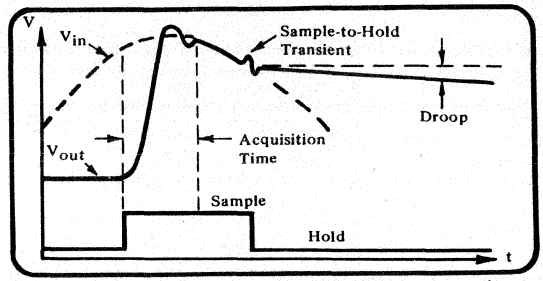


FIGURE 2. Definition of Acquisition Time Droop and Sample-to-Hold Transient.

DROOP RATE

Droop in a sample/hold is the voltage decay at the output due to output amplifier bias current when operating in the HOLD mode. To determine the effects of droop on system accuracy, the droop rate is multiplied by the HOLD period.

FEEDTHROUGH

The amount of input voltage change seen at the output when the sample/hold is in the HOLD mode is feedthrough error. The low feedthrough error of 0.005% preserves the accuracy of the sampled signal and can be used to increase the throughput sample rate, especially in time multiplexed applications.

APERTURE TIME

Aperture time is the delay between the time the sample/hold is given the command to HOLD the input signal and the time that this actually occurs. The SHM60 aperture time of 12 nanoseconds is sufficiently small to make aperture errors negligible for most applications.

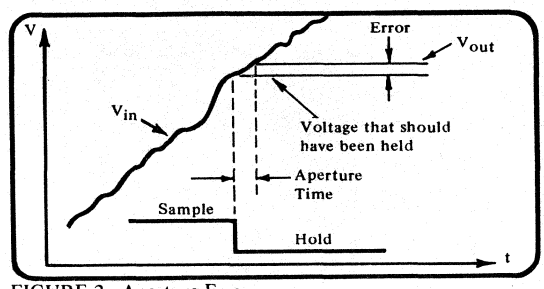


FIGURE 3. Aperture Error.

SYSTEM ERROR CONSIDERATIONS

The 1 μsec acquisition time and 12 nanoseconds aperture window of the SHM60 offer an excellent way of reducing system sampling error at high throughput rates for sinusoidal data. Taking the maximum slope of a sine wave at the zero crossing where maximum sampling error occurs, the error voltage as a percentage of full scale is proportional to the product of frequency and aperture time (Δt):

$$\% \text{ Aperture Error} = \frac{\Delta V}{V} \times 100 = 2\pi f \Delta t \times 100$$

where ΔV = Aperture error
V = Peak signal amplitude
f = Maximum signal frequency
Δt = Aperture time

INSTALLATION and OPERATING INSTRUCTIONS

OPTIONAL VOLTAGE and CHARGE OFFSET ADJUSTMENTS

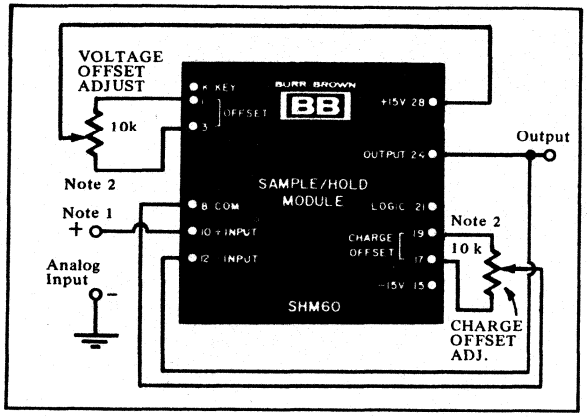


FIGURE 4. Optional CHARGE and VOLTAGE OFFSET Adjustment Connections.

Throughput OFFSET error may normally be adjusted to zero with a single external VOLTAGE OFFSET adjust control, as shown in Figure 4. A small CHARGE OFFSET error of 1 mV to 3 mV in the HOLD mode may occur. This CHARGE OFFSET error may also be adjusted to zero with an optional external CHARGE OFFSET adjustment as shown in Figure 4.

NOTES:
1. The analog input signal should not be run under or over the module as this may degrade feedthrough in the HOLD mode.
2. Potentiometers should have a TCR of 100 ppm/°C or less.

- Care must be taken to provide a good low impedance common as there is an appreciable amount of current returned to the power supplies.
- Power supply bypass capacitors are provided in the module, but additional bypassing may be required if excessive noise is present on the power supply lines.

CONNECTIONS FOR GAINS OTHER THAN UNITY

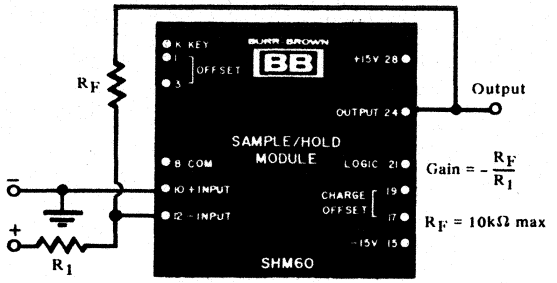


FIGURE 5. SHM60 Connections for Inverting GAIN.

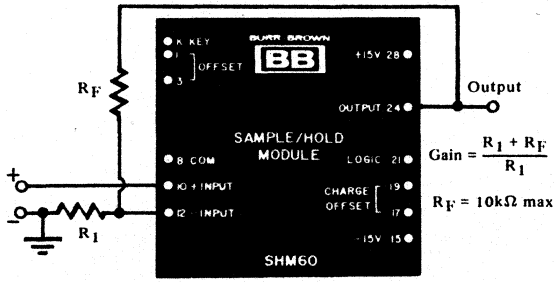
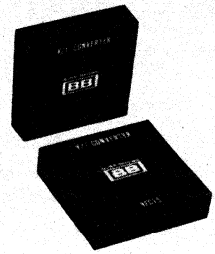


FIGURE 6. SHM 60 Connections for Non-Inverting GAIN.

Although optimum performance is at unity gain, the SHM60 may be operated to provide gains ranging from ±1 to ±1000 as shown in Figures 5 and 6. For these configurations, the unit may be treated as an operational amplifier. Acquisition time will get longer as gain increases, approximately 2.5 μsec settling to ±0.01% for a gain of 5 and 4 μsec for a gain of 10 for 10 volt output steps. Voltage drift can be computed as with an op amp using 10 μV/°C as the input drift.

NOTES:
- Gain accuracy and drift is dependent on the absolute accuracy and thermal tracking properties of the gain setting resistors R_1 and R_F. Metal film or better quality low drift resistors are recommended.
- Charge offset is independent of gain, and is referred to the output.

BURR-BROWN



VFC12
VFC15
VFC12LD
VFC15LD

VOLTAGE-TO-FREQUENCY CONVERTERS

APPLICATIONS

A/D CONVERSION - 13-bit accuracy

DPM FRONT END - 3+ digits accuracy

LONG-LINE SIGNAL TRANSMISSION
Increase noise immunity using only one transmission line

OPTICAL ISOLATION
Use simpler isolation techniques than with analog isolation and with only one isolator

FEED RATE GENERATOR AND CONTROL
0.05% accuracy over 0°C to +70°C

FEATURES

LOW COST

ONE SIGNAL LINE TRANSMISSION COMPACT
1.5" x 1.5" x 0.4" module package

ACCURATE
0.005% linearity gives you 13-bit accuracy

STABLE
10ppm/°C max gain drift (LD versions) gives you excellent stability over temperature

VERSATILE
Many simple-to-implement scaling options
Unipolar or bipolar operation - VFC15

CONVENIENTLY SCALED
1kHz per volt

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PDS-314
Printed in U.S.A. July, 1978

GENERAL DESCRIPTION

Voltage-to-frequency conversion is a simple and low cost method of converting analog signals into an equivalent digital form. The output is a TTL/DTL compatible digital pulse train whose repetition rate is proportional to the amplitude of the analog input signal; these pulses have constant width and constant amplitude.

The Burr-Brown Model VFC12 accepts 0 to 10 volt analog signals and is pin compatible with Teledyne Philbrick's Model 4701. The Model VFC15 accepts either 0 to 20 volt or 0 to 20 mA current analog signals.

The VFC12 operates over a DC to 10 kHz frequency range and the VFC15 operates over a DC to 20 kHz frequency range.

The low 0.01% nonlinearity error of these V/F converters makes them excellent for use in applications where digital resolutions of 12 or 13 bits are desired. These 1.5" x 1.5" x 0.4" modular units are completely self-contained and require only ±15 Vdc power and input signal. The gain and offset are adjustable with external potentiometers. A number of optional configurations to scale the input or output for best compatibility with your system are easily realized with simple external circuitry.

THEORY OF OPERATION

The Model VFC12 and Model VFC15 are ultra-linear voltage-to-frequency converters that provide a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. To understand the operation of the circuit consider the block diagram in Figure 1.

Amplifier A1 is connected in an integrator configuration. The integrator capacitor C begins charging at a constant rate in response to the input voltage until the output of A1 reaches a certain potential V_{ref}. At this time a comparator triggers a frequency-controlling charge dispenser which removes a precision amount of charge from C. The frequency at which this charge transfer occurs is linearly related to the input voltage.

A1 need not be an exceptionally high-gain or fast slewing operational amplifier. As long as the average current at the summing junction of A1 is zero, the frequency of oscillation must be directly proportional to the input voltage with little dependence on the gain or speed of A1.

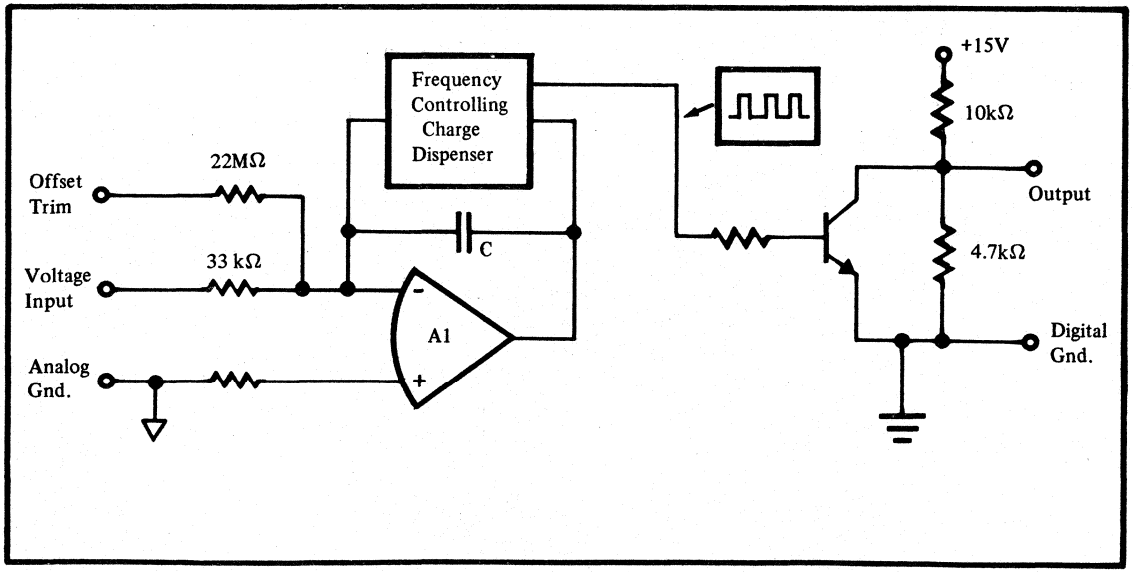


FIGURE 1. Functional Block Diagram of Model VFC12.

SPECIFICATIONS

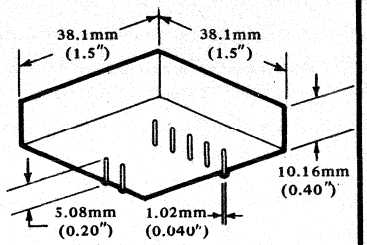
ELECTRICAL

Typical at 25°C and rated power supplies unless otherwise noted.

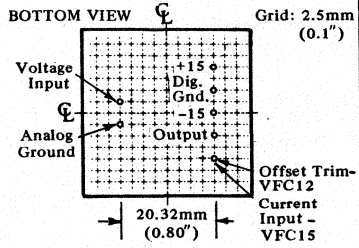
MODEL	VFC12	VFC12LD	VFC15	VFC15LD	UNITS
FREQUENCY RANGE	10		20		kHz
INPUT					
ANALOG INPUT					
Voltage Range	0 to +10		0 to +20		V
Overrange (min)	100		10		% of FSR(1)
Impedance	33		33		kΩ
Maximum Safe Input Voltage	22		22		V
INPUT POWER					
Rated Voltages(2)	±15 ±10%				Vdc
Supply Drain					
Typical	±16				mA
Maximum	±20				mA
TRANSFER CHARACTERISTICS					
TRANSFER EQUATION	$f_{out} = 10^4 \frac{V_{in}}{10}$				Hz
ACCURACY					
Full Scale Gain Error(3)	Adjustable				
Offset Error(4)					
Typical	±0.002		±0.001		% of FSR
Maximum	±0.01		±0.005		% of FSR
Linearity Error (max)					
V_{in} = +1 mV to +10 V	±0.01	±0.005	–		% of FSR
V_{in} = +1 mV to +20 V	–		±0.01	±0.005	% of FSR
Power Supply Sensitivity	±0.005				% of FSR/%
STABILITY (0°C to +70°C)					
Full Scale Drift (Gain + Offset)					
Voltage Input					
Typical	20	8	20	8	ppm of FSR/°C
Maximum	50	10	50	10	ppm of FSR/°C
Current Input	N/A		35	15	ppm of FSR/°C
Stability vs. Time					
Full Scale Drift					
Per day	±100				ppm of FSR
Per month	±200				ppm of FSR
Input Offset Drift					
Per day	±10				ppm of FSR
Per month	±20				ppm of FSR
Offset Drift					
Typical	±2				ppm of FSR/°C
Maximum	±5				ppm of FSR/°C
RESPONSE					
Settling Time for 10V Input Step	2 output pulses of new frequency plus 20 μsec				
Overload Recovery Time	1 to 2 pulses of new frequency				
TEMPERATURE RANGE					
Specification	0 to +70				°C
Operating (derated specifications)	-25 to +85				°C
Storage	-55 to +125				°C
OUTPUT					
Waveform	Train of TTL/DTL compatible pulses				
Pulse Characteristics					
Logic 1 (High)	4.7 ±0.5				V
Logic 0 (Low)	0.2 ±0.1				V
Pulse Width	30				μsec
Fan Out	10 TTL Loads				
Impedance	3				kΩ
Capacitive Load (max)	1000				pF

(1) FSR = Full Scale Range and is 10V for VFC12 and 20V for VFC15.
(2) A regulated supply with 1% or less ripple is recommended.
(3) Adjusted at factory for 9.900V = 10 kHz.
(4) May be externally adjusted to zero.

MECHANICAL

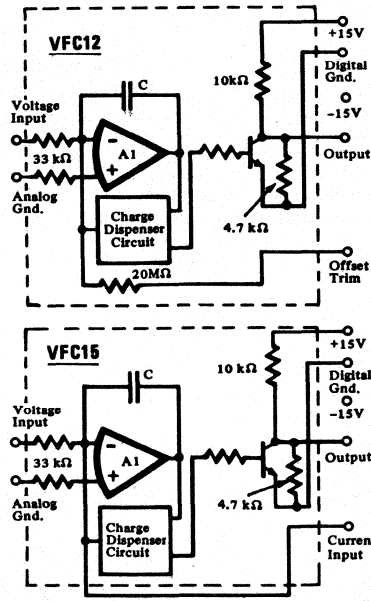


Dimensions in inches are shown in parentheses.



MATERIAL:
Case: Diallyl Phthalate or Epoxy Shell
Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].
Weight: 25 grams (0.875 oz)
Mating Connector: 1400 MC

CIRCUIT DIAGRAMS



DISCUSSION OF SPECIFICATIONS

DYNAMIC SIGNAL RANGE

The VFC12 is specified to operate over a DC to 10 kHz frequency range for an input voltage of 0 to +10 volts. Since this unit has a specified overrange of 100%, it is possible to extend the input signal and output frequency ranges to 20 volts and 20 kHz respectively. However, the linearity is not guaranteed over this range. If the extended range of operation is desired, Burr-Brown recommends using the VFC15 for greater than 10 volt and 10 kHz operation. In addition to the extended voltage and frequency range, the VFC15 has its input summing junction made available for applications requiring current-to-frequency conversion and bipolar input signals up to ±10 volts.

Figure 2 depicts the transfer function of these units. The input current-to-frequency transfer function for the VFC15 is shown for a calibrated 1000 ohm shunt resistor (see page 5-184).

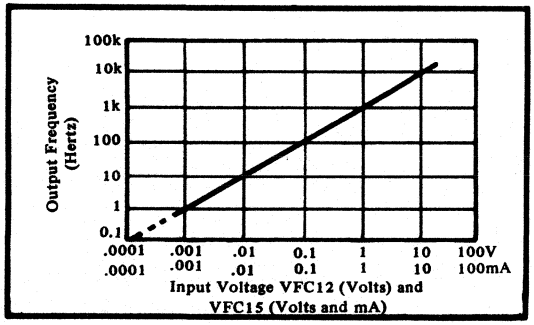


FIGURE 2. Voltage or Current-to-Frequency Characteristic.

ACCURACY

The transfer linearity of these V/F converters is one of the most meaningful measures of accuracy since initial full scale and offset errors are externally adjustable to zero. All VFC12 and VFC15 units are factory calibrated for maximum linearity error of 0.01% of full scale range input signals. Although Burr-Brown guarantees a maximum linearity error of ±0.01% of full scale, the linearity error of these units is typically less than ±0.002% of full scale. The use of regulated power supplies with better than 1% regulation is recommended in order to maintain the accuracy of these units. The 0.01% linearity makes these units excellent for use as a front end for 10 to 12 bit resolution A/D converters, and for highly accurate transfer of analog data over long lines in noisy environments.

FREQUENCY STABILITY vs. TEMPERATURE

Frequency drift is factory tested with the offset and full scale calibration made at 25°C, and is expressed as parts per million of full scale range vs. temperature. Typically, full scale drift is ±20 ppm/°C over the operating temperature range for VFC12 and VFC15. VFC12LD and VFC15LD have typical full scale drifts of 8 ppm/°C.

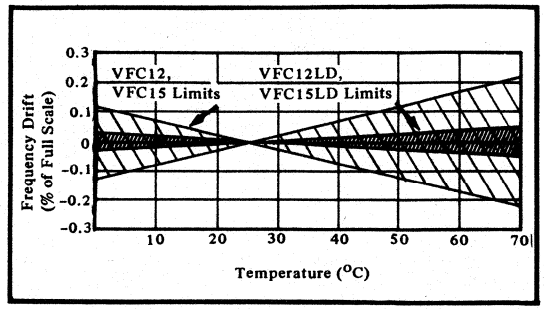


FIGURE 3. Frequency Drift vs. Temperature with Calibration made at 25°C.

FULL SCALE AND OFFSET DRIFT

All units are tested for full scale and offset drift over a 0°C to +70°C operating temperature range. Internal temperature compensation is provided for ±50 ppm/°C maximum full scale drift and ±5 ppm/°C offset drift for VFC12 and VFC15. Maximum full scale drift for VFC12LD and VFC 15LD is ±10ppm/°C. If external full scale and offset trim adjustments are provided, the temperature coefficient of the external components must be added to the specified drift components as shown on page 5-183 to determine the total thermal coefficients of drift.

RESPONSE

The settled response of these units to changes in input signal is specified for an input signal step change of 10 volts and is 20 microseconds plus 2 output pulses of new frequency. For 10 volt input signal steps, the VFC12 operating at 10 kHz full scale frequency range, the step response settling is 220 μsec; for the VFC15 operating at 20 kHz full scale frequency range, the step response settling is 120 μsec. Figure 4 shows the typical response of these units to instantaneous changes in the input signal.

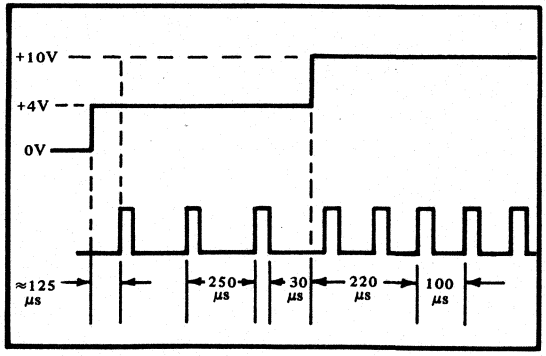


FIGURE 4. Typical Response to Instantaneous Changes in the Input Voltage.

INSTALLATION AND OPERATING INSTRUCTIONS

INSTALLATION

The VFC12 and VFC15 are designed for installation on a flat mounting surface such as a printed circuit board or a chassis. The pins may be hand or dip soldered; for plug in installations, the accessory connector (1400MC) or mounting jacks may be installed on a chassis or p.c. board.

Particular attention should be given to wire or p.c. conductor path routing. All input signal lines should be as short as possible, and coupling from power supply lines should be minimized

For best results, the power supply should have 1% or better regulation and low ripple and noise. The Burr-Brown Model 550 series ±15 volt output modular power supplies provide excellent regulation, and are recommended for use with these V/F converters. Normally external power supply bypass capacitors are not required. However, if a good quality low ripple power source is not available, 1 μF or larger external bypass capacitors are recommended in order to prevent interference from power supply effects.

CAUTION: Do not short Output to -15 Volt Pin.

EXTERNAL CONNECTIONS

FULL SCALE AND OFFSET ADJUSTMENTS

The VFC12 and VFC15 V/F converters are factory calibrated to meet all specifications. However, FULL SCALE and OFFSET may be user adjusted when absolute accuracy better than the specified initial accuracies are required.

These units are factory calibrated to provide a FULL SCALE output frequency of 10 kHz for an input voltage of 9.900 V ±0.05% and may be calibrated to provide 10.000 kHz output frequency for an exact input voltage of 10.000 volts. OFFSET is factory calibrated to provide an output frequency of 1 ±0.2 Hz for an input voltage of 1.0 millivolts.

Normally, OFFSET need not be adjusted unless absolute accuracies of better than ±0.004% are required.

ADJUSTMENT PROCEDURE

Select external potentiometers with low drift coefficients to preserve the drift characteristics of the V/F converter. The drift effects must be added to the ±50 ppm/°C specified FULL SCALE temperature coefficient. For example, external component contribution of R_1 to drift will be:

$$\left[\frac{R_1}{33\,k + R_1} \times \text{Tempco } R_1\right] /^{\circ}C$$

To calibrate these units, first apply +1.0 mV to the analog input terminals and adjust R_2 for f_{out} = 1.0 Hz. Then apply +10.000 volts to the input and adjust R_1 for f_{out} = 10.000 kHz. Interaction between R_1 and R_2 is generally negligible due to the low initial offset voltage; however, repeating the above calibration will insure precise calibration.

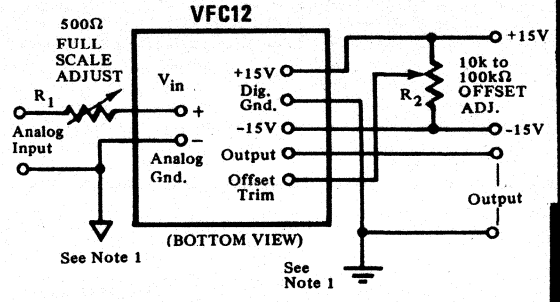


FIGURE 5. VFC12 Optional FULL SCALE and OFFSET Adjustments.

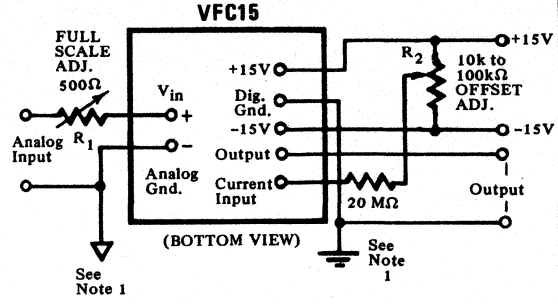


FIGURE 6. VFC15 Optional FULL SCALE and OFFSET Adjust for Voltage Input Signals.

NOTE 1: Digital and Analog grounds should be tied together as close as possible to the power supply common.

OPERATING OPTIONS

CURRENT-TO-FREQUENCY CONVERSION

A method of obtaining direct conversion of input currents of 0 to 10 mA for Model VFC12 and 0 to 20 mA for Model VFC15 corresponding to output frequency ranges of 0 to 10 kHz and 0 to 20 kHz respectively is described in Figure 7. Figure 7 describes a calibrated 1000 ohm shunt resistance across the voltage input terminals. Full scale output is calibrated by adjusting the 1000 ohm shunt performing the usual offset adjustments.

The second technique, described in Figure 8, is a simple current divider into the summing junction (CURRENT INPUT) of the VFC15. This method offers the advantage of limiting the voltage swing on the input terminal to a 3.8 to 5.55 volt range for a 0 to 20 mA input current range, depending on the value of the full scale adjustment potentiometer, offering better compliance to the current source. OFFSET may be adjusted as shown on page 5-183.

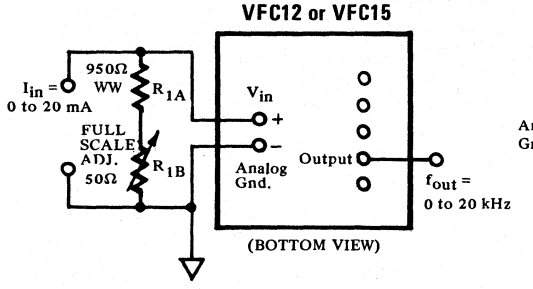


FIGURE 7. VFC15 Current-to-Frequency Conversion using Voltage Input Terminals.

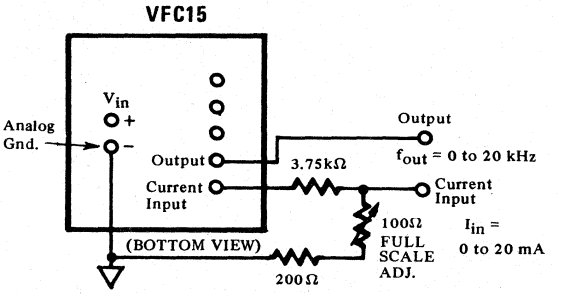


FIGURE 8. VFC15 Current-to-Frequency Conversion using Current Input Terminal.

SCALING FOR BIPOLAR INPUT VOLTAGE RANGE

The summing junction (CURRENT INPUT) of the VFC15 is made available for scaling the unit to accept ±5 volt or ±10 volt input signals. An external reference and scaling resistors must be connected to the CURRENT INPUT. OFFSET is adjusted as shown on page 5-183.

Figures 9a and 9b show an example with a +10 volt reference. The reference regulation and drift should be low in order to preserve signal accuracy. The output frequency range for these input voltage ranges will be centered at 5 kHz for the ±5 volt range and at 10 kHz for the ±10 volt range. The corresponding output frequency ranges will be:

SIGNAL RANGE	INPUT SIGNAL	OUTPUT FREQUENCY (kHz)
±5 V	−5 V	0
	0 V	5
	+5 V	10
±10 V	−10 V	0
	0 V	10
	+10 Volt	20

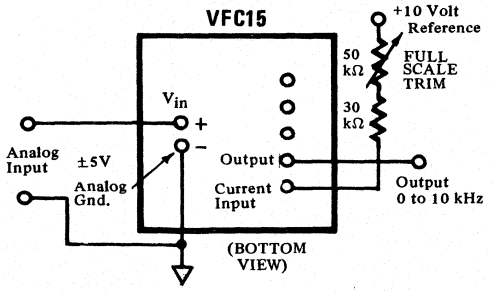


FIGURE 9a. Scaling the VFC15 for ±5 volt Bipolar Operation.

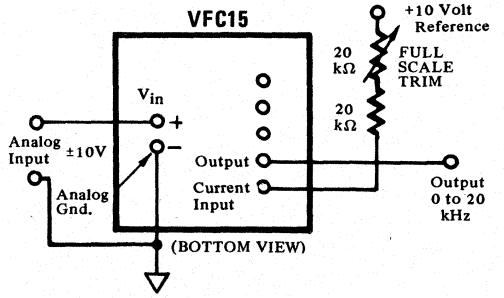


FIGURE 9b. Scaling the VFC15 for ±10 volt Bipolar Operation.

SQUARE-WAVE OUTPUT

A type D flip-flop in a frequency dividing configuration provides a convenient method of obtaining a variable width square wave output from the VFC12 or VFC15 as shown in Figure 10. The output of the V/F converter is used to drive the clock input of the flip-flop.

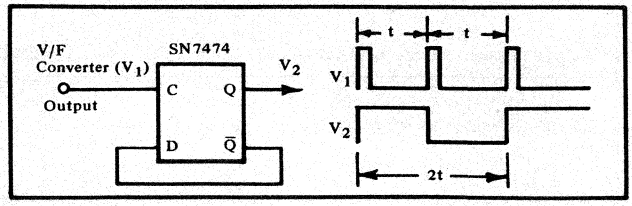


FIGURE 10. Square Wave Output Using a Type D Flip-Flop.

DRIVING HIGH NOISE IMMUNITY LOGIC

A pullup resistor to +15 volts on the V/F converter output as shown in Figure 11 provides 4 volt noise immunity for driving high noise immunity logic (HNIL).

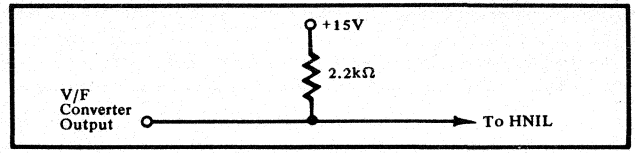


FIGURE 11. Pullup Resistor for Driving HNIL.

OUTPUT ISOLATION

Optical coupling the V/F converter outputs provides an excellent method of obtaining 500 Vdc or 1000 Vac p-p isolation between the V/F converter and a receiving device. The isolation is accomplished digitally, preserving signal accuracy. The common mode capability of the circuit shown in Figure 12 is limited only by the optical isolator and the power supply.

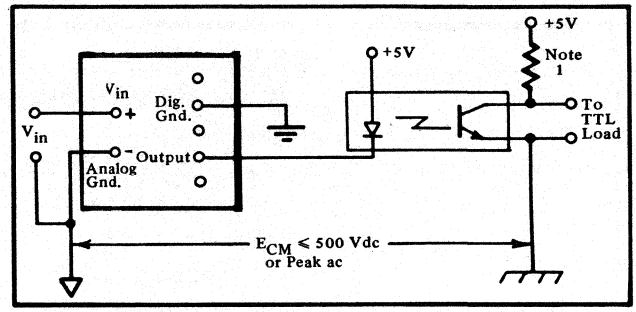


FIGURE 12. Optical Isolation of V/F Converter Output.

NOTE 1: This +5 V supply is isolated from the +5 V supply used for the diode.

SCALING FOR 1kHZ OUTPUT FREQUENCY RANGE

Two methods are described in Figures 13 and 14 for obtaining a 1 kHz full scale V/F converter using the VFC12 or VFC15.

GAIN ATTENUATION

In the circuit of Figure 13 the input is attenuated by a 10:1 divider. This technique is the least expensive to implement but has the disadvantage of added thermal drift of the external components and does not permit the V/F converter to operate over the most linear portion of its frequency range.

FREQUENCY DIVISION

Figure 14 illustrates the best method of obtaining a 1 kHz frequency range using an external decade counter. The disadvantages of the gain attenuation technique are overcome, but this technique is more expensive to implement.

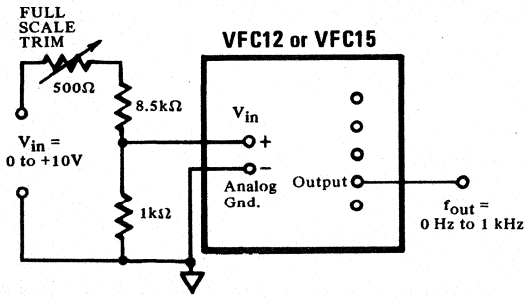


FIGURE 13. 1 kHz Full Scale Output Frequency Range Using Input Attenuation Network.

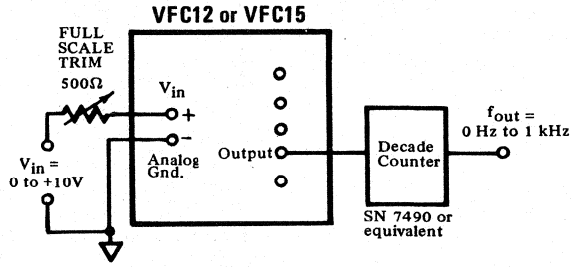
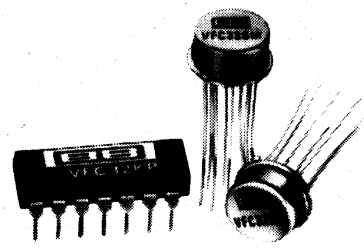


FIGURE 14. 1 kHz Full Scale Output Frequency Range Using Decade Counter.

BURR-BROWN



VFC32

VOLTAGE-TO-FREQUENCY AND FREQUENCY-TO-VOLTAGE CONVERTER

FEATURES

- RELIABLE MONOLITHIC CONSTRUCTION
- HIGH LINEARITY
  - ±0.01% max at 10kHz FS
  - ±0.05% max at 100kHz FS
  - ±0.2% max at 0.5MHz FS
- V/F OR F/V CONVERSION
- 6 DECADE DYNAMIC RANGE
- VOLTAGE OR CURRENT INPUT
- OUTPUT DTL/TTL/CMOS COMPATIBLE

DESCRIPTION

The VFC32 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple, low cost method of converting analog signals into an equivalent digital form. The digital output is an open collector which provides a pulse train whose repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with DTL, TTL, and CMOS logic families, and have a constant width and amplitude. An external RC network sets up the full scale frequency, with guaranteed maximum nonlinearity of ±0.2% at 500kHz. The temperature coefficient of the full scale accuracy is ±100ppm/°C maximum at 10kHz (VFC32BM) and the input offset voltage drift is only ±3ppm/°C maximum.

The VFC32 is available in three models and two package configurations. The TO-100 versions are hermetically sealed, and specified for the -25 to +85°C and -55°C to +125°C ranges, and the epoxy dual-in-line unit is specified from 0 to +70°C.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-372A

Printed in U.S.A. July, 1978

THEORY OF OPERATION

The VFC32 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. To understand the operation of the circuit, refer to Figure 1.

The input amplifier is connected in an integrator configuration. When a positive input voltage is applied at V_{in}, a constant current will flow through the input resistor, causing the voltage at f_{in} to ramp down toward zero, according to $\frac{dV}{dt} = \frac{V_{in}}{R_1 C_2}$ During this time, the constant current sink is disabled by the switch. When the ramp reaches a voltage close to zero (~ -0.6V), the comparator will cause the one-shot to fire. The f_{out} signal will then change logic states, going from a "0" to a "1", and the switch will close, enabling the constant current sink. The ramp voltage will then change direction and begin to ramp up. Since V_{in}/R_1 is always set up to be less than 1mA, the current in the integrating capacitor will flow toward the summing junction, and the ramp voltage rate of change will be $\frac{dV}{dt} = \frac{\frac{V_{in}}{R_1} - 1\ mA}{C_2}$. Before the ramp voltage can saturate the input amplifier, the one-shot will reset, disabling the current sink, changing the output state back to a logic "0", and restarting the cycle. Since the integrating capacitor C_2 affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to V_{in}/R_1, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function. More guidelines on the selection of the external components are given in the Operating Instructions section.

To operate the VFC32 as a highly linear frequency-to-voltage converter, open the connection between V_{out} and f_{in}, and connect V_{in} to V_{out}. The input frequency should be coupled through a capacitor to f_{in}, and a positive output voltage proportional to f_{in} will be generated at the V_{out} connection. Refer to the Operating Instructions section for more detailed information on F/V operation.

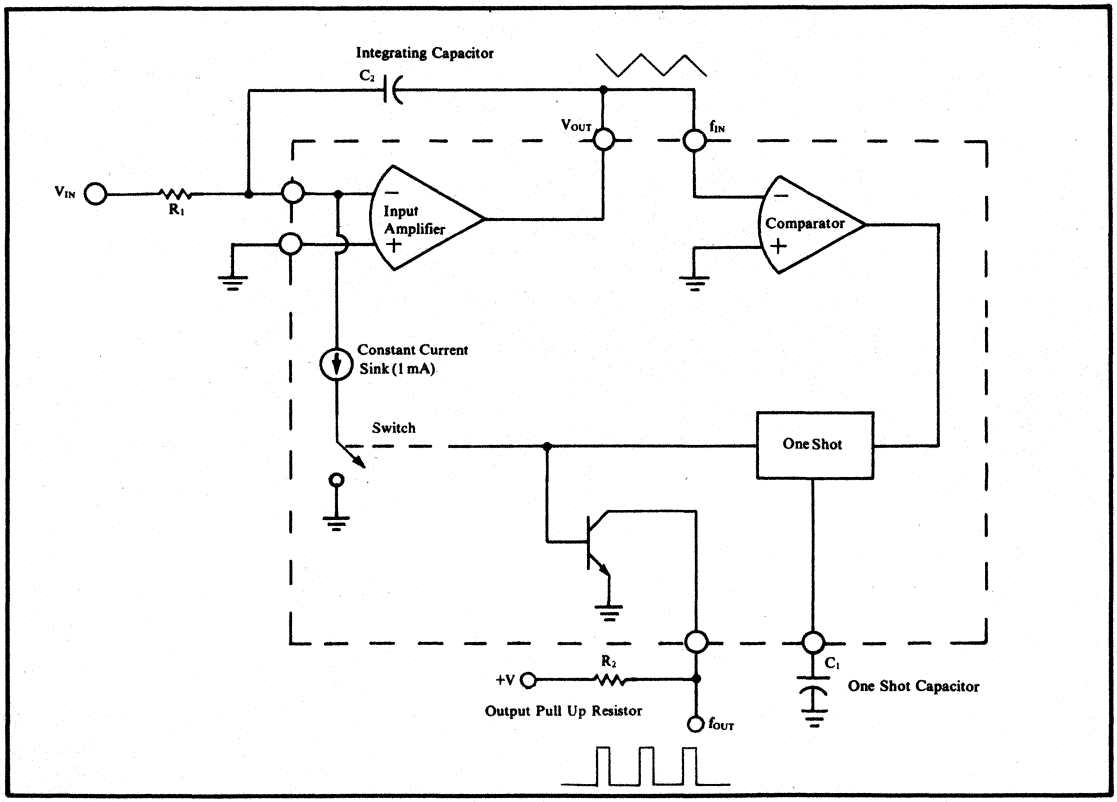


FIGURE 1. Functional Block Diagram

ELECTRICAL SPECIFICATIONS

Specifications at T_A = +25°C and ±15VDC power supply unless otherwise noted.

MODEL	VFC32			UNITS
	MIN	TYP	MAX	
Full Scale Frequency			0.5	MHz
INPUT				
Analog Input (V/F)				
Voltage Ranges	-10 to 0, 0 to +(0.25mA x R_1)			V
Current Range	0 to +0.25			mA
Input Bias Current				
inverting input		6	8	nA
non-inverting input		30	40	nA
Input Offset Voltage (trimmable to zero)		1	4	mV
Differential Impedance	170 || 10	200 || 10		kΩ || pF
Common-mode Impedance	2.5 || 10	3.0 || 10		MΩ || pF
Frequency Input (F/V)				
Logic Levels				
logic "0"	$-V_{cc}$		-0.6	V
logic "1"	+1.0		$+V_{cc}$	V
Pulse Width Range, (refer to "t" in Figure 4)	0.1		150/[F_{max} (kHz)]	μsec
Impedance	1 || 10	1.2 || 10		MΩ || pF
TRANSFER CHARACTERISTICS				
Transfer Functions	$f_O = V_{IN}/7.5\ R_1\ C_1$ $V_O = 7.5\ R_1\ C_1\ f_{IN}$			
Accuracy				
Full Scale Gain Error (adjustable to zero)		5		% of FSR
Linearity Error				
0.01 Hz ≤ F ≤ 10 kHz		±0.005	±0.010[1]	% of FSR
0.1 Hz ≤ F ≤ 100 kHz		±0.025	±0.050	% of FSR
0.5 Hz ≤ F ≤ 0.5 MHz		±0.050	±0.200	% of FSR
Power Supply Sensitivity		±0.0015	±0.002	% of FSR/%
Temperature Stability				
Analog Input				
Gain Drift (f = 10 kHz)				
VFC32KP		±75	±150	ppm/°C
VFC32BM		±50	±100	ppm/°C
VFC32SM		±70	±150	ppm/°C
Offset Drift				
VFC32KP			±3	ppm of FSR/°C
VFC32BM			±3	ppm of FSR/°C
VFC32SM			±3	ppm of FSR/°C
Frequency Input				
Full Scale Drift (Gain & Offset				
VFC32KP at 10kHz)		±50	±150	ppm of FSR/°C
VFC32BM		±50	±100	ppm of FSR/°C
VFC32SM		±70	±150	ppm of FSR/°C
Dynamic Response				
Settling time to within linearity specification for a full scale input step	1 pulse of new frequency plus 1 μsec			
Overload recovery time	1 pulse of new frequency plus 1 μsec			

MODEL	VFC32			UNITS
	MIN	TYP	MAX	
OUTPUT				
Voltage Output				
Voltage Range	0 to +10			V
Output Current	+10			mA
Output Impedance (closed loop)			1	Ω || pF
Capacitive Load			100	pF
Frequency Output (open collector)				
Pulse Characteristics				
logic "1"	V_{pullup}			V
logic "0"			0.4	V
pulse width		1 ($4\ F_{max}$)		sec
Output Sink Current (Logic "0", 0.4V)			8	mA
Output Leakage Current (Logic "1")			100	nA
Fall Time				
I_{out} = -5 mA, C_{load} = 500 pF			400	nsec
POWER SUPPLY REQUIREMENTS				
Rated Supplies		±15		VDC
Supply Range	±9		±20	VDC
Supply Drain (independent of operating frequency)		±4.5	±5.5	mA
TEMPERATURE RANGE				
Specification				
VFC32KP	0		+70	°C
VFC32BM	-25		+85	°C
VFC32SM	-55		+125	°C
Operating				
VFC32BM, SM	-55		+125	°C
VFC32KP	-25		+85	°C
Storage				
VFC32BM, SM	-65		+150	°C
VFC32KP	-25		+85	°C
VFC32KP (0 +70°C) VFC32BM (-25 +85°C) VFC32SM (-55 +125°C)				

ABSOLUTE MAXIMUM RATINGS above which unit may be damaged.

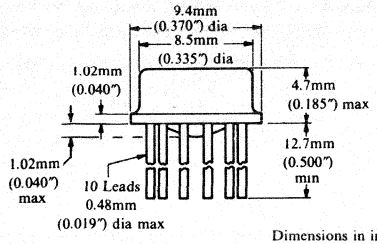
Supply Voltages	±22V
Output Sink Current (F_{output})	50mA
Output Current (V_{output})	+20mA
Input Voltage, -Input	±Supply
Input Voltage, +Input	±Supply
Storage Temperature Range	
VFC32BM, SM	-65°C to +150°C
VFC32KP	-25°C to +85°C

NOTES:

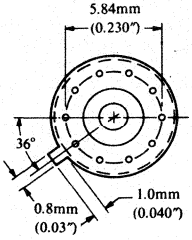
(1) 0.015% for negative input voltages.

MECHANICAL SPECIFICATIONS

VFC32BM, VFC32SM TO-100 PACKAGE



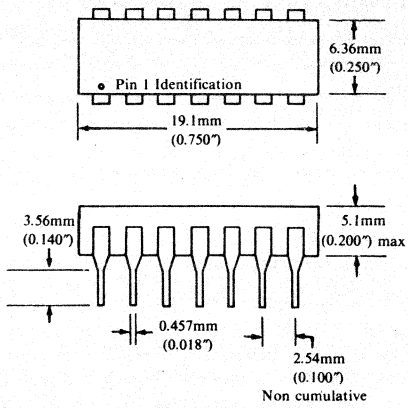
Dimensions in inches are in parentheses.



Pin material and plating composition:
Conforms to Mil-Std-883, Method 2003 (solderability) except paragraph 3.2 (aging).

Hermeticity:
Conforms to Mil-Std-883, Method 1014, Condition C, Step 1, Fluorocarbon (gross leak) and Condition A, Helium, 5 x 10^{-8} cc/sec (fine leak)
Connector: None

VFC32KP EPOXY DUAL-IN-LINE PACKAGE



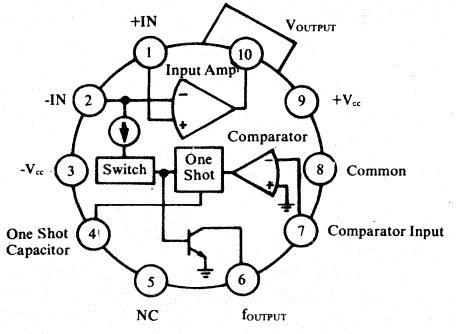
Row Spacing - 7.63mm (0.300")
Connector - 14 pin DIP connector (145MC)

Pin material and plating composition:
Conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)

V/F VFC32

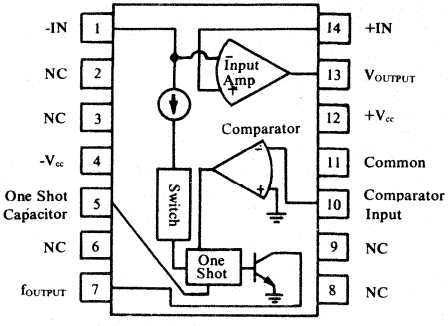
PIN CONFIGURATIONS

VFC32BM, VFC32SM TO-100 PACKAGE



TOP VIEW

VFC32KP EPOXY DUAL-IN-LINE PACKAGE



TOP VIEW

OPERATING INSTRUCTIONS

The VFC32 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figure 2 and 3. The full scale frequency and full scale input voltage (current) are established by the selection of values for R1, C2, and C1. Most applications will require a gain adjustment pot (R3), but the offset adjust network (R4, R5) can be omitted if input offset voltages of 1 to 4 mV can be tolerated. R2 is an output pull up resistor and its value depends on the pull up voltage and output drive requirements.

EXTERNAL COMPONENT SELECTION CRITERIA

Integrating Capacitor C2. C2 is a function of the full scale frequency, according to this equation:

$$C2 = 10^{-4}/f_{max} \text{ farads (1000pF min)}$$

Select the closest standard value to the capacitance given by the equation. The initial tolerance and temperature stability are not critical since these errors do not affect the transfer function. Since the leakage current of the capacitor introduces a gain error, select a capacitor with leakage that is small compared to the full scale input current (0.25mA). A mylar type is recommended.

One-shot Capacitor, C1. This capacitor determines the duration of the output pulse, and is a function of the full scale frequency, according to this equation:

$$C1 = 3.3 \times 10^{-5}/f_{max} - 3.0 \times 10^{-11} \text{ farads}$$

Select the closest standard value to the capacitance given by the equation. The initial tolerance of this capacitor is not critical since R3 will be adjusted to remove initial gain errors. The temperature drift is critical, since it will add directly to the errors in the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize the parasitic capacitance at this connection to the VFC32 and C1 should be mounted as close as possible.

Input Resistor R1. R1 determines the magnitude of the current which charges the integrator capacitor. It is a function of the full scale input voltage, according to this equation:

$$R1(k\Omega) = [90 - \% \text{ tolerance C1}] \times V_{IN} \text{ max}/25mA$$

R1 is scaled down by [1-(initial C1 tolerance +.1)] to allow the addition of a series gain adjusting pot. R1 should have a very low temperature coefficient since this drift adds directly to the errors in the transfer function. If the input signal is a current rather than a voltage, R1 and R3 should be replaced with a short circuit, and the full scale input current should be 0.25mA. Removal of gain error then requires adjustment of C1.

Output Pull Up Resistor R2. The open collector output can sink up to 8 mA and still be TTL compatible. Select R2 according to this equation:

$$R2 \text{ min} = V_{PULLUP}/(8 \text{ mA} - i_{LOAD})$$

A 10% carbon composition resistor is suitable for use as R2.

Trimming Components R3, R4, R5.

R5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm/°C. R4 can be a 20% carbon composition resistor with a value of 10MΩ.

R3 nulls the gain errors of the converter and compensates for initial tolerances of R1 and C1. Its total resistance should be at least 20% of R1, if R1 is selected 10% low (see R1 equation). Its temperature coefficient should be no greater than five times that of R1, to maintain a low drift of the R3 - R1 series combination.

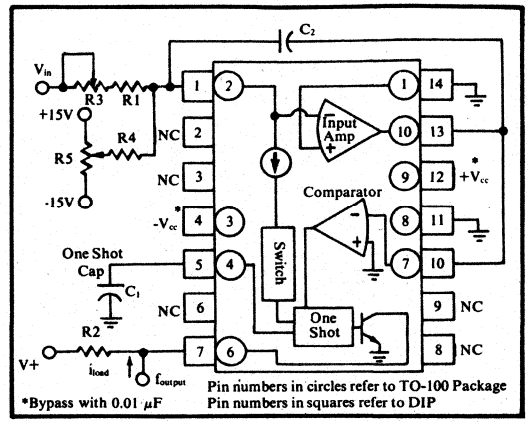


FIGURE 2. Connection Diagram for V/F Conversion, Positive Input Voltages.

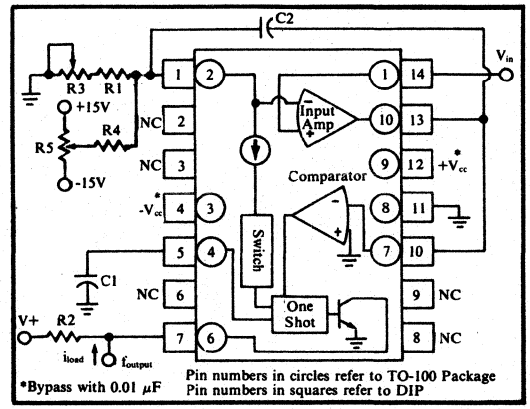


FIGURE 3. Connection Diagram for V/F Conversion, Negative Input Voltages.

GAIN AND OFFSET ADJUSTMENT PROCEDURES:

To null gain and offset errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 X full scale.
2. Adjust R5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R3 for proper output.
5. Repeat steps 2 through 4.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC32 is .02% of FSR/% max. To maintain ±.02% conversion, power supplies which are stable to within ±1% are recommended. These supplies should be bypassed as close as possible to the converter with 0.01μF capacitors.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC32 as a frequency-to-voltage converter, connect the unit as shown in Figure 4. To interface with TTL logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses -0.6V. Choose C3 for appropriate value of t (see Figure 4). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero, to insure that the input signal at pin 10 crosses the -0.6V threshold. Errors are nulled following the procedure given on page 5-190, using 0.001X full scale frequency to null offset, and full scale frequency to null the gain error.

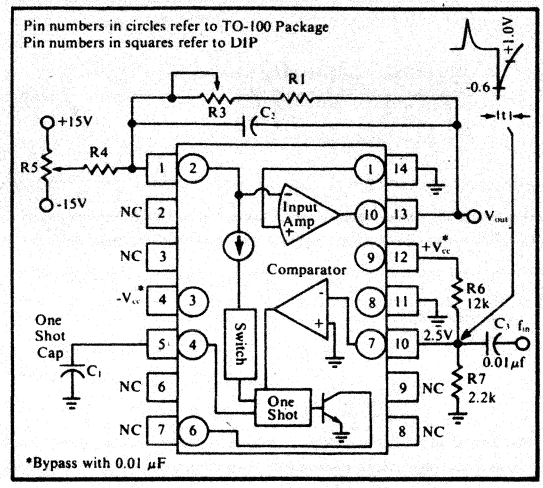


FIGURE 4. Connection Diagram for F/V Conversion

DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (full scale input and zero input). Linearity is the true measure of a VFC's performance, and is a function of the full scale frequency. Refer to Figure 5 to determine the typical linearity errors for your application. The high linearity of the VFC32 makes the device an excellent choice for use as the front end of A/D converters with 8 to 12 bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments.

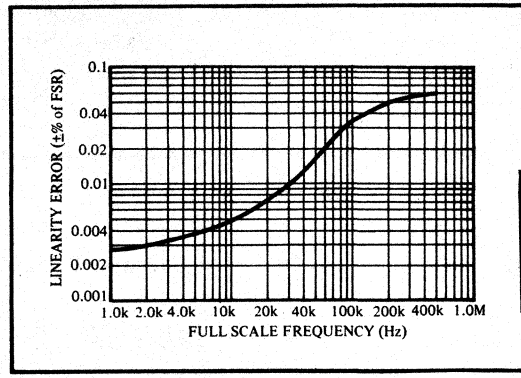


FIGURE 5. Typical Linearity Error vs Full Scale Frequency.

FREQUENCY STABILITY vs. TEMPERATURE

Frequency stability vs. temperature is 100% tested at Burr-Brown. It is expressed as parts per million of full scale range per °C. Since the frequency drift is a function of the specified temperature range, the wide temperature models of the VFC32 are also specified over the restricted temperature ranges, as well as the extended ranges. To determine the total accuracy drift over temperature, the drift coefficients of R_1 and C_1 must be added to the drift of the converter.

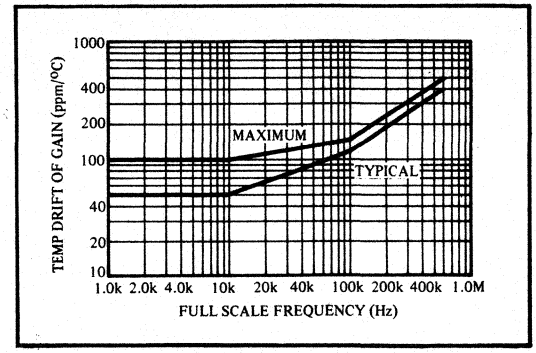
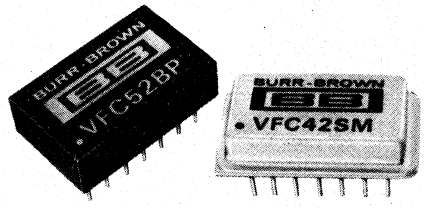


FIGURE 6. Temperature Drift of Gain vs Full Scale Frequency.

RESPONSE

Response of the VFC32 to changes in input signal levels is specified for a full scale step, and is 20 microseconds plus 2 pulses of the new frequency. For 10 volt input signal steps with the VFC32 operating at 100 kHz full scale frequency, the settling time to within ±0.01% of full scale is 40 microseconds.

BURR-BROWN



VFC42
VFC52

VOLTAGE-TO-FREQUENCY AND FREQUENCY-TO-VOLTAGE CONVERTER

FEATURES

- V/F OR F/V CONVERSION
- TWO FREQUENCY RANGES
  10kHz (VFC42)
  100kHz (VFC52)
- LOW NONLINEARITY
  ±0.01% max (VFC42)
  ±0.05% max (VFC52)
- MINIMAL EXTERNAL COMPONENTS REQUIRED
  Add only one external resistor for V/F operation
- 6 DECADE DYNAMIC RANGE
- OUTPUT DTL/TTL/CMOS COMPATIBLE

DESCRIPTION

VFC42 and VFC52 are hybrid microcircuits which can be connected as voltage-to-frequency or frequency-to-voltage converters. They provide a simple, low cost method of converting analog signals into an equivalent digital form. The digital output is an open collector which can be made compatible with DTL, TTL, or CMOS logic. The output is a train of constant-amplitude, constant-width pulses whose repetition rate is proportional to the amplitude of the analog input voltage. In the frequency-to-voltage mode the pulses become the input and the proportional DC voltage, the output.

Both models are offered in epoxy (-25°C to +85°C) and hermetic metal (-25°C to +85°C and -55°C to +125°C) 14-pin DIP packages.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-390 Printed in U.S.A. July, 1978

THEORY OF OPERATION

VFC42 and VFC52 hybrid voltage-to-frequency converters provide a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. To understand the circuit's operation see Figure 1.

The input amplifier is connected in an integrator configuration. When a positive input voltage is applied at V_{IN}, a constant current flows through the input resistor causing voltage at f_{IN} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_2$. During this time the constant current sink is disabled by the switch. When the ramp reaches zero volts, the comparator causes the one-shot to fire. The f_{OUT} signal then changes states, going from logic 0 to logic 1 and the switch closes, enabling the constant current sink. Ramp voltage then changes direction and begins to ramp up. Since V_{IN}/R_1 is always set to be less than 1mA, current in the integrating capacitor flows toward the summing junction and ramp voltage range of change will be

$$\frac{dV}{dt} = \frac{\left(\frac{V_{in}}{R_1}\right) - 1mA}{C_2}$$

Before the ramp voltage can saturate the input amplifier, the one-shot resets, disabling the current sink, changing the output state back to logic 0 and restarting the cycle.

To operate VFC42 and VFC52 as highly linear frequency-to-voltage converters, open the connection between V_{OUT} and f_{IN} and connect V_{IN} to V_{OUT}. The input frequency should be coupled through a capacitor to f_{IN}. A positive output voltage proportional to f_{IN} will be generated at the V_{OUT} connection. An external capacitor connected between pins 13 and 14 (paralleling C2) should be added to reduce output ripple. Refer to Operating Instructions, page 5, for detailed information on F/V operation.

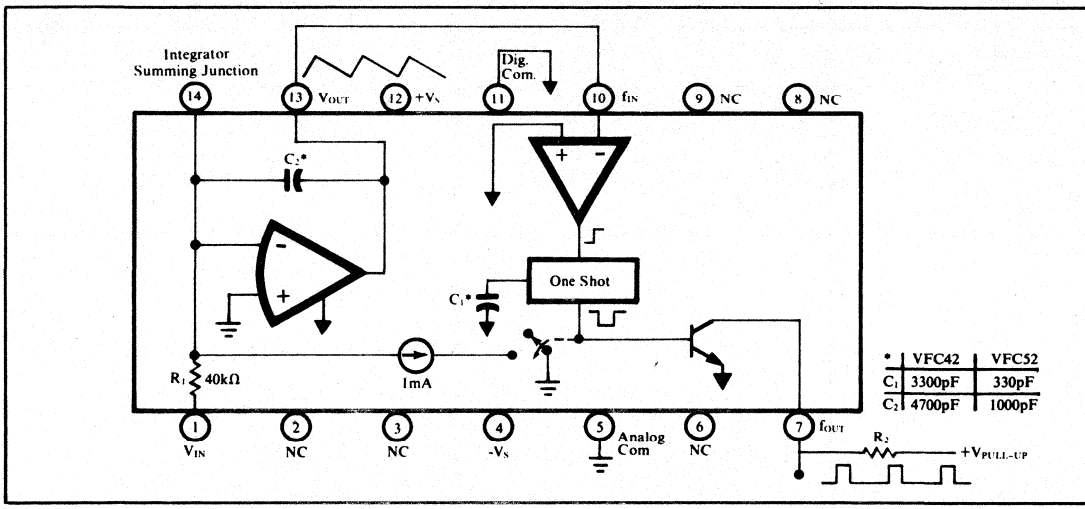


FIGURE 1. Functional Block Diagram

DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity, the maximum deviation of the actual transfer function from a straight line drawn between the end points (full scale input and zero input), is the true measure of a VFC's performance and is a function of full scale frequency. The high linearity of VFC42 and VFC52 makes these devices an excellent choice for use in A/D converters with 10 (0.05%) and 12 bit (0.012%) accuracy and for highly accurate analog data transfer over long lines in noisy environments.

FREQUENCY STABILITY VS TEMPERATURE

Frequency stability vs temperature is expressed as parts per million of full scale range per °C. Since frequency drift is a function of the specified temperature range, the "SM" models will meet the lower drift specifications of the "BM" models over the narrower -25°C to +85°C temperature range. Error sources do not drift linearly over temperature, consequently the units drift much less at higher temperatures.

RESPONSE TIME

Response time of VFC42 and VFC52 to input signal level changes is specified for a full scale step and is 1 μsec plus 1 period of the new frequency. Typical settling time to within rated linearity for a positive input voltage step of +10V is 101 μsec for VFC42 and 11 μsec for VFC52.

ELECTRICAL SPECIFICATIONS

Specifications at T_A = +25°C and ±15VDC power supplies unless otherwise noted.

MODEL	VFC42			VFC52			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Full Scale Frequency		10			100		kHz
INPUT							
Analog Input (V/F)							
Voltage Range	0		+10	0		+10	V
Current Range	0		+0.25	0		+0.25	mA
Input Bias Current (pin 14)							
Inverting Input		6	8		6	8	nA
Input Offset Voltage							
(trimmable to zero)		100	200		100	200	µV
Input Impedance (pin 1)	32	40	48	32	40	48	kΩ
Frequency Input (F/V) (pin 10)							
Logic Levels							
Logic "0"	$-V_{CC}$		-0.6	$-V_{CC}$		-0.6	V
Logic "1"	+1.0		$+V_{CC}$	+1.0		$+V_{CC}$	V
Pulse Width Range (t_2, Fig. 6)	0.1		15	0.1		1.5	µsec
Impedance	1 ‖ 10	1.2 ‖ 10		1 ‖ 10	1.2 ‖ 10		MΩ ‖ pF
TRANSFER CHARACTERISTICS							
Transfer Functions	$f_{OUT} = V_{IN}$ (1.00 x 10^3) $V_{OUT} = f_{IN}$ (10.0 x 10^{-4})			$f_{OUT} = V_{IN}$ (1.00 x 10^4) $V_{OUT} = f_{IN}$ (10.0 x 10^{-5})			Hz VDC
Accuracy							
Full Scale Gain							
(adjustable to zero)		0.1	0.2		0.1	0.2	%
Linearity Error							
0.01Hz ≤ F ≤ 10kHz		0.005	0.01				% of FSR[1]
0.1Hz ≤ F ≤ 100kHz					0.025	0.05	% of FSR
Offset Error (pin 1)		0.001	0.002		0.001	0.002	% of FSR/%
Power Supply Sensitivity[2]		0.0015	0.002		0.0015	0.002	% of FSR/%
Temperature Stability							
Analog Input							
Full Scale Drift (gain & offset)							
Grade: BP (hot/cold)[3]		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
BM		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
SM		±30/±60	±50/±100		±30/±60	±50/±150	ppm/°C
Offset Drift							
Grade: BP		±1	±3		±1	±3	ppm of FSR/°C
BM		±1	±3		±1	±3	ppm of FSR/°C
SM		±1	±3		±1	±3	ppm of FSR/°C
Frequency Input							
Full Scale Drift (gain & offset)							
Grade: BP (hot/cold)[3]		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
BM		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
SM		±30/±60	±50/±100		±30/±60	±50/±150	ppm/°C
Dynamic Response							
Settling Time to within linearity specification for full scale input step	1 period of new frequency + 1µsec			1 period of new frequency + 1µsec			
Overload Recovery Time	1 period of new frequency + 1µsec			1 period of new frequency + 1µsec			
OUTPUT							
Voltage Output							
Voltage Range	0 to +10			0 to +10			V
Output Current	+10			+10			mA
Output Impedance (closed loop)			1			1	Ω
Capacitive Load			100			100	pF
Frequency Output (open collector)							
Pulse Characteristics							
Logic "1"			$+V_{PULL-UP}$			$+V_{PULL-UP}$	V
Logic "0" (at I_O ≤ -8mA	0		+0.4	0		+0.4	V
Pulse Width	20	25		2.0	2.5		µsec
Output Sink Current							
(Logic "0", ≤ 0.4V)			8			8	mA
Output Leakage Current							
(Logic "1")			100			100	nA
Fall Time							
I_{OUT} = -5mA, C_{LOAD} = 500pF			400			400	nsec
POWER SUPPLY REQUIREMENTS							
Rated Supplies		±15			±15		V
Supply Range	±9		±20	±9		±20	V
Supply Drain (independent of operating frequency)		±5.5	±6.5		±5.5	±6.5	mA

ELECTRICAL SPECIFICATIONS CONTINUED:

Specifications at T_A = +25°C and ±15VDC power supply unless otherwise noted.

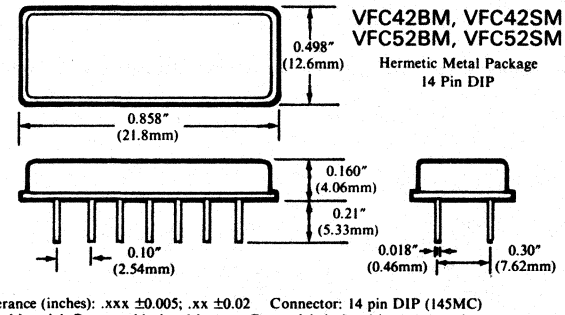
MODEL	VFC42			VFC52			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE							
Specification							
Grade: BP, BM	-25		+85	-25		+85	°C
SM	-55		+125	-55		+125	°C
Operating							
Grade: BM, SM	-55		+125	-55		+125	°C
BP	-55		+100	-55		+100	°C
Storage							
Grade: BP, BM, SM	-55		+125	-55		+125	°C

TABLE I. Electrical Specifications

ABSOLUTE MAXIMUM RATINGS above which unit may be damaged.	
Supply Voltages	±22V
Output Sink Current (F_{output})	50mA
Output Current (V_{output})	+20mA
Input Voltage, Pin 14	±Supply
Input Voltage, Pin 1	±Supply
Storage Temperature Range	
Grade: BP, BM, SM	-55°C to +125°C

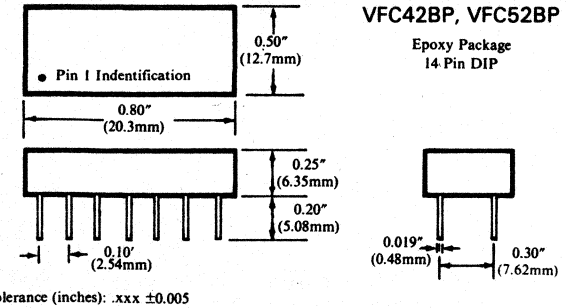
NOTES:
1. % of FSR = % of Full Scale Range.
2. Rated at full scale input and ±15V supplies.
3. Hot = +20°C to highest rated temperature; cold = lowest rated temperature to +20°C.

MECHANICAL SPECIFICATIONS



Tolerance (inches): .xxx ±0.005; .xx ±0.02 Connector: 14 pin DIP (145MC)
Case Material: Base - gold-plated kovar Cap - nickel-plated kovar or steel
Pin material and plating compositions: Conforms to Mil-Std-883, Method 2003 (solderability) except paragraph 3.2 (aging). Hermeticity: Conforms to Mil-Std-883, Method 1014, Condition C, Step 1, Fluorocarbon (gross leak) and Condition A, Helium, 5 x 10^{-4}cc/sec (fine leak)

FIGURE 2. Hermetic Metal Package Specifications



Tolerance (inches): .xxx ±0.005
.xx ±0.02
Connector: 14 pin DIP (145MC)
Case Material: epoxy

Pin material and plating composition:
Conform to Method 2003 (solderability)
of Mil-Std-883 (except paragraph 3.2).

FIGURE 3. Epoxy Package Specifications

CONNECTION DIAGRAMS

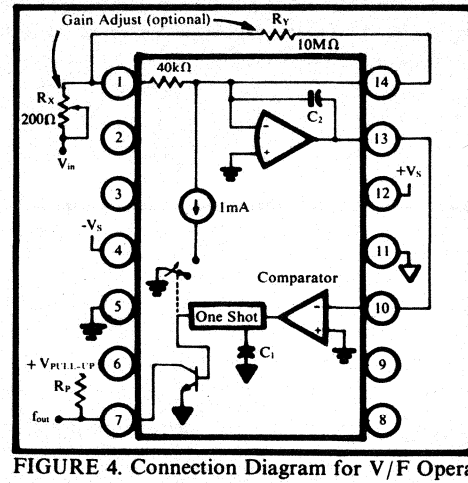


FIGURE 4. Connection Diagram for V/F Operation

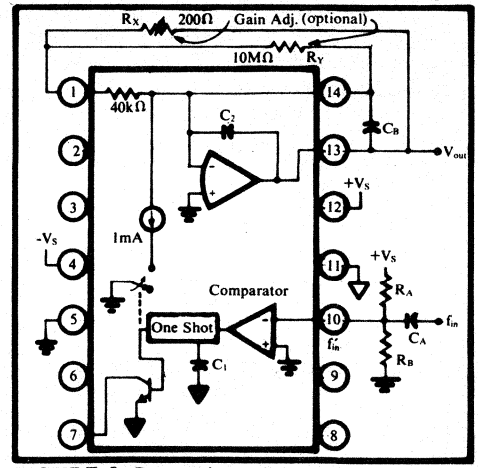


FIGURE 5. Connection Diagram for F/V Operation

OPERATING INSTRUCTIONS

VFC42 and VFC52 can be connected for either V/F or F/V operation. Only one external component, the output pull-up resistor, is required for V/F operation. F/V operation requires the pull-up resistor and input biasing components. Gain error is the most significant error in either configuration and may be nulled out with the optional trim circuit (R_X and R_Y). The offset error is laser trimmed at the factory and no external adjustment is required.

Power Supply Consideration: Power supplies stable to within ±1% are recommended to maintain conversion accuracy. Each supply should be by-passed with 0.01μF capacitors located as close to the VFC as possible.

VOLTAGE-TO-FREQUENCY OPERATION

Calculating the Value of Pull-Up Resistor, R_P: The open collector output can be used to drive DTL, TTL, CMOS or discrete circuits. The maximum collector current allowed for TTL circuits in logic 0 is 8mA. R_P may be calculated by this equation:

$$R_P \text{ min} = V \text{ pull-up}/(8mA - i_{LOAD}).$$

A 10% carbon composition resistor is suitable for this purpose. The collector current may be as great as 30mA if a logic 0 voltage of 1.0V is tolerable.

Gain Adjustment Procedure: Connect R_X and R_Y as shown in Figure 4. Apply positive full scale voltage to the input and adjust R_X until 10kHz ±1Hz (VFC42) or 100kHz ±10Hz (VFC52) is obtained at f_{OUT}. R_X and R_Y should have temperature coefficients of < 500ppm. These external components will add less than 5 ppm/°C to temperature drift.

FREQUENCY-TO-VOLTAGE OPERATION

Input Characteristics: VFC42 and VFC52 can be connected as frequency-to-voltage converters as shown in Figure 5. f_{IN} should be a positive pulse train with minimum pulse width of 1.0μsec and rise and fall times of ≤ 300nsec. The input train (f_{IN}) is differential and applied to the input of the comparator (pin 10). Refer to Figure 6. Threshold voltage of the comparator lies between -0.6 and +1.0V. When comparator input is less than -0.6V it triggers the one shot.

Selecting R_A, R_B, and C_A: Input components R_A, R_B and C_A are selected so that the trigger voltage (V_T) is more negative than -0.6V and transition time (t_2) is between 0.3 and 15 μsec for VFC42 and between 0.3 and 1.5 μsec for VFC52. Table II gives values for input components for several common signal sources. Values for R_A, R_B and C_A may be selected by the user when input signal characteristics differ from those listed. Conditions described above for trigger voltage and transition time must be observed.

Equations to calculate trigger voltage and transition time are:

$$V_T = V_B + V_{in}\,(e^{-t_i/\tau} - 1)$$

$$t_2 = -\tau \ln \left[\frac{1 - V_B}{V_{in}\,(e^{-t_i/\tau} - 1)} \right]$$

V_B = Bias voltage on pin 10

V_{in} = Input pulse amplitude

t_1 = Input pulse width

τ = Time constant of R_A, R_B, C_A as connected

If input pulse amplitude is greater than $+V_S$ - 1V, a voltage larger than $+V_S$ will be applied to pin 10. Since this may damage the unit, a diode connected across R_A with the cathode tied to $+V_S$ is required.

Output Characteristics: Selecting C_B: Output ripple voltage amplitude is inversely proportional to the input frequency and to the value of the integrating capacitance, $C_2 + C_B$. Ripple, therefore, will be greatest at low frequencies and at small values of $C_2 + C_B$. Conversely, time required for the output to settle is directly proportional to the value of $C_2 + C_B$ and is least with small values of $C_2 + C_B$. There is, therefore, a trade-off between output ripple amplitude and output settling time.

Because ripple amplitude is greatest at lowest input frequency it is at this point where the trade-off will usually be made. Ripple voltage and integrating capacitance value are related in this manner:

$$C_B = \frac{-(25 \times 10^{-6})t_{sec}}{\ln \left[1 - \frac{V_{Ripple}}{30V}\right]} \text{ farads}$$

where t is equal to 25 μsec in the VFC42 and 2.5 μsec in the VFC52 and C is the integrating capacitance.

Input Type	V_{INPUT} (V)		V_{BIAS} (V)	VFC42			VFC52		
	Low	High		R_A (kΩ)	R_B (kΩ)	C_A (pF)	R_A (kΩ)	R_B (Ω)	C_A (pF)
TTL	≤+0.4	≥ +2.8	+1.1	12	1.0	1000	8.2	680	680
5V CMOS	≤+0.5	≥ +4.5	+1.2	18	1.6	2200	9.1	820	680
10V CMOS	≤+1.0	≥ +9.0	+1.1	12	1.0	2200	6.2	510	680
15V CMOS	≤+1.5	≥+13.5	+1.1	12	1.0	2200	6.2	510	680

TABLE II. F/V Input Component Selection.

Calculating output response time versus integrating capacitance is an iterative process and is plotted in Figure 7. These curves are for zero to full scale input frequency transitions. If faster response time with lower ripple voltage is desired, a low pass filter can be connected in series with the output.

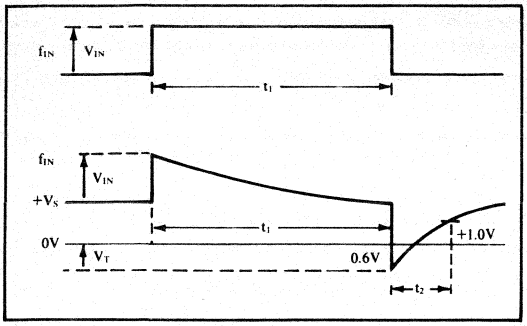


FIGURE 6. F/V Input Waveforms

Gain Adjustment Procedure: Connect R_X and R_Y as shown in Figure 5. Apply full scale frequency to the input and adjust R_X until full scale voltage is +10V ±1mV (discounting ripple). R_X and R_Y should have temperature coefficients of < 500 ppm. These external components will add less than 5 ppm/°C to temperature drift.

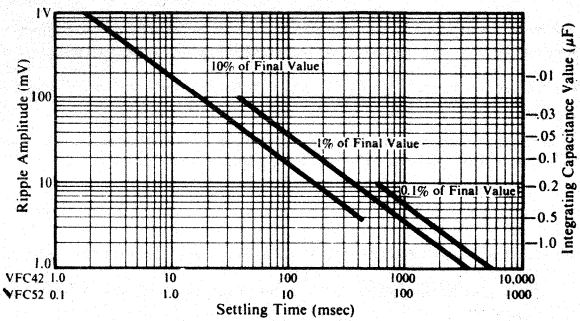


FIGURE 7. F/V Mode Output Settling Time vs. Ripple Voltage Amplitude for Full Scale Frequency Change

APPLICATION

VFC42 and VFC52 can be used to convert analog data into a digital pulse train for transmission over long lines through high EMI environments. Illustrated in Figure 8 is a V/F, F/V combination that can be used to transmit analog data of 0 to +10V span over a 100Ω shielded, twisted-pair. The voltage ripple amplitude at the output will be 10mV for a 10V output and the settling time for a full scale 0 to +10V change is 60 milliseconds.

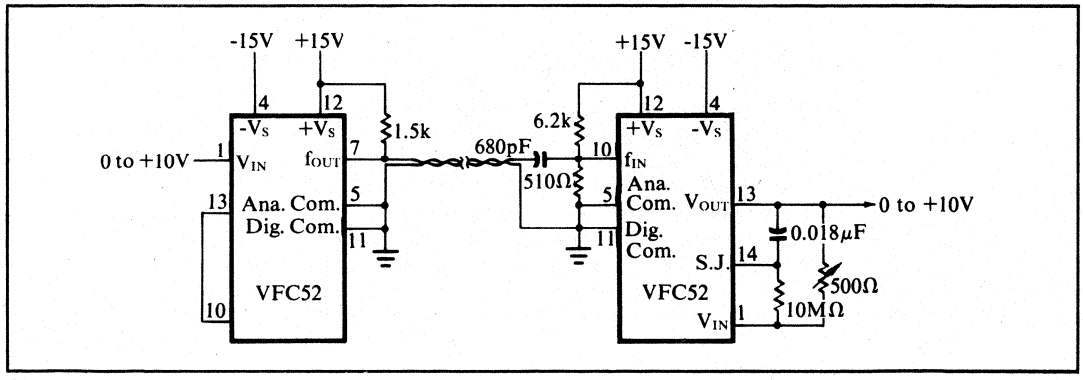
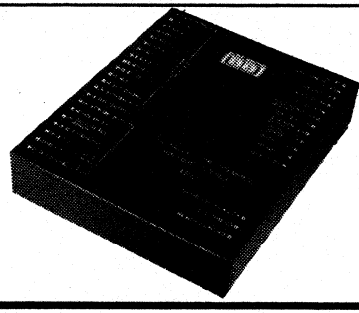


FIGURE 8. V/F, F/V Data Transmission Circuit

BURR-BROWN



4800
4801

DIGITALLY-PROGRAMMED VOLTAGE SOURCE

FEATURES

- CURRENT SOURCE PROGRAMMING
- ±60V, 200mA OUTPUT
- FULL DIGITAL PROGRAMMING OF:
  - Voltage Magnitude
  - Voltage Range
  - Voltage Polarity
  - Current Limit
- DRIVES CAPACITIVE LOADS TO 1μF

DESCRIPTION

The 4800 and 4801 are the industry's first modular digitally-programmed voltage sources (DPVS) designed for use in computer controlled test equipment and process control equipment as well as laboratory applications.

They provide precision regulated DC output voltages at a fraction of the cost of comparable rack mounted supplies. The units consist of digital to analog converters, power output circuitry and all the digital controls and interfaces necessary to allow easy computer control.

Each unit has selectable ±10V or ±60V output ranges. The resolution varies from 2.44mV to 100mV depending upon the model selected and the range used. The load regulation is ±0.0015% full load to no load and line regulation is as good as ±0.003%. The voltage output when driving a resistive load will settle to ±0.01% of final value in 100μsec for any input change.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-306B

Printed in U.S.A. July, 1978

SPECIFICATIONS

The 4800/4801 will operate over a 0 to +70°C temperature range.
All specifications are typical at 25°C unless specified otherwise.

OUTPUT VOLTAGE

The Models 4800 and 4801 provide a precision regulated DC voltage output. The magnitude of the voltage is determined by a digital control word. (12 bits Binary for the 4800; 12 bits Binary Coded Decimal, BCD, for the 4801.) Two bipolar output ranges (10 V and 60 V) are provided. The output polarity and range are programmable independently of the input magnitude word.

ACCURACY

Full Scale Error: The -10 V range has a maximum absolute error of ±20 mV at full scale. This error may be externally trimmed to zero as described in installation instructions on page 5-208. The full scale output voltage on any range will then be accurate within ±0.01%

Linearity Error: A programmed output voltage will be accurate within ±0.012% of the actual full scale value for the range and polarity programmed.

Absolute Error: A programmed output voltage will have a maximum error of ±0.012% if the full scale error is trimmed to zero.

NOISE – (10 Hz to 10 MHz bandwidth)

Range	Noise
10 V	500 μV rms
60 V	1 mV rms

STABILITY - (ppm of output voltage)

Range	Drift vs. Temperature (max)	Drift vs. Time
10 V	(20 ppm +20 μV)/°C	(100 ppm + 100 μV)/mo.
60 V	(20 ppm + 120 μV)/°C	(100 ppm + 600 μV)/mo.

Output drift over a 90 day period will be approximately 300 ppm +300 μV on the 10-volt range and 300 ppm +1.8 mV on the 60-volt range.

RESOLUTION – (also see Table 1)

4800 (12 bit Binary plus sign)	0 to +10 V in 2.44 mV steps 0 to +60 V in 14.65 mV steps
4801 (12 bit BCD plus sign)	0 to +9.99 V in 10 mV steps 0 to +60 V in 100 mV steps

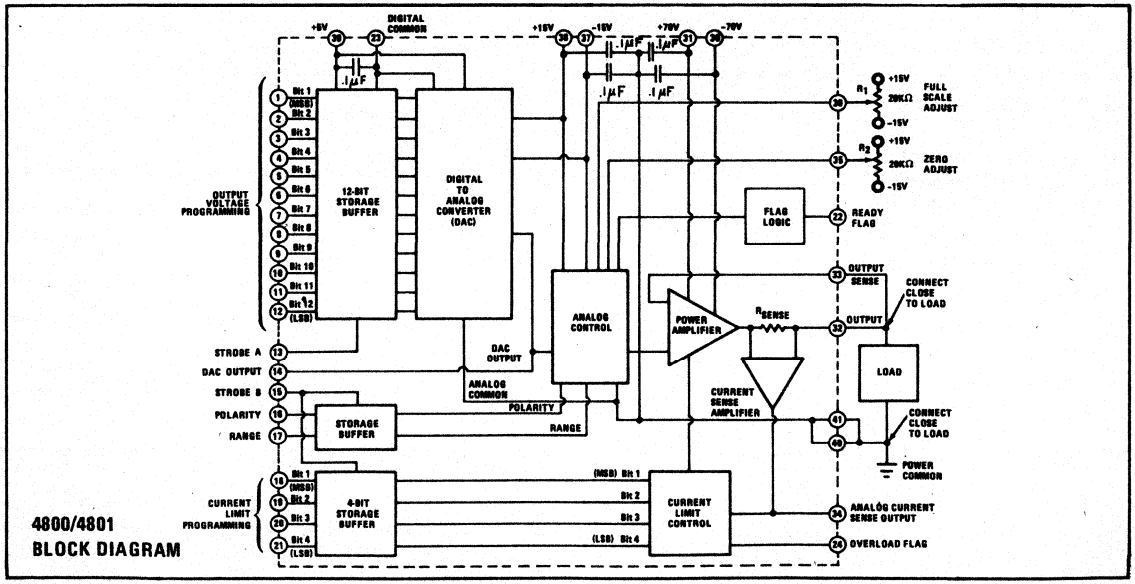
TABLE I. Digital Inputs vs. Analog Output.

	DIGITAL INPUTS		ANALOG OUTPUT (pin 32)	
	Polarity	Output Voltage MSB . . . . LSB	±10 V Range ("0" on pin 17)	±60 V Range ("1" on pin 17)
	(pin 16)	(pin 1). . . (pin 12)		
4800	1	111111111111	10.0000 V	+60.0000 V
	1	111111111110	+9.99756	+59.98535
	1	000000000001	+0.00244	+0.01465
	1	000000000000	0.0000	0.00000
	0	000000000000	0.0000	0.00000
	0	000000000001	- 0.00244	- 0.01465
	0	111111111110	- 9.99756	- 59.98535
	0	111111111111	- 10.0000	- 60.0000
4801	1	1001 1001 1001	+9.99 V	-----* V
	1	1001 1001 1000	+9.98	-----*
	1	0110 0000 0001	+6.01	-----*
	1	0110 0000 0000	+6.00	+60.0
	1	0101 1001 1001	+5.99	+59.9
	1	0000 0000 0001	+0.01	+00.1
	1	0000 0000 0000	0.00	00.0
	0	0000 0000 0000	0.00	00.0
	0	0000 0000 0001	- 0.01	- 00.1
	0	0101 1001 1001	- 5.99	- 59.9
	0	0110 0000 0000	- 6.00	- 60.0
	0	0110 0000 0001	- 6.01	-----*
	0	1001 1001 1000	- 9.98	-----*
	0	1001 1001 1001	- 9.99	-----*

*If commanded to go above 60.0 volts, the output may increase to 62 V or so in 100 mV steps but regulation may not be within specification.

LOAD REGULATION

Output Voltage will change less than ±0.0015% for a load current change of ±200 mA (provided output current limit is programmed to maximum value).



4800/4801 BLOCK DIAGRAM

LINE REGULATION (Supply Sensitivity)

Variations in the power supply voltages will cause small changes in the output voltage. Power supply sensitivity is the ratio of the output voltage change to the power supply voltage change.

Range	$\Delta V_O/\Delta V_S$ 5V Supply	$\Delta V_O/\Delta V_S$ ±15V Supplies	$\Delta V_O/\Delta V_S$ ±70V Supplies ΔV_S@DC	$\Delta V_O/\Delta V_S$ ±70V Supplies ΔV_S@120Hz
10V	10 μV/V	200 μV/%	20 μV/V	160 μV/V
60V	10 μV/V	1.2 mV/%	20 μV/V	1.0 mV/V

OUTPUT CURRENT

The 4800/4801 have current limits that are digitally programmable. An overload flag signals a current limit condition. The DPVS will source up to 200 mA of current but the maximum current sinking ability is 100 mA. (See Figures 1 and 2 for more information.) The 4800/4801 are protected for momentary (up to 1 minute) short circuits to ground at full current (see Figure 2 for continuous short circuit to ground). The current limit circuitry is not activated in the current sink mode, but the overload flag is activated when the sink current exceeds the programmed current limit value.

CURRENT LIMIT RESOLUTION

4 bit Binary: 0 to ±200 mA in 13.3 mA steps.

CURRENT LIMIT ACCURACY

The actual current limit value will be accurate within ±5% of programmed value ±7 mA.

ANALOG CURRENT SENSE OUTPUT

A DC output voltage proportional to the output current is provided $E_{sense} = \frac{I_o}{20}$ for E_{sense} in volts, I_o in mA. E_{sense} is positive for current flowing out of pin 32. The accuracy of the analog current sense output is ±0.2% of reading ±100 μA. If more accuracy or a different E_{sense} voltage range is required, the user may build external current sense circuits as shown on pages 5-204 thru 5-206.

OUTPUT STAGE POWER DISSIPATION

The graphs of Figures 1 and 2 are an aid in determining the amount of internal power dissipation in the 4800 or 4801 under various loading conditions. Note in Figure 2 that output power up to 12 watts (60 Vdc @ 200 mA) can be provided safely. Safe operating areas for different heat sinking conditions at 25°C are indicated by the horizontal lines.

Line (1) represents the safe limit (8-1/2 watts) when mounted on a sheet of aluminum 0.09 inches thick and 35 square inches in total area (see mating connector, page 5-202).

Line (2) represents the internal dissipation limit (7 watts) for operation on a printed circuit board of 0.061 inches thickness, 35 square inches board area, and 80% copper clad.

Line (3) represents the maximum allowable internal dissipation (6 watts) when operating with no heatsink.

Any output loading condition which corresponds to an internal power dissipation lower than these limits is a safe operating point for that set of heatsinking conditions. For operation at ambient temperatures above +50°C, the maximum safe internal power dissipation limits should be reduced by 0.1 watts/°C. For instance, with no heatsink, the maximum internal power dissipation at 60°C is 5 watts. Figures 1 and 2 may still be used with lower power dissipation limits (P_{Diss}).

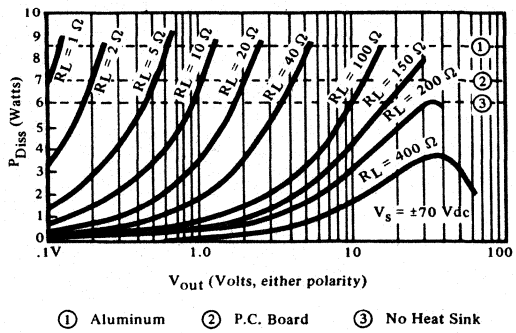


FIGURE 1. Internal Power Dissipation at 25°C vs. Output Voltage and Load Resistance.

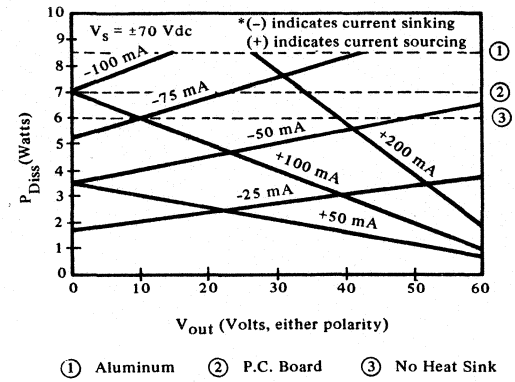


FIGURE 2. Internal Power Dissipation at 25°C when using ±70 Vdc High Voltage Power Supply.

HIGH VOLTAGE SUPPLIES LESS THAN ±70 Vdc

If high voltage power supplies less than ±70 Vdc are used, other combinations of voltage and current than shown in Figure 2 can be used. For instance, 200 mA may be sourced at even 0 volts output if ±30 Vdc high voltage supplies are used. The general rule is that

$$(|V_{supply}| \pm |V_{out}|)\ (\text{output current}) \qquad \text{eq. 1}$$

must be kept lower than the power dissipating ability (6, 7 or 8-1/2 watts), where + $|V_{out}|$ is used if the output is sinking current and - $|V_{out}|$ is used if the output is sourcing current.

CAPACITIVE AND INDUCTIVE LOAD DRIVING CAPABILITIES

The 4800/4801 will drive capacitive loads to 1 μF. Instabilities may result when driving larger capacitive loads. See Figure 3 for settling time versus capacitive load information. The ready flag will signal at the end of 100 μsec even though the actual settling time with capacitive load is longer. When driving inductive loads, the output should be protected with diodes to the high voltage supplies.

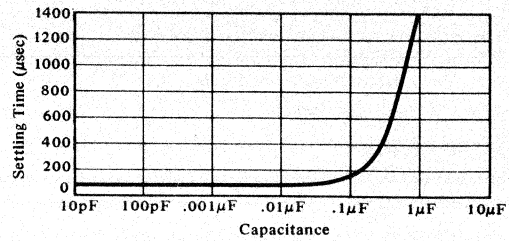


FIGURE 3. Typical Settling Time vs. Capacitive Load.

PROGRAMMING

VOLTAGE PROGRAMMING SPEED

The output voltage will settle within 0.01% of final value in 100 μsec. This settling time assumes a nonreactive load and includes any combination of magnitude, range, or polarity change. See Figure 3 for settling time with capacitive load. The ready flag is simply a 100 μsec timer that signals the end of the programming interval.

VOLTAGE PROGRAMMING TRANSIENTS

The maximum voltage overshoot is 100 mV for any programmed voltage change.

CURRENT LIMIT PROGRAMMING

The current limit value may be re-programmed at any time. If the load current exceeds the new current limit value, the current limit circuitry will be activated within 100 μsec. If the new current limit value causes the DPVS to come out of current limit, the output voltage will settle to 0.01% of final value in 100 μsec. If the load current attempts to exceed the current limit value, it will be held at the programmed value. When the load current drops below the programmed value, the output voltage will settle to 0.01% of final value within 100 μsec.

POWER SUPPLY REQUIREMENTS

REGULATED SUPPLIES

Voltage	Current
±15 Vdc ±1 Vdc	±40 mA
+5 Vdc ±0.5 Vdc	+220 mA

HIGH VOLTAGE SUPPLIES

±70 Vdc nominal	±30 mA plus load current

Supplies less than ±70 Vdc may be used to power the output. The only requirement is that the high voltage supply be 10 volts larger than the maximum required 4800 output voltage. That is, if ±16 Vdc are the maximum power output voltages required then ±26 Vdc supplies may be used. If 0 to 60 V is required, a +70 V and a -10 V supply may be used. If +10 Vdc to +60 Vdc is required, the negative supply input may simply be grounded while the positive supply requires +70 Vdc. If the high voltage supply is less than 70 volts, the maximum output voltage will be less than 60 volts but the size of each digital step is still the same. For instance, the 4801 will have 100 mV steps in the "high" range for ±70 volt or ±25 volt high voltage supplies.

DIGITAL INTERFACE SPECIFICATIONS

DIGITAL INTERFACING

Input Description - The 4800/4801 has 18 digital input programming lines and two associated strobes (see Figure 4). Strobe A controls the 12 voltage magnitude program bits. Strobe B controls the 4 current limit bits and the polarity and range selection bits.

LOGIC SENSE AND FUNCTION

1. Voltage magnitude program bits: logic high corresponds to a true state, i.e., all bits "high" programs full scale output while all bits "low" programs zero volts out.
2. Current limit program bits: logic high input level programs current limit bit value on, i.e., all four bits high programs maximum output current (200 mA).
3. Polarity: logic high = +V out
   logic low = -V out
4. Range: logic high = 60 V range
   logic low = 10 V range
5. Strobes: logic low = input storage buffers in "store" mode.
   logic high = input storage buffers in "track" mode, i.e. output of storage buffer follows input.
6. Flag outputs:
   (1) Ready Flag
   logic low: device is still responding to a programmed output change.
   logic high: device has settled to proper programmed value.

Note: ready flag is meaningless if the overload flag indicates an overload.

   (2) Overload Flag
   logic low: device is overloaded (output in current limit)
   logic high: device is not in current limit.

LOGIC LOADING AND FANOUT

(All digital input and output logic levels are compatible with standard series 7400 TTL levels and 930 series DTL levels.)

1. All digital inputs (except strobes): two 7400 TTL loads per line "1" @ 80 μA – "0" @ -3.2 mA.
2. Strobe A: 26 logic loads "1" @ 1040 μA- "0" @ -41.6 mA.
3. Strobe B: 14 logic loads "1" @ 560 μA- "0" @ -22.4 mA.
4. Flag outputs - each flag output will drive a normalized fanout of ten 7400 TTL loads. "1" @ 400 μA
   "0" @ -16 mA

Note: TTL buffer no. 7440 will provide output current to drive strobe A or B. All other digital input lines may be driven from standard 7400 series TTL logic or 930 series DTL logic. Digital Input Voltages $+2.4 \leq 1 \leq +5.0$ V
$0 \text{ V} \leq 0 \leq +0.8$ V

SYSTEM TIMING

General Notes on System Timing (See Figure 4):

1. The output will begin to respond to the digital program commands as soon as the strobe(s) go high.
2. The storage buffer(s) will latch according to the digital inputs present when the strobe(s) change to the low state.
3. The strobe(s) may be left continuously in a high state and the analog output will follow the digital input (e.g., the output of a 12-bit digital counter may be fed into the voltage programming lines and a ramp output will result). However anytime the digital inputs change while the strobe is high, the ready flag will not be valid and output transients ("glitches") may exceed the 100 mV specification. Also, if a digital input changes state during the last 50 nsec of the strobe, the actual value stored in the buffer will be unpredictable.

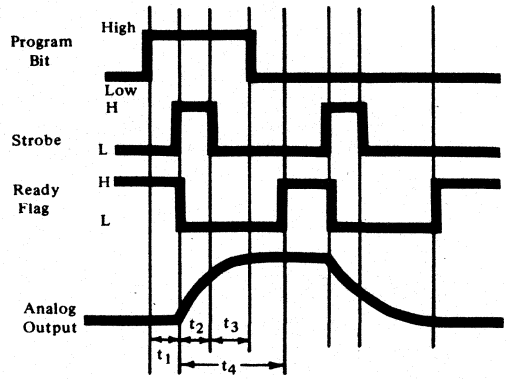
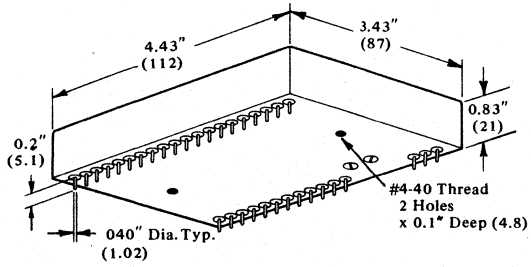
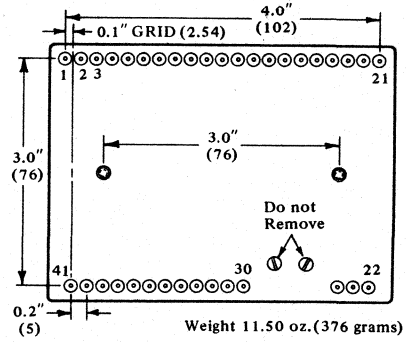


FIGURE 4. Timing Diagram.

MECHANICAL SPECIFICATIONS

Pin material and plating composition meet method 2003 (solderability) of MIL-STD-883 [except paragraph 3.2]
Dimensions in millimeters are shown in parentheses.

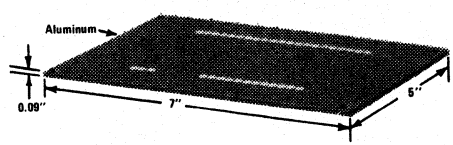




Weight 11.50 oz.(376 grams)

MATING CONNECTOR

The 4301MC is a complete 35 square inch aluminum mounting connector. The 4800/4801 used with the 4301MC will operate at 8.5 watts dissipation as indicated by line (1) in Figures 1 and 2.



Heat sink compound such as Dow Corning 340 silicone is recommended.

SYSTEMS APPLICATIONS

MINICOMPUTER CONNECTIONS

PDP-8

Figure 5 shows a typical interconnection schematic to use the 4800/4801 with a PDP-8 minicomputer. When the 12 data lines have the proper programming data, the address bus to the M103 will be decoded to allow IOP1 or IOP2 to strobe the proper data into the 4800/4801's internal storage registers.

The ready flag may be used to interrupt the computer or command it to skip by using an inverter on M103 and bus drivers from M623 as shown. The computer may then be programmed to either repeatedly check for the ready flag or operate on an interrupt basis to indicate when the 4800/4801 has settled to its programmed output.

Note: The interface for the PDP-8E, PDP-8F and PDP-8M requires only the *M1705 interface card which fits within the computer mainframe.

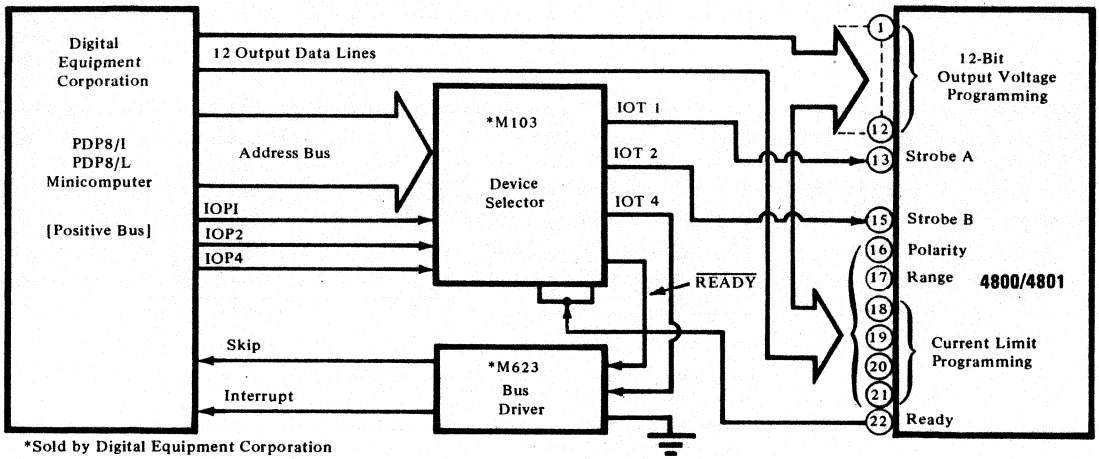


FIGURE 5. Interface Between 4800/4801 and PDP8 Minicomputer.

PDP-11

Figure 6 shows interconnection information for a PDP-11 minicomputer. The 4800/4801 is programmed as shown and the two replies (overload and ready) are returned to the minicomputer to be inspected as desired. Note: The interface may be done using only the *DR11-C interface card which fits within the main frame of the PDP-11.

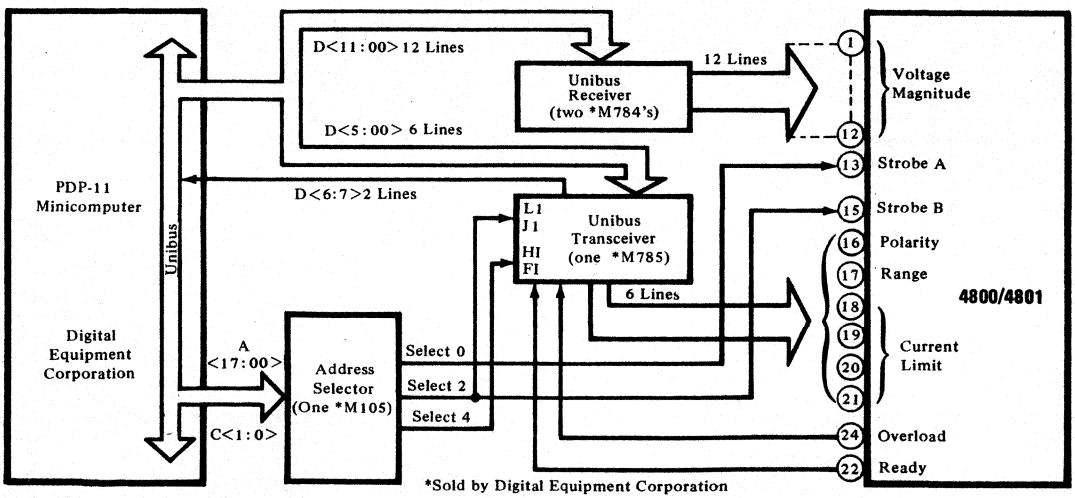


FIGURE 6. PDP-11/4800 Interconnection.

NOVA

Figure 7 shows a typical interconnection schematic to use the 4800/4801 with a NOVA minicomputer. The 4040 General Purpose Interface card which fits within the minicomputer mainframe contains all the circuitry necessary to do the interface. The overload flag (pin 24 of 4800/4801) is shown treated as an input data word.

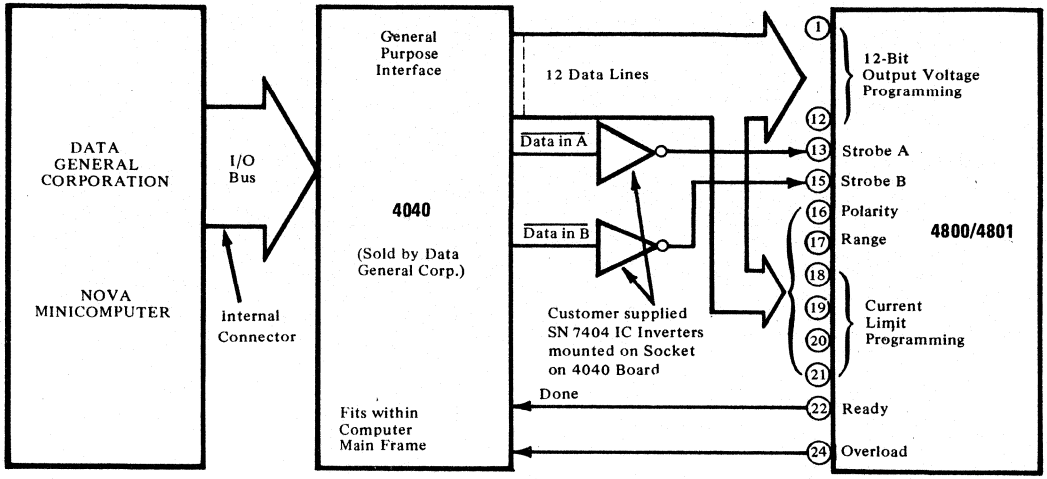


FIGURE 7. Interface between 4800/4801 and NOVA Minicomputer.

CIRCUIT APPLICATIONS

EXTERNAL CURRENT SENSING

If output currents less than 500 μA must be accurately sensed or if a different E_{sense} voltage range is required, one of the following circuits may be used to provide a current sense output.

Moderate DPVS Output Accuracy

If the voltage across the sensing resistor (R_S in Figure 8 below) can be tolerated as an output voltage error and if a sensing resistor can be placed in series with the load to ground, the circuit shown in Figure 8 may be used to sense current. The amplifier simply amplifies the voltage developed across the sense resistor (R_S).

DESIGN EQUATIONS

The transfer function equation for this circuit is:

$$e_O = (1 + \frac{R_2}{R_1})\ (I_L R_S) \qquad I_L = \frac{e_O}{(1 + \frac{R_2}{R_1})\ R_S}$$

If e_O and (I_L R_S) are kept at 10 volts or below, a good, general purpose op amp such as Burr-Brown's 3500A may be used to provide the current sense output. The common mode input impedance must be high and the bias current must be low enough to introduce small errors.

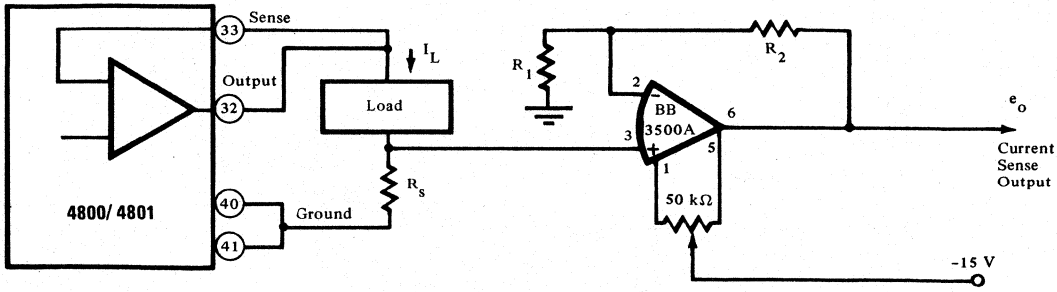


FIGURE 8. External Current Sensing with Moderate DPVS Output Accuracy (Outside Voltage Feedback Loop).

NOTE: If only moderate voltage accuracy is needed and Figure 8 cannot be used, the circuit shown in Figure 9 may be connected outside the voltage sense loop. This means that pin 33 would be connected at point e_1 rather than at the load, and amplifier 3 would not be needed.

DESIGN EXAMPLE

Assume currents in the 1 to 100 μA range must be sensed. With R_S = 1 kΩ the maximum voltage drop ($I_L R_S$) would be (100 x 10^{-6}A) ($10^3\ \Omega$) = 100 mV. If

$$\frac{R_2}{R_1} = 99, e_{o(max)} = (1 + \frac{R_2}{R_1})(I_L R_S) = (100)(100\text{ mV}) = 10\text{V}.$$

The output sensitivity is $\frac{10\text{ V}}{100\ \mu\text{A}} = 100\text{ mV}/\mu\text{A}$.

ERRORS

The common mode input impedance of the 3500A is 5 x $10^9\ \Omega$. $\frac{100\text{ mV}}{5 \times 10^9\Omega} = 20 \times 10^{-3} \times 10^{-9} = 20$ pA is the current drawn due to the input impedance. The 30 nA bias current of the 3500A completely overshadows the 20 pA. The bias current error is

$$\frac{30 \times 10^{-9}\text{ A}}{100 \times 10^{-6}\text{A}} = 0.3 \times 10^{-3}$$

or 0.03% of full scale. If lower bias current errors are required, FET input op amps such as Burr-Brown's 3522 series (or simply a higher grade of Burr-Brown's 3500 series such as the 3500C with 15 nA bias current) may be used. Thus if the R_S, R_1 and R_2 resistances are known accurately, the current sense error will only be ±0.03%. If the maximum current sensed was 10 mA instead of 100 μA, the bias current of the 3500A would have contributed only ±0.0003% of Full Scale Error.

The voltage error added by the R_S sense resistor is a maximum of 100 mV. This is 1% voltage error if 10 volts is the maximum output or 0.18% with 60 volts out.

High DPVS Output Accuracy

If the output voltage across the load must be maintained very accurately, the current sensing circuitry must be kept within the output sense feedback loop. Figure 9 shows this circuitry. Amplifiers #1 and #2 have high impedance inputs and provide the current sense output. Amplifier #3 buffers the output sense input which draws approximately 2 mA. Note: With Amplifier #3 in the circuit, the internal current sense output will be accurate to within ±1%.

DESIGN EQUATIONS

The transfer function equation for this circuit is:

$$e_o = (1 + \frac{R_4}{R_3})(e_1 - e_2) \text{ if } \frac{R_1}{R_2} = \frac{R_4}{R_3}$$

If I_L is the output current and R_S the external sense resistor,

$$e_o = (1 + \frac{R_4}{R_3})(I_L R_S) \text{ or, } I_L = \frac{e_o}{(1 + R_4/R_3) R_S}$$

The ratios of $R_1 : R_2$ and $R_4 : R_3$ must be well matched to provide good common mode rejection and the amplifiers must have good common mode properties (Burr-Brown's 3460 is an excellent high voltage amplifier to use). The input impedance at e_2 must be high to pull no appreciable current from I_L. The input impedance in this configuration is the common mode impedance of this amplifier. For the 3460 this is 10^{11} ohms while the input bias current is only 25 pA. Thus, it will introduce no significant errors in most current measurements.

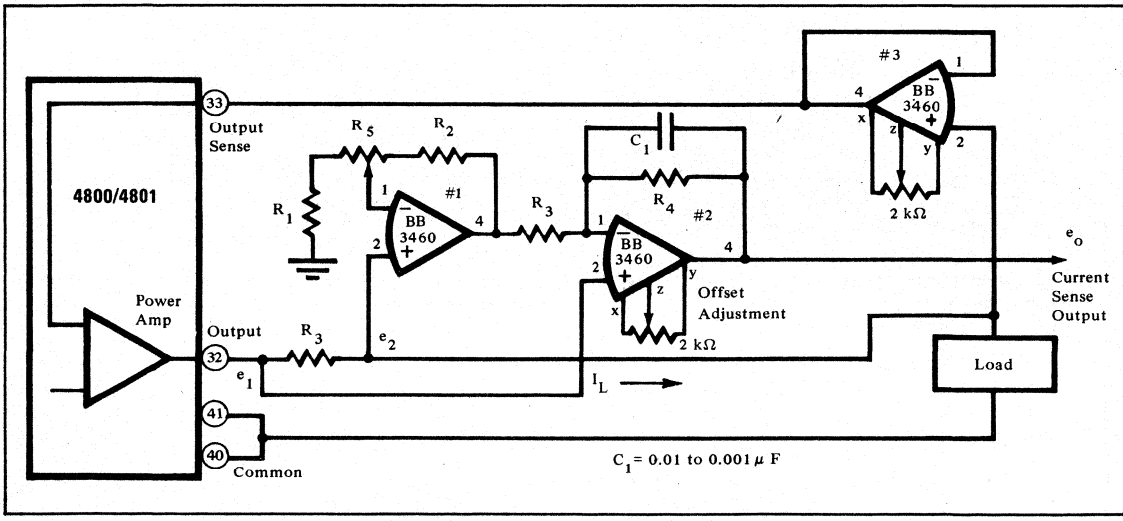


FIGURE 9. External Current Sensing with High DPVS Output Accuracy (within Voltage Feedback Loop).

NOTE: The high voltage supplies (pins 30 and 31 of the 4800/4801) may be used to power the 3460's. The supply rejection is +25 μV/V so that even a 4-volt change in supply voltage would contribute approximately (100)(100μV) = 10 mV error or 0.1% of full scale.

DESIGN EXAMPLE

As an example, assume that currents in the 1 to 100 μA range must be sensed. With R_S = 1 kΩ, the maximum difference voltage ($e_1 - e_2$) would be

$$(100 \times 10^{-6}\ A)(10^3\ ohms) = 100\ mV$$

If $\frac{R_4}{R_3} = \frac{R_1}{R_2} = 99$, $e_{o(max)} = (1 + 99)(100\ mV) = 10.00\ V$.

At the output,

$$\frac{e_{out(max)}}{I_{out(max)}} = \frac{10.00\ V}{100\ \mu A} \text{ or } 100\ mV/\mu A$$

That is, each microamp of output current would be represented by 100 mV at e_o.

OUTPUT CURRENT PROGRAMMING

The 4800/4801 may be current programmed (i.e. output current is controlled independent of the load) by providing the proper current sense feedback voltage to pin 33, the output sense. Three circuits to do this are:

1. Connect the internal current sense output, pin 34, to pin 33 the output sense.
2. Connect the current sense output generated using the moderate accuracy current sense circuit shown in Figure 8, to pin 33.
3. Connect the current sense output generated using the high accuracy current sense circuit shown in Figure 9, to pin 33.

For each of the three circuits, the output range control (pin 17) should be kept on the low range. This allows the current programming to be controlled by a ±10 V signal at pin 33 while maintaining ±60 V compliance at the output.

If two current step resolutions are required, both the 10 V and 60 V ranges may be used.

Internal Current Sense

1. This circuit is shown in Figure 10. It is extremely simple to use. The full scale output current will be 200 mA with approximately 50 μA steps for the binary units (4800) and 200 μA steps for BCD units (4801). The output current accuracy will be about ±10% of reading. Thus, if 50 mA is programmed out, the output will be accurate within approximately ±5 mA.

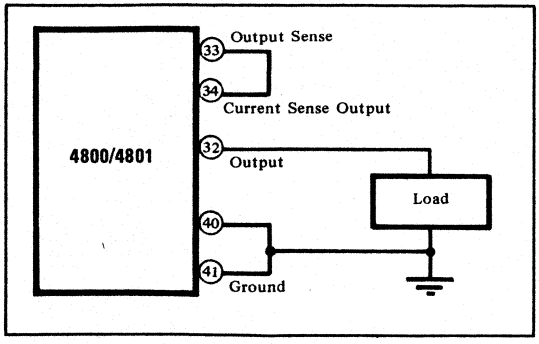


FIGURE 10. Current Programming using the Internal Current Sense Amplifier.

ERRORS

The 3460 input current with a 60 volt common mode signal is $\frac{60\ V}{10^{11}} = 600\ pA$. This error is $\frac{600\ pA}{100\ \mu A} = 0.0006\%$ of full scale current. Bias current errors are also very small since bias current is only 25 pA. The common mode errors introduce the largest errors: If the ratio of R_1/R_2 to R_4/R_3 is matched to 0.01% (ΔM) and the common mode voltage (V_{cm}) is 60 V, the common mode error due to resistor matching will be: (V_{cm}) (ΔM) = (60 V) (.0001) = 6 mV (0.06% of full scale). Potentiometer R_5 may be used to improve the resistor ratio matching.

Note: If the tolerance of each resistor (R_1, R_2, R_3 & R_4) is ΔR, the common mode error will be (V_{cm}) (4 ΔR).

External Current Sense

2. The external current sense circuit shown in Figure 8 may be used for current programming as shown in Figure 11. This is a much more accurate method than that using the internal current sense. It is an excellent one for use if the sense resistor, R_S, may be placed in series with the load to ground. The error analysis is the same as that for the circuit in Figure 8 except that the errors of the 4800/4801 must be added.

The current range of the output is selected by resistors R_S, R_1 and R_2. The load current that provides e_s = 10 V for the 4800 (or 9.99 V for the 4801) will be the full scale output current that will be programmed.

DESIGN EQUATIONS

$$e_S = (I_L R_S)\left(1 + \frac{R_2}{R_1}\right)$$

$$I_L = \frac{e_S}{R_S\left(1 + \frac{R_2}{R_1}\right)}, \quad R_S = \frac{e_S}{I_L\left(1 + \frac{R_2}{R_1}\right)}$$

When the full scale current is known, the step size may be calculated: $\left(\frac{\text{full scale current}}{\text{number of steps}}\right)$ = 1 least significant bit = step size. For 4800 (12 bits binary) number of steps = 4095
For 4801 (3 digit BCD) number of steps = 999

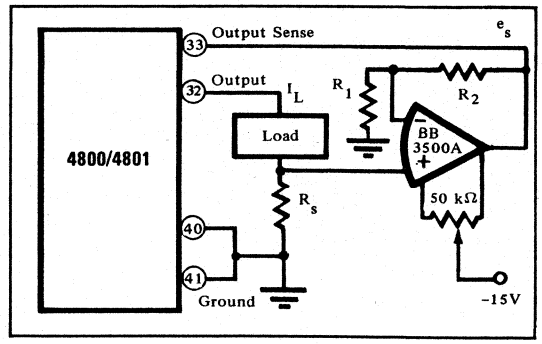


FIGURE 11. Current Programming using the External Current Sense.

DESIGN EXAMPLE

If a full scale output current of 99.9 mA (using the 4801) is required and the gain of the amplifier $(1 + \frac{R_2}{R_1})$ is 100, we have $R_S = \frac{9.99\ V}{(0.0999A)\ (100)} = 1.000\ \Omega$. Each step would be $\frac{99.9\ mA}{999} = 1\ LSB = 100\ \mu A$. For the 4800 (12-bit binary) on the other hand a full scale current of 102.375 mA would yield steps of $\frac{102.375\ mA}{4095} = 1\ LSB = 25\ \mu A$. If the gain of the amplifier is still 100 we have: $R_S = \frac{10.000\ V}{(0.102375A)\ (100)} =$ .97680 Ω. (Note: To use a 1.000 Ω resistor for R_S, the gain of the amplifier should be set to 97.680 to obtain 102.375 mA Full Scale current.) The current settling time to ±0.1% will be approximately 150 μsec.

This circuitry, with a full scale output current as described can be used to provide 10-50 mA or 4-20 mA outputs. The 60-volt compliance of the 4800/4801 will then allow load resistances of 1200 Ω or less for the 10-50 mA range and 3000 Ω or less for the 4-20 mA range. Table II shows the digital inputs necessary to provide these currents values. With other full scale currents chosen, the steps (and the digital inputs) will vary.

4800 Digital Inputs	4801 Digital Inputs	Current Output
MSB LSB	MSB LSB	
000010100000	0000 0100 0000	4 mA
000110010000	0001 0000 0000	10 mA
001100100000	0010 0000 0000	20 mA
011111010000	0101 0000 0000	50 mA
NOTE: 102.375 mA Full Scale current for the 4800 and 99.9 mA Full Scale current for the 4801.		

TABLE II. Digital Inputs for 10-50mA and 4-20mA Outputs.

3. The external current sense circuit shown in Figure 12 may be used to program current if a sense resistor cannot be placed in series with the load to ground (as shown in Figure 11) and a more accurate method than shown in Figure 10 is needed. This basic circuit is also shown in Figure 9. The circuit analysis here is the same as described before.

$$\frac{R_1}{R_2} = \frac{R_4}{R_3},\ e_s = (I_L\ R_s)\ (1 + \frac{R_4}{R_3}),\ I_L = \frac{e_s}{R_s\ (1 + \frac{R_4}{R_3})} \text{ and } R_s = \frac{e_s}{I_L\ (1 + \frac{R_4}{R_3})}$$

Current settling time will be approximately 150 μsec to ±0.1%.

To minimize inaccuracies, the circuit shown in Figure 12 should be calibrated in this sequence:

1) Connect 4800/4801 in the voltage programming mode, i.e., connect pins 32 and 33 while disconnecting the "e_S" line from pin 33. Disconnect load.

2) Monitor pin 32 and program 0 V output on the -10 V range, set the zero adjust potentiometer (connected to pin 35 as shown in figure 13) for a null.

3) Monitor the "e_S" output and null the offset of the 3460's with R_6 in figure 12.

4) Program the 4800/4801 for +60 V at pin 32. Monitor "e_S" output and adjust R_5 for a null.

5) Reconnect circuit for current programming as shown in Figure 12.

6) Program 0 mA output. Set the zero adjust potentiometer (connected to pin 35 as in figure 13) for output null.

7) Program full scale current output, set the full scale adjust potentiometer (connected to pin 36 as in Figure 13) for best full scale accuracy.

For subsequent calibration, steps 6 and 7 only need be repeated.

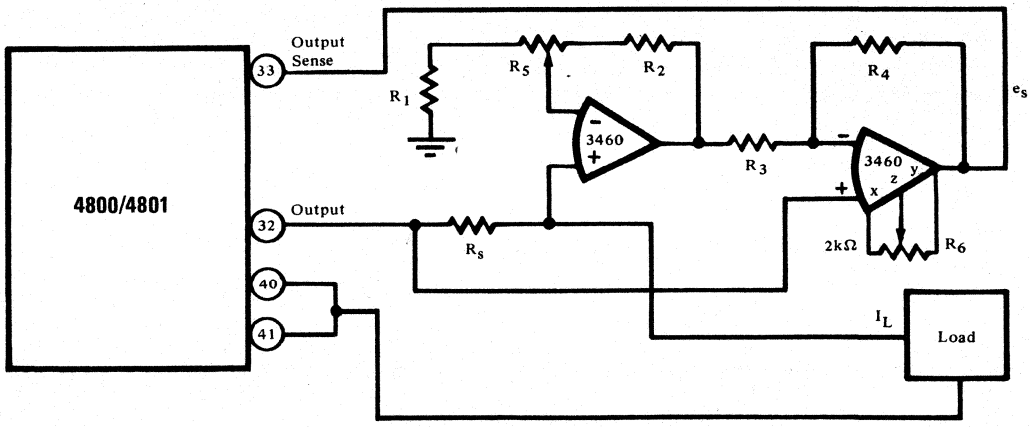


FIGURE 12. Current Programming using External Current Sense.

INSTALLATION INSTRUCTIONS

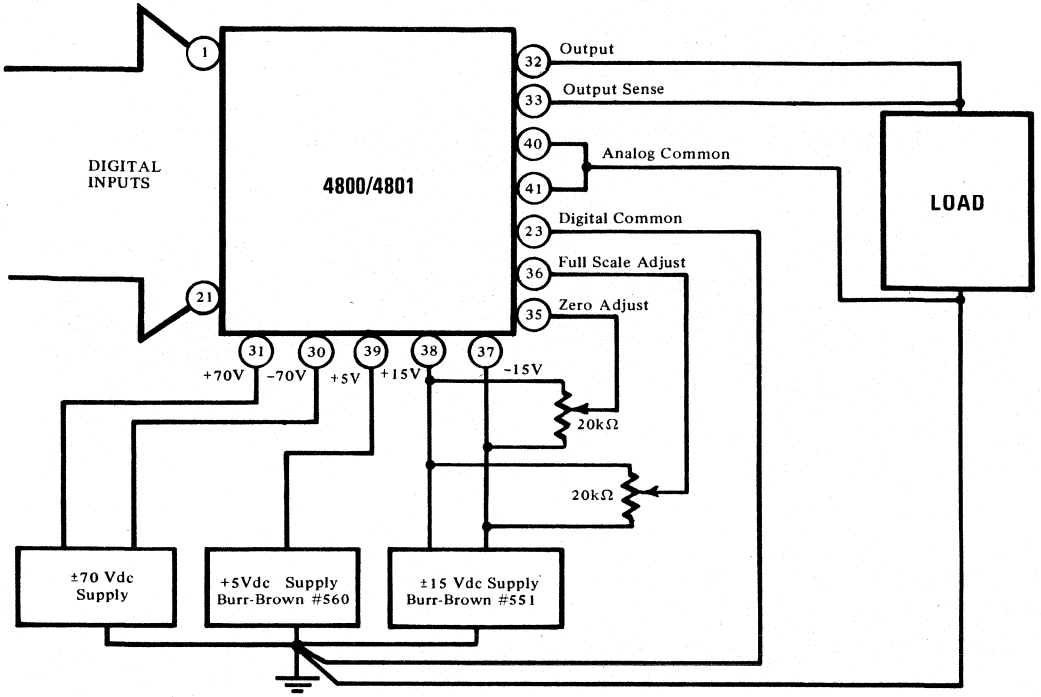


FIGURE 13. Typical Power Supply and Grounding Connections.

The DPVS requires only two adjustments for complete calibration in voltage programming mode. See Figure 13.

ZERO ADJUST - (pin 35)

a. Program 0 V out on the 10 V range, minus polarity.
b. Set zero adjust potentiometer for output null.

FULL SCALE ADJUST - (pin 36)

a. Program full scale output, 10V range, minus polarity.
b. Set full scale adjust potentiometer for E_O = 10.000 V for 4800 or E_O = 9.990 V for 4801.

NOTES:

Output Sense (Pin 33) and Analog Common (pins 40 and 41) are low current, voltage sense inputs. The leads from these points should be of minimum length and they should be placed as closely as possible to the load to maintain optimum performance.

The 4800/4801 may be soldered directly into a printed circuit board or bolted to a metal heat sink (Note: .1" max thread depth). Heat sink requirements can be evaluated by considering Figure 2 after the actual voltage-current output requirements are determined.

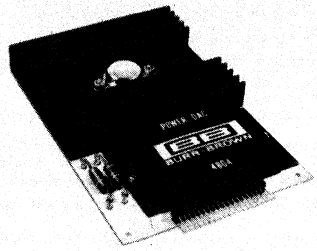
1. The Zero Adjust has approximately ±0.1% of Full Scale adjust range while the Full Scale Adjust has ±0.2% of Full Scale adjust range.

2. If only one range is to be used the Zero and Full Scale Adjust should be made on that range instead of the minus 10 volt range.

3. Power Supply filter capacitors (.1 μF) are provided internally at all DC supply inputs (pins 39, 38, 37, 31, and 30).

NOTE The current limit circuitry is not activated in the current sink mode. See figure 2 of this data sheet for current sink limits. Do NOT connect Power Supply Terminal to the output terminal (pin 32).

BURR-BROWN



4804

Low Cost 12-BIT POWER DAC

FEATURES

- DIGITALLY PROGRAMMABLE VOLTAGE SOURCE ±30VDC, 1A Continuous Output
- RESISTOR-PROGRAMMED VOLTAGE RANGE AND CURRENT LIMIT
- LOW COST
- INPUT STORAGE REGISTER
- ±1/2LSB MAXIMUM NONLINEARITY

DESCRIPTION

The 4804 Power DAC offers versatility and low cost in automatic test equipment and process control applications. The output range is ±30VDC at 1A with built in current limiting at ±1.2A. By adding one external resistor, you can select any full scale output range less than ±30VDC and still maintain 12-bit resolution. Also, the current limiting can be varied by changing the value of two easily accessible resistors. The package was designed for mounting on a PC card and can dissipate up to 20W internally in free air with no external heat sinking required.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-335A

Printed in U.S.A. July, 1978

DETAILED DESCRIPTION

GENERAL

The 4804 consists of a 12-bit storage register with strobed inputs, a 12-bit digital-to-analog converter, and a power output stage. By changing the input code according to Table I, the output voltage may be varied between ±30V with output currents up to 2A continuous. The maximum internal power dissipation for various output conditions is described in Figure 3 and 5. Care must be taken not to exceed the power dissipation limits for the thermal environments described in the figures.

No external adjustments or components are required to achieve the specified accuracy. If improved performance is required, two adjustments will null the offset and gain errors. The procedures for adjusting these parameters are described on page 5-213.

To minimize noise levels in the 4804 the analog and digital signal returns are not internally connected. For proper operation, these two grounds must be externally connected together.

STORAGE REGISTER

The storage register consists of 12 integrated-circuit, positive-edge-triggered flip-flops utilizing TTL circuitry. The logic levels at the register inputs are transferred to the D/A converter on the positive-going edge of the strobe pulse. Strobing occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the strobe input is at either the high or low level, the inputs to the register have no effect on the D/A converter inputs. The strobe and register are fully compatible with most TTL or DTL circuits.

DIGITAL-TO-ANALOG CONVERTER

The D/A converter stage accepts the digital output from the storage register and converts it into a bipolar analog signal according to Table I.

To reduce gain and offset errors below the specified values, OFFSET ADJUST and GAIN ADJUST trim points are provided. Follow the procedure shown on 5-213.

POWER AMPLIFIER

The power amp stage buffers the D/A converter signal and provides the power output capability. Connecting the ±30V RANGE pin to the output will preset the full scale range to ±30V, giving the transfer function described in Table I; i.e. 1 LSB = 14.65mV. R_F and R_S were selected for optimum temperature stability to minimize gain drift errors, and the offset of the Power Amplifier has been nulled at the factory. By connecting a resistor between the V_{OUT} RANGE ADJUST pin and the output, a variety of full scale ranges can be selected while maintaining 12-bit resolution.

For optimum stability, the external resistor should have a T.C. which is less than ±10ppm/°C. The ±35V inputs to the power amplifier may be reduced if full scale ranges less than ±30V are desired. To maintain the best accuracy, these supplies should not be reduced below ±15V. Since the 4804 output current is derived from the ±35V power inputs, the current-carrying capability of these power supply connecting leads should be considered.

R_P and R_M determine the output positive and negative current limits, respectively, of the output. They have been preselected for current limiting of ±1.2A, typ. The current limiting can be changed by replacing R_P and R_M with other values according to the following formula:

$$R = \frac{1.2V}{I_{\text{current limit}}}$$

It is not necessary that R_P and R_M be the same value. Since the output current of the 4804 flows through these resistors, the power dissipation of R_P and R_M should be considered. Both resistors are stud mounted for easy accessibility.

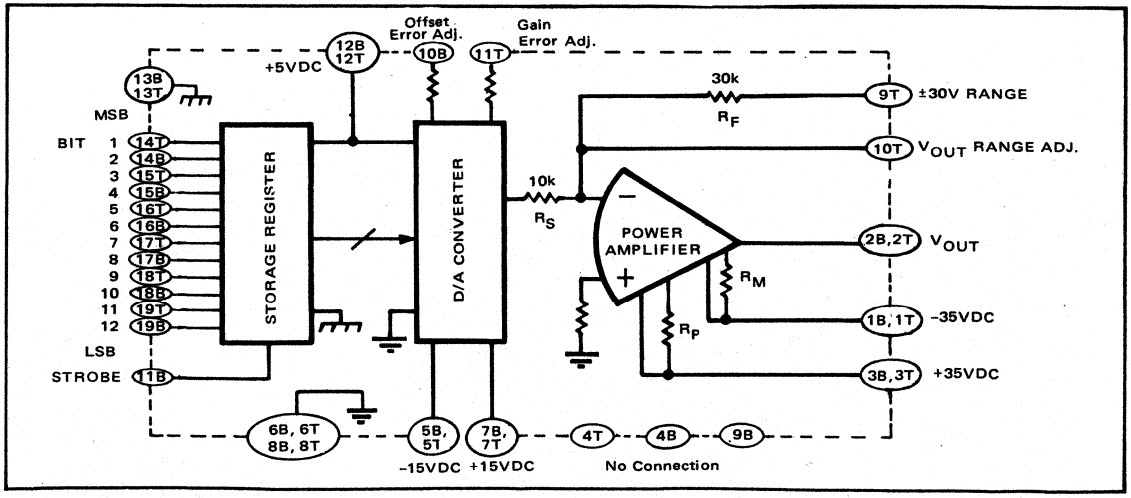


FIGURE 1. Block Diagram

SPECIFICATIONS

Typical at 25°C, rated power supplies, and V_{out} range = ±30 unless otherwise noted.

ELECTRICAL

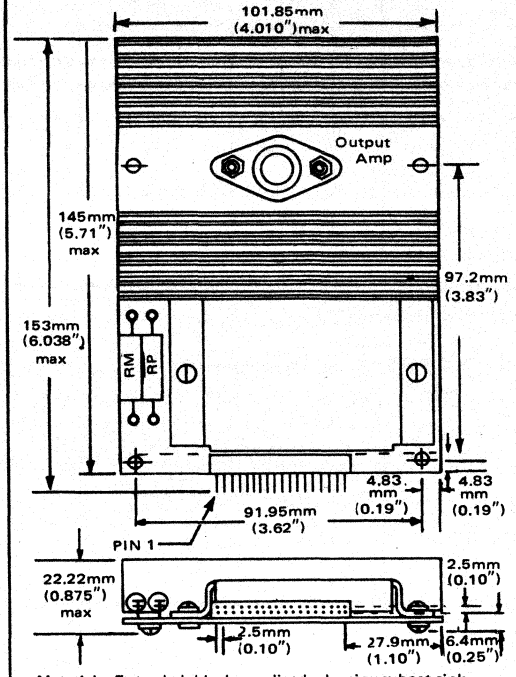
INPUT	
Resolution	12 bits
Logic levels (TTL/CMOS Compatible)	
Logical "1"	$\pm 2V < e_{in} < +5.5V$ @ $\leq +0.1mA$
Logical "0"	$0V < e_{in} < +0.8V$ @ $\leq -0.36mA$
Digital Input Coding	offset binary (see Table I.)
TRANSFER CHARACTERISTICS	
TOTAL ACCURACY	
V_{out} Range = ±30V	±0.05% of reading
Individual Error Contributors	
Linearity Error (0°C to +70°C)	±½LSB max
Differential Linearity Error	±½LSB max
Output Offset Voltage	±3mV max
Drift (0°C to +70°C)	
Gain	±50ppm/°C max
Output Offset Voltage	±70µV/°C max
Differential Linearity	±2ppm/°C
Power Supply Sensitivity	
+15V Supply	2mV/V
-15V Supply	2mV/V
+ 5V Supply	6mV/V for V_{out} = ±30V range
±35V Supplies	400µV/V
Settling Time (to within 0.01% of final value for any input change)	100µsec max
OUTPUT	
Voltage Range @ I_{out} = 1.0A	±29.985V (= 30V -1LSB)
Output Current	(see Figure 5 and Note 1.)
Factory Adjusted Output Current Limit	1.2A typ
Output Resistance	1Ω max
POWER SUPPLY REQUIREMENTS	
Rated Voltages	±15VDC, +5VDC, ±35VDC
Power Supply Operating Ranges	±5%
Supply Drain	
±15V	±25mA
+5	+80mA
±35V	±40mA ±output current
TEMPERATURE RANGE	
Specification	0°C to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +125°C

NOTE 1: Output amplifier is capable of sourcing or sinking 2 amps continuously. Resistors R_M and R_P have been selected to current limit the output current to ±1.2 A typ. To increase I_{out} capability, or modify the current limit setting, replace R_M and R_P according to instructions on page 5-210. Internal power dissipation should be considered, especially at low output voltages.

ABSOLUTE MAXIMUM RATINGS

+5V Supply	+7V
±15V Supplies	±20V
±35 Supplies	±40V
Digital Inputs	+7.0V with +5V supply = +7V
Power Amp Case Temp	+125°C
Output Amplifier Power Dissipation	20W max in free air, derate 0.2W/°C above +25°C
Output Current	See Figure 5 and Note 1

MECHANICAL



Material: Extruded, black-anodized, aluminum heat sink and discrete components mounted on glass epoxy printed circuit board.

4804 Connector: Amp 2 - 86479 - 3

Recommended mating Connectors: PC card: 0806MC
Flexable: Scotchflex 3417 - 0000

Diameter of mounting holes: 3.56mm (0.14")

PIN CONNECTIONS

BOTTOM	PIN	TOP
-35V	1	-35V
Output	2	Output
+35V	3	+35V
N.C.	4	N.C.
-15V	5	-15V
Ana. Com.	6	Ana. Com.
+15V	7	+15V
Ana. Com.	8	Ana. Com.
N.C.	9	+30V Range
Offset Adj.	10	V_{out} Range Adj.
Strobe	11	Gain Adj.
+5V	12	+5V
Dig. Com.	13	Dig. Com.
Bit 2	14	Bit 1
Bit 4	15	Bit 3
Bit 6	16	Bit 5
Bit 8	17	Bit 7
Bit 10	18	Bit 9
Bit 12	19	Bit 11

TYPICAL PERFORMANCE CURVES

(Typical @ 25°C and ±15VDC Power Supplies unless otherwise noted)

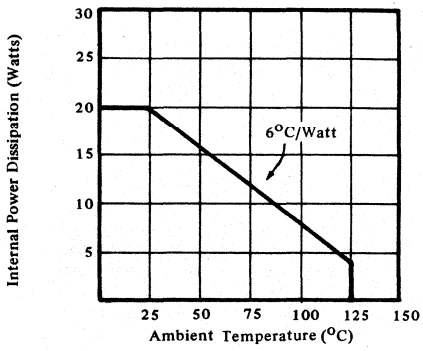


FIGURE 2. Power Derating Curve.

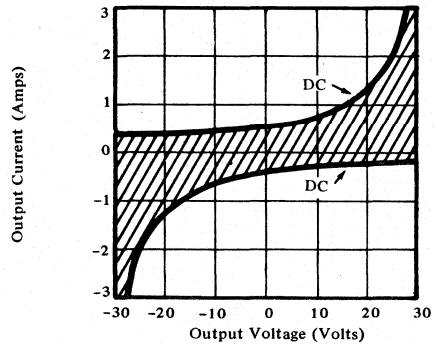


FIGURE 3. Safe Operating Area.

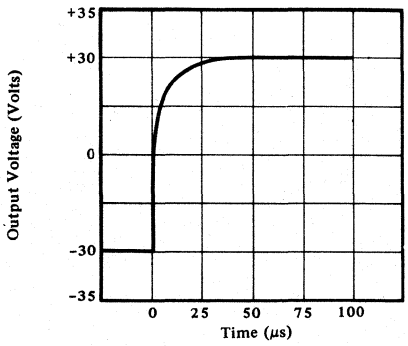


FIGURE 4. Pulse Response.

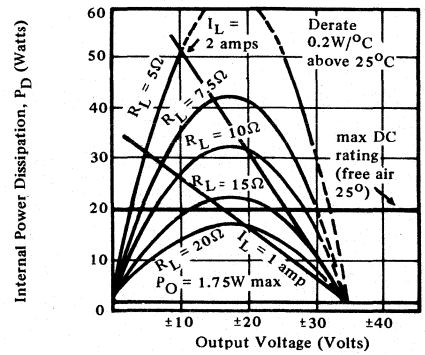


FIGURE 5. Output Amplifier Power Dissipation vs. Output Voltage.

DIGITAL INPUT CODES VS. V_{OUT}		
INPUT CODE MSB LSB	**NOMINAL OUTPUT VOLTAGE**	
	±30V RANGE	**VARIABLE RANGE**
1111 11111 111	+30.000V	$+10.000\left(\frac{R_G}{10k}\right)$ V
1111 1111 1110	+29.985V	$+9.995\left(\frac{R_G}{10k}\right)$ V
1000 00000 000	+14.65mV	$+4.88\left(\frac{R_G}{10k}\right)$ mV
0 11111111 111	0.000V	0.000V
0 111111111 10	-14.65mV	$-4.88\left(\frac{R_G}{10k}\right)$ mV
0000000000001	-29.971V	$-9.990\left(\frac{R_G}{10k}\right)$ V
000000000000	-29.985V	$-9.995\left(\frac{R_G}{10k}\right)$ V

TABLE I.

PROCEDURES FOR ADJUSTING OFFSET AND GAIN ERRORS...

OFFSET AND GAIN ADJUSTMENT

The offset and gain of the D/A converter stage may be trimmed using externally connected OFFSET ADJUST and GAIN ADJUST potentiometers. The adjustment procedure is outlined below. Since the GAIN ADJUST is connected to a high impedance point in the D/A converter, a ceramic capacitor connected between this point and analog common is recommended to minimize noise pickup. The offset error should always be nulled before adjusting the gain error potentiometer.

OFFSET ADJUST PROCEDURE

Apply the digital code which could give the maximum positive voltage output and adjust the OFFSET ADJUST potentiometer for the proper output voltage. For example, if the 4804 is connected for a full scale range of ±30V, apply all ones to the input and adjust the potentiometer for an output of +30.000V.

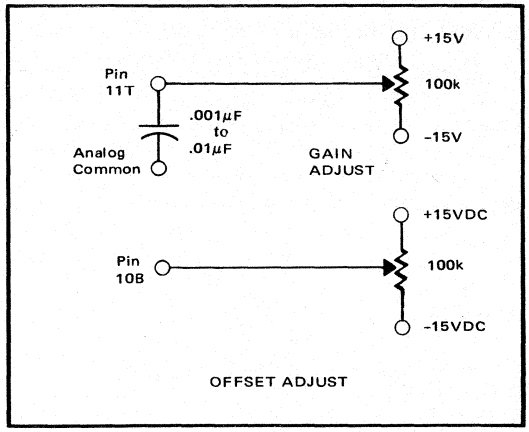


FIGURE 6.

GAIN ADJUST PROCEDURE

Apply the digital code which should give the maximum negative voltage output, and adjust the GAIN ADJUST potentiometer for the proper output voltage. For example, if the 4804 is connected for a full scale range of ±30V, apply all zeros and adjust the potentiometer for an output of -29.985V.

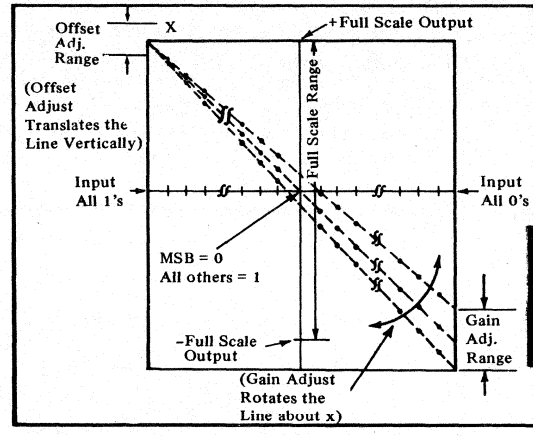


FIGURE 7.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The 4804 accepts TTL and CMOS compatible input codes in binary format. Table I shows the output voltage for selected inputs.

ACCURACY

Total Accuracy is the maximum deviation from the ideal output over the full output range. It is tested at 25°C and represents the maximum allowed value of the sum of the individual errors. The total accuracy is specified as a maximum with the 4804 in the ±30V range configuration. If an output range less than ±30V is selected, the accuracy will improve as the power amplifier gain is reduced.

Lineary Error for the 4804 is specified as a maximum over the temperature range of 0°C to +70°C. This means that the analog output will not vary by more than ±½ LSB maximum from an ideal straight line drawn between the "all bits ON" and "all bits OFF" end points.

Differential Linearity is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error spec of ±½ LSB means that the output voltage step sizes can be anywhere from ½ LSB to 3/2 LSB when the input changes from one adjacent input state to the next.

Monotonicity over 0°C to +70°C is guaranteed in the 4804. This insures that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is measure of the change in the full scale range analog output over temperature. The GAIN DRIFT is determined by testing the end point differences at 0°C, +25°C and +70°C, calculating the GAIN ERROR with respect to the 25°C value, and dividing by the temperature change. This specification is expressed in ppm/°C.

Offset Drift is a measure of the actual change in the output with all bits OFF (all 0's) over the specified temperature range, and is measured at 0°C, +25°C and +70°C.

The maximum change in OFFSET is referenced to the OFFSET at 25°C divided by the temperature range. This drift is expressed in parts per million of full scale ranges per °C (ppm of FSR/°C).

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the effect of a power supply voltage variation on the 4804 output. It is defined as a change in output voltage per change in supply voltage with the ±30V output range. Power supply rejection is improved if a full scale range less than ±30V is selected.

OPERATING INSTRUCTIONS

REMOTE SENSING

In applications requiring that the load be located some distance from the Power DAC, the line resistance from the 4804 to the load can cause significant error, especially during operation at high currents. To minimize this problem, connect the circuit with the line resistance inside the feedback loop of the output amplifier, as shown in Figure 8. This technique effectively divides the line resistance by the open loop gain of the output amplifier (94 dB min, with R_{LOAD} 5Ω). To minimize noise pickup, the external feedback resistor should be located as close as possible to the 4804.

Since the amplifier must still overcome the voltage drop in the line inside the feedback loop, the dynamic range of the load voltage will be reduced by approximately $I_{LOAD} \times R_{LINE}$. Proper grounding of the 4804, load, and digital stimulus will also reduce errors caused by ground loops.

THERMAL CONSIDERATIONS

The absolute maximum internal power dissipation of the output amplifier is 20 watts in free air at 25°C. Derate by 0.2W/°C above 25°C. Thermal resistance from amplifier junction to ambient is 6°C/watt. Figure 5 shows internal power dissipation as a function of otuput voltage and load resistance with ±35V supply voltages.

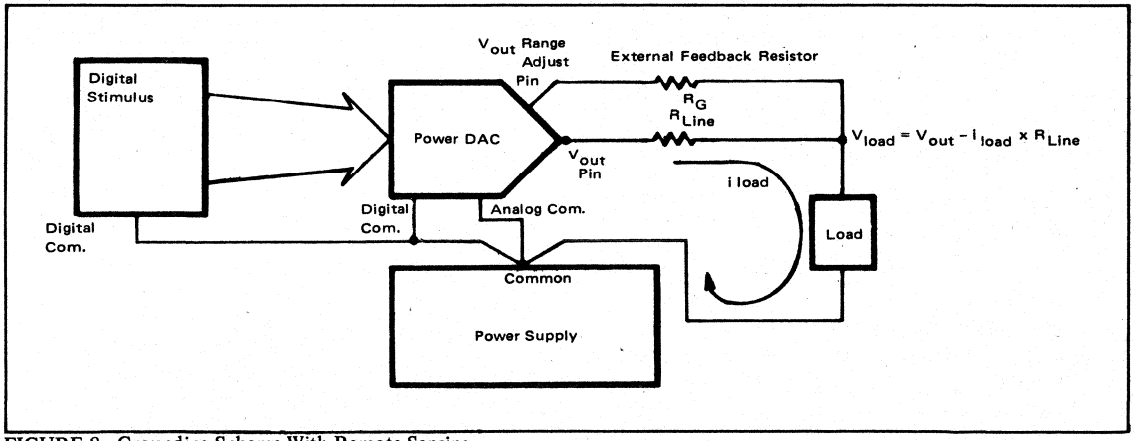
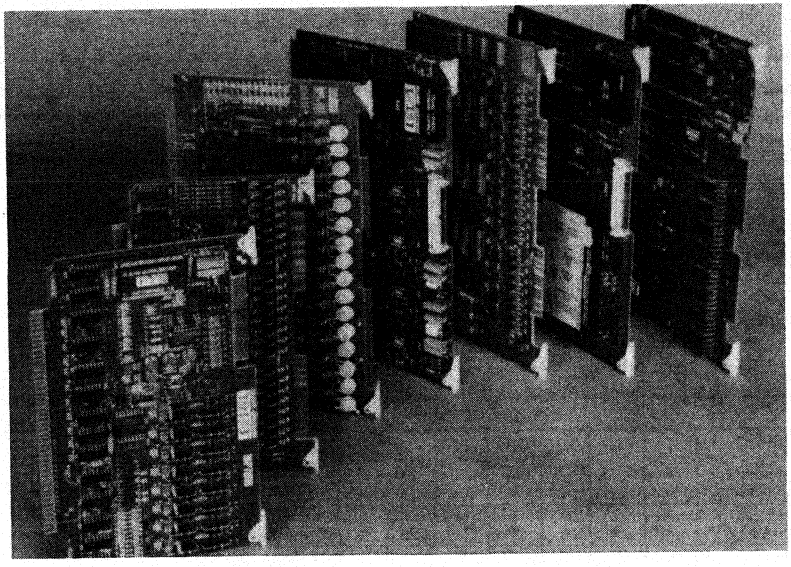


FIGURE 8. Grounding Scheme With Remote Sensing

6. MICROCOMPUTER INPUT/OUTPUT SYSTEMS



Burr-Brown offers a wide variety of analog and isolated digital I/O boards for Intel, Motorola, Zilog, and Pro-Log micromputers.

Analog input systems are available with 8- to 64-input channels and 8- to 12-bit accuracy. They interface to any input signal between ±10V and ±10mV. Since transducer voltage levels can be interfaced directly to these boards, other expensive signal conditioning instrumentation may not be needed. Many analog input systems are available with analog outputs on the same board. Analog output systems are available with 2 to 4 channels and 8- or 12-bit accuracy.

Digital input systems are available with 24 channels and offer 600VDC isolation. These systems will interface directly to voltage or contact-closure inputs. An on-board supply provides "wetting current" for "dry" contact-closures. Digital output systems are available with 16 or 32 channels and offer 600VDC isolation; the outputs are implemented with reed relay switches. Each output, protected by metal oxide varistors, can control 10 watts. The isolation of these boards eliminates ground-loop problems and protects the computer from overvoltages and transients.

Most Burr-Brown microperipheral systems are memory-mapped. This greatly simplifies the software required to access a channel. For instance, only one instruction is needed to acquire a channel of data with the MP8416. All Burr-Brown microperipherals are designed for ease of software interfacing.

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Selection Guide 6-2
Glossary of Terms and Definitions 6-3
Product Data Sheets 6-5

SELECTION GUIDE
Microcomputer I/O Systems

DIGITAL I/O

Compatible With	Microperipheral Model	Digital Input	Digital Output	Number Channels	Isolated	Features		Page
Motorola[1]	MP701 *		●	16	●	Relay output		6-5
	MP702 *		●	32	●	Relay output		6-5
	MP710 *	●		24	●	Contact closure input		6-9
	MP710-NS *	●		24	●	Voltage input		6-9
Intel[2] and National[3]	MP801 *		●	16	●	Relay output		6-15
	MP802 *		●	32	●	Relay output		6-15
	MP810 *	●		24	●	Contact closure input		6-19
	MP810-NS*	●		24	●	Voltage input		6-19

ANALOG I/O

Compatible With	Microperipheral Model	Analog Input	Analog Output	Inputs High Level	Inputs Low Level	Analog Resolution	Number Channels Input	Number Channels Output	Features		Page
Zilog[4]	MP2216 *	●		●	●	12	32 SE		General purpose		6-25
	MP2216-AO *	●	●	●	●	12	32 SE	2	AI/AO on one board		6-25
Pro-Log[5]	MP4102		●			8		2	General purpose		6-33
	MP4216	●		●	●	8	16 DIF		General purpose		6-33
Motorola[1]	MP7104		●			12		4	General purpose		6-41
	MP7105-NS		●			12		4	General purpose		6-41
	MP7208	●		●	●	12	8 DIF		General purpose		6-41
	MP7216	●		●	●	12	16 SE		General purpose		6-41
	MP7218	●		●	●	12	16 SE		Low cost		6-53
	MP7408	●		●	●	8	16 SE		Low cost		6-61
	MP7408-AO	●	●	●	●	8	16 SE	2	AI/AO on one board		6-61
	MP7408-NS	●		●	●	8	16 SE		Low cost		6-61
	MP7408-NS-AO	●	●	●	●	8	16 SE	2	AI/AO on one board		6-61
	MP7432	●		●	●	8	64 SE		Low cost		6-61
	MP7432-AO	●	●	●	●	8	64 SE	2	AI/AO on one board		6-61
	MP7432-NS	●		●	●	8	64 SE		Low cost		6-61
	MP7432-NS-AO	●	●	●	●	8	64 SE	2	AI/AO on one board		6-61
	MP7504		●			8		4	Isolated outputs		6-69
	MP7608	●		●	●	12	8 DIF		Overvoltage protect.		6-73
	MP7608-I	●		●		12	8 DIF		4mA to 20mA inputs		6-73
Intel[2] and National	MP8304		●			12		4	General purpose		6-84
	MP8305		●			12		4	General purpose		6-84
	MP8305-NS		●			12		4	General purpose		6-84
	MP8408	●		●	●	12	8 DIF		General purpose		6-84
	MP8416	●	●	●	●	12	16 SE		General purpose		6-84
	MP8418*	●		●	●	12	32 SE		General purpose		6-96
	MP8418-AO*	●	●	●	●	12	32 SE	2	AI/AO on one board		6-96
	MP8418-PGA*	●		●	●	12	32 SE		PGA		6-96
	MP8418-PGA-AO*	●	●	●	●	12	32 SE	2	PGA		6-96
	MP8608	●		●	●	8	8 DIF		Low cost		6-104
	MP8608-AO	●	●	●	●	8	8 DIF	2	AI/AO on one board		6-104
	MP8608-NS	●		●	●	8	8 DIF		Low cost		6-104
	MP8608-NS-AO	●	●	●	●	8	8 DIF	2	AI/AO on one board		6-104
	MP8616	●		●	●	8	16 SE		Low cost		6-104
	MP8616-AO	●	●	●	●	8	16 SE	2	AI/AO on one board		6-104
	MP8616-NS	●		●	●	8	16 SE		Low cost		6-104
	MP8616-NS-AO	●	●	●	●	8	16 SE	2	AI/AO on one board		6-104
	MP8632	●		●	●	8	64 SE		Low cost		6-104
	MP8632-AO	●	●	●	●	8	64 SE	2	AI/AO on one board		6-104
	MP8632-NS	●		●	●	8	64 SE		Low cost		6-104
	MP8632-NS-AO	●	●	●	●	8	64 SE	2	AI/AO on one board		6-104

1) Micromodule and EXORciser®. 2) SBC80 and Intellec MDS. 3) BLC80. 4) Z-80 MCB and Z-80 MCS. 5) All. 6) Prices for quantities (1-4) (5-9) (10-24).
*New

GLOSSARY OF TERMS & DEFINITIONS
Microcomputer I/O Systems

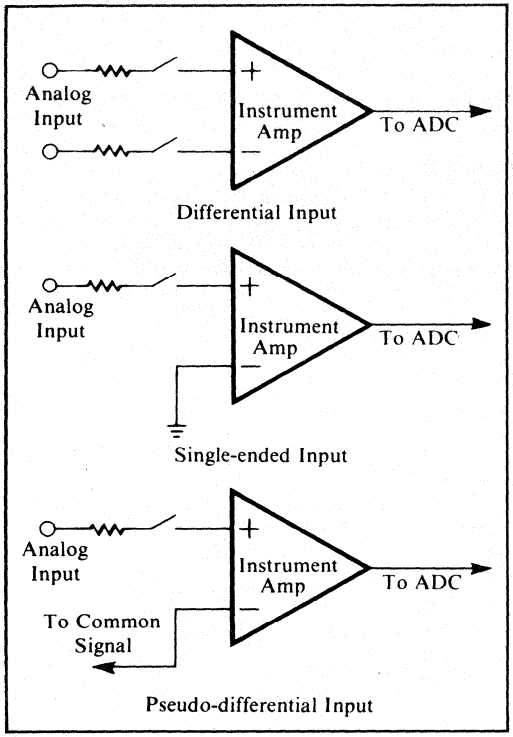
ANALOG INPUT SYSTEM

A system which conditions, multiplexes, digitizes and interfaces analog input signals to a computer.

ANALOG OUTPUT SYSTEM

A system which interfaces a computer's digital data to analog output signals through D/A converters.

ANALOG INPUTS, DIFFERENTIAL, SINGLE-ENDED AND PSEUDO-DIFFERENTIAL



Most Burr-Brown analog input systems may be connected with differential, single-ended or pseudo-differential inputs. Use of differential inputs gain the full benefit of the instrument amplifier. Usually the input signal itself and a ground at the point that the signal is generated are connected via a twisted wire pair to the differential input. In this mode, noise that is picked up between the source and the input system is rejected by the instrument amplifier. In the single-ended mode, one wire per input signal is connected to the analog input system. The inverting amplifier input is grounded. Thus the system provides no common-mode noise rejection.

The differential mode is the recommended mode of operation for any analog inputs. However, more hardware is required for a differential input than a single-ended input; therefore the cost-per-input is higher for differential inputs than for single-ended inputs. Differential inputs should be used with all inputs which are noisy or are less than ±1V full scale. Single-ended inputs may be used with inputs which are not noisy and are more than ±1V full scale.

Pseudo-differential inputs, in some cases, combine the best of both worlds. If all input signals have a common ground, the inverting input of the amplifier may be directly connected to that ground. In this way, the cost-per-channel is the same as the single-ended mode, and the circuit provides noise rejection although not as much as in the differential mode.

ANALOG INPUTS, HIGH LEVEL AND LOW LEVEL

High level analog signals are greater than ±1V full scale. Low level analog signals are less than ±1V full scale, usually much less, such as between 10 and 100mV. Burr-Brown low level systems can digitize analog inputs as low as ±10mV full scale. Low level inputs require more care in signal processing since noise pickup is a more significant error contributor than it is to high level signals. Low level signals should be connected to differential input systems for best noise rejection.

CODES

The digital interface to analog input or analog output systems is available in either of two codes: two's complement and straight binary. Two's complement code is normally used with bipolar input ranges and straight binary code with unipolar input ranges. See the table below:

TWO'S COMPLEMENT

Digital Input/Output		Analog Value
Binary	Hexadecimal	
(0000)* 0111 1111 1111	(0)* 7 FF	positive full scale
(0000) 0111 1111 1110	(0) 7 FE	positive full scale - 1LSB
(0000) 0000 0000 0001	(0) 0 01	midscale + 1LSB
(0000) 0000 0000 0000	(0) 0 00	midscale
(1111) 1111 1111 1111	(F) F FF	midscale - 1LSB
(1111) 1000 0000 0001	(F) 8 01	negative full scale + 1LSB
(1111) 1000 0000 0000	(F) 8 00	negative full scale

*The unused four most significant bits are tied to the most significant bit of the data word.

TABLE I. Two's Complement Coding

STRAIGHT BINARY		
Digital Input/Output		Analog Value
Binary	Hexadecimal	
(0000)* 1111 1111 1111	(0)* FFF	positive full scale
(0000) 1111 1111 1110	(0) FFE	positive full scale - 1LSB
(0000) 1000 0000 0000	(0) 800	midscale
(0000) 0000 0000 0001	(0) 001	negative full scale + 1LSB
(0000) 0000 0000 0000	(0) 000	negative full scale

*The four most significant bits are tied to ground.

TABLE II. Straight Binary Coding

When a 12-bit word is transferred, right justified, to the CPU the four most significant bits are not needed. With Two's Complement Coding these four bits are connected to the most significant bit of the 12-bit data word. Thus the actual 16-bit word in the CPU includes the values shown in parentheses in Table I. For Straight Binary Coding, the four most significant bits are typically tied to ground, as shown in Table II.

For an analog system with an input range (or span) of V_R, one least significant bit (LSB) is $V_R/2^n$ where n is the number of bits of resolution of the converter. For a 12-bit system $2^{12} = 4096$; for an 8-bit system $2^8 = 256$. The positive full scale vaue is $V_R/2$ - 1LSB for bipolar ranges and V_R - 1LSB for unipolar ranges.

The negative full scale value is $-V_R/2$ for bipolar ranges and 0V for unipolar ranges.

COMMON-MODE REJECTION (CMR)

When both inputs of a differential analog input system experience the same common-mode voltage (CMV), the output should, ideally, be unaffected. CMR is the ratio of the common-mode input voltage change to the differential input voltage (error voltage) which produces the same output change.

$$\text{CMR (in dB)} = 20 \log_{10} \frac{\text{CMV}}{\text{Error Voltage}}$$

Thus a CMR of 80dB means than 1V of common-mode voltage will cause an error of 100μV (referred to input).

CONVERSION TIME

The time required in an analog input system from the moment a channel is interrogated (such as with a read instruction) to the moment data is available on the bus. This includes switching time, settling time, acquisition time, and A/D conversion time.

ISOLATION VOLTAGE

The voltage which an isolated circuit will withstand in normal operation. Isolation voltage may be specified from input to input and/or from any input to the computer bus. Isolation breaks ground loops while protecting the computer from voltage transients and malfunctions.

MEMORY-MAPPED I/O

A method of interfacing peripherals to computer systems. Such peripherals interface to the computer as memory and use memory reference instructions to access the I/O. Since most microcomputer instruction sets are designed to optimally access memory, memory reference instructions are the most powerful. Thus memory-mapped systems offer the most efficient software utilization for I/O in a microcomputer.

SETTLING TIME

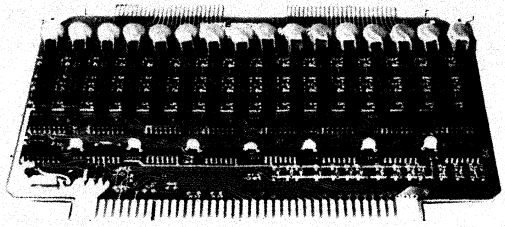
The time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

The total settling time of an analog input system includes the settling times of the input multiplexer, instrumentation amplifier, and sample/hold amplifier.

THROUGHPUT ACCURACY

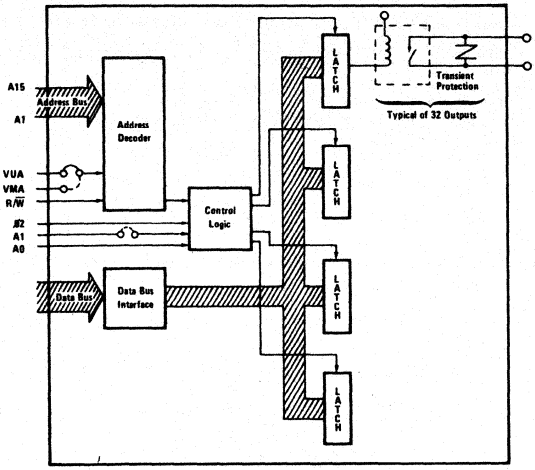
The total accuracy input-to-output in an analog input or output system. This specification includes offset errors, gain errors and linearity errors. Throughput accuracy is usually expressed in terms of the system errors.

BURR-BROWN



MP701
MP702

MICROCOMPUTER DIGITAL OUTPUT SYSTEMS



BLOCK DIAGRAM

DESCRIPTION

The MP701 and MP702 are digital output microperipheral boards designed to be used with Motorola 6800 microcomputer systems. The microperipheral boards are electrically and mechanically compatible with Motorola's Micromodule and EXORciser development system. The MP701 has 16 digital output channels, and the MP702 has 32 digital output channels. Each digital output channel is implemented with a protected reed relay.

Relays are used to provide low "on-impedance", high output current and output isolation. Each output is isolated from the computer bus up to 600VDC and from channel to channel up to 300VDC. This means that the computer is protected from voltage transients and malfunctions. In addition, since each channel is isolated, the voltage switched by each line is not critical, and ground loops are avoided. The varistors protect each relay contact by suppressing high voltage transients such as those encountered in inductive circuits.

These boards appear as memory locations to the user. Data written on the data bus controls the status of each output. A "1" will close an output, a "0" will open an output. Any memory write command may be used. Each write command controls the status of eight channels. Address bits A0 and A1 on the MP702 and A0 on the MP701 select which set of eight outputs are controlled. The remainder of the address lines are used to select the board itself. Because the address block occupied by each board is user selectable, it can be placed anywhere in memory.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-381
Printed in U.S.A. July, 1978

SPECIFICATIONS

Typical at +25°C and rated supplies unless otherwise noted.

ELECTRICAL

NUMBER OF CHANNELS	
MP701	16
MP702	32
DIGITAL OUTPUT	
Watts DC (resistive load) max	10 watts
Amps (resistive load) max	.5 amps
Voltage (resistive load) max	28 Vrms
Life (resistive load) min	10^6 operations
Initial contact resistance max	.2 ohms
Actuate Time	250μsec
De-Actuate time	250μsec
Bounce time	150μsec
TRANSIENT PROTECTION	
Continuous power rating	250mW
Discharge capacity	30 watt-seconds
COMPUTER BUS	
All signals compatible with Motorola EXORciser and Micromodules system	
Logic Loading	1 LSTTL
Output Coding	0 Open Contact 1 Close Contact
POWER REQUIREMENTS	
Voltage	5VDC, ±5% volts
Supply Drain max, MP701	.4 amp
Supply Drain max, MP702	.7 amp
ISOLATION VOLTAGE	
Between microcomputer bus and outputs	600VDC
Between outputs	300VDC
OPERATING TEMPERATURE	0 to +70°C
STORAGE TEMPERATURE	-55 to +125°C

MECHANICAL

Compatible with Micromodules and Exorciser card spacing.

Minimum card spacing: 12.7mm (0.5").

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers (SAE-43D/1-2).

50 pin output edge connector on board.

A mating connector is available from Burr-Brown: 2250MC (Viking # 3VH25/1JN5, solder tab). a Scotchflex connector is available from 3M: 3415-0001.

OPERATING INSTRUCTIONS

PROGRAMMING

Each digital output channel appears as one bit of memory to the microcomputer. The channels are selected in groups of eight by A0 on the MP701 and by A1-A0 on the MP702. Writing a 1 to an output channel closes the output contact; writing a 0 to an output channel opens the output contact. Once an output is defined, it will remain in that state until redefined by another write to that byte. For example, to open channels 0, 2, 6, and close channels 1, 3, 4, 5, 7 with an MP702 as shipped from the factory execute:

```
LDA #$BA
STA $91FC
```

where BA (1011 1010) is the data written to the board and 91FC is the address of channels 0-7. Refer to Table I for a description of which data and address lines control which output channels.

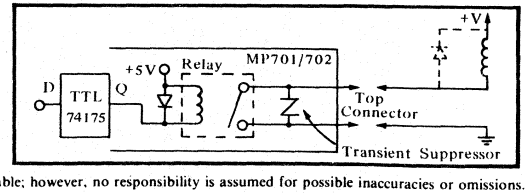
Data Bus	ADDRESS LINES (A1, A0)			
	00	01	10	11
$\overline{D7}$	7	15	23	31
$\overline{D6}$	6	14	22	30
$\overline{D5}$	5	13	21	29
$\overline{D4}$	4	12	20	28
$\overline{D3}$	3	11	19	27
$\overline{D2}$	2	10	18	26
$\overline{D1}$	1	9	17	25
$\overline{D0}$	0	8	16	24
	Channel Number			

TABLE I. Data - Address - Channel Relationship.
0 = open, 1 = close.

The MP701 and MP702 are passive during a read to their memory locations. Therefore, other memory or I/O devices may be placed at the same address without interfering with the microperipheral's activities.

DIGITAL OUTPUT CHANNEL

Each output is capable of switching an inductive load. Transient suppressors are used across each output switch to protect the output relay from damage due to surges when the contact is opened. A typical output circuit and the load circuit that it might drive are shown in the figure below.



Each relay is rated to .5 amps and 100 volts maximum. The transient suppressor reduces the maximum voltage to 28Vrms.

ADDRESSING

The board address is determined by the state of jumpers JP1 to JP22 and W1 to W8. Each jumper pair (JP1-W1, JP2-W2, etc. are jumper pairs) controls one input to a two input quad "exclusive-or" gate. These fifteen "exclusive-or" gates (IC 5-8) comprise the address decoder. An address is valid on the address bus when its compliment appears at the jumpers.

As shipped from the factory, the MP701 occupies addresses 91FE to 91FF, and the MP702 occupies addresses 91FC to 91FF. The most significant byte of the address (91) is set by plated through hole jumpers W1 to W8. The address may be changed by drilling out the plated through hole jumpers with a #54 (1.4mm) drill bit.

For example, to change the most significant byte from 91 to 96, drill out W4, W7, W8 and install JP4, JP7, JP8. (See Jumper Description section.)

The least significant byte of the address is controlled by jumpers JP9 to JP22. As shipped from the factory, JP9 to JP22 are installed on the MP701, and JP9 to JP20 are installed on the MP702, pulling all jumper inputs low. Initially, the address in binary for the MP701 is 1001 0001 1111 111A_0, and for the MP702, 1001 0001 1111 11A_1A_0 where A_0 and A_1 are used to select the output channels.

To change the least significant byte of the address, the user must clip one and only one jumper from each set of jumpers (JP9 - JP10, . . .JP21 - JP22). For example, to change the board address for an MP701 to 1001 0001 1100 000A_0, clip JP11, 9, 14, 18, 20, 16, and 22. (See Jumper Description section.) By clipping jumpers, the board address may vary from 9100 to 91FF for a possible 256 digital output channels.

JUMPER DESCRIPTION

W1-W8
JP1-JP8 These jumpers are used to select the most significant byte of the board address. Changing the address requires drilling out "W" jumpers and installing "JP" jumpers. A pair of jumpers determines the correct address for each address line as shown below.

To Change:

Address Bit	From	To	Drill	Install
A15	1	0	W2	JP2
A14	0	1	W1	JP1
A13	0	1	W3	JP3
A12	1	0	W5	JP5
A11	0	1	W6	JP6
A10	0	1	W4	JP4
A9	0	1	W7	JP7
A8	1	0	W8	JP8

IMPORTANT: If a "W" jumper is drilled out, then the corresponding "JP" jumper must be installed. Also, if a "JP" jumper is installed, then the corresponding "W" jumper must be drilled out.

JP9-JP22* These jumpers are used to select the least significant byte of the board address. All of these jumpers are installed at the factory giving the board an address of 1001 0001 1111 11A_1A_0. Changing the board address requires only clipping jumpers. A pair of jumpers is used to determine the correct address for each address line as shown below.

Address Bit	Clip for "High" (1) Address	Clip for "Low" (0) Address
A7	JP11	JP12
A6	JP9	JP10
A5	JP13	JP14
A4	JP17	JP18
A3	JP19	JP20
A2	JP15	JP16
A1	JP21*	JP22*

* JP21-22 are not installed on the MP702.

IMPORTANT: One and only one jumper must be removed for each address line when changing the board address.

JP23, 28 Installed on MP701, not on MP702. Used to tie A1 into address decoder when present.

JP24 Not installed. When JP24 is present $\overline{D7}$ is pulled low on a read to the board.

JP25 Installed. Ties VUA into address decoder.

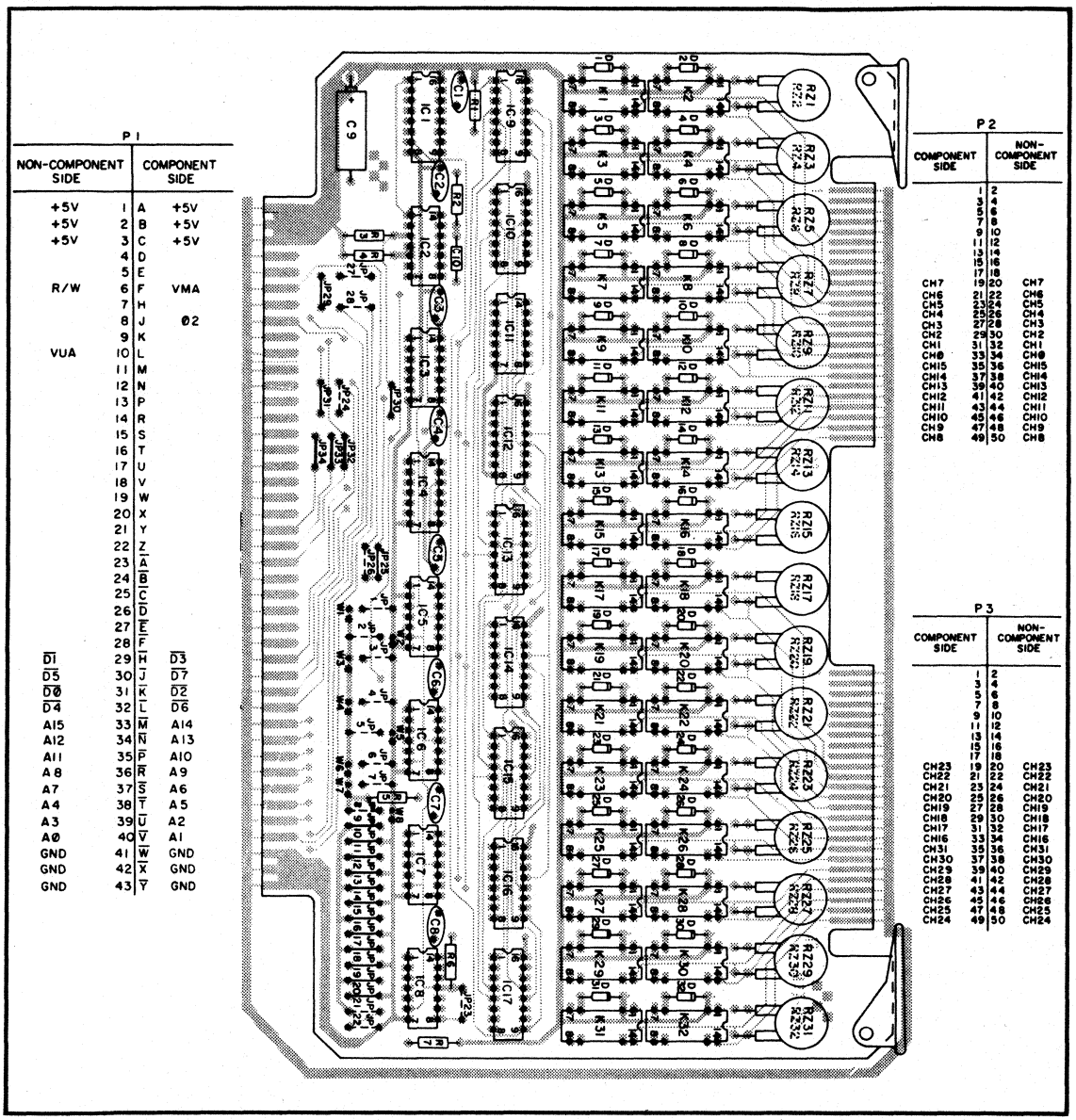
JP26 Not installed. Ties VMA into address decoder when present. Clip JP25 if JP26 is installed.

JP27 Installed on MP701, not installed on MP702. Used to disable write to channels 16-31 when present.

JP29 Not installed on MP701, installed on MP702. Used to tie A1 into channel decoder when present.

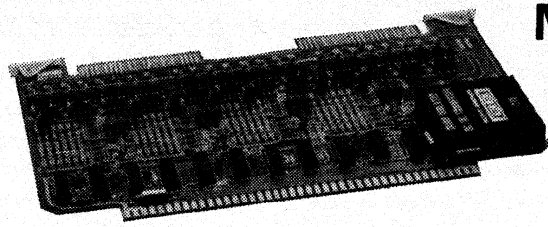
JP30-34 Test point jumpers. Clipped after factory testing is completed.

"W" jumpers are plated through on the board, "JP" jumpers are wired on the board.



MP702 BOARD LAYOUT (TOP VIEW)

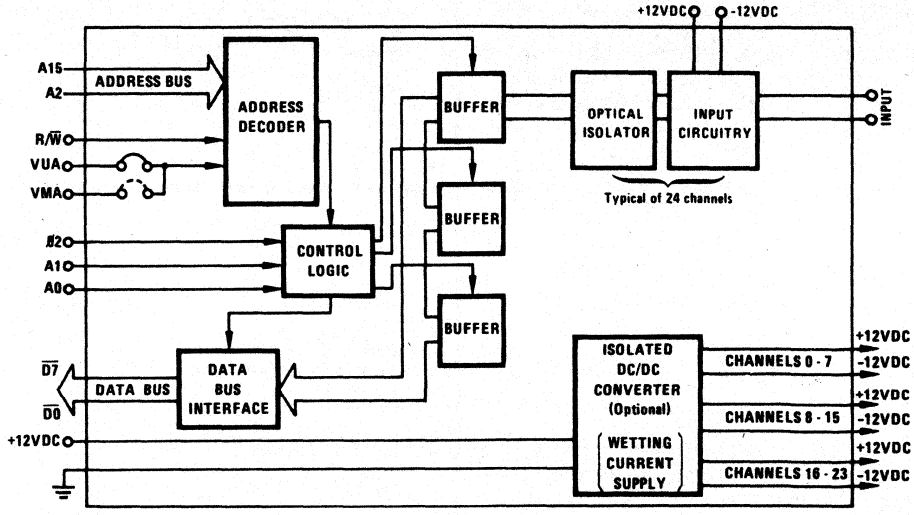
BURR-BROWN



MP710

MICROCOMPUTER DIGITAL INPUT SYSTEM

A 24-CHANNEL ISOLATED DIGITAL INPUT SYSTEM COMPATIBLE WITH MOTOROLA MICROMODULE AND EXORciser®



FEATURES

- ISOLATED FROM COMPUTER BUS AND CHANNEL TO CHANNEL
- CONTACT CLOSURE OR VOLTAGE INPUTS
- REDUCES SYSTEM DEVELOPMENT TIME
  - System engineered and specified
  - Plug compatible
  - Easy to program
  - Operates from computer power supply
- 70°C BURN-IN

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-386 Printed in U.S.A. July, 1978

DESCRIPTION

This microperipheral board provides 24 digital input channels that interface electrically and mechanically with Motorola Micromodule and EXORciser® microcomputers. It is contained on a single printed circuit board that operates from the computer's +5VDC power supply. Digital inputs enter through a card edge connector located opposite the bus connector.

The MP710 operates with dry relay contacts - MP710-NS operates with voltage inputs (wet relay contacts). The MP710 may be modified by jumper selection to operate with voltage or contact closure inputs, or a mixture of both. Inputs are arranged in groups of eight. Each group is isolated from other groups and from the computer bus up to 600 VDC. Isolation between inputs is 300 VDC (MP710-NS). Isolation protects the computer from voltage transients and malfunctions. In addition, since each input is isolated, the voltage switched by each line is not critical and ground loops are avoided.

MP710's are programmed as memory locations. Each input is one memory bit and any read command may be used. When the board is read, logic 0 represents an open contact (low voltage); logic 1, a closed contact (high voltage). Each read command inputs the status of eight channels. Address bits A0 and A1 select the set of inputs to be read. The remainder of the address lines are used to select the board itself. The address block occupied by each board is selectable and can be located anywhere in memory.

INSTALLATION

These units are shipped from the factory ready for immediate use. Installation requires only plugging the card into any empty slot in the computer and wiring the input connector.

MECHANICAL

Compatible with Micromodule and EXORciser card spacing.

Minimum card spacing: 12.7mm (0.5").

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers (SAE-43D/1-2).

Two 50 pin output edge connectors on board.

A mating connector is available from Burr-Brown: 2250MC (Viking # 3VH25/1JN5, solder tab). A Scotchflex connector is available from 3M: 3415-0001.

SPECIFICATIONS

Typical at +25°C and rated supplies unless otherwise noted.

ELECTRICAL

INPUT CHARACTERISTICS	
Number of Channels	24
Input Impedance	15kΩ
Input Delay Times	
Open to closed	25μs, max
Closed to open	100μs, max
VOLTAGE SENSE	
MP710-NS	
Minimum voltage to detect a logic 1	17V
Maximum voltage to detect a logic 0	4V
CONTACT CLOSURE SENSE	
R_{closed}	
MP710 (on board ±12V supply)	6kΩ, max
MP710-NS	
at 24V across contacts	6kΩ, max
at 48V across contacts	30kΩ, max
at 60V across contacts	58kΩ, max
R_{open}	
MP710 (on board ±12V supply)	80kΩ, min
MP710-NS	
at 24V across contacts	80kΩ, min
at 48V across contacts	175kΩ, min
at 60V across contacts	235kΩ, min
Maximum voltage (V_S) across input without damage	
MP710	120VAC, rms, max 60VDC, max
MP710-NS	168VAC, rms, max 84VDC, max
ISOLATION VOLTAGE	
Between microcomputer bus and inputs	600VDC
Between inputs (MP710-NS only)	300VDC
Between groups of 8 inputs	600VDC
POWER REQUIREMENTS	
MP710	+5VDC ±5% at 400mA +12VDC ±5% at 100mA
MP710-NS	+5VDC ±5% at 400mA
COMPUTER BUS	
All signals compatible with Motorola Micromodule and EXORciser systems	
Logic loading	1 LSTTL Load
Input coding	Logic 0: open contact Logic 1: close contact
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55 to +125°C

TABLE I. Electrical Specifications

DEFINITION OF SPECIFICATIONS

INPUT DELAY TIME

OPEN TO CLOSED - The delay required to detect an input contact closure switching from open to closed.

CLOSED TO OPEN - The delay required to detect an input contact closure switching from closed to open.

CONTACT CLOSURE IMPEDANCES

R_{CLOSED} - The impedance of an input contact closure when closed. R_{CLOSED} specifications are the maximum impedance allowed to reliably detect a closure. See Figure 1.

R_{OPEN} - The impedance of an input contact closure when open. R_{OPEN} specification is the lowest impedance allowed to reliably detect an open contact. See Figure 1.

OPERATING INSTRUCTIONS

PROGRAMMING

Each digital input channel appears as one bit of memory to the microcomputer. Channels are selected in groups of eight by A1-A0. Reading a logic 1 from an input channel indicates that the contacts are closed or voltage is present. Reading a logic 0 from an input channel indicates that the contact is open or voltage is not present. Each word read from the MP710 is the instantaneous status of each channel as the read operation occurs. Only one instruction is required to input eight channels of information. For example:

LDA $90FC

will load the accumulator with channels 0-7, where 90FC is the address of channels 0-7. Table II indicates which data and address lines input which channels.

Data Bus	ADDRESS LINES (A1, A0)			
	00	01	10	11
$\overline{D7}$	7	15	23	*
$\overline{D6}$	6	14	22	*
$\overline{D5}$	5	13	21	*
$\overline{D4}$	4	12	20	*
$\overline{D3}$	3	11	19	*
$\overline{D2}$	2	10	18	*
$\overline{D1}$	1	9	17	*
$\overline{D0}$	0	8	16	*
	Channel Number			

* Not used.

TABLE II. Data - Address - Channel Relationship.
0 = open, 1 = close.

MP710 is passive during a write to its memory locations. Therefore, other memory mapped output devices requiring only write instructions may be placed at the same address without interfering with the MP710's activities.

DIGITAL INPUT CHANNEL

Each input can read a contact closure - an input circuit is shown below.

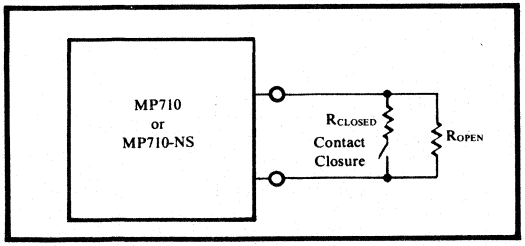


FIGURE 1. Typical Input Circuit

MP710 is designed for dry (without external voltage source) contact closures and its circuit is shown in Figure 2.

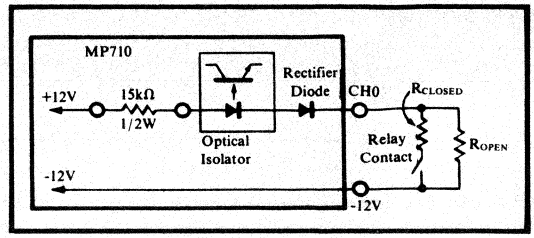


FIGURE 2. MP710, Typical Circuit

The isolated ±12V is obtained from the computer's +12VDC power supply and an optional isolated DC/DC converter. Three separate ±12VDC supplies are used on the MP710, each supplying wetting current for eight channels. Isolation voltage between each group of eight outputs is 600VDC. Table III defines the groups. The contact closure must be placed between the proper channel input and a -12V connection. See Table III for proper -12V pins to be used with each input channel group.

Group	Channel Number	Connector	-12V Pins
1	0 - 7	P2	27, 28, 29, 30
2	8 - 15	P2	39, 40
		P3	15, 16
3	16 - 23	P3	47, 48, 49, 50

TABLE III. Isolation Groups

MP710-NS is designed for voltage inputs and wet (with external voltage source) contact closures. A typical circuit is shown in Figure 3. Voltage input sensitivity of the MP710-NS may be changed by removing the 15kΩ input resistor shown in Figure 3 ($R1_b$ - $R24_b$) and replacing it with a resistance calculated by this formula:

$$R = (V_{IN} - 2)\ 10^3\Omega$$

V_{IN} (in volts) is the voltage required to detect a logic 1 input. If the value of the input resistor is reduced, the "maximum input voltage without damage" specification (see page 6-10) will be reduced proportionally. Likewise, if the input resistance is increased, the "maximum input voltage without damage" will be increased proportionally up to a maximum of 300 VDC.

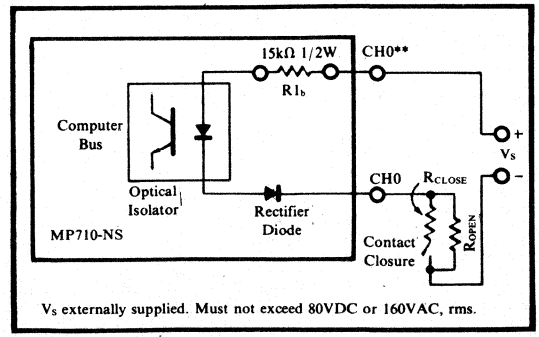


FIGURE 3. MP710-NS, Typical Circuit

The MP710-NS inputs are isolated channel-to-channel by 300VDC within groups defined in Table II. Isolation voltage between each group of eight outputs is 600VDC. See Figure 4 for MP710-NS isolation voltages.

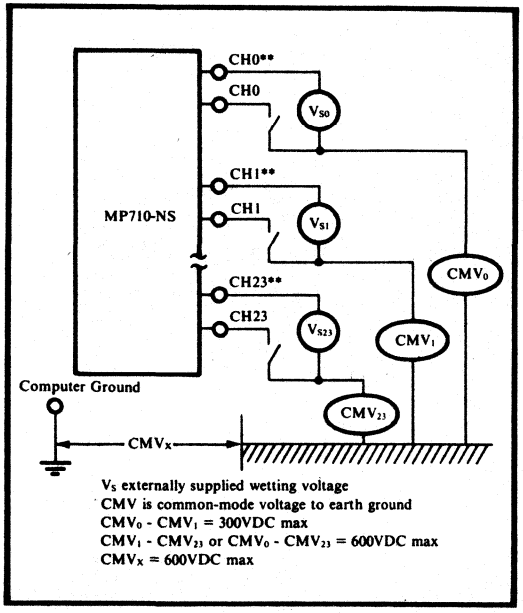


FIGURE 4. MP710-NS Isolation Circuit

ADDRESSING

The board address is determined by the state of jumpers JP1 to JP20 and W1* to W8*. A jumper pair controls one input to a two input quad exclusive-or gate. Fifteen exclusive-or gates comprise the address decoder. An address is valid on the address bus when its complement appears at the jumpers. MP710 and MP710-NS, as shipped from the factory, occupy addresses 90FC to 90FF.

The least significant byte of address is controlled by jumpers JP9 to JP20. As shipped from the factory, JP9 to JP20 are installed, pulling all jumper inputs low. Initially, the binary address for these boards is 1001 0000 1111 $11A_1A_0$, where A_0 and A_1 are used to select the output channels.

Address Bit	Clip for "High" (1) Address	Clip for "Low" (0) Address
A7	JP9	JP10
A6	JP11	JP12
A5	JP13	JP14
A4	JP15	JP16
A3	JP17	JP18
A2	JP19	JP20
IMPORTANT: One and only one jumper must be removed for each address line when changing the board address.		

TABLE IV. A2 - A7 Address Selection

To change the least significant address byte, clip one, and only one, jumper from each set of jumpers (JP9, JP10 ... JP19, JP20). For example, to change the board address to 1001 0000 1100 $00A_1A_0$, clip JP9, 11, 14, 16, 18 and 20. See Table IV. By clipping jumpers, the board address may vary from 9000 to 90FF for a possible 1536 input channels.

The most significant byte of the address (90) is set by plated-through hole jumpers W1* to W8*. The address may be changed by drilling out plated-through hole jumpers with a # 54 (0.055"/1.4mm) drill bit. Exercise caution to prevent damage to the board. Carefully remove any metal particles deposited on the board's surface. See Figure 5.

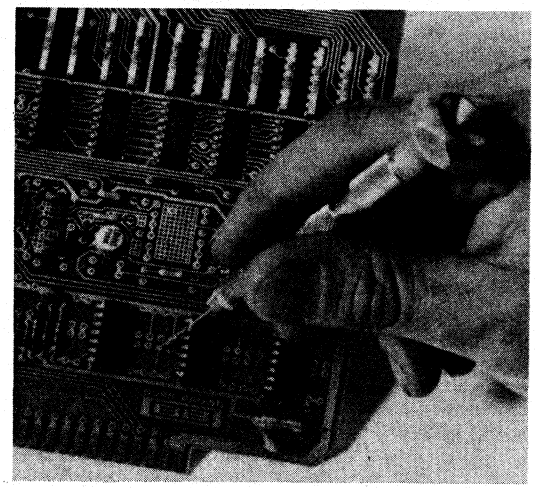


FIGURE 5. Drilling Out Plated-Through Holes.

For example, to change the most significant byte from 90 to 96, drill out W6* and W7* and install JP6 and JP7. See Table V.

To Change:				
Address Bit	From	To	Drill	Install
A15	1	0	W1*	JP1
A14	0	1	W2*	JP2
A13	0	1	W3*	JP3
A12	1	0	W4*	JP4
A11	0	1	W5*	JP5
A10	0	1	W6*	JP6
A9	0	1	W7*	JP7
A8	0	1	W8*	JP8
IMPORTANT: If a "W" jumper is drilled out, then the corresponding "JP" jumper must be instaled. Also, if a "JP" jumper is installed, then the corresponding "W" jumper must be drilled out.				

TABLE V. A8 - A15 Address Selection

DEBOUNCING AND AC SENSE

Debouncing and AC sense circuitry layout is included on the MP710/MP710-NS PC board. These components are not loaded. Contact the factory if more information is required.

Other Burr-Brown Microperipherals for Motorola Microcomputers and Microprocessors.

PC BOARD SUBSYSTEMS - Compatible with Motorola Micromodule and EXORciser Microcomputers

MP7208/MP7216	- general purpose 12 bit resolution Analog Input system
MP7218	- low cost 12 bit resolution Analog Input system
MP7400 series	- low cost 8 bit resolution Analog Input and Output system
MP7104	- general purpose 12 bit resolution Analog Output system
MP7504	- industrial 8 bit resolution Analog Output system with 4-20mA isolated outputs
MP7608	- industrial 12 bit resolution Analog Input system with filtered, protected inputs as well as bridge inputs
MP7608-I	- industrial 12 bit resolution Analog Input system with 4-20mA filtered inputs
MP701/MP702	- 16/32 channel relay output system

COMPONENT SUBSYSTEMS - Compatible with M6800 Microprocessors

MP11	- Analog Output component for M6800 microprocessor systems
MP21	- Analog Input component for M6800 microprocessor systems

JUMPER DESIGNATION

W1*-W8*, JP1-JP8 These jumpers are used to select the most significant byte of the board address. Changing the A_{15}-A_8 address lines requires drilling out "W*" jumpers and installing "JP" jumpers. A pair of jumpers determines the address for each address line. See Table V.

JP9-JP20 These jumpers are used to select the least significant byte of the board address. All of these jumpers are installed at the factory giving the board an address of 1001 0000 1111 $11A_1A_0$. Changing the A_7-A_2 address lines requires only clipping jumpers. A pair of jumpers is used to determine the address for each address line as shown in Table IV.

JP21 Installed. Ties VUA into address decoder.

JP22 Not installed. Ties VMA into address decoder.

JP23-JP26 Not installed. May be used with MP710-NS to tie together ±12V on board supply lines for use with external supplies.

W33-W34 Test point jumpers. Clipped after factory testing is complete.

"W*" jumpers are plated-through on the board. "JP" jumpers are wired on the board.

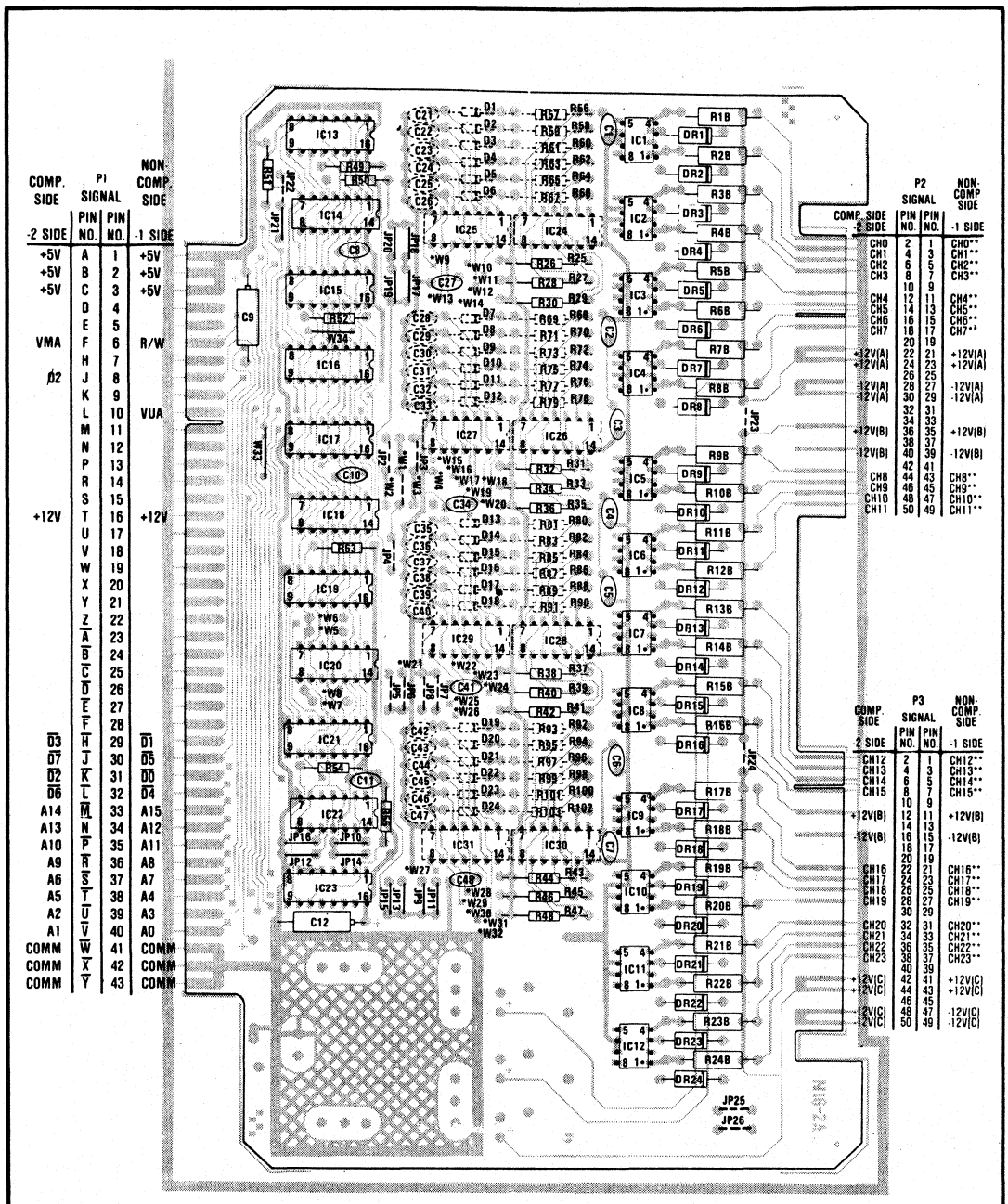
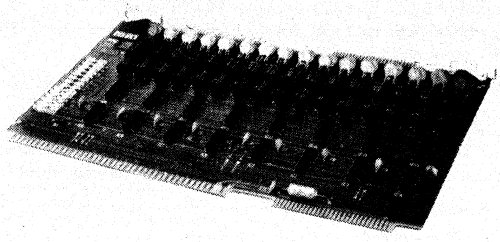


FIGURE 6. MP710 Series Board Layout

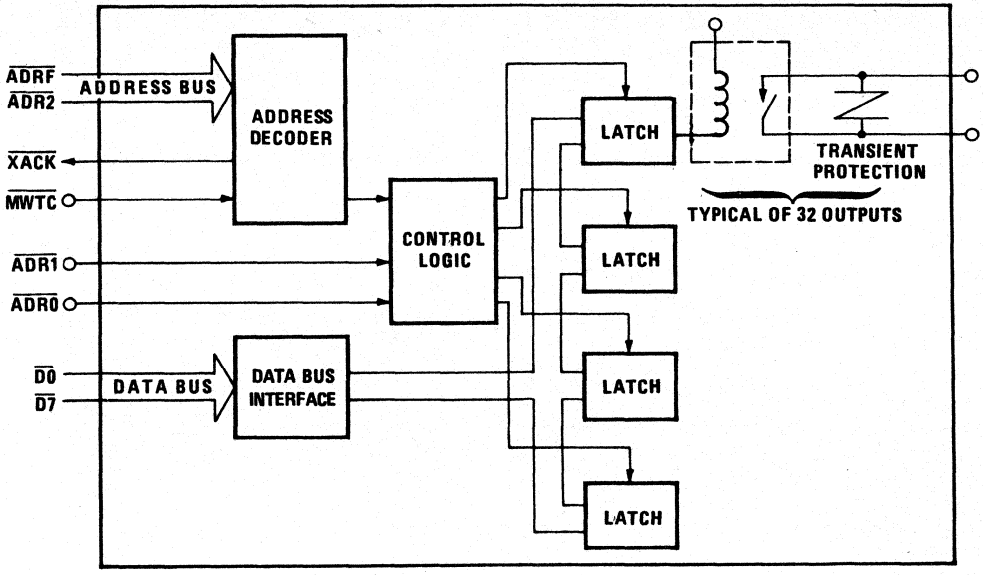
BURR-BROWN



MP801
MP802

MICROCOMPUTER DIGITAL OUTPUT SYSTEMS

A 16- OR 32-CHANNEL RELAY OUTPUT SYSTEM COMPATIBLE WITH INTEL SBC80 AND INTELLEC MDS MICROCOMPUTERS



FEATURES

- ISOLATED FROM COMPUTER BUS AND CHANNEL TO CHANNEL
- TRANSIENT PROTECTION
- EASY TO PROGRAM AND USE
- MEMORY-MAPPED
- 70°C BURN-IN

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-384

Printed in U.S.A. July, 1978

DESCRIPTION

The MP801 and MP802 are digital output (contact closure) microperipheral boards that are electrically and mechanically compatible with Intel's SBC80 and Intellec MDS microcomputer systems. The MP801 offers 16 digital output channels and the MP802, 32 digital output channels.

Each channel is implemented by a protected reed relay and can handle up to 10 watts. Relays provide low "on-impedance" and high output current and isolate output channels from the computer bus and from channel to channel. Isolation insures that ground loop problems are avoided. The computer is protected from component failures caused by voltage transients and malfunctions occurring in the outside world.

MP801 and MP802 appear as memory locations and data written on the data bus controls the status of each output. A logic 1 will close an output. A logic 0 will open an output. Any memory write instruction may be used.

SPECIFICATIONS

Typical at +25°C and rated supplies unless otherwise noted

ELECTRICAL

NUMBER OF CHANNELS	
MP801	16
MP802	32
DIGITAL OUTPUT	
Watts DC (resistive load) max	10 watts
Amps (resistive load) max	0.5 amps
Voltage (resistive load) max	28 Vrms
Life (resistive load) min	10^8 operations
Initial contact resistance max	0.3 ohms
Actuate Time	1msec
De-Actuate time	250μsec
Bounce time	150μsec
TRANSIENT PROTECTION	
Continuous power rating	250mW
Discharge capacity	30 watt-seconds
Leakage current through transient suppressor at 28V	5mA
COMPUTER BUS	
All signals compatible with Intel SBC 80 and MDS Systems	
Logic Loading	1 LSTTL
Output Coding	0 Open Contact 1 Close Contact
POWER REQUIREMENTS	
Voltage	5VDC, ±5%
Supply Drain max, MP801	0.3 amp
Supply Drain max, MP802	0.5 amp
ISOLATION VOLTAGE	
Between microcomputer bus and outputs	600VDC
Between outputs	300VDC
OPERATING TEMPERATURE	0 to +70°C
STORAGE TEMPERATURE	-55 to +125°C

TABLE I. Electrical Specifications

MECHANICAL

Compatible with SBC 80 and Intellec MDS card spacing.

Minimum card spacing: 12.7mm (0.5").

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers (SAE-43D/1-2).

Two 50 pin output edge connectors on board. One is used for MP801, both are used for MP802.

A mating connector is available from Burr-Brown: 2250MC (Viking # 3VH25/1JN5, solder tab). A Scotchflex connector is available from 3M: 3415-0001.

OPERATING INSTRUCTIONS

PROGRAMMING

Each digital output channel appears as one bit of memory to the microcomputer. The channels are selected in groups of eight by $\overline{ADR0}$ on the MP801 and by $\overline{ADR1}$-$\overline{ADR0}$ on the MP802. The remainder of the address lines are used to select the board itself. Because the address block occupied by each board is user selectable, it can be placed anywhere in memory. Writing a logic 1 to an output channel closes the output contact; writing a logic 0 to an output channel opens the output contact. Once an output is defined, it will remain in that state until redefined by another write to that byte. For example, to open channels 0, 2, 6, and close channels 1, 3, 4, 5, 7 with an MP802 as shipped from the factory execute:

```
MVI   A, BAH
STA   F700H
```

where BA (1011 1010) is the data written to the board and F700 is the address of channels 0-7. Refer to Table II for a description of which data and address lines control which output channels.

Data Bus	ADDRESS LINES (A1, A0)			
	00	01	10	11
$\overline{D7}$	7	15	23	31
$\overline{D6}$	6	14	22	30
$\overline{D5}$	5	13	21	29
$\overline{D4}$	4	12	20	28
$\overline{D3}$	3	11	19	27
$\overline{D2}$	2	10	18	26
$\overline{D1}$	1	9	17	25
$\overline{D0}$	0	8	16	24

TABLE II. Data - Address - Channel Relationship.
Logic 0 = open, Logic 1 = close.

The MP801 and MP802 are passive during a read to their memory locations. Therefore, other memory or I/O devices may be placed at the same address without interfering with the microperipheral's activities.

DIGITAL OUTPUT CHANNEL

Each output is capable of switching an inductive load. Transient suppressors are used across each output switch to protect the output relay from damage due to surges when the contact is opened. A typical output circuit and

the load circuit that it might drive are shown in Figure 1 below.

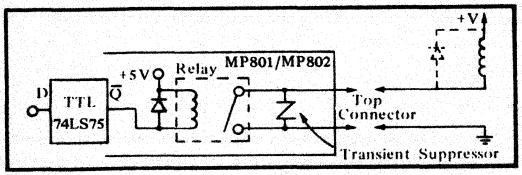


FIGURE 1. Typical Output Circuit, With Load.

Each relay is rated to .5 amps and 100 volts maximum. The transient suppressor reduces the maximum voltage to 28Vrms.

ADDRESSING

The board address is determined by the state of jumpers W1 - W12. Each jumper pair (W1 - W7, W2 - W8, W3 - W9, etc., are jumper pairs) controls one input to a two input exclusive-or gate. These fifteen exclusive-or gates (IC 5-8) comprise the address decoder. An address is valid on the address bus when its complement appears at the jumpers.

As shipped from the factory, the MP801 occupies addresses F700 and F701, and the MP802 occupies addresses F700 to F703. The most significant byte of the address (F7) is set by plated-through holes. However, the address may be changed by drilling out the plated-through holes. See Table IV.

The least significant byte of the address is controlled by jumpers W1 - W12. As shipped from the factory, W1 to W12 are installed on both the MP801 and MP802, pulling all jumper inputs low. Initially, the address in binary for the MP801 is 1111 0111 0000 000A_0, and for the MP802, 1111 0111 0000 00A_1A_0 where A_0 and A_1 are used to select the output channels.

To change the least significant byte of the address clip one, and only one, jumper from each set of jumpers (W1-W7, . . . W6 - W12). For example, to change the board address for an MP801 to 1111 0111 1100 000A_0, clip W7, 8, 3, 4, 5 and 6. (See Table III). By clipping jumpers, the board address may vary from F700 to F7FF for a possible 256 digital output channels (A_0 and A_1 represent $\overline{ADR0}$ and $\overline{ADR1}$).

JUMPER DESCRIPTION

W1-W12 These jumpers are used to select the least significant byte of the board address. All of these jumpers are installed at the factory, giving the board an address of 1111 0111 0000 00A_1A_0. Changing the board address only requires clipping jumpers. A pair of jumpers is used to determine the correct address for each address line as shown in Table III.

Address Bit	Clip for "High" (1) Address	Clip for "Low" (0) Address
$\overline{ADR7}$	W7	W1
$\overline{ADR6}$	W8	W2
$\overline{ADR5}$	W9	W3
$\overline{ADR4}$	W10	W4
$\overline{ADR3}$	W11	W5
$\overline{ADR2}$	W12	W6
IMPORTANT: One, and only one, jumper must be removed for each address line when changing the board address.		

TABLE III. Address Modification, $\overline{ADR2}$ through $\overline{ADR7}$.

W13-W17 Test point jumpers. Clipped after factory testing is completed.

W18-W41* These jumpers are used to select the eight most significant bits of the board address if changed from F7 as set at the factory. Changing the address requires drilling out plated-through hole W* jumpers and installing W jumpers. A # 54 drill (0.055"/1.4mm) should be used for drilling out plated jumpers. Exercise caution to prevent damage to the board. Carefully remove any metal particles deposited on the board's surface. See Figure 2.

For each address line changed, one plated-through hole must be drilled out and one jumper installed as shown in Table IV.

Address Line	Factory Set	Drill Out Plated Hole	Install For 0	Install For 1
$\overline{ADRF}$	1	W*41	W26	W18
$\overline{ADRE}$	1	W*40	W27	W19
$\overline{ADRD}$	1	W*39	W28	W20
$\overline{ADRC}$	1	W*38	W29	W21
$\overline{ADRB}$	0	W*37	W30	W22
$\overline{ADRA}$	1	W*36	W31	W23
$\overline{ADR9}$	1	W*35	W32	W24
$\overline{ADR8}$	1	W*34	W33	W25

TABLE IV. Address Modification, $\overline{ADR8}$ through $\overline{ADRF}$.

FIGURE 2. Drilling Out Plated-Through Holes.

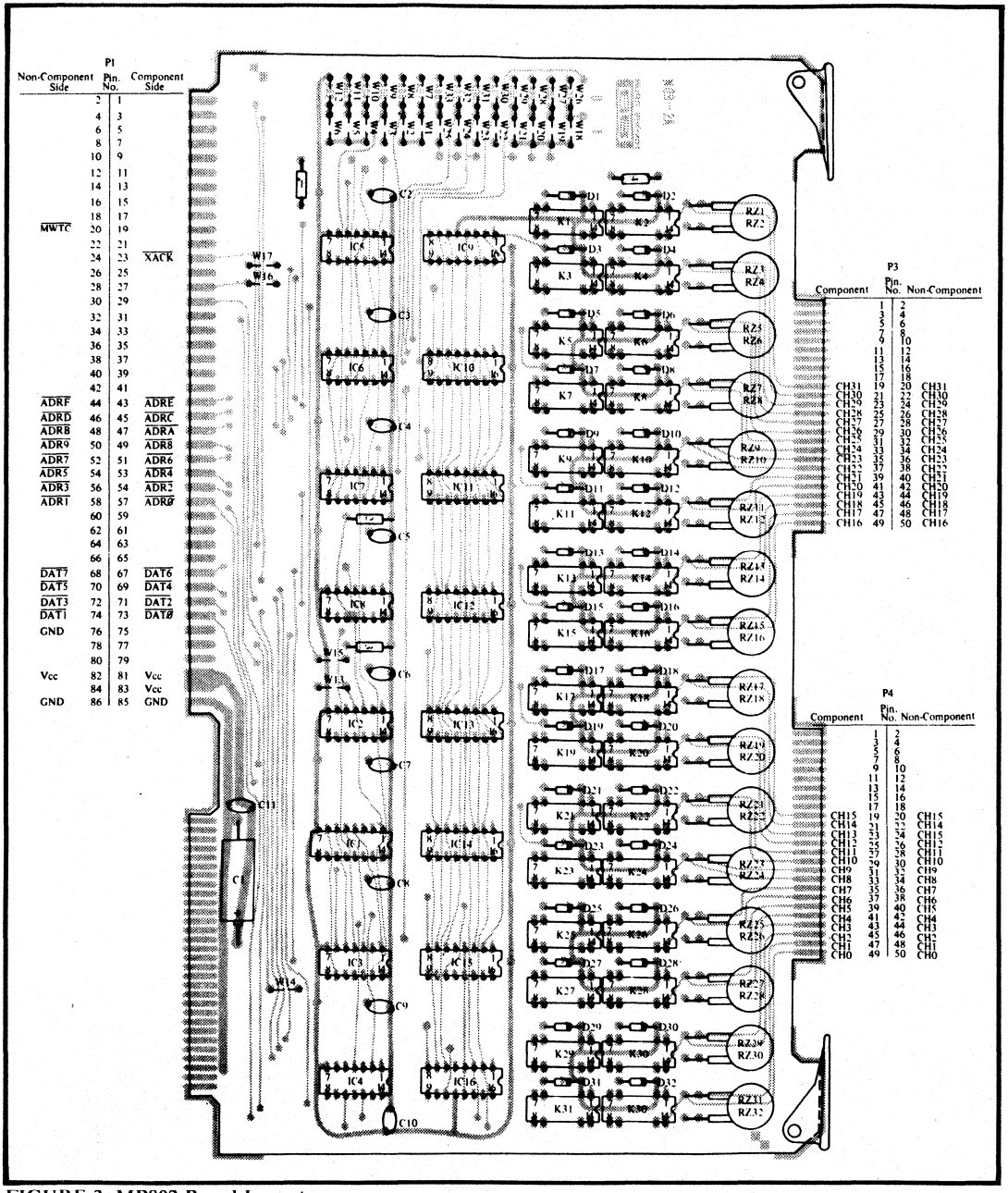


FIGURE 3. MP802 Board Layout.

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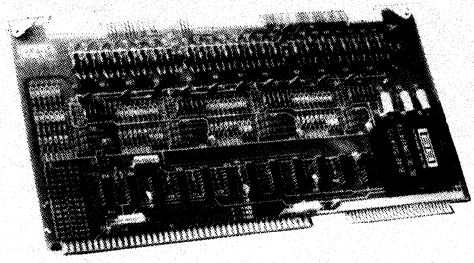
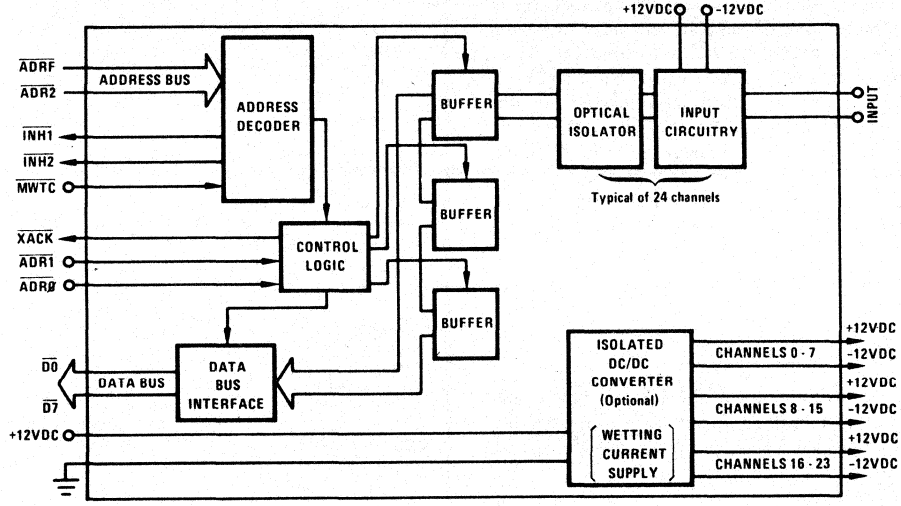


MP810

MICROCOMPUTER DIGITAL INPUT SYSTEM

A 24-CHANNEL ISOLATED DIGITAL INPUT SYSTEM COMPATIBLE WITH INTEL SBC80, NATIONAL BLC80 AND INTELLEC MDS



FEATURES

- ISOLATED FROM COMPUTER BUS AND CHANNEL TO CHANNEL
- CONTACT CLOSURE OR VOLTAGE INPUTS
- REDUCES SYSTEM DEVELOPMENT TIME
  - System engineered and specified
  - Plug compatible
  - Easy to program
  - Operates from computer power supply
- 70°C burn-in

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PDS-391

Printed in U.S.A. July, 1978

DESCRIPTION

The MP810 and MP810-NS are 24 channel, optically isolated, digital input microperipheral boards that are electrically and mechanically compatible with Intel SBC80, National BLC80 and Intellec MDS microcomputer systems. Each printed circuit board operates from the computer's power supplies. Digital inputs enter through card edge connectors located opposite the bus connector.

The MP810 operates with dry relay contacts. The MP810-NS operates with voltage inputs (wet relay contacts). The MP810 may be modified by jumper selection to operate with voltage or contact closure inputs, or a mixture of both. Inputs are arranged in groups of eight. Each group is isolated from other groups and from the computer bus up to 600VDC. Isolation between inputs is 300VDC (MP810-NS). Isolation protects the computer from voltage transients and malfunctions. In addition, since each input is isolated, the voltage switched by each line is not critical and ground loops are avoided.

MP810's are programmed as memory locations. Each input is one memory bit, therefore any memory read instruction may be executed. When the board is read, logic 0 represents an open contact (low voltage); logic 1, a closed contact (high voltage). Each read command inputs the status of eight channels. Address bits ADR0 and ADR1 select that set of inputs to be read. The remainder of the address lines are used to select the board itself. The address block occupied by each board is selectable and can be located anywhere in memory.

INSTALLATION

These units are shipped from the factory ready for immediate use. Installation requires only plugging the card into any empty slot in the computer and wiring the input connector.

MECHANICAL

Compatible with SBC80, BLC80 and Intellec MDS spacing.

Minimum card spacing: 12.7mm (0.5").

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers (SAE-43D/1-2).

Two 50 pin input connectors on each board.

A mating connector is available from Burr-Brown: 2250MC (Viking # 3VH25/1JN5, solder tab). A Scotchflex connector is available from 3M: 3415-0001.

SPECIFICATIONS

Typical at +25°C and rated supplies unless otherwise noted.

ELECTRICAL

INPUT CHARACTERISTICS	
Number of Channels	24
Input Impedance	15kΩ
Input Delay Times	
Open to closed	25μs, max
Closed to open	100μs, max
VOLTAGE SENSE	
MP810-NS	
Minimum voltage to detect a logic 1	17V
Maximum voltage to detect a logic 0	4V
CONTACT CLOSURE SENSE	
R_{closed}	
MP810 (on board ±12V supply)	6kΩ, max
MP810-NS	
at 24V across contacts	6kΩ, max
at 48V across contacts	30kΩ, max
at 60V across contacts	58kΩ, max
R_{open}	
MP810 (on board ±12V supply)	80kΩ, min
MP810-NS	
at 24V across contacts	80kΩ, min
at 48V across contacts	175kΩ, min
at 60V across contacts	235kΩ, min
Maximum voltage (V_S) across input without damage	
MP810	120VAC, rms, max 60VDC, max
MP810-NS	168VAC, rms, max 84VDC, max
ISOLATION VOLTAGE	
Between microcomputer bus and inputs	600VDC
Between inputs (MP810-NS only)	300VDC
Between groups of 8 inputs (MP810/MP810-NS)	600VDC
POWER REQUIREMENTS	
MP810	+5VDC ±5% at 400mA +12VDC ±5% at 100mA
MP810-NS	+5VDC ±5% at 400mA
COMPUTER BUS	
All signals compatible with Microcomputer bus	
Logic loading	1 LSTTL Load
Input coding	Logic 0: open contact Logic 1: close contact
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55 to +125°C

TABLE I. Electrical Specifications

DEFINITION OF SPECIFICATIONS

INPUT DELAY TIME

OPEN TO CLOSED - The delay required to detect an input contact closure switching from open to closed.

CLOSED TO OPEN - The delay required to detect an input contact closure switching from closed to open.

CONTACT CLOSURE IMPEDANCES

R_{CLOSED} - The impedance of an input contact when closed. R_{CLOSED} specification is the maximum impedance allowed to reliably detect a closure See Figure 1.

R_{OPEN} - The impedance of an input contact closure when open. R_{OPEN} specification is the lowest impedance allowed to reliably detect an open contact.

OPERATING INSTRUCTIONS

PROGRAMMING

Each digital input channel appears as one bit of memory to the microcomputer. Channels are selected in groups of eight by ADR1-ADR0. Reading a logic 1 from an input channel indicates that the contacts are closed or voltage is present. Reading a logic 0 from an input channel indicates that the contact is open or voltage is not present. Each word read from the MP810 is the instantaneous status of each channel as the read operation occurs. Only one instruction is required to input eight channels of information. For example:

LDA F600H

will load the accumulator with channels 0-7, where F600 is the address of channels 0-7. Table II indicates which data and address lines input which channels.

Data Bus	ADDRESS LINES (ADR1, ADR0)			
	00	01	10	11
$\overline{D7}$	7	15	23	*
$\overline{D6}$	6	14	22	*
$\overline{D5}$	5	13	21	*
$\overline{D4}$	4	12	20	*
$\overline{D3}$	3	11	19	*
$\overline{D2}$	2	10	18	*
$\overline{D1}$	1	9	17	*
$\overline{D0}$	0	8	16	*
	Channel Number			

* Not used.

TABLE II. Data - Address - Channel Relationship. 0 = open, 1 = close.

MP810 is passive during a write to its memory locations. Therefore, other memory mapped output devices may be placed at the same address without interfering with the MP810's functions.

DIGITAL INPUT CHANNEL

Each input can read a contact closure - an input circuit is shown below.

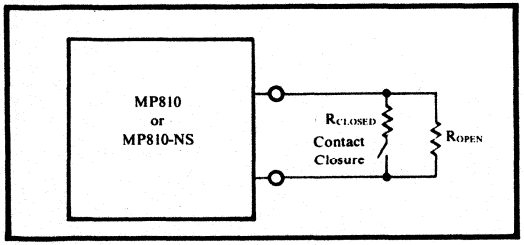

FIGURE 1. Typical Input Circuit

MP810 is designed for dry (without external voltage source) contact closures and its circuit is shown in Figure 2.

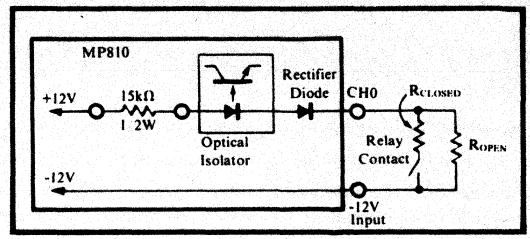

FIGURE 2. MP810, Typical Circuit

The isolated ±12V is obtained from the computer's +12VDC power supply and an optional isolated DC/DC converter. Three separate ±12VDC supplies are used on the MP810, each supplying wetting current for eight channels. Isolation voltage between each group of eight outputs is 600VDC. Table III defines the groups. The contact closure must be placed between the proper channel input and a -12V connection. See Table III for proper -12V pins to be used with each input channel group.

Group	Channel Number	Connector	-12V Pins
1	0 - 7	P3	27, 28, 29, 30
2	8 - 15	P3	39, 40
		P4	15, 16
3	16 - 23	P4	47, 48, 49, 50

TABLE III. Isolation Groups

MP810-NS is designed for voltage inputs and wet (with external voltage source) contact closures. A typical circuit is shown in Figure 3. Voltage input sensitivity of the MP810-NS may be changed by removing the 15kΩ input resistor shown in Figure 3 ($R1_b$ - $R24_b$) and replacing it with a resistance calculated by this formula:

$$R = (V_{IN} - 2)\ 10^3\Omega.$$

V_{IN} (in volts) is the voltage required to detect a logic 1 input. If the value of the input resistor is reduced, the "maximum input voltage without damage" specification (see page 6-20) will be reduced proportionally. Likewise, if the input resistance is increased, the "maximum input voltage without damage" will be increased proportionally up to a maximum of 300VDC.

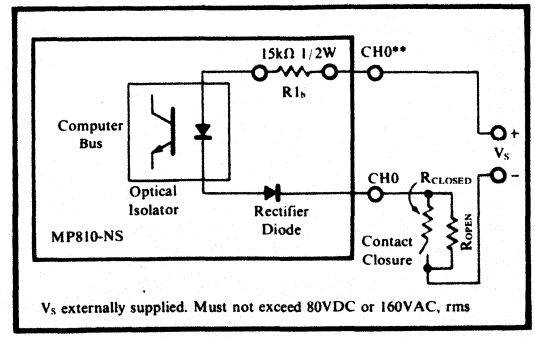

FIGURE 3. MP810-NS, Typical Circuit

The MP810-NS inputs are isolated channel-to-channel by 300VDC within groups defined in Table II. Isolation voltage between each group of eight outputs is 600VDC. See Figure 4 for MP810-NS isolation voltages.

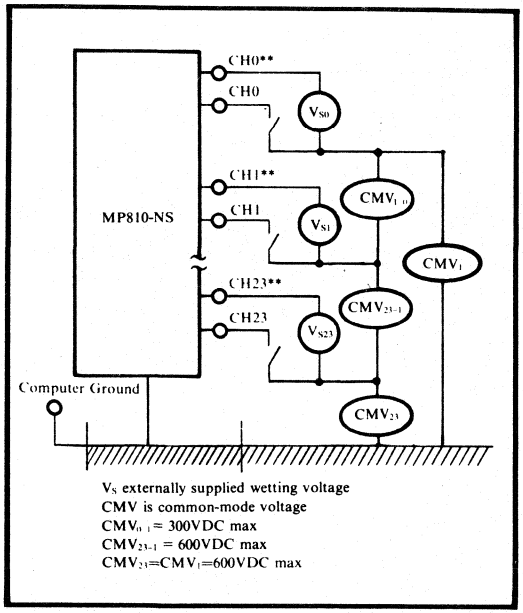

FIGURE 4. MP810-NS Isolation Circuit

ADDRESSING

The board address is determined by the state of jumpers W1 to W28 and W38* to W44*. A jumper pair controls one input to a two-input quad exclusive-or gate. Fourteen exclusive-or gates comprise the address decoder. An address is valid on the address bus when its complement appears at the jumpers. MP810 and MP810-NS, as shipped from the factory, occupy address F600 to F602.

The least significant byte of address is controlled by jumpers W1 to W12. As shipped from the factory, W1 to W12 are installed, pulling all jumper inputs low. Initially, the binary address for these boards is 1111 0110 0000 $00A_1A_0$, where A_0 and A_1 are used to select the input channels.

ADDRESS BIT	CLIP FOR "HIGH" (1) ADDRESS	CLIP FOR "LOW" (0) ADDRESS
ADR7	W11	W12
ADR6	W7	W8
ADR5	W5	W6
ADR4	W9	W10
ADR3	W1	W2
ADR2	W3	W4
IMPORTANT: One and only one jumper must be removed for each address line when changing the board address.		

TABLE IV. ADR2 - ADR7 Address Selection

To change the least significnt address byte, clip one and only one, jumper from each set of jumpers (W1, W12 ... W11, W12). For example, to change the board address to 1111 0110 1100 $00A_1A_0$, clip W11, 7, 6, 10, 2 and 4. See Table IV. By clipping jumpers, the board addresses may vary from F600 to F6FF for a possible 1536 input channels.

The most signficant byte of the address (F6) is set by plated-through hole jumpers W38* to W44*. The address may be changed by drilling out plated-through hole jumpers with a #54 (0.055"/1.4mm) drill bit. Exercise caution to prevent damage to the board. Carefully remove any metal particles deposited on the board's surface. See Figure 5.

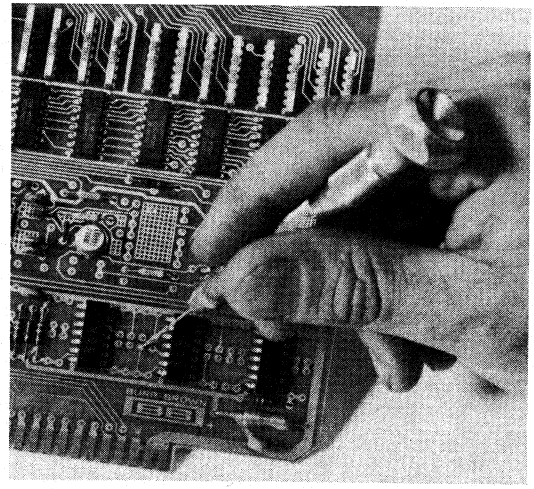

FIGURE 5. Drilling Out Plated-Through Holes.

For example, to change the most significant byte from F6 to F0, drill out W43* and W44* and install W19 and W13. See Table V.

TO CHANGE:			
ADDRESS BIT	DRILL	INSTALL FOR 0	INSTALL FOR 1
ADRF	W38*	W23	W24
ADRE	W39*	W17	W18
ADRD	W40*	W15	W16
ADRC	W41*	W27	W28
ADRB	W42*	W21	W22
ADRA	W43*	W19	W20
ADR9	W44*	W13	W14
ADR8	W45*	W25	W26
IMPORTANT: If a W* jumper is drilled out, then the corresponding "W" jumper must be installed. Also, if a "W" jumper is installed, then the corresponding "W*" jumper must be drilled out.			

TABLE V. ADR8-ADRF Address Selection.

DEBOUNCING AND AC SENSE

Debouncing and AC sense circuitry layout is included on the MP810/MP810-NS PC board. These components are not loaded. Contact the factory if more information is required.

Other Burr-Brown Microperipherals for Intel Microcomputers and Microprocessors.

PC BOARD SUBSYSTEMS - Compatible with Intel SBC80, National BLC80 and Intellec MDS Microcomputers.

MP8408/MP8416	- general purpose 12 bit resolution Analog Input systems
MP8600 series	- low cost 8 bit resolution Analog Input and Output system
MP8304	- general purpose 12 bit resolution Analog Output system
MP8418	- low cost 12 bit resolution Analog Input and Output system
MP8418-PGA	- general purpose 12 bit resolution Analog Input and Output system with software programmable gain amplifier
MP801/MP802	- 16/32 channel relay output system

COMPONENT SUBSYSTEMS - Compatible with 8080 Microprocessors

MP10	- Analog Output component for 8080 microprocessor systems
MP20	- Analog Input component for 8080 microprocessor systems
MP22	- Analog Input component for 8080 microprocessor systems

JUMPER DESIGNATION

W38*-W45* W13-W28 These jumpers are used to select the most significant byte of the board address. Changing the ADRF-ADR8 address lines requires drilling out "W*" jumpers and installing "W" jumpers. A pair of jumpers determines the address for each address line. See Table V.

W1-W12 These jumpers are used to select the least significant byte of the board address. All of these jumpers are installed at the factory giving the board an address of 1111 0110 0000 00A_1A_0. Changing the ADR7-ADR2 address lines requires only clipping jumpers. A pair of jumpers is used to determine the address for each address line as shown in Table IV.

W34-W37 Not installed. May be used with MP810-NS to tie together ±12V on board supply lines for use with external supplies.

W30-W33 Test point jumpers. Clipped after factory testing is complete.

"W*" jumpers are plated-through on the board

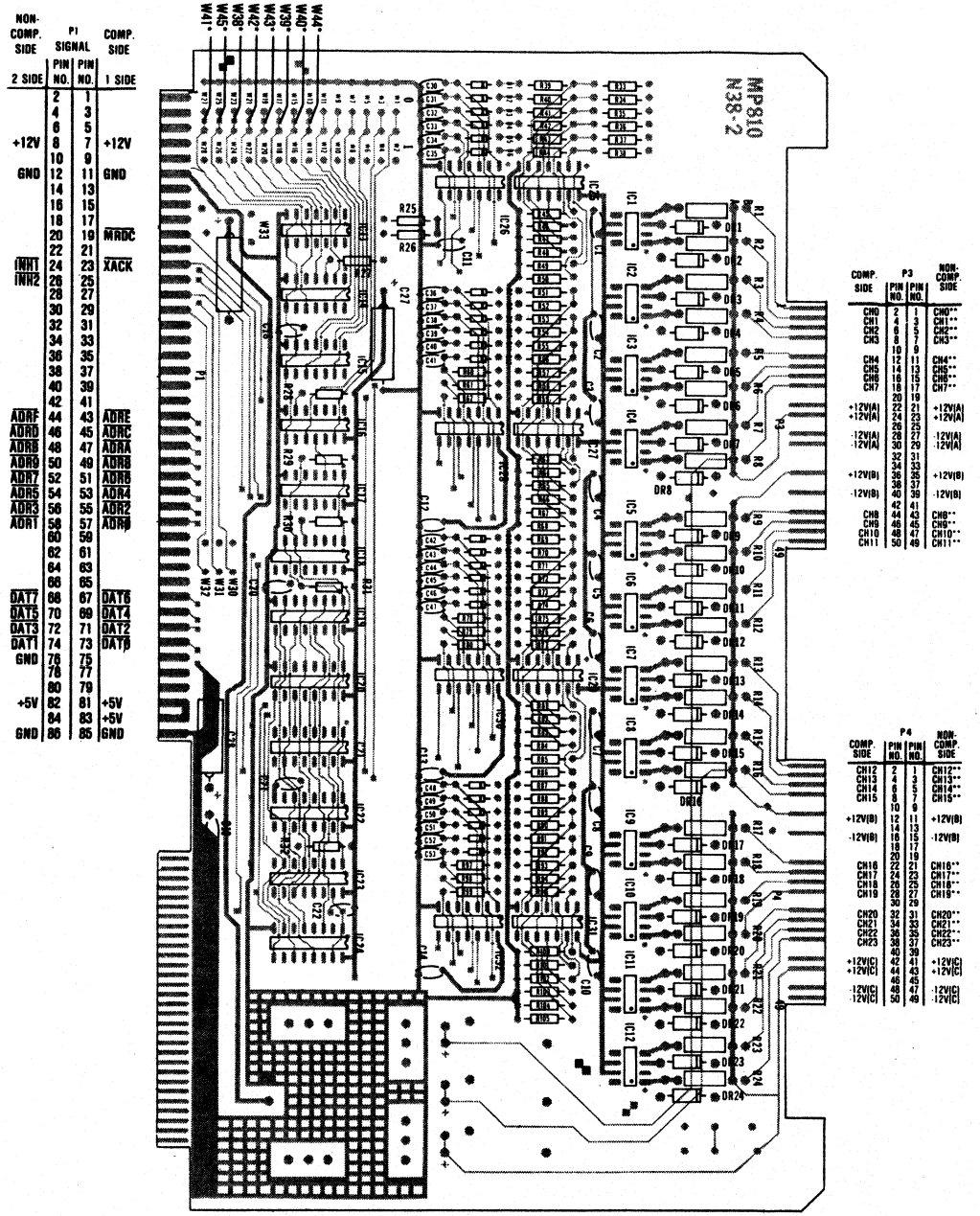

FIGURE 6. MP810 Series Board Layout

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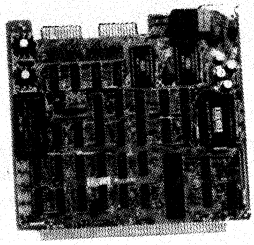


MP2216

ADVANCE INFORMATION
Subject to Change

MICROPERIPHERAL ANALOG INPUT/OUTPUT SYSTEM

A 12-BIT 32 CHANNEL ANALOG INPUT/ 2 CHANNEL ANALOG OUTPUT SYSTEM COMPATIBLE WITH ZILOG MICROCOMPUTERS

FEATURES

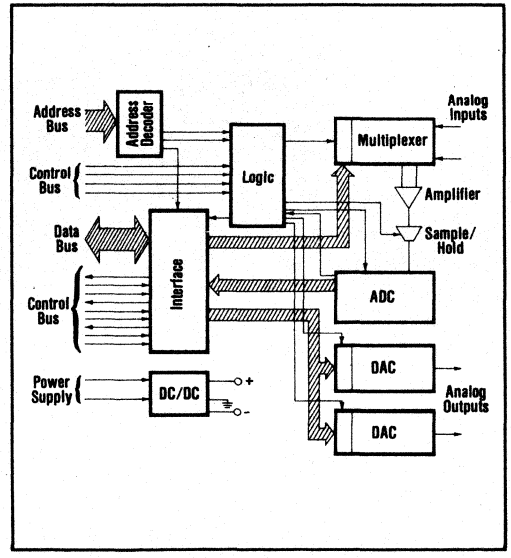
- ANALOG I/O ON THE SAME BOARD
- OPERATES FROM COMPUTER POWER SUPPLY
- HIGH LEVEL OR LOW LEVEL INPUTS

DESCRIPTION

Completely compatible with Zilog's Z-80 MCB® and Z-80 MCS series of microcomputers, MP2216 provides a single board 12-bit resolution analog input/output system. The input section accepts 16 differential or 32 single-ended channels. Inputs ranging from millivolts to volts can be digitized because of MP2216's variable gain instrumentation amplifier.

Two optional channels of analog voltage are provided in the output section of the MP2216. The input data for each digital-to-analog converter is double buffered to minimize output glitches during a data update. Several output ranges and bipolar or unipolar operation are selected by on-board programming.

The MP2216 is mechanically, electrically and logically compatible with the Zilog systems. Power is derived from the +5V logic supply. Logic levels and drive capacity are matched to the system bus. Interfacing is accomplished primarily through a Z-80 PIO contained within the system.



μC I/O MP2216

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PDS-392 Printed in U.S.A. July, 1978

INSTALLATION

MP2216 is shipped from the factory calibrated and ready for immediate use. Installation only requires plugging the card into any of the I/O slots in the MCS chassis. For the MCB system, any slot can be used provided it has first been connected with the proper bus signals. Figure 5 indicates the bus signals required by the MP2216.

THEORY OF OPERATION

The MP2216 interfaces with the Z-80 I/O bus-occupying 10 locations for the complete input/output system. The first four locations are required for the PIO. The next two locations transfer input channel address and board status. The remaining locations are used to pass data to the two digital-to-analog converters.

Data can be acquired from the analog inputs in either the POLLING or INTERRUPT mode:

POLLING MODE - A conversion is initiated by writing the analog channel address to the address register. The program must then periodically test the conversion bit in the status register to determine when the conversion is completed. During initialization of the MP2216's PIO, the interrupt enable must be reset (both ports) to prevent generation of interrupts.

The following program may be used to input a channel of data to the BC register pair:

```
LDA, XX              Load accumulator with channel address (XX) of data
                     to be converted.
OUT (YY), A          Outputs channel address to MP2216's address
                     register (location YY). This starts conversion.
 :                   Other software if desired for conversion time.
 :
STATUS IN A, (ZZ)    Input status bit from location ZZ.
BIT 0, A             Test status bit.
JP Z, STATUS         Jump to STATUS until conversion is complete.
IN A, (WW)           Transfers the least significant byte to the
                     accumulator. WW is PIO port A DATA register.
LD C, A
IN A, (WW + 1)       Transfers the most significant byte to the
                     accumulator. WW + 1 is PIO port B DATA register.
LD B, A
```

INTERRUPT MODE - After setting the board's PIO interrupt enable and vector address, conversion is initiated by writing to the address register. Program execution may then continue until the conversion is complete. At that point the system PIO generates an interrupt vector causing the CPU to begin execution of the MP2216's interrupt service routine. Software for this mode is the same as that of the polling mode, but without the status loop.

Outputting of data from the MP2216's two digital-to-analog converters is straightforward. Each converter occupies two addresses on the I/O bus. The least significant 8 bits of the 12-bit data word are written to the first of these data words while the four most signficant bits are written to the second data word.

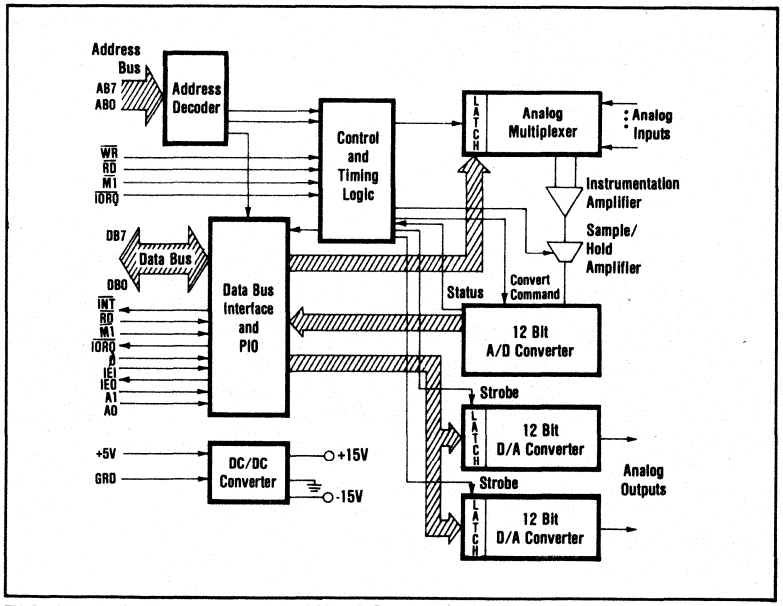


FIGURE 1. Block Diagram MP2216-AO

ELECTRICAL SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

ANALOG INPUT SECTION	
INPUT CHARACTERISTICS	
Number of Channels	32 single-ended/16 differential
ADC Gain Ranges (Jumper Selectable)	0 - 5V, 0 - 10V, ±2.5V, ±5V, ±10V
Amplifier Gain Ranges (resistor programmable)	1 to 1000
Maximum Input Voltage Without Damage	±26 volts
Input Impedance	100MΩ, 10pF OFF Channel 100MΩ, 100pF ON Channel
Bias Current	20nA
Differential Bias Current	10nA
TRANSFER CHARACTERISTICS	
Resolution	12 Bits
Throughput Time (max) G = 1	45μsec/channel
Throughput time (max) G = 1000	100μsec/channel
ACCURACY	
System Accuracy G = 1 (max)[1]	±0.025% FSR[2]
System Accuracy G = 1000	±0.1% FSR
Linearity	±1/2 LSB
Differential Linearity	±1/2 LSB
Quantizing Error	±1/2 LSB
Monotonicity[3]	Guaranteed 0°C to +70°C
STABILITY OVER TEMPERATURE[4]	
System Accuracy Drift (max) G = 1	±30 ppm of FSR/°C
System Accuracy Drift (max) G = 1000	±80 ppm of FSR/°C
DYNAMIC ACCURACY	
Sample and Hold Aperture Time	30ns
Aperture Time Uncertainty	±5ns
Differential Amplifier CMR	74dB (DC to 1kHz)
Channel Crosstalk	80dB down at 1kHz, for OFF channel to ON channel
ANALOG OUTPUT SECTION	
OUTPUT CHARACTERISTICS	
Number of Channels	2
Output Voltage Range (strap selectable)	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA
Output Impedance	1Ω
TRANSFER CHARACTERISTICS	
Resolution	12 Bits
Output Settling Time (max)	10μsec
ACCURACY	
Output Accuracy	±0.0125% FSR
Temperature Coefficient of Accuracy	±30 ppm of FSR/°C
POWER REQUIREMENTS	
MP2216, MP2216-AO	+5V ±5% at 1.6 amp
ENVIRONMENTAL	
Operating Temperature	0°C to +70°C
Storage Temperature	-25°C to +85°C
Relative Humidity	95% noncondensing

TABLE I. Electrical Specifications

NOTES:
1. Includes offset errors, gain errors, linearity errors.
2. FSR means Full Scale Range.
3. No missing codes guaranteed.
4. Includes offset drift, gain drift and linearity drift.

SYSTEM CONFIGURATIONS

The MP2216 microperipheral board is available in two versions.
MP2216-AO: All features of the MP2216 system are included in this configuration.
MP2216: Provides all features except the two digital-to-analog converters.

MP8004: Cable assembly - two required.

MECHANICAL SPECIFICATIONS

Compatible with Zilog Z-80 MCB and Z-80 MCS card spacing.
Minimum card spacing: 12.7mm (0.5")
Microcomputer bus connector: 122 pin PC edge connector with 0.1" contact centers (Augat 14005-1P1).

Analog I/O is accessible through two 26-pin edge connectors on board. The mating connector is Ansley 609-2615M. A 15" mating cable assembly is available from Burr-Brown. The cable assembly includes the Ansley 609-2615M connector at one end and an Ansley 609-25S female pin and socket connector at the opposite end. A male pin and socket connector for user connection of input and outputs is also provided.

The mating cable assembly part number is MP8004, two are required. 16 analog inputs and two analog outputs are available through one connector while the second 16 analog inputs are available through the other connector.

PROGRAMMING

Programming these analog I/O boards is simple. All are treated as I/O locations. Table II indicates the assignment of these locations.

I/O ADDR	Function	
80	Port A Data	PIO Locations
81	Port B Data	
82	Port A Control	
83	Port B Control	
88	Address Register (Select Ch. #)	
89	Status Register	
8C	Low Byte Output Data Register (DAC1)	
8D	High Byte Output Data Register (DAC1)	
8E	Low Byte Output Data Register (DAC2)	
8F	High Byte Output Data Register (DAC2)	

TABLE II. Board I/O Address Assignments

INPUT PROGRAMMING

The first four locations (80_{16} - 83_{16}) are used to program the on-board PIO. A detailed description of the PIO's operation can be found in the Zilog Z80-PIO Product Specification Sheet. Normal operation of the board requires programming the PIO as follows.

Polling Mode - Initialization: Both A and B Mode Control registers must be set for Mode 1. When Mode 1 is active, data from the analog to digital converter can be input to the processor. In addition, the Interrupt Enable must be turned off. The following initialization program illustrates the procedure:

```
DI              ;   DISABLE INTERRUPT
LD A, 4FH       ;
OUT 82H, A      ;   SET PORT A FOR MODE 1
OUT 83H, A      ;   SET PORT B FOR MODE 1
LD A, 07H
OUT 82H, A      ;   DISABLE PORT A INTERRUPT
OUT 83H, A      ;   DISABLE PORT B INTERRUPT
IN A, 80H       ;   INITIALIZE PORT A DATA
IN A, 81H       ;   INITIALIZE PORT B DATA
```

The remaining board locations are treated as described in the following paragraphs which discuss non-PIO locations.

Interrupt Mode - Initialization: As in the Polling Mode, the A and B Mode Control Registers must be set for Mode 1. The PIO interrupt system is enabled by first loading the interrupt vector address and then setting the interrupt enable. Only Port B interrupt enable should be set. This program illustrates the procedure (In addition to initializing the PIO the program also loads the Z80's Interrupt Vector Register.):

```
DI              ;   DISABLE INTERRUPT
LD A, N         ;   LOAD I VECTOR REGISTER
LD I, A
LD A, M         ;   SET PIO INTERRUPT VECTOR*
OUT 83H, A
LD A, 4FH
OUT 82H, A      ;   SET PORT A FOR MODE 1
OUT 83H, A      ;   SET PORT B FOR MODE 1
LD A, 07H       ;   DISABLE PORT A INTERRUPT
OUT 82H, A
LD A, 87H       ;   SET PORT B INTERRUPT
OUT 83H, A
IN A, 80H       ;   INITIALIZE PORT A DATA
IN A, 81H       ;   INITIALIZE PORT B DATA
IM 2
EI
```

*Bit 0 of M should be 0 to signify an interrupt vector.

The remaining non-PIO locations are programmed with either the Polling or Interrupt Mode in this manner:

Non-PIO Locations - Location 88_{16} specifies the particular analog input channel to be digitized. Writing the channel number ($0\text{-}1F_{16}$) into the Address Register at this location will cause a conversion to be performed.

The Status Register (see Figure 2), at location 89_{16}, provides data indicating if the analog-to-digital converter is performing a conversion and, also, if the converted data has been read. During a conversion in progress, DB0 displays a 0. At all other times it displays a 1. DB1 is 0 after a conversion has been performed and then changes to 1 after the first complete reading of the converted data.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	X	X	X	X	READ STATUS	A/D STATUS

FIGURE 2. Status Register

OUTPUT PROGRAMMING

As shown in Table II, the two digital-to-analog converters occupy locations $8C_{16}$ - $8F_{16}$. Either converter is programmed by first loading the least significant eight bits of data into its Low Byte location. The most significant four bits of data are then loaded into the right-most bits of the converter's High Byte. The most significant four bits of this byte are unused. Figure 3 illustrates this bit placement.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0

Low Byte ($8C_{16}$ or $8E_{16}$)

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	X	X	B_{11}	B_{10}	B_9	B_8

High Byte ($8D_{16}$ or $8F_{16}$)

FIGURE 3. DAC Bit Placement

ADDRESS MODIFICATION

As received from the factory MP2216 is wired to occupy those locations shown in Table II. However, it is possible to move the on-board PIO and the on-board registers independently throughout the I/O address space. The only limitations on address selection are that the PIO and board registers cannot occupy the same locations and that the three most significant address bits of the PIO and of the board registers must be the same.

Address modification is achieved by first removing the existing address selection jumpers and then installing those indicated in Tables III and IV for the desired address. Wherever a "1" occurs in the address the "1" jumper should be installed and where a zero occurs the "0" jumper should be installed.

Address Bit	Jumper for "1"	Jumper for "0"
2	JP39	JP38
3	JP41	JP40
4	JP30	JP31
5	JP32	JP33
6	JP27	JP26
7	JP28	JP29

TABLE III. PIO Address Selection Jumpers.

Address Bit	Jumper for "1"	Jumper for "0"
3	JP37	JP36
4	JP34	JP35
5	JP32	JP33
6	JP27	JP26
7	JP28	JP29

TABLE IV. Register Address Selection Jumpers.

INPUT RANGE SELECTION

Two elements determine the voltage range of the input system: the input range setting jumpers and the gain of the instrumentation amplifier. As shipped from the factory, the input range is set for ±10V and the instrumentation amplifier gain is 1.

Other input ranges are possible and can be selected as shown in Table V.

RANGE	JUMPERS
±10V	W8*, W7*, W9*, W10*
±5V	W8*, JP21, W9*, W10*
±2.5V	W8*, JP20, JP21, W9*, W10*
0 - +10V	JP23, JP21, JP25, JP43
0 - +5V	JP23, JP20, JP21, JP25, JP43

TABLE V. Input Range Setting Jumpers.

All "W" jumpers marked with an asterisk are installed at the factory and are implemented by a plated-through hole connecting pads on the upper and lower surfaces of the board. These can be removed by careful manual drilling with a 0.055"/1.4mm (#54) drill. All "JP" jumpers are wire and should be sleeved whenever a possible short could occur.

When the range is changed, those existing jumpers that are not used for the new range must first be removed and then the additional jumpers installed.

Analog-to-digital converter output data is normally presented in 2's complement format for bipolar ranges. For straight binary operation, remove wire jumper W9* and install JP25.

DIFFERENTIAL, SINGLE-ENDED SELECTION

MP2216 is shipped from the factory to operate in 16-channel differential mode. The input system can be changed from differential to single-ended (or vice versa) by changing a few jumpers. Table VI shows the jumpers required. Jumpers for the current mode should be removed and jumpers for the desired range installed.

Differential operation is generally used to minimize common-mode noise during low level operation and is recommended for all voltage inputs. Single-ended operation may be used for large input signals (over 1 volt full scale) with a minimum of noise. A sizeable noise reduction can often be achieved in single-ended operation by making a "pseudo differential" connection. This involves sensing the ground at the signal source rather than at the board. To use this method, all input signals must be on the same ground system at their source.

Jumpers for pseudo differential operation are connected as shown in Table VI for single-ended operation, except that jumper JP18 is removed and JP1 installed.

Jumpers Required For 16 Channel Differential	Jumpers Required For 32 Channel Single-ended
W6* JP5 JP3	JP16 JP18 JP6 JP2

TABLE VI. Differential/Single-ended Operation

BIPOLAR - TWO'S COMPLEMENT			
Digital Input/Output	±10V	±5V	±2.5V
(0000)* 0111...11 ($0*7FF_{16}$)	+9.9951V	+4.9975V	+2.4988V
(1111)* 100...00 ($F*800_{16}$)	-10.0000V	-5.0000V	-2.5000V
*The unused four most significant bits are connected to the most significant bit of the data word.			

UNIPOLAR - STRAIGHT BINARY		
Digital Input/Output	0 to +10V	0 to +5
(0000)* 111...111 ($0*FFF_{16}$)	9.9975V	4.9988
(0000)* 000...00 ($0*000_{16}$)	0.0000V	0.0000V
*The unused four most significant bits are connected to ground.		

TABLE VII. Analog Input Full Scale Range Values

INPUT SYSTEM LOW LEVEL OPERATION

When the input system instrumentation amplifier is operated at other than unity gain, a gain setting resistance must be added. R8 and R9 in parallel form this resistance. The value of the gain setting resistance (R) can be calculated from this formula:

$$\text{Gain} = 20k\Omega/R - 1$$

Stable (10ppm/°C) wire-wound resistors should be used.

Increasing amplifier gain also increases its settling time. As a result, the delay of the system delay timer must be increased by increasing the value of R15 and the optional parallel resistor R14. Delays and values of R15 || R14 versus Gain are shown in Table VIII.

Amplifier Gain	Delay Time (μs)	R15 || R14 (±5%)
1	20	13.3k
10	30	14.3k
100	40	19k
1000	100	47.5k

TABLE VIII. Delay Time vs. Amplifier Gain

INPUT SYSTEM APPLICATION

The data acquisition system incorporated in MP2216 uses a fixed timing sequence (the system delay timer) between channel selection and the start of data conversion to allow for the settling time of the multiplexer, instrument amplifier and sample/hold. If desired, this time may be increased by increasing the value of R15 || R14. This procedure is described in the low level operation section.

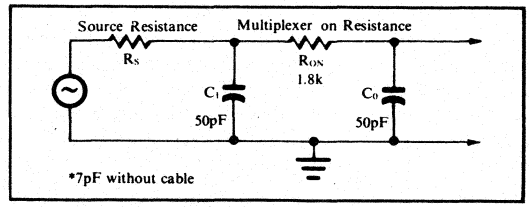


FIGURE 4. "ON" Channel Multiplexer Circuit Model for Single-Ended Operation.

Time allowed by MP2216 for multiplexer settling is 20μs, sufficient for most applications. The only external factor which affects the multiplexer settling time is output impedance (R_S) of the source connected to a channel. A circuit model of an "ON" channel is shown in Figure 4. The input capacitance of 50pF (C_I) for single-ended operation does not affect the settling time since it is continuously connected to the source. The signal at the output of the multiplexer must be allowed to settle to ±0.01% (nine time constants) to maintain full accuracy of the system. The multiplexer time constant can be calculated with the formula: $\tau = (R_S + R_{on})C_o$. For a source resistance of 1kΩ, $\tau = (1 + 1.8)k\Omega \times 50pF = 140ns$. Thus, 1.20$\mu s$ is needed to settle to ±0.01%. This is well below the fixed 20μs allowed for settling time so that the accuracy of the system is preserved.

If the source bandwidth can be limited, high impedance sources may be accurately handled by placing a large

capacitor across the multiplexer input. An analysis of such a circuit shows that a capacitor of 0.5μF is sufficient. For such a capacitance the multiplexer time constant becomes 90ns. If this method cannot be used, time allowed for settling can be increased as described in the section on low level operation.

The ON-resistor is the channel resistance of a FET, a nonlinear function of the applied voltages. As a result, the previous calculations are only an approximation derived from a linearized model. Another factor not considered is the addressing delay of the multiplexer. This is typically 250ns and is added to the calculated times listed.

For differential units the same considerations apply. Even though two input circuits are involved there is sufficient component matching within the multiplexer to prevent measurable differences in the transfer functions for each half of the signal. When operated in the differential mode, C_o in Figure 4 becomes 12.5pF with an R_{on} = 1.8k in each leg. Therefore, the time constant becomes 1/2 the time constant for a single-ended channel.

Analog inputs have reverse biased diode circuits which prevent damage from discharge of static electricity. However, reasonable precautions should be taken against static discharge.

For a more complete discussion on the application of analog data acquisition systems, obtain a copy of Burr-Brown Application Note AN-79, "Principles of Data Acquisition and Conversion."

INPUT SYSTEM CALIBRATION

System calibration is typically performed on a single channel while running the following program (the program assumes that the Polling Mode initialization has been performed as described in the Programming section):

```
AD:     LD BC, 0H
        LD D, 64H
AE:     LD A, 0H          ;Load addr. reg with ch. #0
        OUT 88H, A
AC:     IN A, 89H         ;Is conversion complete?
        AND 01H
        JP Z, AC          ;No.
        IN A, 80H         ;Yes. Read data
        LD L, A
        IN A, 81H
        LD A, L           ;Is data = low ref.?
        SUB REF           ;Ref = 0H for offset adj.
                          ;REf = FFH for gain adj.
        JP Z, AA
        INC C             ;No. Increment count
        JP AB
AA:     INC B             ;Yes. Increment count
AB:     DEC D             ;Have 100 conversions been
                          performed?
        JP NZ, AE
AF:     JP AD             ;Yes. Repeat
        END
```

This program has been written assuming the board is wired for the addresses shown in Table II. If the board responds to other addresses, the program references to I/O locations must be made to conform to these new locations. After assembling and loading, insert a breakpoint at location AF.

Calibration is performed by connecting a precision voltage source capable of 0.005% accuracy to CH0. (This could also be a DC voltage source of less absolute accuracy whose output is monitored by a 0.005% DVM.) Offset and gain adjustments on the system are made while applying the voltages shown in Table IX. For other ranges the offset voltage adjustment is made at the most negative value of the range, less one-half least significant bit (LSB). An LSB is equal to the span (full scale range) divided by 4096 for 12-bit resolution. Gain adjustment is made at the most positive value of the range, less 1-1/2LSB. Thus for a range of ±50mV, an LSB is 100mV/4096 = 24.4μV. The offset adjustment is made at -50mV + 12.2μV = -49.988mV and the gain adjustment at +50mV -36.6μV = +49.963mV. Before making these adjustments allow the unit to reach thermal equilibrium (about 30 minutes under power).

Offset adjustment is made first by using the calibration program. After 100 conversions the calibration program will halt at the breakpoint. The contents of B and C registers should be compared for approximately equal values. If a difference of more than 10_{16} is present, slightly readjust the offset control and restart the program. Repeat this procedure until the registers' contents are within 10_{16} of each other.

The gain adjustment is made in the same manner. However, the value of REF is changed for 0 to FF. The appropriate gain voltage is then applied and the calibration procedure performed as described for the offset adjustment.

RANGE	OFFSET	GAIN
±10V	-9.9976V	+9.9926V
±5V	-4.9988V	+4.9963V
±2.5V	-2.4994V	+2.4981V
0 to +10	+1.22mV	+9.9953V
0 to +5	+0.61mV	+4.9981V

TABLE IX. Data Acquisition Calibration Values.

OUTPUT RANGE SELECTION

Each DAC is jumpered at the factory for ±10 volt operation and two's complement coding. However, it is possible to alter these jumpers as shown in Table X for other output voltages. Jumpers indicated by an asterisk are plated-through holes on the board and should be removed by careful manual drilling with a 0.055"/1.4mm (#54) drill. When making a change first remove jumpers indicated for the present range and replace them with jumpers required for the desired range.

	JUMPERS	
RANGE	DAC1	DAC2
±10V	W1*, W2*	W3*, W4*
±5V	JP11, W2*	JP15, W4*
±2.5V	JP11, W2*, JP9	JP15, W4*, JP13
0 - +10V	JP11, JP8	JP15, JP12
0 - +5V	JP11, JP8, JP9	JP15, JP12, JP13

TABLE X. Output Range Selection Jumpers.

To convert from two's complement operation to straight binary coding, W5* should be removed and JP7

installed. Two's complement coding is normally using with bipolar ranges and straight binary coding with unipolar ranges. However, either code may be used with either range.

OUTPUT SYSTEM CALIBRATION

The output system is calibrated through the use of the following program:

```
START: LD A,LSB   ;LSB = 0H for offset adj.
                  ;LSB = FFH for gain adj.

       OUT (DAC L), A   ;Output LSB to DAC low byte reg.

       LD A, MSB  ;MSB = F8H for bipolar offset
                  ;MSB = 0H for unipolar offset
                  ;MSB = 7H for bipolar gain
                  ;MSB = FH for unipolar gain
       OUT (DAC H), A   ;Output MSB to high byte reg.
            JP START
       DAC L EQU XX
       DAC H EQU XX
            END
```

Before the program is assembled, the above references to DACL and DACH must be set to the I/O addresses of the Low and High Bytes of the digital-to-analog converter being calibrated.

After assembling and loading, a breakpoint should be set at the Jump instruction. When the program has been run, the desired converter will be set at its most negative output. The DAC should then be set by its offset control for its most negative, full scale output value. Table XI shows these values by range. Before making this adjustment allow the board to reach thermal equilibrium - about 30 minutes under power. A five-digit DVM capable of ±0.005% accuracy should be used for all voltage measurements.

After the offset adjustment has been made, the appropriate values of LSB and MSB for gain adjustment must be deposited into the program. The previous procedure must then be repeated, but adjust the gain control for the most positive full scale output value.

RANGE	LOW	HIGH	1LSB
±10V	-10.000V	+9.9951V	4.8848mV
±5V	-5.000V	+4.9976V	2.4414mV
±2.5V	-2.500V	+2.4987V	1.2207mV
0 to ±10	0.0V	+9.9975V	2.4414mV
0 to ±5V	0.0V	+4.9988V	1.2207mV

TABLE XI. DAC Calibration Values.

OPERATION SUMMARY

These units are shipped from the factory ready for immediate use. However, they have several user selectable options which are summarized below:

1. Programming Mode. The analog input system on this board must be initialized to operate in either the polling mode or the interrupt mode as described on page 6-26. The analog output system does not require initialization.
2. Address. These units are treated as I/O locations. The analog input system is factory set to occupy I/O addresses 80 - 89 while the analog output system is factory set to occupy I/O address 8C - 8F (Table II). Tables III and IV describe the jumpers which allow the user to configure these units for any address.
3. Analog Input Range. Two elements determine the voltage range of the input system: 1) the input range setting jumpers of the A/D converter and 2) the gain of the instrumentation amplifier. The input range of the A/D converter is factory set for ±10V. It may be user set for any of five ranges (Table V). The instrumentation amplifier is factory set for a gain of 1. It may be user set (by adding a resistor) for gains of 1 to 1000 as shown in Table VIII. These units are factory set as 16 channels differential. They may be user set for 32 channels single-ended as shown in Table VI. They may also be connected as 32 channels pseudo differential. The analog input calibration procedure is described on the previous page.
4. Analog Output Range. The D/A converters on the MP2216-AO are factory set for a range of ±10V. The D/A converters may be user set for any of five ranges as shown in Table X. Analog Output calibration is described on the previous page.
5. Analog I/O Connections. See below.

ANALOG I/O PIN CONNECTIONS

SIGNAL	ON BOARD CONNECTOR P2 Pin No.	CABLE CONNECTOR Pin No.
CH 23, RT 7	1, 2	13
CH 22, RT 6	3	25
CH 21, RT 5	4	12
CH 20, RT 4	5	24
CH 19, RT 3	6	11
CH 18, RT 2	7	23
CH 17, RT 1	8	10
CH 16, RT 0	9	22
CH 7	10	9
CH 6	11	21
CH 5	12	8
CH 4	13	20
CH 3	14	7
CH 2	15	19
CH 1	16	6
CH 0	17	18
SM1 - GND	18	5
SM1 - FB	19	17
Ana. Common	20	4
SM2 - GND	21	16
SM1 - OUT	22	3
SM2 - OUT	23	15
SM2 - FB	24	2
15V	25	14
+15V	26	1

SIGNAL	ON BOARD CONNECTOR P3 Pin No.	CABLE CONNECTOR Pin No.
Remote Common	1, 2	13
-15V	3	25
+15V	4	12
Ana. Common	5	24
Ana. Common	6	11
Ana. Common	7	23
Ana. Common	8	10
Ana. Common	9	22
Ana. Common	10	9
CH 30, RT 14	11	21
CH 31, RT 15	12	8
CH 28, RT 12	13	20
CH 29, RT 13	14	7
CH 26, RT 10	15	19
CH 27, RT 11	16	6
CH 24, RT 8	17	18
CH 25, RT 9	18	5
CH 14	19	17
CH 15	20	4
CH 12	21	16
CH 13	22	3
CH 10	23	15
CH 11	24	2
CH 8	25	14
CH 9	26	1

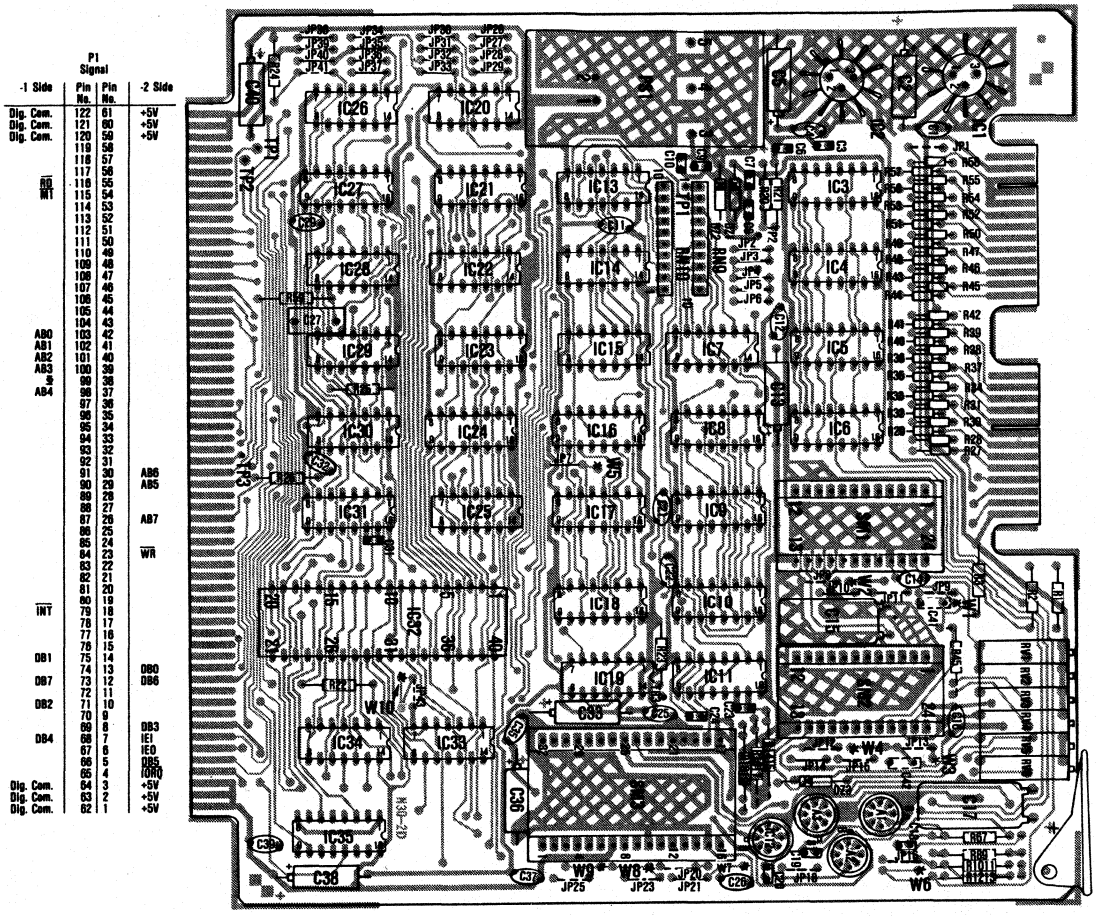
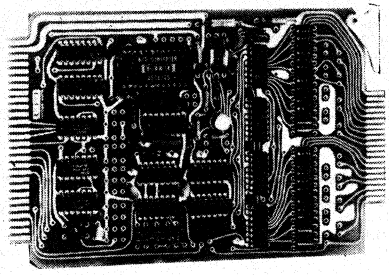


FIGURE 5. PC Board Layout.

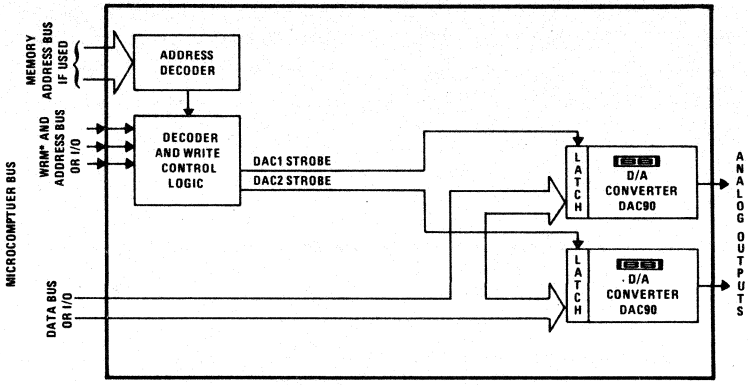
BURR-BROWN



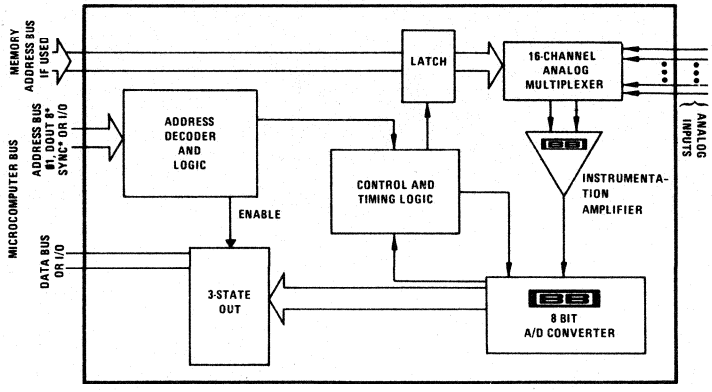
MP4102
MP4216

MICROCOMPUTER ANALOG I/O SYSTEMS

ANALOG OUTPUT SYSTEM - MP4102



ANALOG INPUT SYSTEM - MP4216



FEATURES

- **REDUCES SYSTEM DEVELOPMENT TIME**
  - System engineered and specified
  - Directly compatible with Pro-Log 8- or 4-bit microcomputers
- **EASY TO PROGRAM**
  - Systems are treated as memory or I/O

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PDS-361A Printed in U.S.A. July, 1978

DESCRIPTION

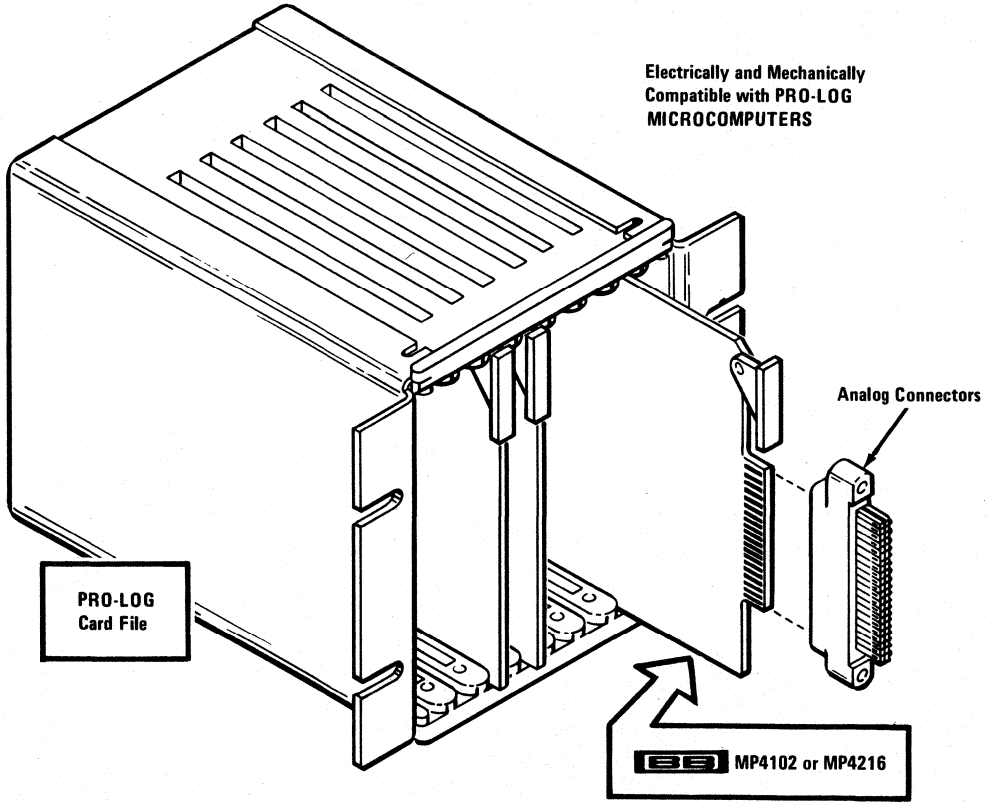
These microcomputer peripherals provide two much needed functions that interface directly to Pro-Log microcomputers. The functions are: 1) Analog Data Acquisition and 2) Analog Output. The devices are electrically and mechanically compatible with any Pro-Log microcomputer. Each analog system is contained on a single printed circuit board that is treated as memory or as I/O by the CPU. The analog interface for each system is at a card edge connector at the opposite edge of the board from the bus connector.

The Data Acquisition System is the MP4216 a 16 channel differential input system. The data acquisition system includes an input multiplexer, instrumentation amplifier, and 8 bit A/D converter along with all the necessary timing, decoding and control logic.

The MP4102, an analog output system, provides two analog output channels.

When programming with these peripherals, they may be treated as memory locations or as I/O. As memory, both the A/D converter output and the D/A converter input are 8 bit words so one 8 bit memory location is needed for each channel. Because the address block occupied by each peripheral is strap selectable, it can be placed anywhere in memory. If these units are treated as memory, only one instruction is needed to read two input channels or to set the input of two D/A converters in 8080 based systems. For instance, an LHLD instruction is used to read two data channels from the MP4216. It will automatically select the desired channel, initiate conversion and when conversion is complete transfer the A/D converter output for those channels to the CPU (see page 6-36).

The analog input systems are jumpered at the factory with the first channel at address $FF00_{16}$ (that's 1111 1111 0000 0000 in binary). Each subsequent channel is one memory location past the start of the last channel so that the second channel is at location $FF01_{16}$ (1111 1111 0000 0001).



SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ANALOG INPUT	
Number of analog inputs	
16 channel differential	MP4216
Input voltage range[1]	±10mV to ±10V
Input current loop ranges (resistor programmable)	4-20mA, 10-50mA, etc.
ADC gain ranges (strap selectable)	±10V, 0 to 10V
Amplifier gain range (resistor programmable)	1 to 1000 V/V
Amplifier gain equation (resistor programmable)	$G = 100k\Omega/R_{EXT}$
Input overvoltage protection	±15V
Input impedance	100 megohms
Bias current	
0 - 70°C	350 nA
Amplifier input offset voltage (max)	$\pm(0.4 + \frac{100}{G})$mV
Amplifier input offset voltage drift (max)	$\left(5 + \frac{1000}{G}\right)$ µV/°C
TRANSFER CHARACTERISTICS	
Resolution	8 bits binary
Throughput accuracy, ±10V range (max)	±0.5% FSR[2]
±10mV range	±0.7% FSR
Temperature coefficient of accuracy	
±10V range (max)	±0.02% FSR/°C
±10mV range	±0.07% FSR/°C
Conversion time	
Gain = 1000	60 microseconds[3]
Gain = 1	20 microseconds
CMRR (for differential inputs) Gain = 1	60dB (DC to 60 Hz)
Gain = 1000	96dB (DC to 60 Hz)
DIGITAL INPUT/OUTPUT	
All signals are compatible with Micro-computer bus	
Output coding	Bipolar Two's Complement unipolar, straight binary
An analog input channel is selected by:	The address bus or 4 I/O lines
The output data bits are read by:	An 8 bit data bus 8 I/O lines
POWER REQUIREMENTS	
	+5VDC ±3% at 450mA, 25mV ripple +15VDC ±3% at 45mA, 5mV ripple -15VDC ±3% at -60mA, 5mV ripple
TEMPERATURE RANGE	0 to 70°C

ANALOG OUTPUT	
Number of analog outputs: 2	MP4102
Output voltage range [1]	±10V, 0 to 10V at 5mA (strap selectable)
Output impedance	1Ω
Output settling time	< 30 microseconds
TRANSFER CHARACTERISTICS	
Resolution	8 bits binary
Throughput accuracy (max)	±0.4% FSR
Temperature coefficient of accuracy	
Unipolar	±0.013% FSR/°C
Bipolar	±0.025% FSR/°C
DIGITAL INPUT/OUTPUT	
All signals are compatible with Micro-computer bus	
An analog otuput channel is selected by:	The address bus or 1 I/O line
The input data bits are read by:	An 8 bit Data Bus or 8 I/O Lines
POWER REQUIREMENTS	
	+5VDC ±5% at 175mA ±5mV ripple +15VDC ±3% 25mA, 5mV ripple -15VDC ±3% at 25mA, 5mV ripple
TEMPERATURE RANGE	0 to 70°C

OPERATING INSTRUCTIONS

INSTALLATION

The MP4102 and the MP4216 are shipped from the factory calibrated and ready for immediate use. Installation requires only wire wrapping the bus connector in the microcomputer card rack for these boards and connecting analog inputs and ±15VDC power through the analog connector provided on the board (see page 6-34). The boards are set up for 8080 based systems. To use a 6800 based system, the address should be changed as described on page 6-37 and for the MP4102, W31 should be removed and W32 inserted.

PROGRAMMING

The MP4216 and MP4102 are easily programmed. They may be treated as memory or as I/O. The table below outlines the various Pro-Log systems with which they may be used.

The voltage data for these boards is represented by an 8 bit two's complement binary number. Each bit has a value of 78.1mV (±10V range) with the polarity of the voltage indicated by the sign of the binary number.

Pro-Log System:	These boards may be used as:
Any 4 bit system	I/O only
PLS-881	I/O only
PLS-891	I/O only
MPS-803	I/O or memory
MPS-805	I/O or memory
MPS-863*	I/O or memory
MPS-865*	I/O or memory
MPS-883	I/O or memory
MPS-885	I/O or memory
8111	I/O or memory
8611	I/O or memory
8811A	I/O or memory
8821	I/O or memory
8921	I/O or memory

MECHANICAL CHARACTERISTICS

Compatible with Pro-Log card cages.

Minimum card spacing: 12.7mm (0.5")

Microcomputer bus connector required: 56 pin PC edge connector with 0.125" contact centers.

44 pin analog card edge connector with 0.100" contact centers on board.

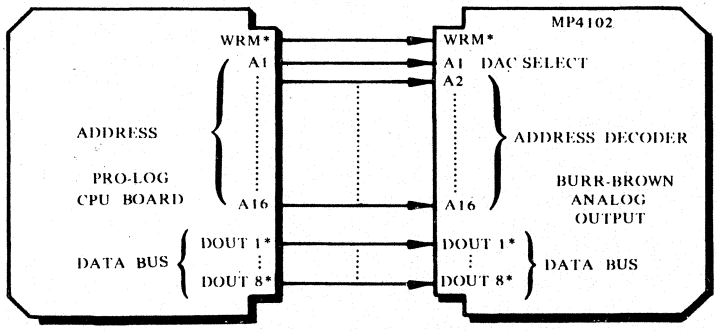
Mating connector, one required for each board: 2201MC (Viking 3VH22/1JNS - solder tab).

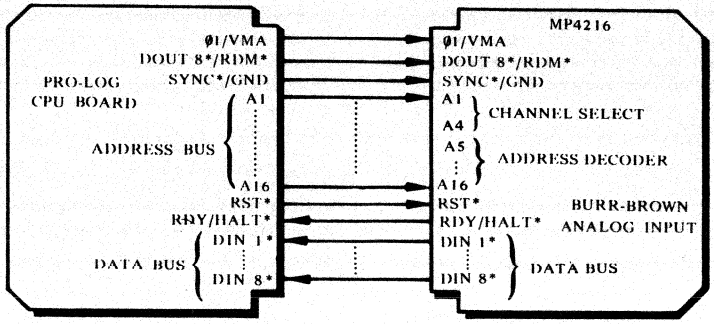
1) Connected at the factory for ±10V range with G = 1.
2) FSR is Full Scale Range (i.e., 20V for ±10V range.) 10V for 0 to +10V range.
3) Set at factory for 60 microseconds can be user set as low as 20 microseconds.

PROGRAMMING TABLE

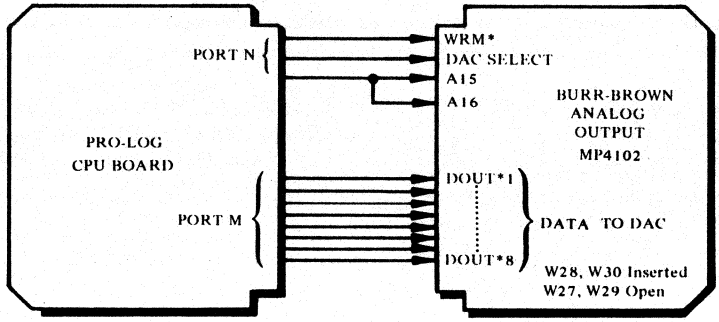
Pro-Log System Based On	Microperipherals Treated As:	Transfer an 8-bit data word from the CPU to the input of a selected DAC.		Initial conversion of a selected channel and when conversion is complete transfer the 8-bit value to the CPU.	
		MP4102		MP4216	
8080	MEMORY One channel	(START)LXI H, XXXX MOV M, A (JMP START)	XXXX is address of selected channel. transfers accumulator contents to selected DAC.	(START)LXI H, XXXX MOV A, M OUT PORTV JMP START	XXXX is address of selected channel. starts conversion of selected channel and at end of conversion transfers result to accumulator. Output conversion to PORTV
	Two channels	SHLD, XXXX	XXXX is address of first selected channel transfers contents of L register to DAC at XXXX; transfers contents of H register to DAC at XXXX + 1.	LHLD, XXXX	XXXX is address of first selected channel. Starts conversion of channel XXXX and at end of conversion transfers result to L register, then immediately starts conversion of channel XXXX + 1 and at end of conversion transfers result to H register.
	I/O	(START)MVI A, XX OUT PORT N MVI A, XX OUT PORT M MVIA, XX OUT PORT N MVI A, XX OUT PORT N (JMP START)	XX is the initial value for WRM*, and A15/A16 and DAC select. WRM = 1, A15/A16 = 0 initialize board. XX is the output data to selected DAC. XX is value of WRM*, A15/A16 and DAC select. WRM* = 1, A15/A16 = 1. XX is value of WRM*, and A15/A16 and DAC select. WRM = 0, A15/A16 = 1. commands conversion.	(START)MVI A, XX OUT PORT W MVI A, XX OUT PORT W MVIA, XX OUT PORT W LOOP: IN PORT Y ANI 01 JZ LOOP IN PORT Z OUT PORT V JMP START	XX is initial value for 01, DOUT8*, SYNC*, A15/A16 and channel select. 01 = 0, DOUT 8* = 1 SYNC* = 1, A15/A16 = 0. initialize board. XX is value for 01, DOUT 8*, SYNC* and channel select 01 = 1, DOUT 8* = 0, SYNC* = 0, A15/A16 = 1. starts conversion. XX is value for 01, DOUT 8*, SYNC*, A15/A16 and channel select 01 = 0, DOUT 8* = 1 SYNC* = 1, A15/A16 = 1. RDDY Signal check, loop until RDY = 1. read data. Output conversion to PORT V
6800	MEMORY	(START)STAA XXXX (JMP START)	transfers accumulator contents to DAC addressed by XXXX.	(START)LDAA XXXX NOP LDAA XXXX OUT PORT V (JMP START)	starts conversion of channel with XXXX address. halts CPU during conversion. reads data. Output conversion to PORT V
	I/O	(START)LDAA # XX STAA OPT N LDAA # XX STAA OPT M LDAA # XX STAA OPT N LDAA # XX STAA OPT N (JMP START)	XX is initial value for WRM*, A15/A16 and DAC select. WRM* # 1, A15/A16 = 0. initialize board. XX is the output data to selected DAC. XX is value of WRM*, A15/A16 and DAC select. WRM* = 1, A15/A16 = 1. XX is value for WRM*, A15/A16 and DAC select. WRM* = 0, A15/A16 = 1. commands conversion.	(START)LDAA # XX STAA OPT W LDAA # XX STAA OPT W LDAA # XX STAA OPT W LOOP: LDAA IPTY ANDA # 1 BEQ LOOP LDAA INP Z STAA OPT V (JMP START)	XX is initial value of VMA, RDM*, GND, A15/A16 and channel select. VMA = 0, RDM* = 1, GND = 1, A15/A16 = 0. initialize board. XX is value for VMA, RDM*, GND, A15/A16 and channel select. VMA = 1, RDM* = 0, GND = 0, A15/A16 = 1. starts conversion. XX is value for VMA, RDM*, GND, A15/A16 and channel select. VMA = 0, RDM* = 1, GND = 1, A15/A16 = 1. RDY Signal check, loop until RDY = 1. read data. Output conversion to PORT V

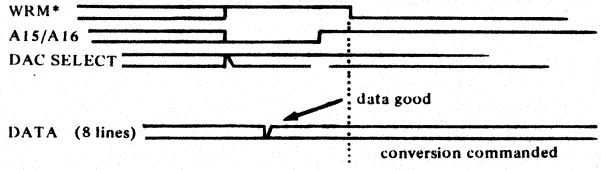
MEMORY-MAPPED MODE

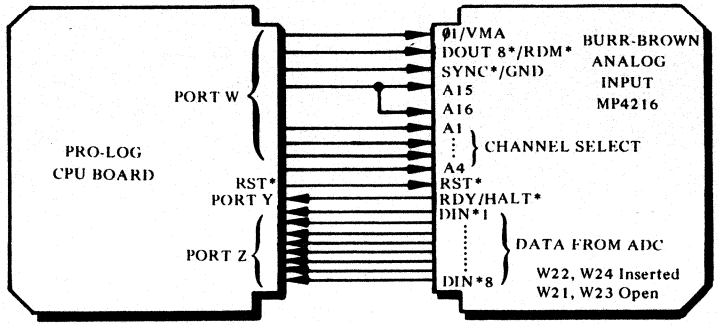


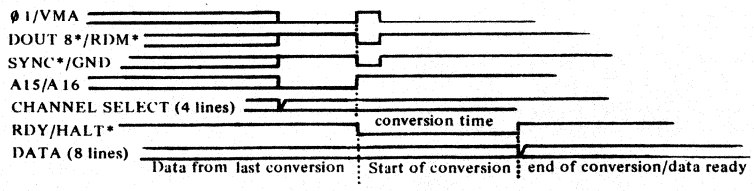


I/O INTERFACE MODE









In the memory mapped mode, the MP4102 uses any memory reference instruction that can write data from a register or the accumulator. In a similar manner, a channel in the MP4216 can be read by any memory reference instruction that can read data into a register or the accumulator. It will automatically select the desired channel, initiate conversion, halt the CPU for 60 μsec and when conversion is complete, transfer the A/D converter output for that channel to the CPU. If the boards are interfaced as I/O, the MP4102 requires 11 output bits and the MP4216 requires 8 output bits and 9 input bits.

Page 6-36 shows software routines which can be used with both 8080 and 6800 based Pro-Log systems. The portions of the programs in parenthesis should only be used to make the program repetitive. This may be done in testing or calibration of the boards for easy accessibility to the repetitive signals.

ADDRESS MODIFICATION

An address selector is included to set the base address of these boards when operating in the memory mapped mode. The base address can be set to any value by properly jumpering the address selector. The address selector is factory jumpered to FF00 for the MP4216 and to FE00 for the MP4102. To change the sense of a bit simply reverse the connection of the jumper. If multiple boards of the same type are to be used with the same CPU, the address of the second board should be set to follow the last address of the first. For instance, with an MP4216, which requires 16 memory locations per board, the first board would have a base address of FF00 as it comes from the factory, the second board a base address FF10 (16 locations away), etc. For applications with Pro-Log boards using Motorola's M6800 microprocessor, the base address should be set lower by the user (for instance, to 0200 for the MP4102 and to 0300 for the MP4216).

If the board is treated as I/O not memory, the address selector must be disabled. It may be disabled by removing jumper W46 (MP4102) or jumper W33 (MP4216). Pins 24 and 26 (A15 and A16) of the digital bus connector need to be tied together and driven by an output of the system CPU. See page 6-37 for specific timing of the enable output.

Removal of plated through jumpers is accomplished by drilling out the barrel of these holes with a 0.055" (no. 54) drill mounted in a hand vise (see Figure 1). Caution must be exercised to prevent damage to the board and the scattering of metal particles over its surface.

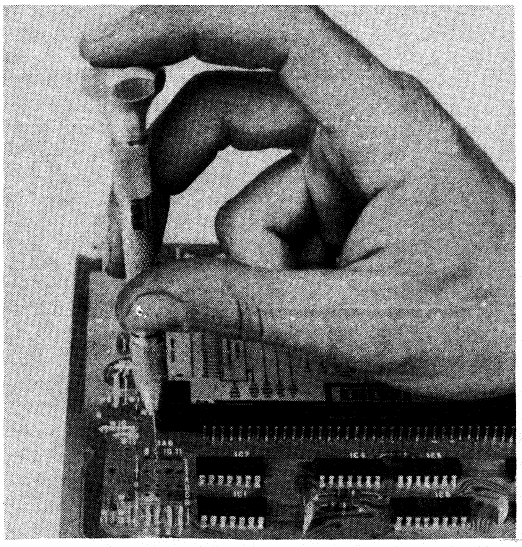


FIGURE 1. Drilling Out Plated Through Holes.

MP4102 OUTPUT RANGE SELECTION

Each DAC is jumpered at the factory for ±10 volt operation (two's complement coding). However, it is possible to alter these jumpers as shown in Figure 2 for straight binary coding. When making a change first remove those jumpers indicated for the present range and replace them with those jumpers required for the desired range.

	DAC1	DAC2
Coding		
Two's Complement	W37, W39, W44	W33, W35, W42
Straight Binary	W40, W43	W36, W41

FIGURE 2. MP4102 Output Selection Jumpers.

BIPOLAR - TWO'S COMPLEMENT		UNIPOLAR - STRAIGHT BINARY	
Digital Input/Output	±10V	Digital Input/Output	0 to +10V
0111...11($7F_{16}$)	+9.922V	111...111(FF_{16})	9.961V
100...00(80_{16})	-10.0000V	000...00(00_{16})	0.0000V

FIGURE 3. Analog input and analog output full scale range values.

MP4216 INPUT RANGE SELECTION

The data acquisition system on this board has been factory jumpered for ±10V operation. 0 to +10V operation is possible as shown in Figure 4. When making a change, first remove those jumpers indicated for the present range and replace them with those jumpers required for the desired range.

Range	Jumpers
±10V	W26, W28, W30
0 to +10V	W25, W29, W31

FIGURE 4. MP4216 Range.

As configured at the factory, these boards are jumpered for two's complement operation (see Figure 3) with jumper W28 inserted and W29 open. For operation in the straight binary mode (any range), jumper W28 is open and W29 is inserted.

MP4216 LOW LEVEL OPERATION

The input range of the MP4216 may be user adjusted from ±10V to ±10mV. This is done by setting the on-board instrumentation amplifier for a gain of 1 to 1000. The gain can be calculated by this formula: Gain = 100kΩ/R_{EXT}. The accuracy of the gain equation is: ±(0.5 - 0.003 x Gain)%. R_{EXT} is the gain setting resistance of the amplifier (R12 and R68 in parallel form R_{EXT} in Figure 6). As shipped from the factory, R_{EXT} = 100kΩ(R68 is open, R12 = 100kΩ). Stable (50ppm/°C) resistors should be used for R_{EXT}. When operating the amplifier at high gain the overall accuracy of the system declines. At a gain of 1000, accuracies of ±0.7% can be expected. This is due to increased noise and a loss in amplifier linearity.

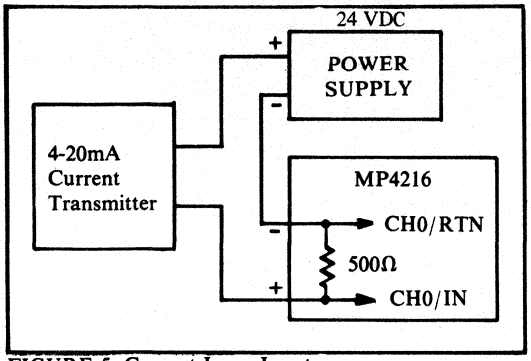


FIGURE 5. Current Loop Input

MP4216 PROCESS CURRENT LOOP INPUT OPERATION

The MP4216 is designed to allow the user to easily add the dropping resistors (R46-R61, Figure 6) needed to input process current loop signals such as 4-20 mA and 10-50 mA. Table I shows the resistor value and settings required. The resistor values may be reduced and thus the voltage drops minimized, by increasing the amplifier gain, (at gain = 2, a 250Ω resistor is needed for 4-20 mA inputs).

Current Loop	Input Resistor	Amplifier Gain	ADC Range	Resolution
4-20 mA	500Ω	1	0 to 10V	78μA
10-50 mA	200Ω	1	0 to 10V	195μA

TABLE I. Current Loop Inputs

POWER SUPPLIES

These boards require power supply voltages of +5VDC and ±15VDC. The +5VDC power should be supplied through the digital bus connector and the ±15VDC should be supplied through the analog connector on the opposite side of the board.

POWER SUPPLY CONNECTIONS

	MP4102	MP4216
Digital Connector:		
+5VDC Ground	Pins 1, 2 Pins 3, 4	Pins 1,2 Pins 3, 4
Analog Connector:		
+15VDC -15VDC Ground	Pins 27, 28, 29, 30 Pins 35, 36, 37 38 Pins 19, 20, 21, 22	Pins 3, 4 Pins 21, 22 Pins 1, 2

4216 DIGITAL CONNECTOR PINOUT

COMPONENT SIDE	PIN	NON-COMPONENT SIDE
	1 2	
+5V	3 4	+5V
GND	5 6	Ana. GND
	7 8	TP
DOUT 8*/RDM*	9 10	DIN 8*
	11 12	DIN 7*
	13 14	DIN 6*
	15 16	DIN 5*
	17 18	DIN 4*
	19 20	DIN 3*
	21 22	DIN 2*
A8	23 24	DIN 1*
A7	25 26	A16
A6	27 28	A15
A5	29 30	A14
A4	31 32	A13
A3	33 34	A12
A2	35 36	A11
A1	37 38	A10
	39 40	A9
	41 42	TP
	43 44	TP
	45 46	
	47 48	
RDY/Halt*	49 50	
ϕ1/VMA	51 52	
RST*	53 54	SYNC*/GND
	55 56	

4216 ANALOG CONNECTOR PINOUT

COMPONENT SIDE	PIN	NON-COMPONENT SIDE
Ana. GND	1 2	Ana. GND
+15V	3 4	+15V
RTN3	5 6	CH3
RTN5	7 8	CH5
RTN0	9 10	CH0
RTN7	11 12	CH7
RTN1	13 14	CH1
RTN6	15 16	CH6
RTN2	17 18	CH2
RTN4	19 20	CH4
-15V	21 22	-15V
TP	23 24	TP
RTN11	25 26	CH11
RTN13	27 28	CH13
RTN8	29 30	CH8
RTN15	31 32	CH15
RTN9	33 34	CH9
RTN14	35 36	CH14
RTN10	37 38	CH10
RTN12	39 40	CH12
TP	41 42	
TP	43 44	TP

4102 DIGITAL CONNECTOR PINOUT

COMPONENT SIDE	PIN	NON-COMPONENT SIDE
+5V	1 2	+5V
Dig. Com.	3 4	Ana. Com.
	5 6	
DOUT 8*	7 8	
DOUT 7*	9 10	
DOUT 6*	11 12	
DOUT 5*	13 14	
DOUT 4*	15 16	
DOUT 3*	17 18	
DOUT 2*	19 20	
DOUT 1*	21 22	
A8	23 24	A16
A7	25 26	A15
A6	27 28	A14
A5	29 30	A13
A4	31 32	A12
A3	33 34	A11
A2	35 36	A10
A1	37 38	A9
	39 40	
	41 42	
WRM*	43 44	
	45 46	
	47 48	
	49 50	
	51 52	
	53 54	
	55 56	

4102 ANALOG CONNECTOR PINOUT

COMPONENT SIDE	PIN	NON-COMPONENT SIDE
	1 2	TP
	3 4	TP
	5 6	TP
	7 8	TP
	9 10	TP
	11 12	
	13 14	
	15 16	
	17 18	
Ana. Com.	19 20	Ana. Com.
Ana. Com.	21 22	Ana. Com.
CH2	23 24	CH2 Com.
CH2	25 26	CH2 Com.
+15V	27 28	+15V
+15V	29 30	+15V
CH1	31 32	CH1 Com.
CH1	33 34	CH1 Com.
-15V	35 36	-15V
-15V	37 38	-15V
	39 40	TP
	41 42	TP
	43 44	

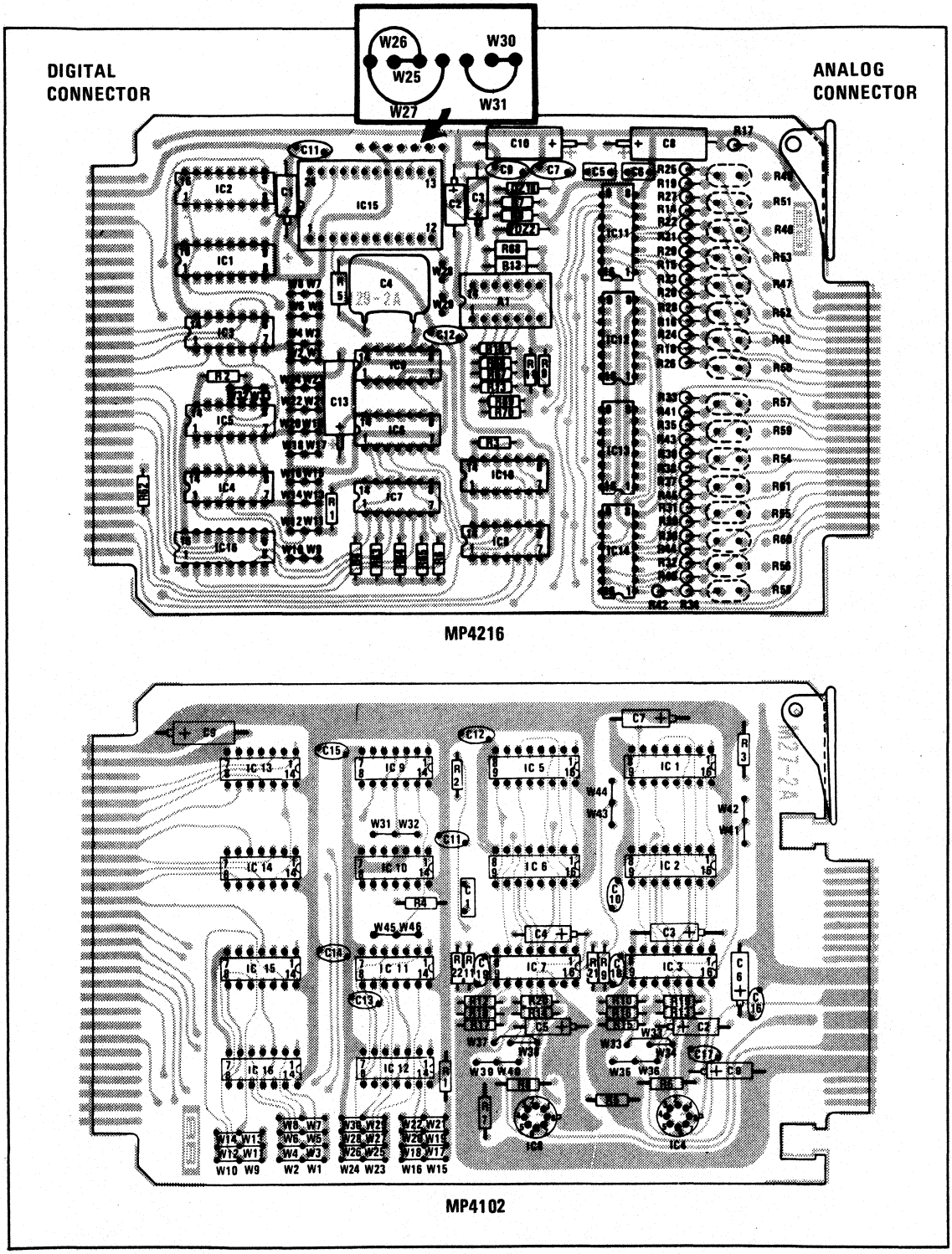
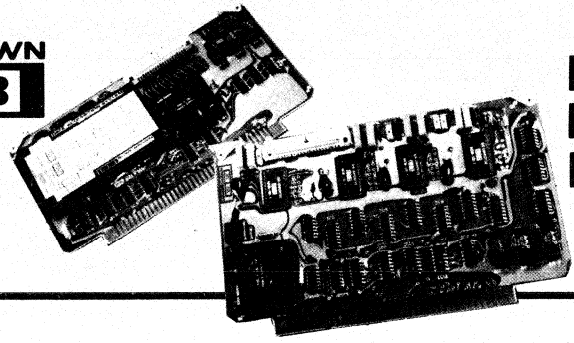


FIGURE 6. Board Layouts

BURR-BROWN



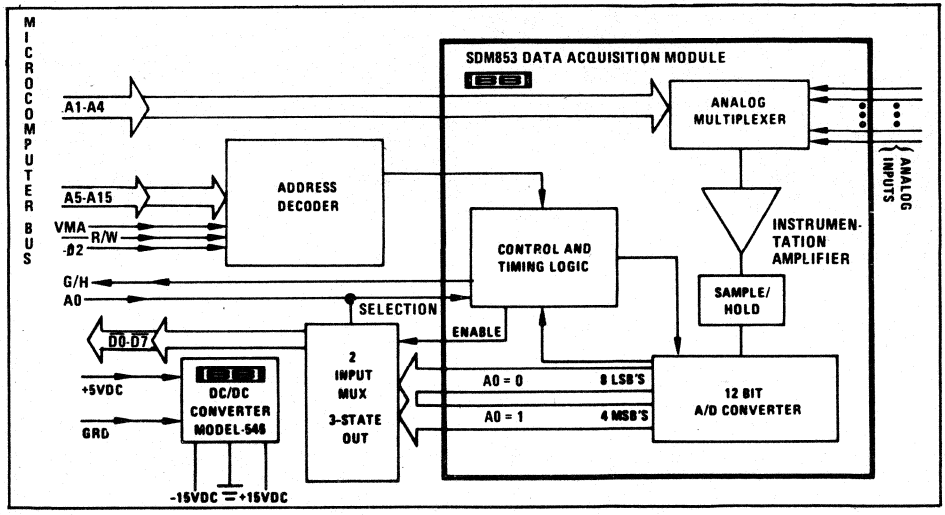
MP7104
MP7208
MP7216

MICROCOMPUTER ANALOG I/O SYSTEMS

MP7104 - Analog Output System
MP7208 - Data Acquisition System
MP7216 - Data Acquisition System

FEATURES

- COMPATIBLE WITH MOTOROLA MICROMODULE AND EXORciser®
- REDUCES SYSTEM DEVELOPMENT TIME
  - System engineered and specified
  - Plug compatible
  - Operates from +5VDC power supply
- EASY TO USE
  - All cabling and connectors are included



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PDS-352B
Printed in U.S.A. July, 1978

DESCRIPTION

These microcomputer peripherals provide two much needed functions that interface directly to Motorola's Micromodule and EXORciser microcomputers. The functions are: 1) Analog Data Acquisition and 2) Analog Output. The devices are electrically and mechanically compatible with Motorola microcomputers. Each analog system is contained on a single printed circuit board that is treated as memory input and output by the CPU. The cards will mate to any memory or I/O slot. The analog interface for each system is at a flat cable connector at the opposite edge of the board from the bus connector.

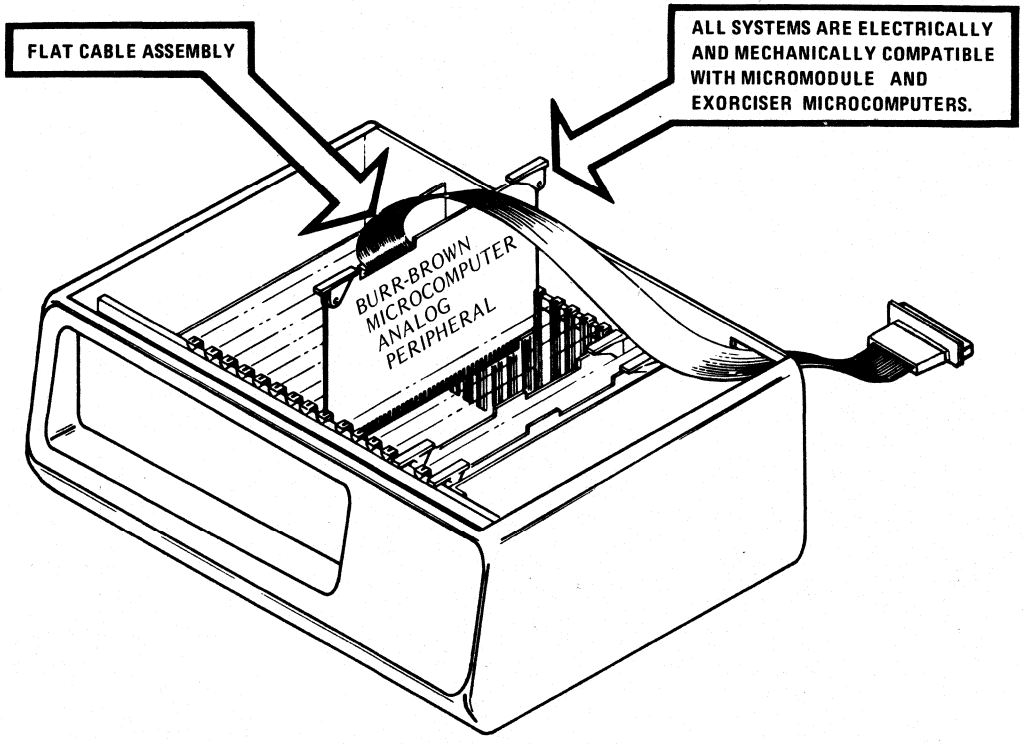
The Data Acquisition Systems consist of the MP7208, an 8 channel differential input system; and the MP7216, a 16 channel single-ended input system. Burr-Brown's SDM853 modular data acquisition system is used to implement these systems. The data acquisition systems include an input multiplexer, high gain instrumentation amplifier, sample/hold and 12 bit A/D converter along with all the necessary timing, decoding and control logic. The model 546 DC/DC converter (+5V to ±15V) is also used so that only the microcomputer's +5VDC power supply is required.

The MP7104, an analog output system, provides four analog output channels (using four of Burr-Brown's hybrid 12 bit DAC80 D/A converters). This board also contains the 546 DC/DC converter to assure operation on +5VDC power. The input of the D/A converters are double buffered so that a complete 12 bit word can be strobed into a D/A converter's input register to minimize output glitches.

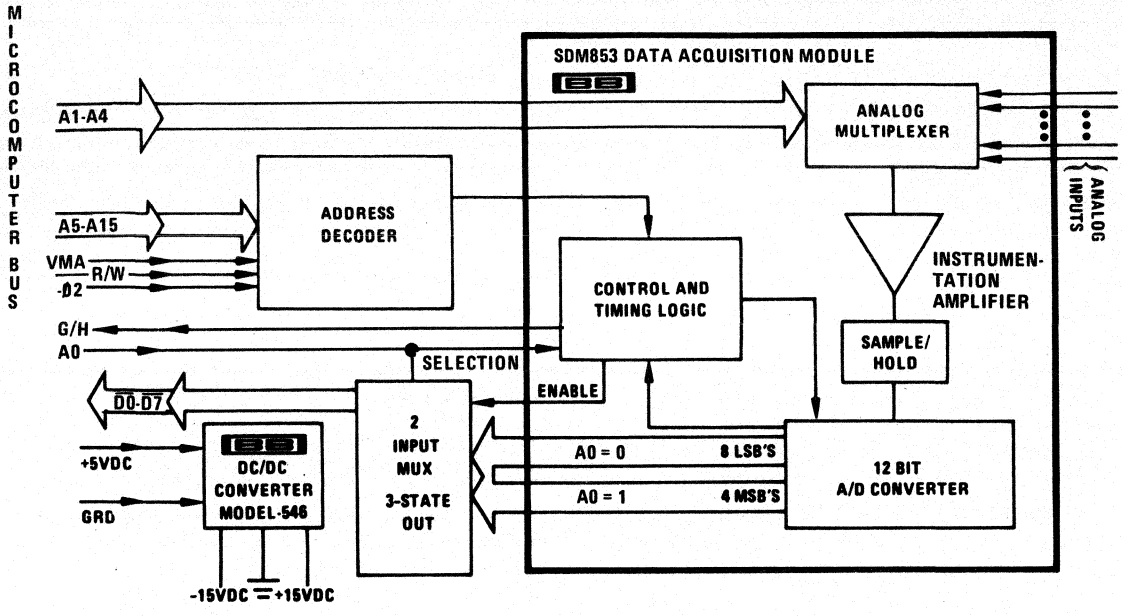
THEORY OF OPERATION

When programming with these peripherals, they are treated as memory locations. Both the A/D converter output and the D/A converter input are 12 bit words so two 8 bit memory locations are needed for each channel. But, because the address block occupied by each peripheral is switch selectable, it can be placed anywhere in memory. Since these units are treated as memory, a single instruction is all that's needed to set the input of a D/A converter. For instance, the STX (write) instruction followed by the proper address is used to write data from the index register to the MP7104. The four most significant bits are written first followed by the eight least significant bits. Through double buffering in the MP7104 only one 12 bit data transfer is made to the DAC to minimize glitching.

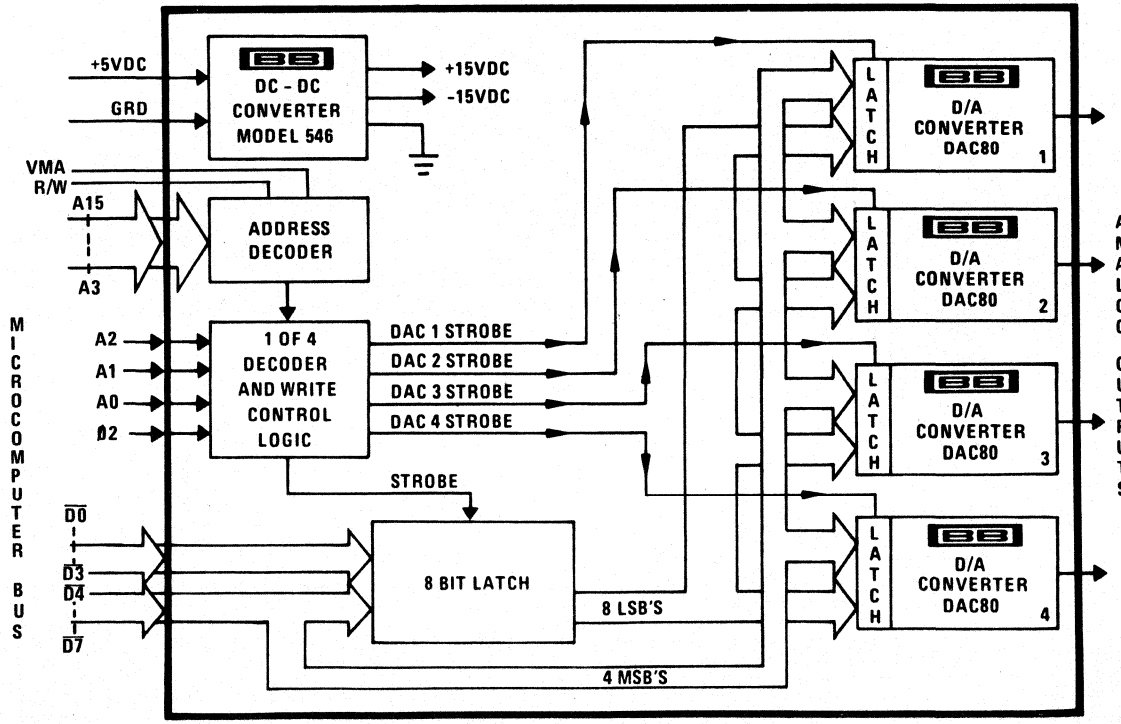
All of these systems are jumpered at the factory with the first channel at address $EF00_{16}$ (that's 1110 1111 0000 0000 in binary). Each subsequent channel is two memory locations past the start of the last channel so that the second channel is at location $EF02_{16}$ (1110 1111 0000 0010).



ANALOG INPUT SYSTEM - MP7208/7216



ANALOG OUTPUT SYSTEM - MP7104



SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ANALOG INPUT	
Number of analog inputs	
8 channel differential	MP7208
16 channel single-ended	MP7216
Input voltage range[1]	±10mV to ±10V
Input current loop ranges (resistor programmable)	4-20mA, 10-50mA
ADC gain ranges (strap selectable)	±10V, 0 to 10V, 0 to 5V ±5, ±2.5V
Amplifier gain range (resistor programmable)	1 to 1000 V/V
Amplifier gain equation (resistor programmable)	$G = 1 + 20k\Omega/R_{EXT}$
Input overvoltage protection	±15V
Input impedance	100 megohms
Bias current	
25°C	20nA
0 to 70°C	50nA
Amplifier output noise (Gain = 100 R_s = 500Ω)	1.2mV, rms; 7mV, p-p
Amplifier input offset voltage (max)[4]	400μV
Amplifier input offset voltage drift (max)	$2 + \frac{20}{G}$ μV/°C
TRANSFER CHARACTERISTICS	
Resolution	12 bits binary
Throughput accuracy, ±10V range (max)	±0.025% FSR[2]
±10mV range	±0.1% FSR
Temperature coefficient of accuracy	
±10V range (max)	±0.003% FSR/°C
±10mV range	±0.01% FSR/°C
Conversion time ±10V range	33 microseconds
±10mV range	100 microseconds
CMRR (for differential inputs)	74 dB (DC to 2000 Hz)
Sample hold aperture time	30ns
DIGITAL INPUT/OUTPUT	
All signals are compatible with Microcomputer bus	
Output coding	Bipolar, Two's Complement; unipolar, straight binary
An analog input channel is selected by:	A1 through A4
The output data bits are read into:[3]	D0 through D7
POWER REQUIREMENTS	
MP7208, MP7216	+5VDC ±5% at 1 amp, 25mV ripple +5VDC ±5% at +500mA, 25mV ripple +15VDC±3% at +50mA, 5mV ripple -15VDC ±3% at -75mA, 5mV ripple
MP7217-NS, MP7209-NS	
TEMPERATURE RANGE	
Temperature	0 to 70°C
ANALOG OUTPUT	
Number of analog outputs: 4	MP7104
Output voltage range[1]	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA (strap selectable)
Output impedance	1Ω
Output settling time	< 10 microseconds
TRANSFER CHARACTERISTICS	
Resolution	12 bits binary
Throughput accuracy (max)	±0.0125% FSR
Temperature coefficient of accuracy	
Unipolar	±0.003% FSR/°C
Bipolar	±0.0045% FSR/°C
DIGITAL INPUT/OUTPUT	
All signals are compatible with Microcomputer bus	
An analog output channel is selected by:	A1 and A2
The input data bits are read by:	D0 through D7
POWER REQUIREMENTS	
MP7104	+5VDC ±5% at +1 amp, 25mV ripple
MP7105-NS	+5VDC ±5% at +500 mA ±5mV ripple +15VDC±3% at +100mA, 5mV ripple -15VDC ±3% at -100mA, 5mV ripple
TEMPERATURE RANGE	
Temperature	0 to 70°C

OPERATING INSTRUCTIONS

INSTALLATION

The MP7104, MP7208 and the MP7216 are shipped from the factory calibrated and ready for immediate use. Installation requires only plugging the card into any empty slot in the EXORciser or with a Micromodule and routing the board's mating I/O cable to the back panel. Cable placement is shown on page 6-42. The cable supplied with each board is shielded and, in the case of the MP7104, provided with the proper terminations.

PROGRAMMING

Programming of these analog I/O boards is easily accomplished since all are treated as memory locations. The MP7104 uses any memory reference instruction that can write data from the index and stack point registers or the accumulators. In a similar manner a channel in the MP7208 or MP7216 can be read by any memory reference instruction that can read data into the index and stack pointer registers or the accumulators.

The voltage data for these boards is represented by a 12 bit two's complement binary number. Each bit has a value of 4.88mV, with the polarity of the voltage indicated by the sign of the binary number. Since the index, stack pointer and A and B accumulator pair registers are 16 bits long and the data word is 12 bits, the MP7208 and MP7216 set these unused bits to the same value as the most significant bit of the data. This assures the proper representation of the data's sign.

Each board is set at the factory for a block of addresses beginning at EF00. Any analog data channel requires two memory locations since the digital data is 12 bits. The most significant 4 bits of data are always located in an even location while the remaining 8 bits are located in the next higher location. Thus, the first analog channel is located at EF00 and EF01 while the second analog channel is located at EF02 and EF03. When moving data, all boards require that the most significant bits (even addresses) be referenced first. In addition, the MP7208 and MP7216 systems require the most significant data to be read followed by a NOP instruction for proper starting of the conversion process. This can be illustrated as shown below:

```
LDAA    EF00    Starts conversion of CH0
NOP             Allows processor to halt
                during conversion
LDX     EF00    Reads data as soon as
                conversion is complete
```

(1) Connected at the factory for ±10V range.
(2) FSR is Full Scale Range (i.e., 20V for ±10V range, 10V for 0 to +10V range).
(3) The 4 MSB's when conversion is complete, followed by the 8 LSB's.
(4) Adjustable to zero.

ADDRESS MODIFICATION

The base address of a board can be set to any value by properly setting its address selector switches. Hexidecimal rotary switches (SW1-3) are used to select the most significant 12 bit (11 bits for MP7216) of the address. For the MP7104 system the thirteenth most significant bit must also be set. This is done by toggle switch S4 which can be set to the binary value indicated on the board. The remaining lesser ordered address bits are used internally by the boards to select the desired analog data channel.

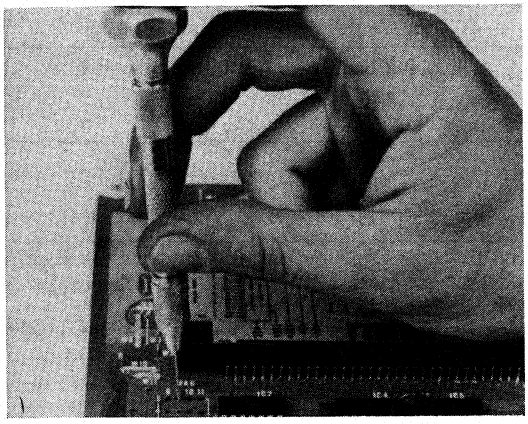
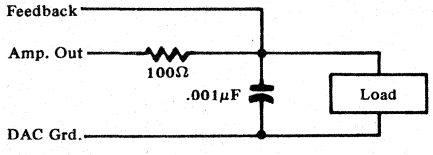


FIGURE 1. Drilling Out Plated Through Holes.

MP7104 APPLICATION

The MP7104 system includes an MP8003-cable assembly that is required for proper operation. This is because the feedback for each DAC output amplifier is connected to the amplifier output through a low pass filter at the end of the cable. For those applications requiring a different cable, this feedback connection must be considered. Where increased noise may be tolerated, the feedback can be connected directly on the board via jumpers W6, W12, W18 and W50. However, if noise performance is to be optimized the feedback must be connected at the load through shielded cable and terminated as follows:



It is always necessary to recalibrate when the output cable is changed. For whatever feedback technique used, maximum accuracy and minimum noise requires the corresponding DAC ground to be used as the return from the load.

Test points at the top edge of the board make each DAC output (white) and analog common (black) available for easy reference. However, these points should never be used for calibration.

MP7208/7216 APPLICATION

The data acquisition system module (Burr-Brown SDM853) incorporated into the MP7208/7216 uses a fixed timing sequence between channel selection and the start of data conversion. If desired, this time may be increased by the addition of an external resistor and capacitor. This procedure is described in the low level operation section.

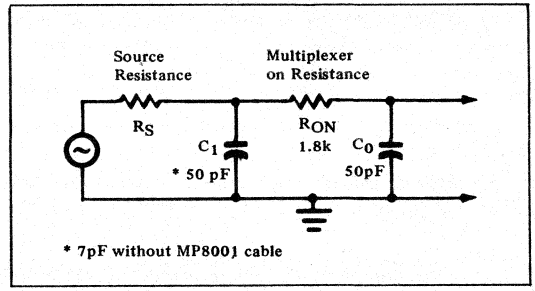


FIGURE 2. On Channel Multiplexer Circuit Model for Single-Ended Operation.

As normally supplied, the time allowed for multiplexer settling is 9 μs which is sufficient for most applications. The only external factor which affects the multiplexer settling time is the output impedance (R_S) of the source connected to a channel. A circuit model of an "On" channel is shown in Figure 2. The input capacitance (C_I) of 50 pF for single-ended operation does not affect the settling time since it is continuously connected to the source. The signal at the output of the multiplexer must be allowed to settle to ±0.01% (nine time constants) to maintain the full accuracy of the system. The multiplexer time constant can be calculated with the formula: $\tau = (R_s + R_{on})C_o$. For a source resistance of 1 kΩ, $\tau = (1 + 1.8)$ kΩ x 50 pF = 140ns. Thus, 1.20 μs is needed to settle to ±0.01%. This is well below the fixed 9 μs allowed for multiplexer settling so that the accuracy of the system is preserved.

If the source bandwidth can be limited, high impedance sources may be accurately handled by placing a large capacitor across the multiplexer input. An analysis of such a circuit shows that a capacitor of 0.5 μF is sufficient. For such a capacitance the multiplexer time constant becomes 90ns. If this method cannot be used the time allowed for settling can be increased as described in the section on low level operation.

For switching of large signals it must be remembered that the on resistance is the channel resistance of a FET which is a nonlinear function of the applied voltages. As a result the previous calculations are only an approximation derived from a linearized model. Another factor not considered is the addressing delay of the multiplexer. This is typically 250ns and is additive to the above calculated times.

For differential units the same considerations apply. Even though two input circuits are involved there is sufficient component matching within the multiplexer to prevent measurable differences in the transfer functions for each half of the signal. When operated in the differential mode, C_o in Figure 2 becomes 12.5 pF with an R_{on} = 1.8k in each leg. Therefore, the time constant becomes 1/2 the time constant for a single-ended channel.

The analog inputs have reversed biased diode circuits which prevent damage from discharge of static electricity. However, it is still wise to take reasonable precautions against static discharge.

The MP8001 input cable provided with the MP7208 and MP7216 systems provides a shielded connection to the EXORciser's rear panel. If a cable other than this is to be used, it should also be shielded for maximum noise immunity.

For a more complete discussion on the application of analog data acquisition systems, obtain a copy of Burr-Brown Application Note AN-79, and the SDM853 users manual, PDS-358.

MP7104 OUTPUT RANGE SELECTION

Each DAC is jumpered at the factory for ±10 volt operation (two's complement coding). However, it is possible to alter these jumpers as shown in Figure 3 for other output voltages. Jumpers indicated by an asterisk are plated through holes on the board and should be removed by drilling as described below. When making a change first remove those jumpers indicated for the present range and replacing them with those jumpers required for the desired range.

Removal of plated through jumpers is accomplished by drilling out the barrel of these holes. A 0.055" (No. 54) drill mounted in a hand vise should be used (see Figure 1). Extreme caution must be exercised to prevent damage to the board and the scattering of metal particles over its surface.

Range	DAC1	DAC2	DAC3	DAC4
±10V	W1*, W2*	W7*, W8*	W13*, W14*	W19*, W20*
±5V	W4, W2*	W10, W8*	W16, W14*	W22, W20*
±2.5V	W4, W2*	W10, W8*	W16, W14*	W22, W20*
	W5	W11	W17	W23
0 to +10V	W4, W3	W10, W9	W16, W15	W22, W21
0 to +5V	W4, W3	W10, W9	W16, W15	W22, W21
	W5	W11	W17	W23

FIGURE 3. MP7104 Output Selection Jumpers.

When converting from bipolar to unipolar operation W51* should be removed and W52 installed. This converts from two's complement operation to straight binary operation. However, the data to all four DACs is affected by this change. If not all DACs are converted to unipolar operation, it will be necessary to perform this inversion in software for bipolar DACs.

BIPOLAR - TWO'S COMPLEMENT			
Digital Input/Output	±10V	±5V	±2.5V
0111...11($7FF_{16}$) 100...00(800_{16})	+9.9951V -10.0000V	+4.9975V -5.0000V	+2.4988V -2.5000V
UNIPOLAR - STRAIGHT BINARY			
Digital Input/Output	0 to +10V	0 to +5	
111...111(FFF_{16}) 000...00(000_{16})	9.9975V 0.0000V	4.9988 0.0000V	

TABLE I. Analog input and analog output full scale range values.

MP7208/7216 INPUT RANGE SELECTION

The data acquisition module on these boards has been externally jumpered for ±10V operation. Other ranges are possible and can be selected as shown in Figure 4.

Range	Jumpers
±10V	W14, W18
±5V	W14, W19
±2.5V	W14, W19, W22
0 to +10V	W13, W19,
0 to +5V	W13, W19, W22

FIGURE 4. MP7208/MP7216 Range Setting Jumpers.

As configured at the factory, these boards are jumpered for two's complement operation (see Table I above) with jumper W8 inserted and W7 open. For operation in the straight binary mode (any range), jumper W8 is open and W7 is inserted.

MP7208 PROCESS CURRENT LOOP INPUT OPERATION

The MP7208 is designed to allow the user to easily add the dropping resistors (R12-R19, Figure 6) needed to input process current loop signals such as 4-20 mA and 10-50 mA. Table II shows the resistor value and settings required.

Current Loop	Input Resistor	Amplifier Gain	ADC Range	Resolution
4-20 mA	250Ω	1	0 to 5V	4.88μA
10-50 mA	100Ω	1	0 to 5V	12.2μA

TABLE II. Current Loop Inputs

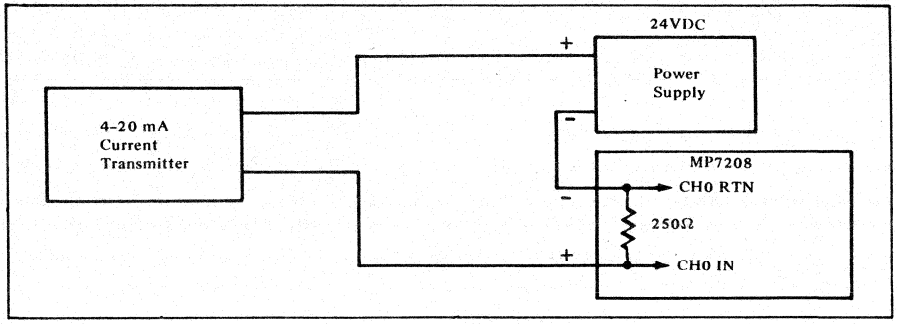


FIGURE 5. Typical Current Transmitter Interface.

ADDING EXTERNAL POWER SUPPLIES

The MP7208/7216/7104 boards require approximately 1 amp at 5V. In some applications it may be necessary to add an external power supply.

An external power supply can be added to supply ±15 volts to each board through its rear panel connector. When this is done, the loading of the 5 volt supply by the board is reduced by half. Before external power can be applied, the DC to DC converter must be disconnected. This is done on the MP7104 by removing plated through jumpers W53* - W55* and jumpers W1* - W3* for the MP7208 and MP7216. These plated through jumpers are removed according to the technique described for MP7104 output range selection.

Of course, MP7209-NS/7217-NS/7105-NS are connected at the factory for use with an external ±15VDC power supply. Connect these supplies to the analog connector pins described on the last page.

MP7208/7216 LOW LEVEL OPERATION

Terminals for external gain setting resistors (see Figure 6) have been provided so that the SDM853's instrumentation amplifier can be set for gains to 1000. The following formula can be used to calculate the value of this resistance Gain = $1 + 20\,k\Omega/R_{ext}$. Where R_{ext} is the resistance between pins 26 and 27 of the SDM853. (R7 and R8 in parallel form R_{EXT} on Figure 6). The internal gain adjustment potentiometer in the SDM853 module will give an adjustment range of ±0.5%. Very stable (10ppm) wire wound resistors should be used.

At high gains the instrumentation amplifier requires a longer settling time than that set internally. Pads have been provided (R10, R9, C7) to allow the addition of external settling, see Figure 7. As normally shipped the amplifier gain is set for unity and the delay time set for 9 μs. For a gain of 100 this time should be set for 25μs. See Table III. The delay time may be measured at pin 18 or pin 59 of the SDM853 or with a high impedance oscilloscope probe on either side of C7.

At very high gains, the system offset may be so large as to be beyond the range of the board's offset adjustment. When this occurs a 250k potentiometer (Spectrol 64P254) (R11 in Figure 6), a 1/10 watt 50ppm 51.1k metal film resistor (R20 in Figure 6) and jumper W21 must be added. This control becomes the coarse offset adjustment that is used to extend the range of the module's fine adjustment.

When operating the amplifier at high gain the overall accuracy of the system declines. At a gain of 1000 accuracies of ±0.1% can be expected. This is due to increased noise and a loss in amplifier linearity (see Table III). For lowest system noise, the ADC range should be set on the ±10V or 0 to 10V ranges with the amplifier providing all the system gain.

Amplifier Gain V/V	System Accuracy	Delay Time (microseconds)	Total Conversion Time (microseconds)
1	±0.025%	9	33
10	±0.03%	18	40
100	±0.08%	25	50
1000	±0.1%	70	95

TABLE III. Typical System Performance

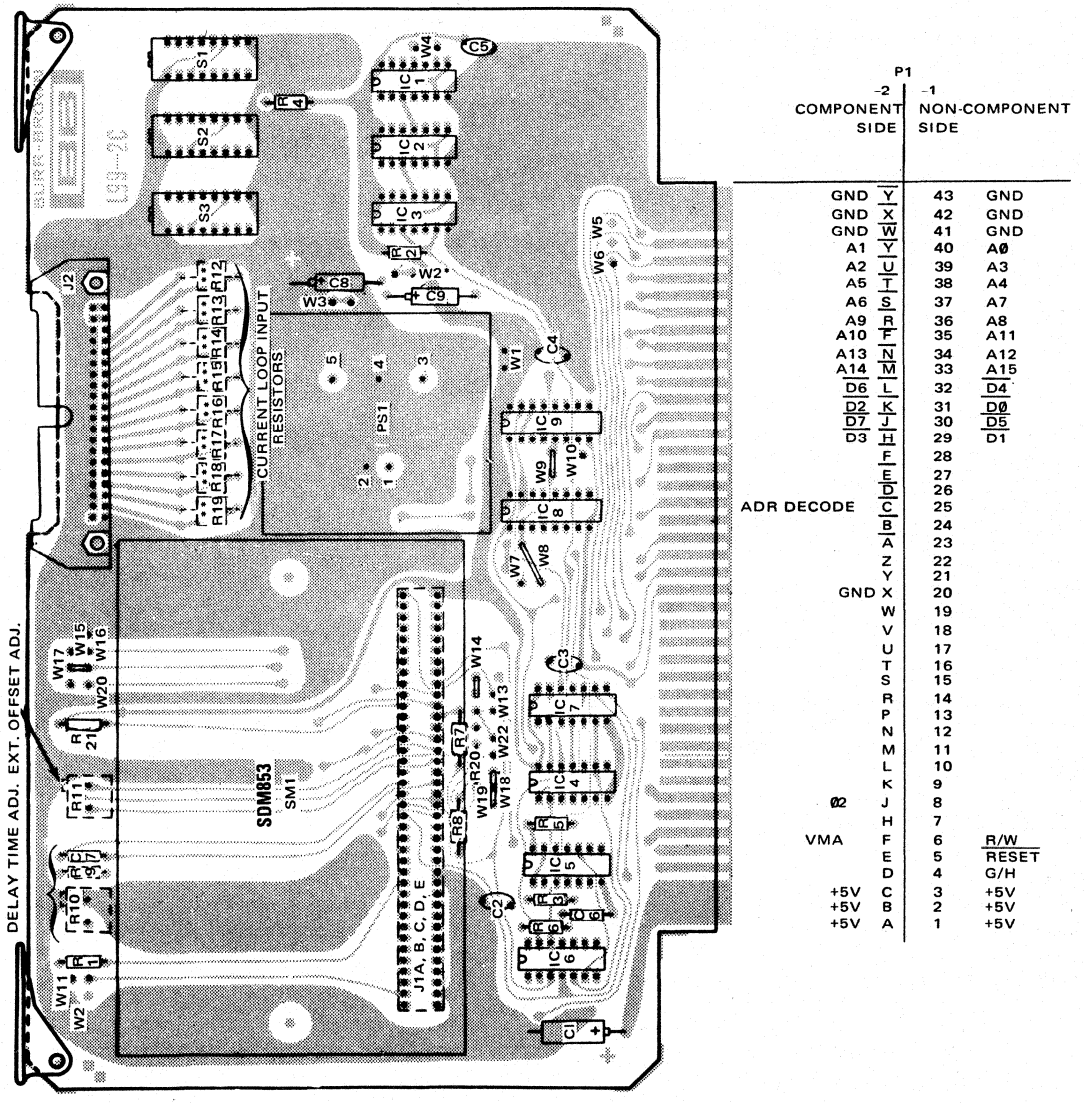


FIGURE 6. Analog Input System

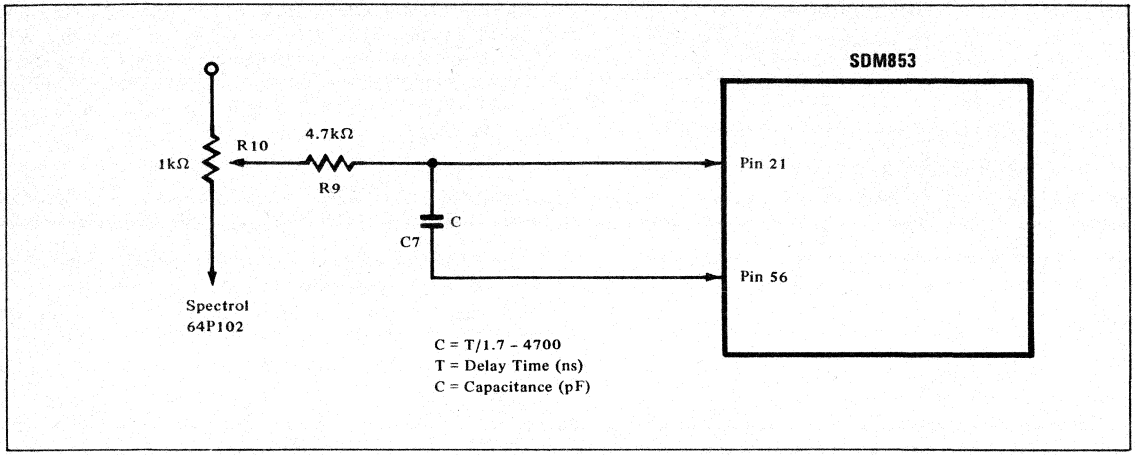


FIGURE 7. Delay Timer Adjustment

MP7104 CALIBRATION

The MP7104 board is calibrated through the use of the following program.

EXORCISER DAC CALIBRATION

```
        ORG $100
START   LDX #$800      CE   Set DAC data for
                            neg. voltage
                       08
        00             00
        STX  $EF00     FF   Load data into DAC1
                       EF
                       00
        STX  $EF02     FF   Load data into DAC2
                       EF
                       02
        STX  $EF04     FF   Load data into DAC3
                       EF
                       04
        STX  $EF06     FF   Load data into DAC4
                       EF
                       06
        BRA  START     20   Load data again
                       EF
        END
```

This program assumes that DAC1 occupies locations EF00 and EF01. If the board address has been changed the addresses associated with each STX instruction needs to be altered accordingly. The program also assumes that the board is jumpered for two's complement operation. If it has been changed to straight binary, the 12 bit data associated with the LDX instruction must have its most significant bit complemented.

After assembling and loading, a breakpoint should be set at the branch instruction via a 10F; V command to the EXbug MAID function. The program is then started with a 100; G command. When control is returned to the monitor from the breakpoint, all DACs will be programmed for their most negative output. Each DAC should then be set by its offset control for its most negative full scale output value. Figure 8 shows these values by range. However, before making these adjustments the board should be allowed to reach thermal equilibrium (about 30 minutes under power).

After all offset adjustments have been made, the data associated with LDX immediately should be changed to 07FF. Then repeat the above procedure but adjust the gain control for the most positive full scale output value for each DAC.

Calibration must always be made at the end of the cable that is normally used with the DAC. A five digital DVM which is capable of ±0.005% accuracy should be used.

Range	Low	High	1 LSB
±10V	-10.000V	+9.9951V	4.8828mV
±5V	-5.000V	+4.9976V	2.4414mV
±2.5V	-2.500V	+2.4987V	1.2207mV
0 to ±10V	0.0V	+9.9975V	2.4414mV
0 to ±5V	0.0V	+4.9988V	1.2207mV

FIGURE 8. DAC Calibration Values.

```
        ORG $100
START   LDAA #$64       86
                        64
        STAA COUNT      B7
                        01
                        1E
        CLRA            4F      Clear Accumulators
        CLRB            5F
CONV    LDX  $EF00      FE      Begin Conversion
                        EF
                        00
        NOP             01
        LDX  $EF00      FE      Read Data
                        EF
                        00
        CPX  #$XXXX     8C      Is Data = Low Ref
                        F8
                        00
        BEQ  AA         27
                        03
        INCB            5C      No. Increment Count
        BRA  AB         20
                        01
AA      INCA            4C      Yes. Increment = Count
AB      DEC COUNT       7A      Have Conversions reached
                                  100?
                        01
                        1E
        BNE  CONV       26      No. Do another Conversion
                        EB
        BRA  START      20      Yes. Begin next run
                        E2
COUNT 0
        END
```

XXXX is F800 for offset, 07FF for gain

The program assumes that the boards are set for channel zero located at EF00 and EF01. If the board has been reprogrammed for some other address this value should follow the program's two LDX instructions.

After assembling and loading insert a breakpoint at location 11C via a 11C; V command to EXbug's MAID function. The program is started with a 100; G command.

Calibration is performed by connecting a precision voltage source capable of 0.005% accuracy to CH0. (This could also be a DC voltage source of less absolute accuracy whose output is monitored by a 0.005% DVM.) The offset and gain adjustments on the SDM853 are made while applying the voltages shown in Figure 9. For other ranges, the offset voltage adjustment is made at the most negative value of the range less one half least significant bit (LSB). An LSB is equal to the span (full scale range) divided by 4096 for 12 bit resolution. The gain adjustment is made at the most positive value of the range less 1 1/2 LSB. Thus, for a range of ±50 mV, an LSB is 100 mV/4096 = 24.4μV. The offset adjustment is made at -50 mV + 12.2μV = -49.988 mV and the gain adjustment at +50 mV -36.6 μV = +49.963 mV. Before making these adjustments, however, the unit should be allowed to reach thermal equilibrium (about 30 minutes under power).

The offset adjustment is made first by using the appropriate offset calibration voltage. The calibration program is then run and after 100 conversions will halt at the breakpoint. Control will return to the MAID function which will then print the contents of all of the program registers at the time of the breakpoint. The contents of each accumulator should be compared for approximately equal values. If a difference of more than 10_{16} is present, slightly readjust the offset control and restart the program with a ;P command. Repeat this procedure until the accumulators' contents are within 10_{16} of each other.

The gain adjustment is made in much the same manner. However, the data associated with the CPX instruction in the calibration program must be changed from F800 to 7FF. The appropriate gain voltage is then applied and the calibration procedure performed as described for the offset adjustment.

Range	Offset	Gain
±10V	-9.9976V	+9.9926V
±5V	-4.9988V	+4.9963V
±2.5V	-2.4994V	+2.4981V
0 to +10	+1.22mV	+9.9963V
0 to +5	+0.61mV	+4.9981V

FIGURE 9. Data Acquisition Calibration Values.

DIFFERENTIAL-SINGLE ENDED SELECTION

An input board can be converted from single ended operation (MP7216) to differential operation (MP7208) or vice versa by simply changing several board jumpers. Figure 10 indicates those jumpers that must be present for a given mode of operation. To convert from one mode to the other remove those jumpers indicated for the present type of operation and install those necessary for the desired mode of operation.

MP7208 (Differential) required jumpers	MP7216 (Single-Ended) required jumpers
W12	W11
W5	W4
W17	W6
	W16
	W20

FIGURE 10. Input Mode Selection Jumpers.

It must be kept in mind that 16 channel operation requires 32 memory locations. Therefore, S1 of the address selector can only be set to even values.

TROUBLE SHOOTING

The calibration programs for these boards can also be used as an aid for troubleshooting. Through the programs all of the necessary EXORciser signals are repetitively generated so that a scope or logic probe can be used for signal tracing. When using these programs in this way no breakpoints should be inserted. The interface portion of each board is straightforward and can easily be followed if all of the EXORciser bus signals and the board's function diagram are understood.

MECHANICAL CHARACTERISTICS

Compatible with EXORciser and Micromodule card spacing.

Minimum card spacing: 12.7mm (0.5")

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers (SAE-43D/1-2).

40 pin analog connector (3M - 3432) provided on board. Mating connector (for OEM versions) is 3M - 3417. Recommended cable also by 3M: 3476/40.

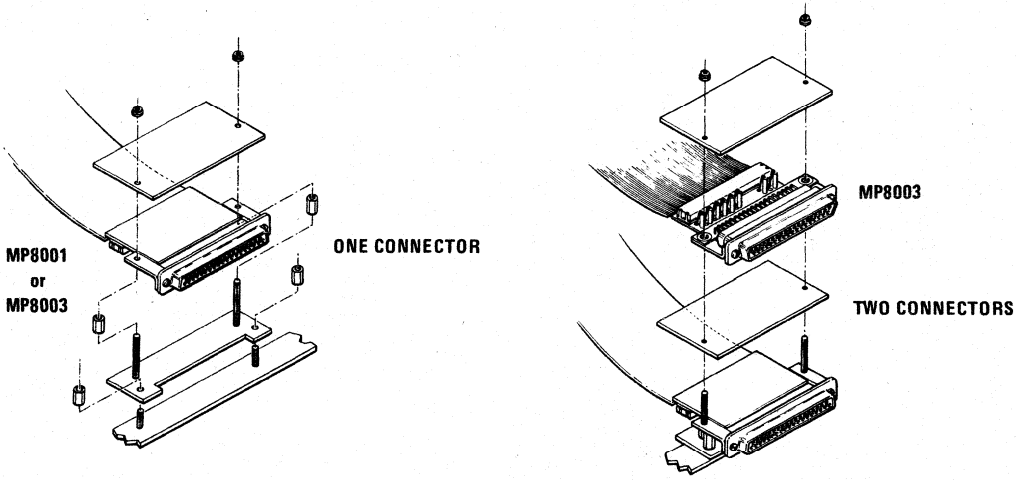
ANALOG CONNECTOR AT THE BACKPANEL

MP7104 BACKPANEL PINOUT PIN NO.				MP7208 BACKPANEL PINOUT PIN NO.				MP7216 BACKPANEL PINOUT PIN NO.			
Cable Shield GND	1	2	DAC1 - FB	Cable Shield GND	1	2	CH0 Return	Cable Shield GND	1	2	CH8 IN
DAC1 - OUT	3	4	DAC1 - GND	CH0 IN	3	4	CH1 Return	CH0 IN	3	4	CH9 IN
-15V	5	6	N/C	CH1 IN	5	6	CH2 Return	CH1 IN	5	6	CH10 IN
N/C	7	8	GND	CH2 IN	7	8	CH3 Return	CH2 IN	7	8	CH11 IN
+15V	9	10	DAC2 - FB	CH3 IN	9	10	CH4 Return	CH3 IN	9	10	CH12 IN
DAC2 - OUT	11	12	DAC2 - GND	CH4 IN	11	12	CH5 Return	CH4 IN	11	12	CH13 IN
DAC4 - FB	13	14	DAC4 - OUT	CH5 IN	13	14	CH6 Return	CH5 IN	13	14	CH14 IN
DAC4 - GND	15	16	GND	CH6 IN	15	16	CH7 Return	CH6 IN	15	16	CH15 IN
DAC3 - FB	17	18	DAC3 - OUT	CH7 IN	17	18	GND	CH7 IN	17	18	GND
DAC3 - GND	19	20	N/C	-15V	19	20	N/C	-15V	19	20	Remote COM
N/C	21	22	N/C	GND	21	22	GND	CH8 COM	21	22	CH0 COM
N/C	23	24	-15V	GND	23	24	GND	CH9 COM	23	24	CH1 COM
N/C	25	26	GND	GND	25	26	GND	CH10 COM	25	26	CH2 COM
+15V	27	28	N/C	GND	27	28	GND	CH11 COM	27	28	CH3 COM
N/C	29	30	N/C	GND	29	30	GND	CH12 COM	29	30	CH4 COM
N/C	31	32	N/C	GND	31	32	GND	CH13 COM	31	32	CH5 COM
N/C	33	34	N/C	GND	33	34	GND	CH14 COM	33	34	CH6 COM
N/C	35	36	N/C	GND	35	36	GND	CH15 COM	35	36	CH7 COM
N/C	37			-15V	37			+15V	37		

ANALOG CONNECTOR AT THE ANALOG BOARD

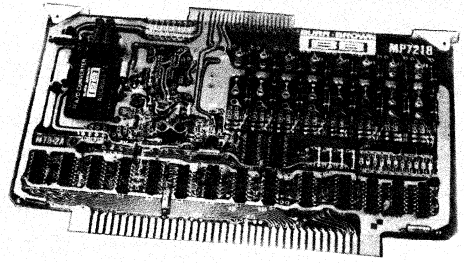
MP7104 and MP7105-NS BOARD ANALOG CONNECTOR PINOUT PIN NO.				MP7208 and MP7209-NS BOARD ANALOG CONNECTOR PINOUT PIN NO.				MP7216 and MP7217-NS BOARD ANALOG CONNECTOR PINOUT PIN NO.			
GND	1	2	GND	GND	1	2	Remote COM	GND	1	2	Remote COM
GND	3	4	GND	RET	3	4	GND	IN8	3	4	GND
DAC1 - GND	5	6	DAC1 - FB	IN0	5	6	GND	IN0	5	6	GND
DAC1 - OUT	7	8	DAC1 - GND	RET1	7	8	GND	IN9	7	8	GND
-15V	9	10	-15V	IN1	9	10	GND	IN1	9	10	GND
-15V	11	12	-15V	RET2	11	12	GND	IN10	11	12	GND
GND	13	14	-15V	IN2	13	14	GND	IN2	13	14	GND
GND	15	16	-15V	RET3	15	16	GND	IN11	15	16	GND
GND	17	18	-15V	IN3	17	18	GND	IN3	17	18	GND
DAC2 - GND	19	20	DAC2 - GND	RET4	19	20	GND	IN12	19	20	GND
DAC2 - OUT	21	22	DAC2 - OUT	IN4	21	22	GND	IN4	21	22	GND
DAC2 - FB	23	24	DAC2 - FB	RET5	23	24	GND	IN13	23	24	GND
DAC2 - GND	25	26	DAC2 - GND	IN5	25	26	GND	IN5	25	26	GND
DAC4 - GND	27	28	DAC4 - GND	RET6	27	28	GND	IN14	27	28	GND
DAC4 - FBD	29	30	DAC4 - FB	IN6	29	30	GND	IN6	29	30	GND
DAC4 - OUT	31	32	DAC4 - OUT	RET7	31	32	GND	IN15	31	32	GND
DAC4 - GND	33	34	DAC4 - GND	IN7	33	34	GND	IN7	33	34	GND
GND	35	36	GND	GND	35	36	GND	GND	35	36	GND
DAC3 - GND	37	38	DAC3 - FB	-15V	37	38	-15V	-15V	37	38	-15V
DAC3 - OUT	39	40	DAC3 - GND	-15V	39	40	-15V	+15V	39	40	+15

MP8001	Cable and Assembly for MP7208 and MP7216
MP8002	Connector Kit for MP7104, MP7208, MP7216
MP8003	Cable and Assembly for MP7104
MP7104	4 Channel DAC Output System (consists of MP7105, MP8002, MP8003)
MP7105-NS	MP7104 OEM version without MP8002, MP8003, and DC/DC converter
MP7208	8 Channel differential analog input system (consists of MP7209, MP8001, MP8002)
MP7209-NS	MP7208 OEM version without MP8001, MP8002, and DC/DC converter
MP7216	16 Channel single-ended analog input system (consists of MP7217, MP8001, MP8002)
MP7217-NS	MP7216 OEM version without MP8001, MP8002, and DC/DC converter



BACKPANEL CONNECTOR INSTALLATION IN EXORCISER SYSTEMS

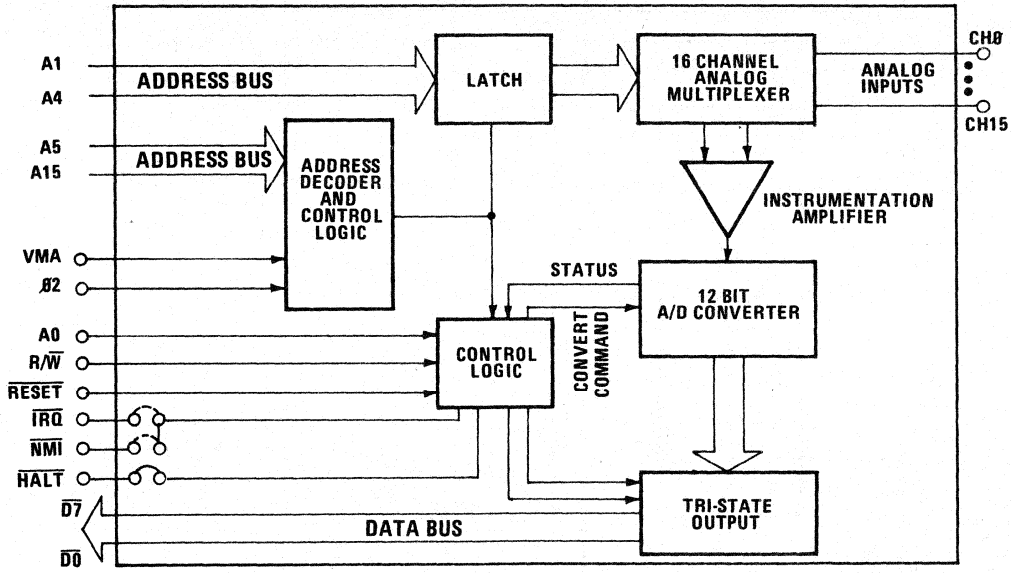
BURR-BROWN



MP7218

MICROCOMPUTER ANALOG INPUT SYSTEM

A LOW-COST 12-BIT, 16-CHANNEL ANALOG INPUT SYSTEM COMPATIBLE WITH MOTOROLA MICROMODULE AND EXORciser® MICROCOMPUTERS



FEATURES

- 70°C BURN-IN
- OPERATES FROM COMPUTER'S ±12VDC, +5VDC POWER SUPPLY
- ACCEPTS LOW LEVEL INPUTS
- EASY TO PROGRAM

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-382A

Printed in U.S.A. July, 1978

DESCRIPTION

The MP7218 is an analog input microperipheral board designed to be used with Motorola's Micromodule and EXORciser®microcomputer systems. It is electrically and mechanically compatible with these systems. The analog system is contained on a single printed circuit board that is treated as memory by the CPU. The analog interface is at a connector on the opposite edge of the board from the bus connector.

This data acquisition system includes 25V input overvoltage protection, an analog multiplexer, high gain instrumentation amplifier, and 12 bit A/D converter along with all the necessary timing, decoding and control logic. The unit operates from the microcomputer's +5VDC and ±12VDC power supplies. The MP7218 is capable of interfacing ±10mV to ±5V signal levels.

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When programming with this peripheral, it is treated as memory. The A/D converter output is a 12 bit word so two 8 bit memory locations are needed for each channel. Address bits A15-A5 select the board and A4-A1 select the analog input channel to be digitized. To start a conversion the board is written to using an STA or similar instruction. After conversion data remains in the output latches waiting to be read until another conversion is initiated. This unit may be used with or without halting the CPU or in the interrupt mode.

The MP7218 is jumpered at the factory with the first channel at address $93E0_{16}$, the second at $93E2_{16}$, etc. By changing jumpers, the boards may be placed anywhere in memory.

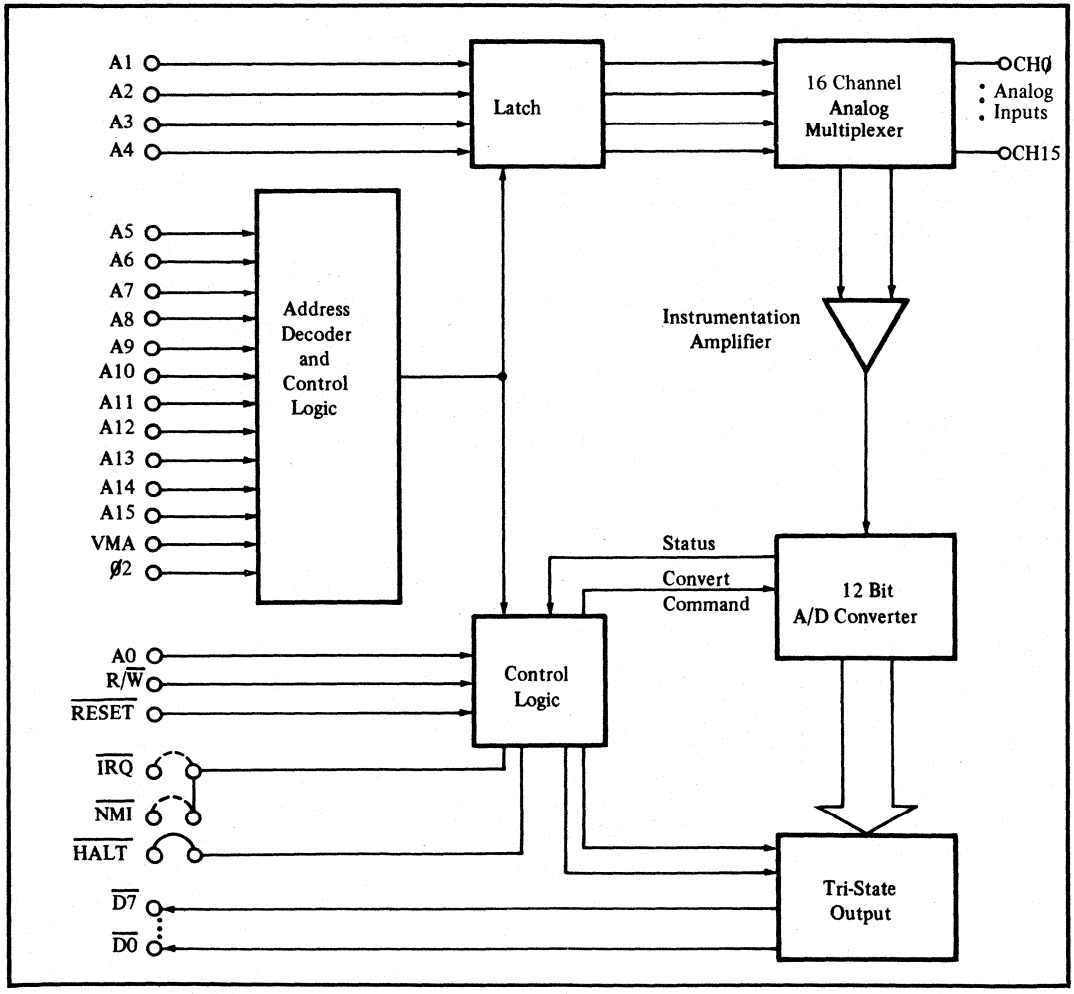


FIGURE 1. MP7218 Block Diagram

SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ANALOG INPUT	MP7218
Number of analog inputs	8 differential/16 single-ended[1]
Input range	±10mV to ±5V[2]
ADC gain ranges	0 to 5V
(strap selectable)	±5V, ±2.5V
Amplifier gain range	1 to 1000
Factory set gain	1
Amplifier gain equation	$G = 1 + 20k\Omega/R_{EXT}$
(resistor programmable)	
Input overvoltage protection	±25V
Input impedance, DC	100 megohms
Bias current	
25°C	20nA
0 to 70°C	50nA
Amplifier output noise	1.2mV, rms; 7mV, p-p
(Gain = 100 R_S = 500Ω)	
Amplifier input offset voltage, max	400μV
Amplifier input offset voltage	(2 + 20/G)μV/°C
drift, max	
TRANSFER CHARACTERISTICS	
Resolution	12 bits binary
Throughput accuracy, (±5V range, max)	±0.025% FSR[3]
±10mV range	±0.1% FSR
Temperature coefficient of accuracy range, max	
±5V	±0.004% FSR/°C
±10mV range	±0.01% FSR/°C
Conversion time ±5V range	50 microseconds
±10mV range	100 microseconds
CMRR (for differential inputs)	90dB (DC to 60 Hz)
DIGITAL INPUT/OUTPUT	
All signals are compatible with	
Microcomputer bus	
Output coding	Bipolar, two's complement[4]
Logic loading (all inputs)	One LSTTL load
Data bus output drive	20 TTL loads
$\overline{HALT}$, $\overline{IRQ}$, $\overline{NMI}$ output drive	10 TTL loads
POWER REQUIREMENTS	
Power supply voltages	+5VDC at 100mA,
	+12VDC at 50mA
	-12VDC at 75mA
Range for rated accuracy	4.75V to 5.25V and
	±11.4V to ±12.6V
TEMPERATURE RANGE	
Temperature	0°C to 70°C

(1) Connected at the factory as 8 channels differential.
(2) Connected at the factory for ±5V range.
(3) FSR is Full Scale Range (i.e., 10V for ±5V range, 5V for 0 to +5V range).
(4) Straight binary jumper selectable. (W80, W81)

MECHANICAL CHARACTERISTICS

Compatible with EXORciser and Micromodule card spacing.

Minimum card spacing: 12.7mm (0.5")

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers (SAE-43D/1-2).

Analog connector: 50 pin PC edge connector with 0.100" contact centers. Burr-Brown part number: 2250MC - $14 (Viking # 3VH25/1JN5 - solder tab). Scotchflex cable connector also available from 3M (# 3415-0001).

OPERATING INSTRUCTIONS

INSTALLATION

The MP7218 is shipped from the factory calibrated and ready for immediate use. Installation requires only plugging the card into any empty slot and connecting the analog signals.

PROGRAMMING

Programming of this analog I/O board is easily accomplished since it is treated as memory. The A/D converter output is a 12 bit word so two 8 bit memory locations are needed for each channel. This board is jumpered at the factory with a base address of $93E0_{16}$ (the first channel is at $93E0_{16}$, the second at $93E2_{16}$, etc.). To start conversion, write to the board using the correct address. For example, with a board base address of $93E0_{16}$ (1001 0011 1110 0000), use

```
STAA $93E6
```

to start conversion of channel 3. The data written to the board is irrelevant.

To input the 12 data bits after conversion is complete read the board using the base address. For example,

```
LDX $93E0
```

may be used to read the board. This instruction places the most significant byte into the upper half of the Index Register and the least significant byte into the lower half of the Index Register. Any other memory read instruction(s) can be used provided it reads the most significant byte first. Address bits A4-A1 are irrelevant. The most significant byte of data is ready with a valid address and AO = 0, the least significant byte with AO = 1 (Table I and III). As shipped from the factory, D4-D7 are jumpered to the most significant bit (B11) of the 12 bit A/D converter word when reading the most significant byte of data. D4, D5 and D7 may be jumpered for other functions. D7 may optionally be tied to ground and with a pull-up resistor elsewhere in the system. D7 may be read to determine which boards in a system are plugged in. D5 may be connected to display the status of the interrupt (0 indicates interrupt active). D4 may be connected to display the status of the analog to digital converter output ("1" indicates conversion complete). When making a change, first remove those jumpers indicated for the present mode and replace them with the jumpers required for the desired mode.

Normal Mode	Optional Mode
D7 = B11	1 (Indicates that board is plugged in)
D6 = B11	Not used
D5 = B11	Interrupt Status (0 Indicates Interrupt active)
D4 = B11	A/D Status (1 Indicates conversion complete)
D3 = B11	B11
D2 = B10	B10
D1 = B9	B9
D0 = B8	B8

TABLE I. Most Significant Byte Output (A0 = 0).

Data Bit	MSB B11	Optional Function
$\overline{D7}$	W70	W66
$\overline{D6}$	W69	W65
$\overline{D5}$	W68	W58
$\overline{D4}$	W67	W57

TABLE II. Jumpers for D7 - D4 Optional Function.

$\overline{D7}$ = B7
$\overline{D6}$ = B6
$\overline{D5}$ = B5
$\overline{D4}$ = B4
$\overline{D3}$ = B3
$\overline{D2}$ = B2
$\overline{D1}$ = B1
$\overline{D0}$ = B0 LSB

TABLE III. Least Significant Byte Output (A0 = 1).

The data from the most recent conversion will remain on the board until a new conversion is intiated by a write instruction to the board.

The board may be read at any time to determine its current status. The most significant byte is read with a valid address and A0 = 0.

MODES OF OPERATION

Halt Mode. This is the normal mode of operation as shipped from the factory. Jumper W64 is installed and W24, W25 removed. The start conversion command is followed with a NOP instruction. This method allows the board to halt the processor during a conversion and resume program operation after conversion is complete. The software in this mode is simpler than in any other. These instructions will read channel 3 at location $93E6_{16}$:

```
STAA    $93E6    Starts conversion
NOP              Allows MP7218 to Halt CPU
LDX     $93E0    Loads converted data to the index
                 register.
```

Polling Mode. Jumpers W24, W25, and W64 are removed. After a convert command is issued, the computer is not allowed, by software control, to read the board for 50μs. To assure that the conversion has been completed, the status bits may be interrogated. These instructions will read channel 3 at location $93E6_{16}$:

```
        STAA    $93E6    Starts conversion
                  :      }
                  :      } Other software for conversion time
                  :      }
CC      LDAA    $93E0    Load MSB of data (with status bit in D4)
                         to accumulator
        BITA    $10      }
        BNE CC           } Check for D4 = "1"
        LDX     $93E0    Load data word to index register when
                         when D4 = "1"
```

Interrupt Mode. Jumper W64 is removed and W24 or W25 installed (W24 for the maskable interrupt, $\overline{IRQ}$, and W25 for the non-maskable interrupt, $\overline{NMI}$). After a conversion is completed, the interrupt line will go low and remain low until a board read is completed. The interrupt line may be tied to a vectored or nonvectored interrupt system. The interrupt line is optionally available as a data bit, $\overline{D5}$, and may be read by a skip chain software interrupt system.

THEORY OF OPERATION

The combination of a valid address and a write command triggers a one-shot which generates a 25μs delay pulse. The low to high transition of this pulse latches the channel address. The 25μs delay allows the analog multiplexer and instrumentation amplifier time to settle to $\pm$0.01% before triggering the successive approximation A/D converter. The falling edge of the 25μs delay pulse triggers another one-shot that delivers a 1μs pulse. The rising edge of this pulse starts the A/D converter.

There are two control lines which may be connected to the bus: Halt and Interrupt.

The $\overline{HALT}$ control line goes low when the first one-shot is triggered and remains low until the conversion is complete (50μs). The $\overline{IRQ}$ or $\overline{NMI}$ interrupt line goes low when the conversion is completed and remains low until the board is read.

DIFFERENTIAL/SINGLE-ENDED SELECTION

The MP7218 is an 8 channel differential voltage input unit which can be user connected as 16 channels single-ended. Table IV shows the jumper connections necessary to change from differential to single-ended. When changing modes, remove the jumpers indicated for the present mode, then insert the jumpers indicated for the desired mode.

8 Channel Differential Jumpers	16 Channel Single-Ended Jumpers
W42, W46	W43, W45, W47

TABLE IV. Differential/Single-Ended Conversion.

INPUT RANGES

The on-board instrumentation amplifier can be resistor programmed for gains from 1 to 1000. The MP7218 is shipped with a gain of 1 and a $\pm$5V A/D converter range. The board may be set for other A/D converter input ranges as shown in Table VII. The gain of the instrumentation amplifier may be set to any value between 1 and 1000 by adding gain setting resistors. R65 and R66 in parallel (W48 inserted), R63 and R64 in parallel (W49 inserted) and R62 may be used to set the gain. These resistors and the gain setting formula are shown in Figure 2.

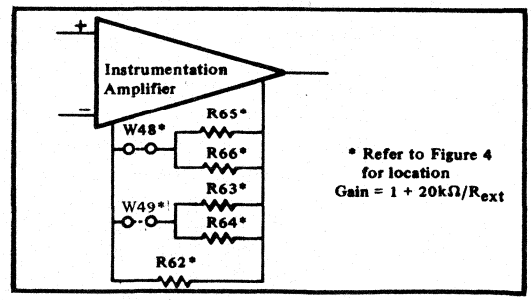


FIGURE 2. Setting Instrumentation Amplifier Gain.

An on-board delay timer allows for the settling time of the multiplexer and instrumentation amplifier before starting the A/D converter. The instrumentation amplifier settling time increases as the gain increases. The MP7218 delay timer is factory set to 25μsec which is sufficient for gains of up to 5. The delay timer may be set to longer delay times by removing R36 and adding R35*. For the higher gains, see Table V for the delay time and R35. The MP7218 is connected for two's complement output coding (W80 inserted). To convert to straight binary coding remove W80 and insert W81.

Amplifier Gain V/V	Delay Time (microseconds)	R35 (±20%)
1	25	15.4kΩ
10	30	18.7kΩ
100	40	24.3kΩ
1000	100	60.4kΩ

TABLE V. Delay Time vs. Amplifier Gain.

Gain	Full Scale Value/Resolution for ADC Ranges			
		±5V	±2.5V	0 to 5V
1	Range	±5V	±2.5V	0 to 5V
	Resolution	2.44mV	1.22mV	1.22mV
5	Range	±1V	±0.5V	0 to 1V
	Resolution	488μV	244μV	244μV
100	Range	±50mV	±25mV	0 to 50mV
	Resolution	24.4μV	12.2μV	12.2μV

TABLE VI. Input Voltage Ranges.

Range	Jumpers
±5V	W56, W52
±2.5V	W54, W56, W52
0 to +5V	W54, W56, W53

TABLE VII. MP7218 Range-setting Jumpers.

OVERVOLTAGE PROTECTION/FILTERS

Each input channel is protected to 25V overvoltage. The circuitry is shown in Figure 3.

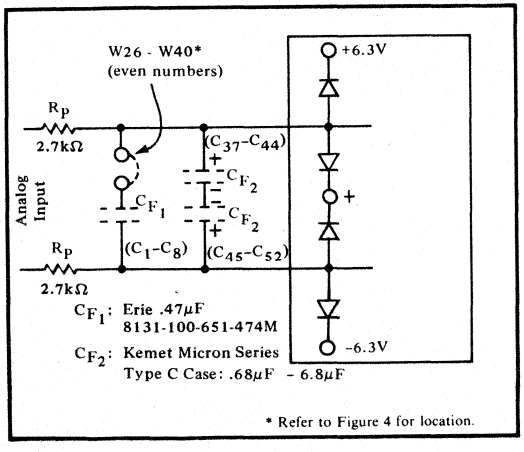


FIGURE 3. Input Overvoltage Protection and Filtering.

The input protection resistors (R_P) limit the current which flows through the protection diodes when overvoltages are applied to the inputs. Optional capacitors may be added to each differential input channel, which together with the input protection resistors form a single pole input filter. A nonpolarized capacitor C_{F1} may be added and/or back-to-back polarized capacitors can be used as shown in Figure 3 to form this filter. Each C_{F1} has a jumper that must be connected to complete the filter.

Channel	Filter Capacitor Jumper	Current Loop Resistor Jumper
0	W26	W27
1	W28	W29
2	W30	W31
3	W32	W33
4	W34	W35
5	W36	W37
6	W38	W39
7	W40	W41

TABLE VIII. Input Jumpers.

ADDRESS MODIFICATION

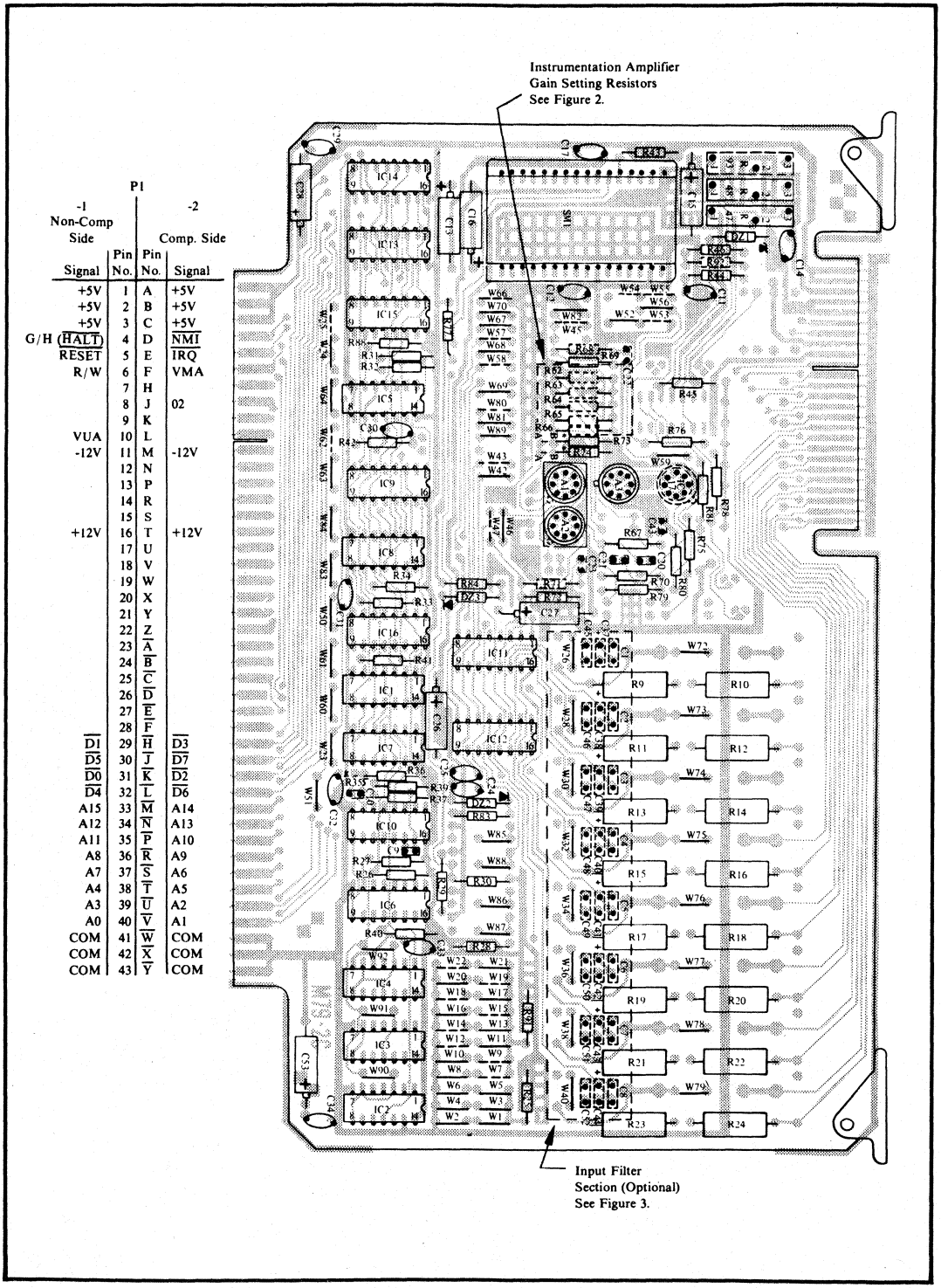
The base address of a board can be set to any value by changing the address selector jumpers on the input of eleven exclusive-or gates. The base address of these boards is set at the factory to $93E0_{16}$. Table IX shows the jumpers required for each address line.

Address Line	Factory Set	"0"	"1"
A15	1	W19	W20
A14	0	W21	W22
A13	0	W17	W18
A12	1	W15	W16
A11	0	W11	W12
A10	0	W13	W14
A9	1	W9	W10
A8	1	W7	W8
A7	1	W3	W4
A6	1	W5	W6
A5	1	W1	W2

TABLE IX. Address Selection Jumpers.

Address lines A8-A15 are set to 93_{16} by jumpers as shown in Table IX. Address lines A5-A7 are factory set to "1" by inserting both the "0" and the "1" jumpers from Table IX. This is done so that the base address of lines A5-A7 can be changed simply by removing jumpers. For instance, to change the A5 address to a "0", jumper W2 must be removed. However, because of a shared pull-up resistor W3 and W5 for A6 and A7 must also be removed. Whenever an address other than 111 is programed for A5-A7 only those jumpers required for the address should be present.

When changing addresses care should be taken to first remove the present address jumpers before installing the new jumpers.



P1

-1 Non-Comp Side Signal	Pin No.	Pin No.	-2 Comp. Side Signal
+5V	1	A	+5V
+5V	2	B	+5V
+5V	3	C	+5V
G/H (HALT)	4	D	NMI
RESET	5	E	IRQ
R/W	6	F	VMA
	7	H	
	8	J	02
	9	K	
VUA	10	L	
-12V	11	M	-12V
	12	N	
	13	P	
	14	R	
	15	S	
+12V	16	T	+12V
	17	U	
	18	V	
	19	W	
	20	X	
	21	Y	
	22	Z	
	23	A	
	24	B	
	25	C	
	26	D	
	27	E	
	28	F	
D1	29	H	D3
D5	30	J	D7
D0	31	K	D2
D4	32	L	D6
A15	33	M	A14
A12	34	N	A13
A11	35	P	A10
A8	36	R	A9
A7	37	S	A6
A4	38	T	A5
A3	39	U	A2
A0	40	V	A1
COM	41	W	COM
COM	42	X	COM
COM	43	Y	COM

FIGURE 4. Analog Input System

CALIBRATION

The MP7218 board can be calibrated with the following program.

```
                        ORG $00FD
00FD 8E                 LSP  $037F
     03
     7F
0100 86    START        LDAA #$64
     64
0102 B7                 STAA COUNT
     01
     1B
0105 4F                 CLRA            Clear Accumulators
0102 5F                 CLRB
0107 B7    CONV         STAA $93E0      Begin Conversion
     93
     E0
010A 01                 NOP
010B FE                 LDX  $93E0      Read Data
     93
     E0
010E 8C                 CPX             Is Data = Low Ref
     F8                                 Ref BTC Offset
     00
0111 26                 BNE  AA         No
     01
0113 5C                 INCB            Yes. Increment
                                        Count
0114 7A    AA           DEC  COUNT      Have Conversions
                                        reached 100?
     01
     1B
0117 26                 BNE  CONV       No. Do another
                                        Conversion
     EE
0119 20                 BRA  START      Yes. Begin next run
     E5
011B       COUNT        RMB  1
                        END
```

This program assumes that it is under control of the Motorola EXORciser EXbug monitor. If either the Mikbug or Microbug monitor is available, the following printout software may be added by replacing all codes starting from location 0119_{16}. In addition, the references to COUNT at 0104_{16} and 0116_{16} must be changed from 1B to $2F_{16}$.

```
                        Mikbug   Microbug
OUT2H                   EQU $E0BF.....$FD98
OUTEEE                  EQU $E1D1.....$FD26

0119 F7                 STA B   STR0
     01
     30
011C CE                 LDX     #STR0
     01
     30
011F BD                 JSR OUT2H       Print no. of true conversions.
     E0
     BF
0122 86                 LDAA    #0D
     0D
0124 BD                 JSR OUTEEE
     E1
     D1
0127 86                 LDAA #0A
     0A
0129 BD                 JSR OUTEEE
     E1
     D1
012C 7E                 JMP START
     01
     00
012F       COUNT        RMB 1
0130       STR0         RMB 2
                        END
```

The reference values for straight binary coding are Offset Ref = 0000_{16} and Gain Full Scale Ref = $FFFF_{16}$. For two's complement binary coding, Offset Ref = $F800_{16}$ and Gain Full Scale Ref = $07FF_{16}$.

The program assumes that the boards are set for channel zero located at $93F0_{16}$ and $93E1_{16}$. If the board has been reprogrammed for some other address this value should follow the program's LDX and STAA instruction at $010B_{16}$ and 0107_{16}.

When using an EXORciser and after assembling and loading, insert a breakpoint at location 119_{16} via a 12C; V command to EXbug's MAID functions. The program is started with a 00FD; G command.

If using Microbug or Mikbug, start program with GØØFD.

Calibration is performed by connecting a precision voltage source capable of 0.005% accuracy to CH0. (This could also be a DC voltage source of less absolute accuracy whose output is monitored by a 0.005% DVM.) The offset and gain adjustments are made while applying the voltages shown in Table X. For other ranges the offset voltage adjustment is made at the most negative value of the range plus one half least significant bit (LSB). An LSB is equal to the span (full scale range) divided by 4096 for 12 bit resolution. The gain adjustment is made at the most positive value of the range less 1 ½ LSB. Thus, for a range of ±100mV, an LSB is 200mV/4096 = 48.8μV. The offset adjustment is made at -100mV + 24.4μV = -99.976 mV and the gain adjustment at +100mV -73.2μV = +99.927 mV. Before making these adjustments, however, the unit should be allowed to reach thermal equilibrium (about 30 minutes under power).

The offset adjustment is made first by using the appropriate offset calibration voltage. With EXORciser the calibration program is then run and after 100 conversions will halt at the breakpoint. Control will return to the MAID function which will then print the contents of all program registers at the time of the breakpoint. The contents of accumulator B should be 32_{16}. If a difference of more than 10_{16} is present, slightly readjust the offset control and restart the program with a ;P command. Repeat this procedure until the accumulators' contents are within 10_{16} of each other. If using Microbug or Mikbug the B register will be printed after 100 conversions and the next 100 conversions started. Printout should be $32 \pm 10_{16}$. If not, adjust offset control.

The gain adjustment is made in much the same manner. However, the data associated with the CPX instruction in the calibration program must be changed from $F800_{16}$ to $7FF_{16}$ (two's complement). The appropriate gain voltage is then applied and the calibration procedure performed as described for the offset adjustment.

Range	Offset	Gain
±5V	-4.9988V	+4.9963V
±2.5V	-2.4994V	+2.4981V
0 to +5	+0.61mV	+4.9981V
±1V	+0.99976V	+0.99927V
±0.5V	-0.49988V	+0.49963V
0 to +2V	+0.244mV	+1.9993V
0 to +1V	+0.122mV	+0.99953V
±50mV	-49.988mV	+49.963mV
±25mV	-24.994mV	+24.981mV
0 to 100mV	+12.2μV	+99.953mV
0 to 50mV	+6.1μV	+49.981mV

TABLE X. Calibration Values.

JUMPER SUMMARY

W1 - W20 — Address selection jumpers, set at the factory for $93E0_{16}$. If A5, A6 or A7 is changed, one jumper must be removed from each address line (A5, A6, A7). See page 6-57.

W26 - W40 (even numbers) — If installed, these jumpers will selectively insert user supplied input filter capacitors. See page 6-57.

W27 - W41 (odd numbers) — If installed, these jumpers will selectively insert user supplied 250Ω input current loop resistors. See MP7608-I Data Sheet (PDS-380).

Jumper	Channel
W27	0
W29	1
W31	2
W33	3
W35	4
W37	5
W39	6
W41	7

W42 — Jumper is inserted at factory to program multiplexer for 8 channel differential input operation. Remove jumper for 16 channel single-ended operation.

W43 — Insert jumper to program multiplexer for 16 channel single-ended input operation.

W45 — Insert jumper for 16 channel single-ended voltage input operation. This connects the non-inverting input of the instrumentation amplifier to REMOTE COMMON (W82 connects REMOTE COMMON to system common.)

W46 — Jumper is inserted at the factory for 8 channel differential input operation. This connects the inverting input of the instrumentation amplifier to RET0-RET7.

W47 — Insert jumper for 16 channel single-ended voltage input operation. This connects the outputs of both 8 channel multiplexers to the non-inverting input of the instrumentation amplifier.

W24 - W25 — Used to obtain a maskable or nonmaskable interrupt. W24 for $\overline{IRQ}$, W25 for $\overline{NMI}$. W24 and W25 are open as shipped from the factory.

W62 - W63 — W62 is inserted for VMA input, W63 for VUA input. W62 is open and W63 inserted at the factory (VUA input). For VMA input, W62 is inserted and W63 open.

W64 — Jumper inserted at the factory to allow for HALT mode of operation. W64 should be open for interrupt or polling operation. See page 6-56.

W80 — Inserted at factory for two's complements output coding.

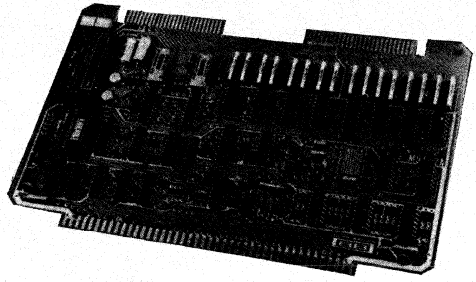
W81 — W81 is installed and W80 removed for straight binary output coding.

W82 — Inserted at factory to connect REMOTE COMMON to system common. W82 connects the I.A. low input to system common for single-ended input operation. Remove for pseudo-differential input operation where REMOTE COMMON is connected to a separate external ground that is common to all inputs.

Component Side		Non Component Side	
+5V	1	2	+5V
+5V	3	4	+5V
+12V	5	6	+12V
GND	7	8	GND
GND	9	10	GND
	11	12	GND
REMOTE COMMON	13	14	GND
	15	16	
-12V	17	18	-12V
IN 0	19	20	RET0/IN 8
	21	22	
IN 1	23	24	RET1/IN 9
	25	26	
IN 2	27	28	RET2/IN 10
	29	30	
IN 3	31	32	RET3/IN 11
	33	34	
IN 4	35	36	RET4/IN 12
	37	38	
IN 5	39	40	RET5/IN 13
	41	42	
IN 6	43	44	RET6/IN 14
	45	46	
IN 7	47	48	RET7/IN 15
	49	50	

TABLE XI. Analog Connections.

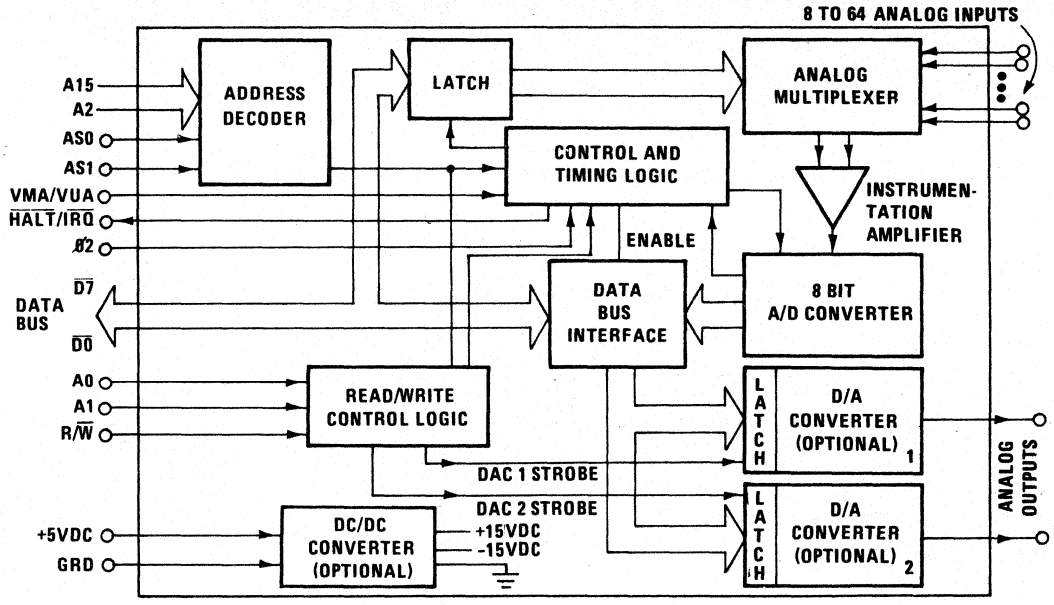
BURR-BROWN



MP7408
MP7432

MICROCOMPUTER ANALOG I/O SYSTEM

A LOW-COST 64-CHANNEL ANALOG INPUT/2 CHANNEL ANALOG OUTPUT SYSTEM COMPATIBLE WITH MOTOROLA MICROMODULE AND EXORciser® SYSTEMS



FEATURES

- EASY TO PROGRAM
  - Systems are treated as memory
- REDUCES SYSTEM DEVELOPMENT TIME
- EASY TO USE
  - 8 to 64 input channels on one board
  - Analog input and output on one board
  - High level or low level inputs
- 70°C BURN-IN

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PDS-378

Printed in U.S.A. July, 1978

DESCRIPTION

This microcomputer peripheral provides two functions that interface directly to Motorola's Micromodule and EXORciser microcomputers. The functions are: (1) Analog Data Acquisition and (2) Analog Output. Both analog input and output systems are contained on a single printed circuit board that is treated as memory input or output by the CPU. The analog interface is at connectors on the opposite edge of the board from the bus connector.

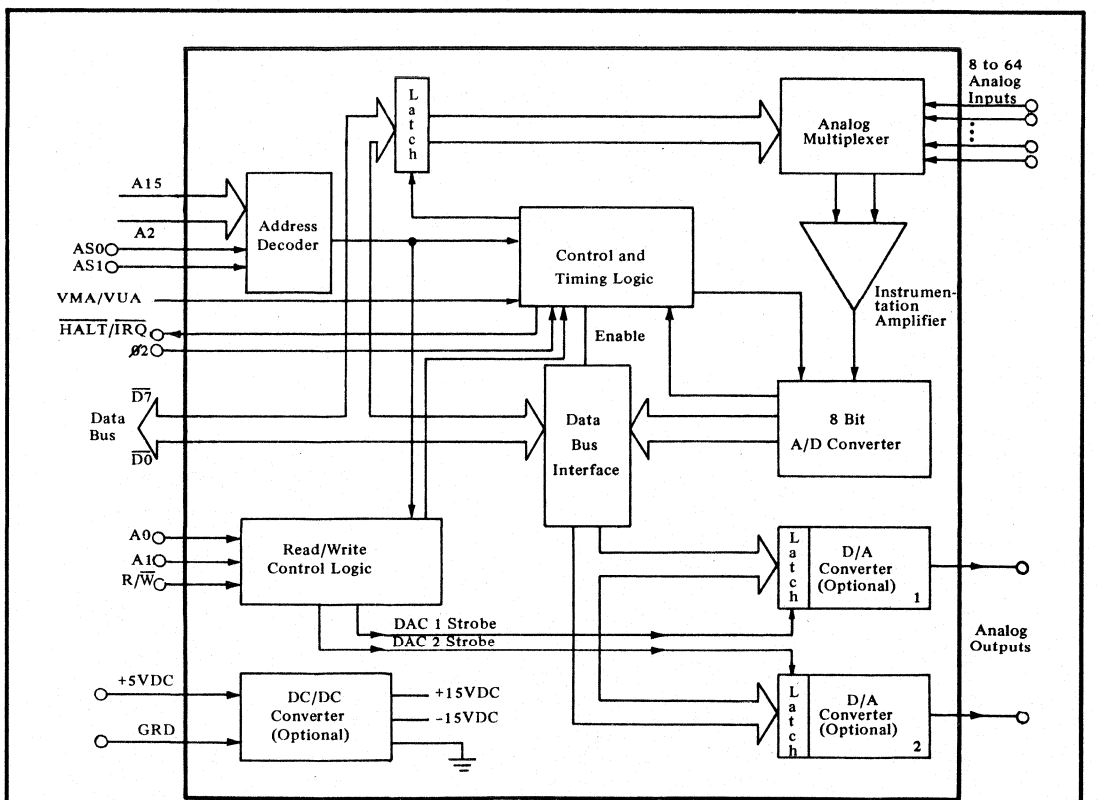
The Data Acquisition System is available with up to 32 channels differential (64 channels single-ended) on one board. It includes an input multiplexer, high gain instrumentation amplifier, 8-bit A/D converter along with all the necessary timing, decoding and control logic. This system can digitize low level or high level analog signals. The gain of the internal instrumentation amplifier can be programmed with a single external resistor to allow input signal ranges as low as ±2.5mV. This means that the MP7400 can be connected to low level sensors such as thermocouples and strain gauges without external signal amplification. A DC/DC converter (+5V to ±15V) is also available so that only the computer's power supply is required. The Data Acquisition System is available with two optional 8-bit D/A converters to provide analog output in addition to input on the same board.

THEORY OF OPERATION

When programming these peripherals, they are treated as memory locations. Any memory reference instruction can be used. Two memory locations are used by the analog input system. One location is used to select the channel and start conversion. The same location provides status information when read. The other location contains the converted data. The analog output system also uses two memory locations, one for each channel.

Because these units are treated as memory, a minimum of instructions are needed to read an input channel or to set the output of a D/A converter. The MP7400's versatile memory mapped operation allows it to be used with or without halting the CPU or in the interrupt mode.

All of these units are jumpered at the factory for address 95F0 through 95F3.



MP7400 BLOCK DIAGRAM

SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ANALOG INPUT/OUTPUT SYSTEM

ANALOG INPUT

Number of analog inputs	
8 differential (16 signal-ended)[5]	MP7408
32 differential (64 single-ended)[6]	MP7432
Input voltage range[1]	±5mV to ±5V
ADC gain ranges[1]	±10V, 0 to 10V 0 to 5V
(strap selectable)	±5V, ±2.5V
Amplifier gain range[1]	1 to 1000
(resistor programmable)	
Amplifier gain equation	$G = 100k\Omega / R_{EXT}$
Input overvoltage protection	±15V
Input impedance	100 megohms
Bias current	
25°C (max)	+300nA
0°C to 70°C	-2nA/°C
Amplifier input offset voltage drift	$\pm\left(5 + \frac{1000}{G}\right)$ μV/°C

ANALOG INPUT TRANSFER CHARACTERISTICS

Resolution	8 bit binary
Throughput accuracy ±5V range (max)	±0.4% FSR[2]
Throughput accuracy ±10mV range	±0.5% FSR
Temperature coefficient of accuracy	
±5V range (max)	±0.02% FSR/°C
±10mV range	±0.07% FSR/°C
Conversion time ±5V range (max)	44 microseconds
Conversion time ±10mV range (max)	84 microseoends
CMRR (for differential inputs)[3]	66 dB (Gain = 2)
	86 dB (Gain = 100)

ANALOG OUTPUT

Number of analog outputs	2
Output voltage range[4]	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA (strap selectable)
Output impedance	1Ω
Output settling time (max)	< 5 microseconds

ANALOG OUTPUT TRANSFER CHARACTERISTICS

Resolution	8 bit binary
Throughput accuracy (max)	±0.4% FSR
Temperature coefficient of accuracy	
Unipolar	±0.005% FSR/°C
Bipolar	±0.01% FSR/°C

DIGITAL INPUT/OUTPUT

All signals are compatible with Motorola Microcomputer Bus	
Output coding	Bipolar, two's complement; Unipolar, straight binary
An analog input channel is selected by:	$\overline{D0}$ through $\overline{D5}$
An analog output channel is selected by:	A0
The input/output data bits are read through:	$\overline{D0}$ through $\overline{D7}$

POWER REQUIREMENTS

MP7408, MP7432	+5VDC +5% at 1 amp
MP7408-NS, MP7432-NS	+5VDC ±5% at 500mA +15VDC ±5% at 40mA -15VDC ±5% at 40mA
With analog output	
MP7408-AO, MP7432-AO	+5VDC ±5% at 2 amp
MP7408-NS-AO, MP7432-NS-AO	+5VDC ±5% at 500mA +15VDC ±5% at 100mA -15VDC ±5% at 100mA

TEMPERATURE RANGE

0°C to 70°C

OPERATING INSTRUCTIONS

INSTALLATION

These units are shipped from the factory calibrated and ready for immediate use. Installation requires only plugging the card into any empty slot in the computer and wiring the analog connector.

PROGRAMMING

Programming of this analog I/O board is easily accomplished since the channel selection location is treated as a memory location. Any memory reference instruction can be used.

ANALOG OUTPUTS

One memory location is used for each analog output. The data written to those locations is transferred to the D/A converter. A single STA instruction may be used to load the accumulator contents to one of the D/A converters. A single instruction can also be used to set the inputs of both D/A converters. An STX instruction referenced to DAC1 will load the 8 most significant bits of the index register into DAC1 and the 8 least significant bits of the index register into the DAC2. DAC1 is located at 95F2 and DAC2 at 95F3.

ANALOG INPUTS

Two memory locations are required to input analog data. Conversion is started by writing the channel address to location 95F0. The converted data is read from a second location, 95F1. The analog input system may be operated with or without halting the CPU or in the interrupt mode.

Halt Mode - The normal operation of this board halts the CPU during the conversion time of the analog input

MECHANICAL CHARACTERISTICS

Compatible with Micromodule and EXORciser card spacing.

Minimum card spacing: 12.7mm (0.5").

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers (SAE-43D/1-2).

50 pin analog edge connectors on board.
A mating connector is available from Burr-Brown: 2250MC (Viking # 3VH25/1JN5, solder tab). A Scotchflex connector is available from 3M: 3415-0001.

NOTES:
(1) Connected at the factory for ±5V range (ADC range = ±10V, Gain = 2).
(2) FSR is Full Scale Range (i.e., 10V for ±5V range).
(3) DC to 60 Hz with 1 kΩ source unbalance.
(4) Connected at the factory for ±10V range.
(5) Connected at the factory as 8 differential.
(6) Connected at the factory as 32 differential.

system. The software in this mode is simpler than in any other. To start a conversion, write the channel number into location 95F0. This is followed by a NOP to provide a safe location for the program to halt. The next instruction should read location 95F1. Thus, when conversion is complete and the CPU goes out of the halt state, the converted data will be automatically read. These instructions will read channel 7:

```
LDAA   #$07    Loads channel number (07) to
               accumulator A.
STAA   $95F0   Writes channel number to MP7400
NOP            Allows MP7400 to halt CPU
LDAA   $95F1   Loads converted data from channel
               7 to accumulator A.
```

Polling Mode - The MP7400 may be operated with the halt disabled. Table I shows the jumpers required. When making a change, first remove those jumpers indicated for the present mode and replace them with the jumpers required for the desired mode. As in the Halt Mode the conversion is started by writing the channel number into location 95F0. Continue with sufficient other software for completion of conversion (44 to 84 microseconds) then read the converted data from location 95F1. A status bit may be read from location 95F0 (bit D7). When conversion is complete and the data at location 95F1 is current, the status bit will be zero. During conversion the status bit is one. These instructions will read a channel at location 30.

```
      LDAA   #30     Loads channel number 30 into
                     accumulator
      STAA   $95F0   Writes channel number to MP7400

                     Other software

STAT  LDAA   $95F0   Load status bit to accumulator
      BMI    STAT    Check for status bit = 0
      LDAA   $95F1   Load accumulator with converted
                     data when status bit = 0.
```

Interrupt Mode - The MP7400 maybe operated in the interrupt mode by connecting jumpers as shown in Table I. When making a change, first remove those jumpers indicated for the present mode and replace them with the jumpers required for the desired mode. In this mode as before, a conversion is started by writing the channel number into location 95F0. The program may then continue. When conversion is complete and the current data is available at location 95F1, the MP7400 will interrupt and the status bit will go to a one. When the converted data is read, the status bit will go to zero. The software to read a channel in the Interrupt Mode is very similar to that shown for the Polling Mode. The main differences are a BPL instruction is used instead of a BMI and the status check is part of the interrupt service routine.

HALT MODE	POLLING MODE	INTERRUPT MODE
JP37, JP39, JP41, JP42	JP37, JP39, JP41	JP27, JP36, JP40, JP43

TABLE I. Program Mode Selection Jumpers

DATA REPRESENTATION

The voltage data for these boards are typically represented by two's complement binary numbers for bipolar operation and straight binary for unipolar operation. Refer to the Input or Output Range Selection sections for a more thorough discussion.

The value of a least significant bit (LSB) of data is dependent upon the range of the input or output selected. This value can be determined by dividing the full scale range (see Tables V and VII) by 256.

ADDRESS MODIFICATION

The base address of a board can be set to any value by properly jumpering its address selector (see Table II). The most significant 8 bits of the address (A8-A15) are jumpered to read 95 on all boards. A15-A13 use wire jumpers. A12-A8 use plated-through jumpers. The plated-through addresses can be changed by first drilling out the hole that makes the connection (Figure 1) and then soldering a wire jumper between the bit and logical zero or one. A 0.055" (No. 54) drill should be used for this purpose. Caution must be exercised to prevent damage to the board and the scattering of metal particles over its surface.

For address lines A4 through A7 both address select jumpers are installed at the factory, therefore each line responds to a one in the address. To change these settings, clip the appropriate jumpers for each line. All four lines must be set even if only one line needs changing. Address lines A2 and A3 are set to respond to a zero in the address. When the jumpers which correspond to these lines are cut they will respond to a one unless otherwise programmed by the AS0 and AS1 lines. These address select lines allow the address of the board to be externally programmed.

ADDRESS	1	0
2	Remove JP44	JP44
3	Remove JP45	JP45
4	JP63	JP64
5	JP61	JP62
6	JP59	JP60
7	JP57	JP58
8	W8*	JP56
9	JP55	W7*
10	W6*	JP54
11	JP53	W5*
12	W4*	JP52
13	JP50	JP51
14	JP48	JP49
15	JP46	JP47

* Plated-Through Jumpers.

TABLE II. Address Jumpers

ANALOG OUTPUT RANGE SELECTION

When included, each DAC is jumpered at the factory for ±10 volt operation (two's complement coding). However,

it is possible to alter the jumpers shown in Table III for other output voltages and coding. When making a change, first remove those jumpers indicated for the present range and replace them with those jumpers required for the desired range.

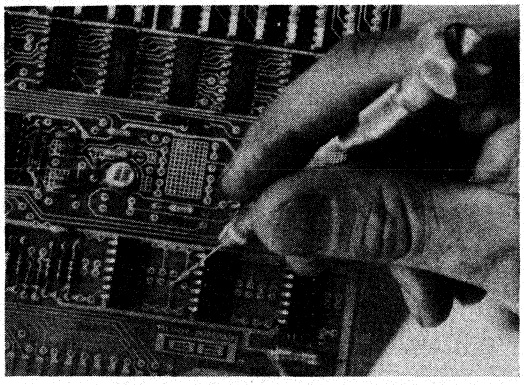


FIGURE 1. Drilling Out Plated-Through Holes

RANGE	DAC 1	DAC 2
±10 ±5 ±2.5 0 to +10 0 to +5	JP1, JP4 JP2, JP4 JP2, JP3, JP4 JP2, JP5 JP2, JP3, JP5	JP6, JP9 JP7, JP9 JP7, JP8, JP9 JP7, JP10 JP7, JP8, JP10
CODING		
TWO'S COMPLEMENT STRAIGHT BINARY	JP24 JP23	JP26 JP25

TABLE III. Analog Output Range Selection

Two's complement coding is typically used for bipolar ranges and straight binary for unipolar ranges, but either coding can be used for any range. The coding used for a particular DAC can be determined by the jumpers shown in Table III.

RANGE	JUMPERS
±10V	JP17, JP19
±5V	JP16, JP19
±2.5V	JP16, JP18, JP19
0 to +10V	JP16, JP20
0 to +5V	JP16, JP18, JP20

TABLE IV. A/D Converter Range Setting Jumpers

ANALOG INPUT RANGE SELECTION

The analog input system can be set for any range between ±5V and ±5mV. It is set for ±5V (two's complement coding) at the factory. There are two gain determining elements in the system: the A/D converter and the instrumentation amplifier (IA). The A/D converter is set for a ±10V range and the IA for a gain of 2 at the factory. The A/D converter can be set for other ranges simply by changing jumpers as shown in Table IV. Before adding new jumpers, remove those indicated for the present range. The input voltage presented to the analog multiplexer must not exceed 5.25VDC for proper operation.

BIPOLAR - TWO'S COMPLEMENT			
Digital Input Output	±10V	±5V	±2.5V
01111111 ($7F_{16}$) 10000000 (80_{16})	+9.922V -10.000V	+4.961V -5.000V	+2.480V -2.500V
UNIPOLAR - STRAIGHT BINARY			
Digital Input/Output	0 to +10V	0 to +5V	
11111111 (FF_{16}) 00000000 (00_{16})	9.961V 0.000V	4.980V 0.000V	

TABLE V. Analog Full Scale Range Values.

As configured at the factory, this board is jumpered for two's complement operation (see Table V above) with jumper JP21 inserted and JP22 open. For operation in the straight binary mode (any range) jumper JP21 is open and JP22 is inserted.

ANALOG INPUT LOW LEVEL OPERATION

Pads for external gain setting resistors (see Figure 2) have been provided so that the instrumentation amplifier can be user set for gains to 1000. When low level signals are to be processed the lowest system noise is attained when the ADC range is set on the ±10V or 0 to 10V ranges with the amplifier providing all the system gain. The following formula can be used to calculate the value of the resistance: Gain = $100k\Omega/R_{EXT}$, where R_{EXT} is the resistance between pins 1 and 4 of the IA (R17, 18 in parallel form R_{EXT} in Figure 2). The gain adjustment potentiometer on the board will give an adjustment range of ±1%. Therefore, if an R_{EXT} with an accuracy of ±0.5% is used, the on-board potentiometer will have sufficient range for adjustment. Stable (50ppm) resistors should be used in this application. As shipped from the factory, R17 = 49.9kΩ for an amplifier gain of two.

The settling time of the amplifier increases as the gain increases. A delay time of 41 microseconds is set at the factory to allow for multiplexer and amplifier setting times. This delay time is sufficient for amplifier gains of up to 50. For gains larger than 50, a longer delay time is required. A delay time of 81 microseconds will be obtained by removing R4. This delay time is sufficient for gains of up to 1000.

SINGLE-ENDED, DIFFERENTIAL OPERATION

A board can be converted from single-ended operation to differential operation or vice versa by simply changing a few board jumpers. Table VI indicates those jumpers that must be present for a given mode of operation. To convert from one mode to the other remove those jumpers

8 Channel Differential	16 Channel Single-ended	32 Channel Differential	64 Channel Single-ended
JP11, JP13, JP31	JP12, JP14 JP29, JP30	JP31, JP33	JP15, JP29, JP30

TABLE VI. Channel Conversion

indicated for the present type of operation and install those necessary for the desired mode of operation.

The differential mode of operation should be used for analog signals in noisy environments. The differential mode is particularly useful for low level signals (less than one volt) since they are more prone to noise than high level signals. This board can also operate in a pseudo-differential mode. In this mode the system has the number of channels of the single-ended mode, but the inverting input of the IA is connected to a remote common (via pin 49 connector P-2) rather than grounded on the board. This mode of operation is useful if there is a remote ground common to all the input signals. In this way the advantages of single-ended operation (maximum number of channels) and differential operation (better noise rejection) are combined. Jumpers JP28 and JP30 are installed and JP29 or JP31 is removed for this mode of operation.

ANALOG OUTPUT CHECKOUT

A static check of the two analog outputs is very simple. Load the upper half of the index register with the DAC 1 data word and the lower half with the DAC 2 data word. An STX instruction can then be used to transfer the data to the DAC's. The addresses of the analog outputs are set at the factory to values of $95F2_{16}$ and $95F3_{16}$. The ideal values for plus and minus full scale are shown in Table VII.

DATA WORD	RANGE				
	±2.5V	±5.0V	±10V	0 to +5V	0 to +10V
80_{16}	-2.500	-5.000	-10.000		
$7F_{16}$	+2.480	+4.961	+9.922		
00_{16}				0.000	0.000
FF_{16}				+4.980	+9.961

TABLE VII. DAC Full Scale Values

Two's complement coding is shown for bipolar ranges; straight binary for unipolar ranges.

To check the dynamic characteristics of the analog outputs the following program can be used.

```
0150                    ORG     $0150
0150 CE 95F2            LDX     #$95F2   Initialize index reg.
0153 86 7F              LDA A   #$7F     Initialize reg. A
0155 A7 00      LOOP    STA A   X        Write into DAC1
0157 08                 INX
0158 A7 00              STA A   X        Write into DAC2
015A 09                 DEX
015B 43                 COM A            Compliment Data
015C 20 F7              BRA     LOOP     and begin again
                        END
```

A 19 kHz square-wave will be present on both DAC outputs.

ANALOG INPUT CALIBRATION

These systems are set at the factory for a ±5V input range. If the input system range is to be changed or eventually needs to be calibrated, the following program may be used to adjust gain and offset.

```
                ORG     $100
STACK   EQU     $037F
MP74C   EQU     $95F0
MP74D   EQU     $95F1
REF     EQU     $80              Ref = 80 for
*                                offset, 7F for gain
0100 8E 037F            LDS #STACK       Set stack pointer
0103 C6 64      START   LDAB #100        Initialize conversion
                                         counter
0105 4F                 CLRA             Clear # of true
                                         conversions counter
0106 B7 011F            STAA COUNT
0109 4F         RLOOP   CLR A            Start conversion
010A B7 95F0            STAA MP74C
010D 01                 NOP
010E B6 95F1            LDAA MP74D       Read data
0111 81 80              CMPA #REF        If data = ref increment
                                         count
0113 26 03              BNE SINC
0115 7C 011F            INC COUNT
0118 5A         SINC    DEC B
0119 26 EE              BNE RLOOP        Continue if 100
                                         conversions completed
011B 8D 03              BSR PRINT        If finished print count
011D 20 E4              BRA START
011F 0001       COUNT   RMB 1
                *
                *Use this routine with Micromodule monitor
                *
0120 CE 011F PRINT      LDX #COUNT       Print count
0123 BD FD98            JSR $FD98
0126 86 0D              LDAA #$0D        Print a carriage return
                                         and line feed
0128 BD FD26            JSR $FD26
012B 86 0A              LDAA #$0A
012D BD FD26            JSR $FD26
0130 39                 RTS
                        END
                *
                *Use this routine with the EXORcisor
                *
0120 B6 011F PRINT      LDA A   COUNT    Load A with count
0123 44                 LSR A            Print count MSbyte
0124 44                 LSR A
0125 44                 LSR A
0126 44                 LSR A
0127 8D 10              BSR     PAR
0129 B6 011F            LDA A   COUNT
012C 84 0F              AND A   #$0F     Print count LSbyte
012E 8D 09              BSR     PAR
0130 86 0D              LDA A   #$0D     Print a carriage return
0132 8D 0E              BSR     TOC
0134 86 0A              LDA A   #$0A     Print a line feed
0136 8D 0A              BSR     TOC
0138 39                 RTS
0139 8B 90      PAR     ADD A   #$90     Convert A to ASCII hex
013B 19                 DAA
013C 89 40              ADC A   #$40
013E 19                 DAA
013F 8D 01              BSR     TOC      Print character
0141 39                 RTS
0142 F6 FCF4 TOC        LDA B   $FCF4
0145 C5 02              BIT B   #2
0147 27 F9              BEQ     TOC
0149 B7 FCF5            STA A   $FCF5
014C 39                 RTS
                        END
```

This program may be used for both offset and gain calibration. The system offset should be adjusted first, followed by the gain adjustment.

The base address of the board is assumed to be 95F0. If it is not, the STAA and LDAA instructions should reflect that change. The reference values assume two's complement binary coding, Offset Ref = 80 and Gain/Full Scale Ref = 7F. For binary coding, Offset Ref = 0 and Gain/Full Scale Ref = FF.

A G 0100 command to the Micromodule monitor or a 100;G command to EXbug will begin program execution. After 100 conversions have been made a two digit hex number will be printed on the terminal. This value represents the number of times the data read from the board was equal to "REF" (80_{16} for offset, $7F_{16}$ for gain). The program will continue to convert and print until a reset is performed.

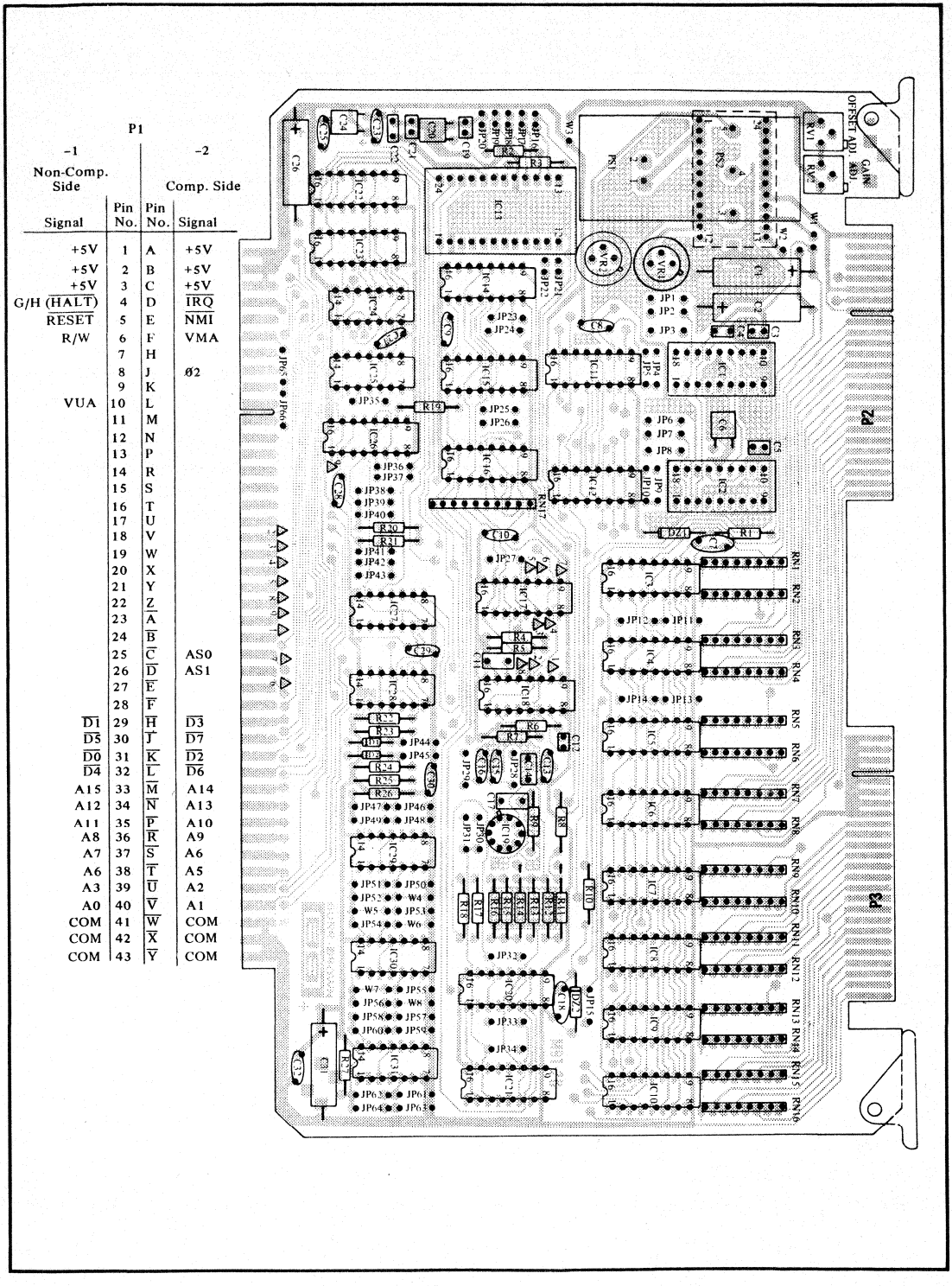


FIGURE 2. MP7400 Series Board Layout

RANGE	OFFSET	GAIN
±5V	-4.980	+4.941
0 to +10	+19.53mV	+9.941
0 to +5	+9.766mV	+4.971

TABLE VIII. Analog Input Calibration Values

Calibration is performed by connecting a voltage source capable of 0.1% accuracy to input channel zero (this could also be a DC voltage source of less absolute accuracy whose output is monitored by 0.1% DVM).

The offset and gain adjustments are made while applying the voltage shown in Table VIII. For other ranges, the offset voltage adjustment is made at the most negative value of the range less one-half least significant bit (LSB). An LSB is equal to the span (full scale range) divided by 256 for 8 bit resolution. The gain adjustment is made at the most positive value of the range less 1-1/2 LSB. Thus for a range of ±50mV, an LSB is 100mV/256 = 391μV. The offset adjustment is made at -50mV + 195μV = -49.80mV and the gain adjustment at +50mV -586μV = 49.41mV. Before making these adjustments, however, the unit should be allowed to reach thermal equilibrium (about 30 minutes under power).

The offset adjustment is made first by using the appropriate offset calibration voltage. Run the calibration program and adjust the on board offset potentiometer until the output value is between $1E_{16}$ and 46_{16} (30_{10} and 70_{10}).

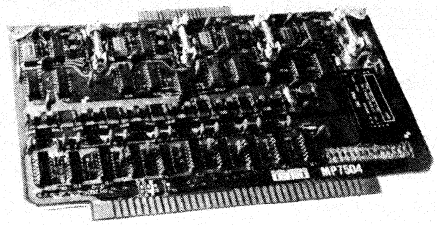
To perform the gain adjustment change the data labeled "REF" in the calibration program from 80 to 7F, set the input voltage to the correct value as shown in Table VIII and adjust the on board pin gain potentiometer in the same manner as described for offset.

ANALOG INPUT/OUTPUT PIN CONNECTIONS

8 Channels P-2				32 Channels P-2				32 Channels P-3			
Digital GND	1	2	Digital GND	Digital GND	1	2	Digital GND		1	2	
+15	3	4	+15	+15	3	4	+15		3	4	
-15	5	6	-15	-15	5	6	-15		5	6	
Analog GND	7	8	Analog GND	Analog GND	7	8	Analog GND	Digital	7	8	Digital
Analog Out 1	9	10	AO Return 1	Analog Out 1	9	10	AO Return 1	Ground	9	10	Ground
Digital GND	11	12	Digital GND	Digital GND	11	12	Digital GND		11	12	
Analog Out 2	13	14	AO Return 2	Analog Out 2	13	14	AO Return 2		13	14	
Digital GND	15	16	Digital GND	Digital GND	15	16	Digital GND		15	16	
RET0/IN8	17	18	IN0	RET0/IN32	17	18	IN0	RET16/IN48	17	18	IN16
RET1/IN9	19	20	IN1	RET1/IN33	19	20	IN1	RET17/IN49	19	20	IN17
RET2/IN10	21	22	IN2	RET2/IN34	21	22	IN2	RET18/IN50	21	22	IN18
RET3/IN11	23	24	IN3	RET3/IN35	23	24	IN3	RET19/IN51	23	24	IN19
RET4/IN12	25	26	IN4	RET4/IN36	25	26	IN4	RET20/IN52	25	26	IN20
RET5/IN13	27	28	IN5	RET5/IN37	27	28	IN5	RET21/IN53	27	28	IN21
RET6/IN14	29	30	IN6	RET6/IN38	29	30	IN6	RET22/IN54	29	30	IN22
RET7/IN15	31	32	IN7	RET7/IN39	31	32	IN7	RET23/IN55	31	32	IN23
	33	34		RET8/IN40	33	34	IN8	RET24/IN56	33	34	IN24
	35	36		RET9/IN41	35	36	IN9	RET25/IN57	35	36	IN25
	37	38		RET10/IN42	37	38	IN10	RET26/IN58	37	38	IN26
	39	40		RET11/IN43	39	40	IN11	RET27/IN59	39	40	IN27
NC	41	42	NC	RET12/IN44	41	42	IN12	RET28/IN60	41	42	IN28
	43	44		RET13/IN45	43	44	IN13	RET29/IN61	43	44	IN29
	45	46		RET14/IN46	45	46	IN14	RET30/IN62	45	46	IN30
	47	48		RET15/IN47	47	48	IN15	RET31/IN63	47	48	IN31
Remote Common	49	50	Digital GND	Remote Common	49	50	Digital GND	Digital GND	49	50	Digital GND

MP7408	8-channel differential analog input system (may be connected as 16 channels single-ended)	
MP7408-AO	MP7408 with two channel analog output	
MP7408-NS	MP7408 without DC/DC converter	
MP7408-NS-AO	MP7408-NS with two channel analog output	
MP7432	32-channel differential analog input system (may be connected as 64-channel single-ended)	
MP7432-AO	MP7432 with two channel analog output	
MP7432-NS	MP7432 without DC/DC converter	
MP7432-NS-AO	MP7432-NS with two channel analog output	
2250MC	Analog connector: one required for 8/16 channel units; two required for 32/64 channel units	

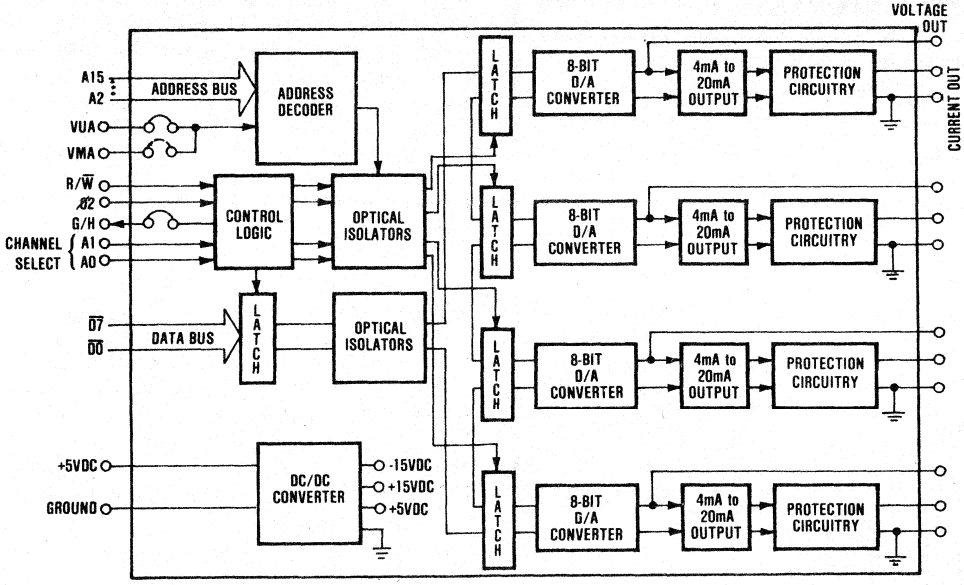
BURR-BROWN



MP7504

MICROCOMPUTER ANALOG OUTPUT SYSTEM

A 4-CHANNEL, 8-BIT ISOLATED ANALOG OUTPUT SYSTEM COMPATIBLE WITH MOTOROLA MICROMODULE AND EXORciser® MICROCOMPUTERS



FEATURES

- OUTPUT ISOLATION/OUTPUT PROTECTION
- REDUCES SYSTEM DEVELOPMENT TIME
  - System engineered and specified
  - Plug compatible
  - Operates from computer power supply
  - Easy to program
- MOTOROLA MICROMODULE AND EXORciser® COMPATIBLE
- 4-CHANNEL ANALOG OUTPUT SYSTEM
- 4mA TO 20mA OUTPUT
- 70°C BURN-IN

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PDS-385 Printed in U.S.A. July, 1978

DESCRIPTION

This microcomputer peripheral, burned in at 70°C to increase reliability and reduce aging shift, provides four optically isolated 8 bit fused analog outputs that interface directly with Motorola's Micromodule and EXORciser microcomputers. The MP7504, electrically and mechanically compatible with these MPU's, is contained on a single printed circuit board that operates from the computer's +5 VDC power supply. Analog interface is through a card edge (direct) connector located on the opposite edge of the board from the bus connector.

The MP7504 which outputs 4-20mA and 0-10 volts on each channel is programmed as memory locations. The address block used by each peripheral is selectable and can be placed anywhere in memory. A single instruction sets the input of a D/A converter.

SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ELECTRICAL

ANALOG OUTPUT	
Number of analog outputs	4
Output current range	4-20mA
Maximum load	400 ohms
Compliance	8 volts
Output settling time	50 μsec
Output voltage range	0 - 10V at 5mA
Output impedance	1 ohm
Output settling time	30 μsec
TRANSFER CHARACTERISTICS	
Resolution	8 bits binary
One LSB (voltage)	39.1mV
(current)	62.5 μA
Throughput accuracy, max	±0.4% of FSR
Temperature coefficient of accuracy	
Voltage output	±50ppm of FSR/°C
Current output	±150ppm of FSR/°C
ISOLATION	
Isolation voltage between Microcomputer bus and outputs	600 VDC
DIGITAL INPUT/OUTPUT	
All signals compatible with Microcomputer bus	
Logic loading (all inputs)	One LSTTL load
Analog output channels selected by:	A0, A1
Input data read by:	$\overline{D0}$ - $\overline{D7}$
POWER REQUIREMENTS	
Rated voltage	+5 VDC
Range for rated accuracy	4.75 to 5.25 VDC
Supply drain at 5 VDC	1.2A, typical; 1.8A max
TEMPERATURE RANGE	
Operating	0°C to 70°C

TABLE I. Electrical Specifications

MECHANICAL

Compatible with Micromodule and EXORciser card spacing.

Minimum card spacing: 12.7mm (0.5").

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers (SAE-43D/1-2).

Analog Connector: 50-pin output P.C.B. edge connector. A mating connector is available from Burr-Brown:

2250MC (Viking # 3 VH25/1JN5, solder tab).

A Scotchflex connector (3415-0001) is available from 3M.

OPERATING INSTRUCTIONS

PROGRAMMING

Because this analog output board is treated as memory, programming is simple. The MP7504 uses any memory reference instruction that can write data from the CPU.

Each board is factory set for a block of addresses beginning at 94FC. Each analog data channel requires one memory location. When a data word is written to the MP7504 it is stored in an input latch. The optical isolators following the input latch require 15 microseconds to transfer new data to the D/A converter latches. Do not write to the board during this transmission period. To insure proper operation, use one of these modes:

1) HALT mode (shipped in this mode):

Jumper W33 is installed. The conversion command (write instruction) is followed with a NOP instruction. In this mode, the board halts the processor during data transfer sequences. For example:

STAA 94FE	Transfers data in accumulator to MP7504 for channel 2.
NOP	Allows MP7504 to halt processor for 15 microseconds during transfer of data to channel 2.

2) COUNT DOWN mode

Jumper W33 is removed. Software control does not permit the program to write to the board for 15 microseconds. For example:

STAA 94FE	Transfers data in accumulator to MP7504 for channel 2.
• • •	{ System software does not allow another write to the MP7504 for 15 microseconds.

CHANNEL	FACTORY SET LOCATION
0	94FC
1	94FD
2	94FE
3	94FF

TABLE II. Analog Output Channel Locations.

ADDRESSING

The board address is determined by the state of jumpers W2 to W29. Jumper pairs control one input to each two-input quad exclusive-or gate. These 14 exclusive-or gates comprise the address decoder. An address is valid on the address bus when its complement appears at the jumpers.

The MP7504 as shipped from the factory occupies addresses 94FC to 94FF. The most significant byte of the address (94) is set by jumpers W2 - W17 at the factory. The address may be changed by removing and replacing jumpers as shown in Table III. For example, changing the most significant byte from 94 to 92 requires removal of jumpers W11 and W14 and installation of jumpers W10 and W15.

ADDRESS BIT	FACTORY SET	INSERT JUMPER FOR ADDRESS "1"	"0"
A15	1	W5	W4
A14	0	W3	W2
A13	0	W7	W6
A12	1	W9	W8
A11	0	W13	W12
A10	1	W11	W10
A9	0	W15	W14
A8	0	W17	W16

TABLE III. Address Modification, A8 through A15.

Jumpers W18 to W29 control the least significant byte of the address. These jumpers, installed at the factory, pull all jumper inputs low. Initially, the binary address is 1001 0100 1111 $11A_1A_0$ where A_0 and A_1 are used to select the output channels.

To change the least significant address byte, clip one, and only one jumper from each set of jumpers (W18, W19... W22, W23, etc.) as shown in Table IV. For example, to change the board address to 1001 0100 1100 $00A_1A_0$, clip W18, W22, W25, W21, W27 and W29. The board address may, by clipping jumpers, vary from 9400 to 94FF for a possible 1536 output channels.

ADDRESS BIT	FACTORY SET	CLIP FOR "HIGH" (1) ADDRESS	CLIP FOR "LOW" (0) ADDRESS
A7	1	W18	W19
A6	1	W22	W23
A5	1	W24	W25
A4	1	W20	W21
A3	1	W26	W27
A2	1	W28	W29
NOTE: One, and only one, jumper must be removed for each address line when changing A2 - A7.			

TABLE IV. Address Modification, A2 through A7.

OUTPUT RANGES

Each DAC (digital/analog converter) provides a 0 to +10V and a 4-20mA output. Input coding is straight binary. Table V lists input codes and output values. The current outputs are designated I and the voltage outputs V for each output channel on the pin connection table (page 6-72). As indicated in Figure 1 the load should be connected between the I output and any COMM pin.

DIGITAL INPUT CODES		OUTPUT RANGE VOLTAGE 0 to +10V	OUTPUT RANGE CURRENT 4 to 20mA	Defined As:
MSB	LSB			
1111	1111	+9.961V	+19.938mA	+Full Scale
1000	0000	+5.000V	+12.000mA	Mid Scale
0111	1111	+4.961V	+11.938mA	Mid Scale -1 LSB
0000	0000	0.000V	4.000mA	Zero
One LSB		39.1mV	0.063mA	$\frac{FSR}{2^n}$, n = 8

TABLE V. Input Codes/Output Values

OUTPUT PROTECTION AND DRIVE CAPABILITY

Each 4-20mA output is protected from shorts to AC line voltages by the circuit shown in Figure 1. Loads up to 400 ohms can be driven with the on-board isolated power supply. The output can drive up to 500 ohms if the protection fuse is by-passed with a jumper (W39 - W42).

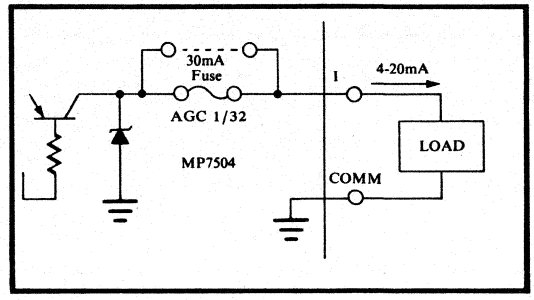


FIGURE 1. Output Circuitry and Connections.

ANALOG OUTPUT CHECKOUT

It is easy to perform a static check of the four analog outputs: After loading the accumulator with the data word, use an LDA instruction to transfer the data to each DAC in turn. Addresses of the analog outputs are set at the factory to values of 94FC to 94FF. Ideal values for plus full scale and zero are listed in Table V.

Use the following program to check dynamic characteristics of the analog outputs.

```
0100                    ORG     $0100
0100 86 FF              LDA A   #$FF        INITIALIZE REG A
0102 CE 94FC            LDX     #$94FC      INITIALIZE INDEX REG
0105 A7 00      LOOP    STA A   0,X         WRITE TO DAC 1
0107 01                 NOP
0108 A7 01              STA A   1,X         WRITE TO DAC 2
010A 01                 NOP
010B A7 02              STA A   2,X         WRITE TO DAC 3
010D 01                 NOP
010E A7 03              STA A   3,X         WRITE TO DAC 4
0110 01                 NOP
0111 43                 COM A               COMPLEMENT DATA
0112 20 F1              BRA     LOOP        BEGIN AGAIN
                        END
```

A 6kHz (approximately) square wave (0 to 10V or 4 to 20mA) wil be present on all DAC outputs.

JUMPER DESCRIPTIONS

W2 - W29 These jumpers select the board address. A pair of jumpers determine the address for each address line. See Table III and IV.

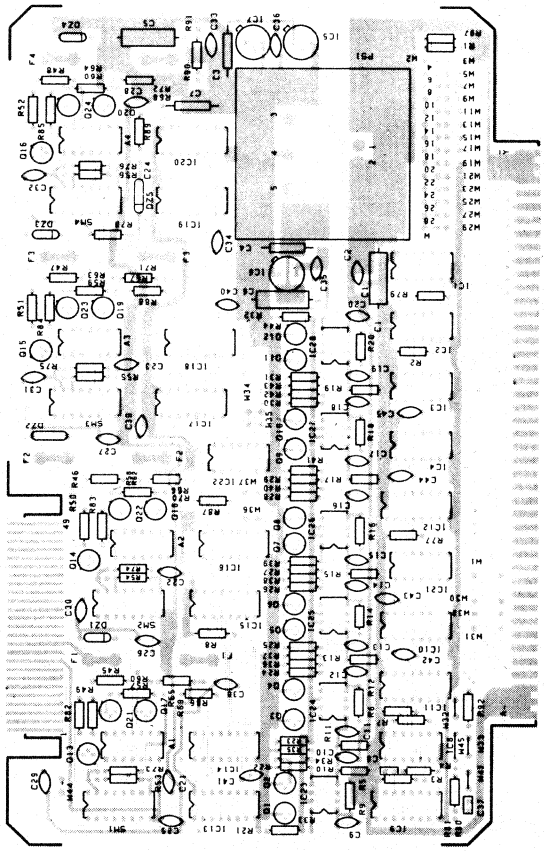
W30 - W31 Jumper W30 is inserted at the factory to allow for VUA input (pin 10). W30 may be removed and W31 installed to permit VMA input (pin F).

W33 Jumper inserted at factory to allow for HALT mode of operation. See Programming Section, page 6-70.

W39 - W42 These jumpers are not factory installed. They are used only to by-pass the output fuse protection and thereby increase the output compliance.

ANALOG OUTPUT PIN CONNECTIONS

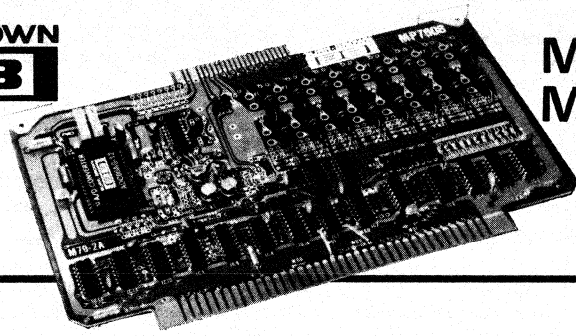
Component Side	MP7504 Pin No.		Non-Component Side
N.C	1	2	N.C
N.C	3	4	N.C
+15V	5	6	+15V
COMM	7	8	COMM
COMM	9	10	COMM
6.3V	11	12	COMM
COMM	13	14	COMM
N.C	15	16	N.C
-15V	17	18	15V
V1	19	20	COMM
I1	21	22	COMM
V2	23	24	COMM
I2	25	26	COMM
V3	27	28	COMM
I3	29	30	COMM
V4	31	32	COMM
I4	33	34	COMM
	35	36	
	37	38	
	39	40	
N.C	41	42	N.C
	43	44	
	45	46	
	47	48	
	49	50	



COMPONENT SIDE	P1 PIN		NON-COMPONENT SIDE
COMM	Y	43	COMM
COMM	X	42	COMM
COMM	W	41	COMM
A1	V	40	A0
A3	U	39	A3
A5	T	38	A4
A6	S	37	A7
A9	R	36	A8
A10	P	35	A11
A13	N	34	A12
A14	M	33	A15
$\overline{D6}$	L	32	$\overline{D4}$
$\overline{D2}$	K	31	$\overline{D0}$
$\overline{D7}$	J	30	$\overline{D5}$
$\overline{D3}$	H	29	$\overline{D1}$
	G	28	
	F	27	
	E	26	
	D	25	
	C	24	
	B	23	
	A	22	
	Z	21	
	Y	20	
	X	19	
	W	18	
	V	17	
	U	16	
	T	15	
	S	14	
	R	13	
	P	12	
	N	11	
	M	10	VUA
	L	9	
	K	8	
Ø2	J	7	
VMA	H	6	R/$\overline{W}$
	F	5	
	E	4	G/$\overline{H}$
+5V	D	3	+5V
+5V	C	2	+5V
+5V	B	1	+5V
	A		

FIGURE 2. MP7504 Board Layout, Top View.

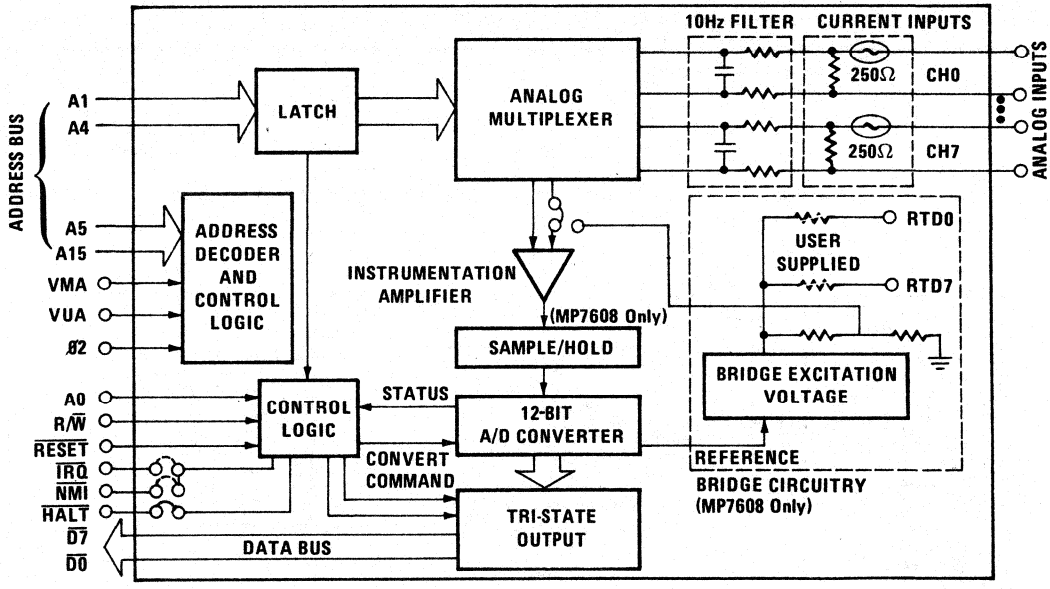
BURR-BROWN



MP7608
MP7608-I

MICROCOMPUTER ANALOG INPUT SYSTEMS

A 12-BIT, 8-CHANNEL "INDUSTRIAL" ANALOG INPUT SYSTEM COMPATIBLE WITH MOTOROLA MICROMODULE AND EXORciser® MICROCOMPUTERS



FEATURES

- CURRENT-LOOP INPUTS
- HIGH OR LOW LEVEL VOLTAGE INPUTS
- INPUTS PROTECTED TO 200VDC
- CURRENT INPUTS FUSED
- IMMUNE TO NOISE
  Input filter on each channel
  Differential inputs
- BRIDGE INPUTS
- 70°C BURN-IN

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PDS-380 Printed in U.S.A. July, 1978

DESCRIPTION

The MP7608 and MP7608-I are analog input microperipheral boards designed to be used with Motorola's Micromodule and EXORciser microcomputer systems. They are electrically and mechanically compatible with Motorola microcomputers. Each analog system is contained on a single printed circuit board that is treated as memory by the CPU. The analog interface for each system is at a connector at the opposite edge of the board from the bus connector.

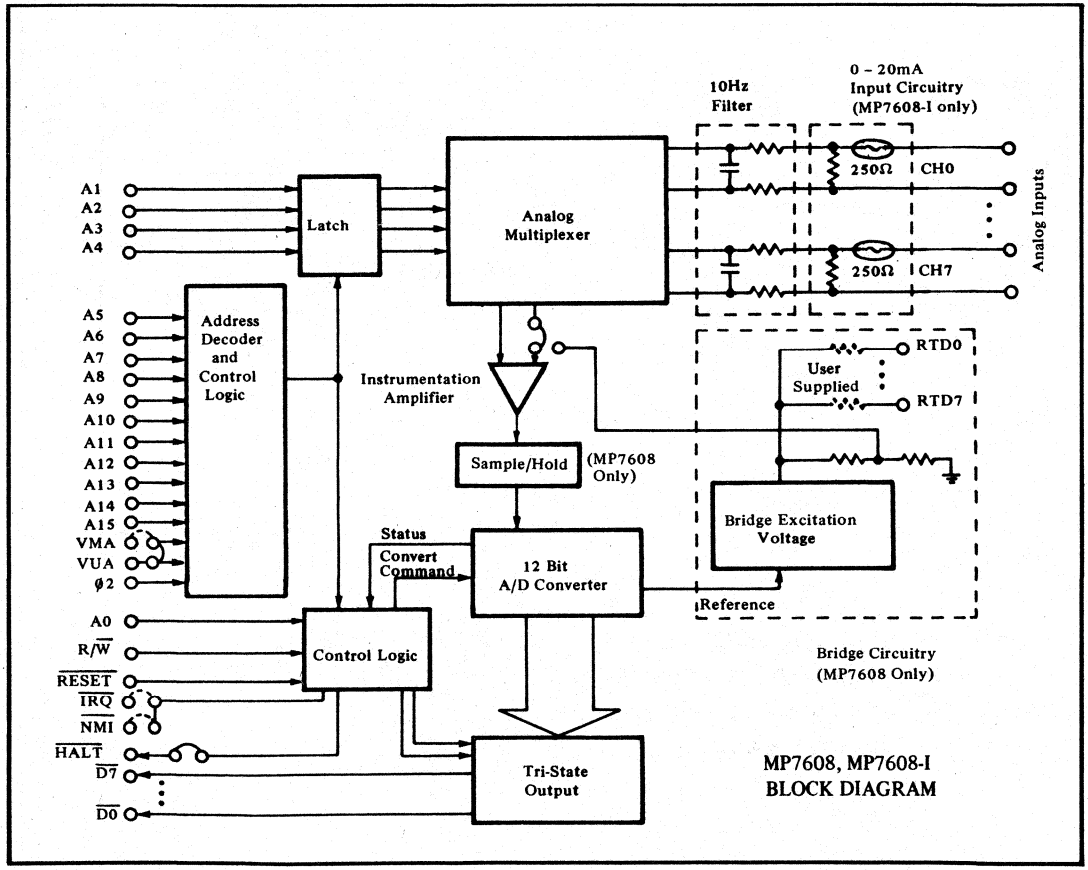
These data acquisition systems include 200V input overvoltage protection, an input filter, analog multiplexer, high gain instrumentation amplifier, sample/hold and 12 bit A/D converter along with all the necessary timing, decoding and control logic. They operate from the microcomputer's +5VDC and ±12VDC power supplies.

The MP7608 is a voltage input system capable of interfacing ±10mV to ±5V signal levels. Excitation and bridge circuitry is also included on this board for interface to sensors such as RTD's and strain gages. The MP7608-I is a current input system designed to interface to 4-20mA current loop signals. The MP7608-I also includes input fuses to protect the 250Ω precision input current resistors.

THEORY OF OPERATION

When programming with these peripherals, they are treated as memory locations. The A/D converter output is a 12 bit word so two 8 bit memory locations are needed for each channel. Address bits A15-A5 select the board and A4-A1 select the analog input channel to be digitized. To start a conversion the board is written to using an STA or similar instruction. The data remains in the output latches waiting to be read until another conversion is initiated. These peripherals may be used with or without halting the CPU or in the interrupt mode.

The MP7608/MP7608-I are jumpered at the factory with the first channel at address $93E0_{16}$, the second at $93E2_{16}$, etc. By changing jumpers, the boards may be placed anywhere in memory.



SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ELECTRICAL

ANALOG INPUT	MP7608-I	MP7608
Number of analog inputs	8 differential[1]	8 differential[1]
Input range	0-20mA[2]	±10mV to ±5V[3]
ADC gain ranges (strap selectable)	±10V, 0 to 10V, 0 to 5V, ±5V, ±2.5V	±10V, 0 to 10V, 0 to 5V, ±5V, ±2.5V
Amplifier gain range	1 to 500	1 to 500
Factory set gain	1	1[5]
Amplifier gain equation (resistor programmable)	$G = 1 + 20k\Omega/R_{EXT}$	$G = 1 + 20k\Omega/R_{EXT}$
Input overvoltage protection	±200V	±200V
Input filter	One pole RC, 10Hz	One pole RC, 10Hz
Input impedance, DC	250Ω	100 megohms
Bias current		
25°C	20nA	7nA
0 to 70°C	50nA	10nA
Amplifier output noise (Gain = 100 R_S = 500Ω)	1.2mV rms; 7mV p-p	0.5mV rms; 3mV p-p
Amplifier input offset voltage, max	400μV	200μV
Amplifier input offset voltage drift, max	2 + 20/G μV/°C	1 + 20/G μV/°C
TRANSFER CHARACTERISTICS		
Resolution	12 bits binary	12 bits binary
Throughput accuracy,		
±5V or 0-20mA range, max	±0.025% FSR[4]	±0.025% FSR[4]
±10mV range	±0.1% FSR	±0.1% FSR
Temperature coefficient of accuracy		
±5V or 0-20mA range, max	±0.004% FSR/°C	±0.004% FSR/°C
±10mV range	±0.01% FSR/°C	±0.01% FSR/°C
Conversion time ±5V or 0-20mA range	60 microseconds	175 microseconds
±10mV range	125 microseconds	525 microseconds
CMRR (for differential inputs)	90dB (DC to 60Hz)	90dB (DC to 60Hz)
DIGITAL INPUT/OUTPUT		
All signals are compatible with Microcomputer bus		
Output coding	unipolar, straight binary	bipolar,[6] two's complement
Logic loading (all inputs)	one LSTTL load	one LSTTL load
Data bus output drive	20 TTL loads	20 TTL loads
$\overline{HALT}$, $\overline{IRQ}$, $\overline{NMI}$ output drive	10 TTL loads	10 TTL loads
POWER REQUIREMENTS		
Power supply voltages	+5VDC at 100mA, +12VDC at 50mA, -12VDC at 75mA	+5VDC at 100mA, +12VDC at 50mA, -12VDC at 75mA
Range for rated accuracy	4.75V to 5.25V and ±11.4V to ±12.6V	4.75V to 5.25V and ±11.4V to ±12.6V
TEMPERATURE RANGE		
Temperature	0 to 70°C	0 to 70°C

(1) May be connected as 16 channels single-ended without input filtering.
(2) May be set up to accept voltage signals.
(3) Connected at the factory for ±5V range.
(4) FSR is Full Scale Range (i.e., 10V for ±5V range, 5V for 0 to +5V range).
(5) Gains of 5 and 100 can be attained by adding jumpers.
(6) Unipolar straight binary is jumper selectable (W80, W81).

OPERATING INSTRUCTIONS

INSTALLATION

The MP7608/MP7608-I are shipped from the factory calibrated and ready for immediate use. Installation requires only plugging the card into any empty slot and connecting the analog signals.

PROGRAMMING

Programming of these analog I/O boards is easily accomplished since all are treated as memory locations. The A/D converter output is a 12 bit word so two 8 bit memory locations are needed for each channel. These boards are jumpered at the factory with a base address of $93E0_{16}$ (the first channel is at $93E0_{16}$, the second at $93E2_{16}$, etc.). To start conversion, write to the board using the correct address. For example, with a base address of $93E0_{16}$ (1001 0011 1110 0000),

```
STAA $93E6
```

may be used to start conversion of channel 3. The data written to the board is irrevelant.

To input the 12 data bits, after conversion is complete, read the board using the base address. For example,

```
LDX $93E0
```

may be used to read the board. This instruction places the most significant byte into the upper half of the Index Register and the least significant byte into the lower half of the Index Register. Address bits A4-A1 are irrelevant. The most significant byte of data is read with a valid address and A0 = 0, the least significant bit with A0 = 1, (Tables I and II). As shipped from the factory, $\overline{D4}$-$\overline{D7}$ are jumpered to the most significant bit (B11) of the 12 bit A/D converter word when reading the most significant byte of data. $\overline{D4}$, $\overline{D5}$ and $\overline{D7}$ may be jumpered for other functions. $\overline{D7}$ may optionally be tied to ground. Thus, with a pull-up resistor elsewhere in the system, $\overline{D7}$ may be read to determine which boards in a system are plugged-in. $\overline{D5}$ may be connected to display the status of the interrupt (0 indicates interrupt active). $\overline{D4}$ may be connected to display the status of the $\overline{HALT}$ output ("1" indicates conversion complete). When making a change, first remove those jumpers indicated for the present mode and replace them with the jumpers required for the desired mode (Table III).

MECHANICAL CHARACTERISTICS

Compatible with EXORciser and Micromodules card spacing.

Minimum card spacing: 12.7mm (0.5")

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers (SAE-43D/1-2).

Analog connector: 50 pin PC edge connector with 0.100" contact centers. Burr-Brown part number: 2250MC (Viking = 3VH25/1JN5 - solder tab). Scotchflex cable connector also available from 3M (# 3415-0001).

Normal Mode	Optional Mode
$\overline{D7}$ = B11	1 (Indicates that board is plugged in)
$\overline{D6}$ = B11	Not used
$\overline{D5}$ = B11	Interrupt Status (0 Indicates active)
$\overline{D4}$ = B11	Halt Status (1 Indicates conversion complete)
$\overline{D3}$ = B11	B11
$\overline{D2}$ = B10	B10
$\overline{D1}$ = B9	B9
$\overline{D0}$ = B8	B8

TABLE I. Most Significant Byte Output (A0 = 0).

$\overline{D7}$ = B7	
$\overline{D6}$ = B6	
$\overline{D5}$ = B5	
$\overline{D4}$ = B4	
$\overline{D3}$ = B3	
$\overline{D2}$ = B2	
$\overline{D1}$ = B1	
$\overline{D0}$ = B0	LSB

TABLE II. Least Significant Byte Output (A0 = 1).

Data Bit	MSB B11	Optional Function
$\overline{D7}$	W70	W66
$\overline{D5}$	W68	W58
$\overline{D4}$	W67	W57

TABLE III. Jumpers for $\overline{D7}$-$\overline{D4}$ Optional Function.

The data from the most recent conversion will remain on the board until a new conversion is initiated by a write instruction to the board.

The board may be read at any time to determine its current status or data. The most significant byte is read with a valid address and A0 = 0.

MODES OF OPERATION

Halt Mode. This is the normal mode of operation as shipped from the factory. Jumper W64 is installed and W24-25 removed. This method allows the board to halt the processor during a conversion and resume program operation after conversion is complete. For this reason a NOP instruction must follow the start of conversion command to provide a halting point for the program. The software in this mode is simpler than in any other. These instructions will read channel 3 at location $93E6_{16}$:

```
STAA   $93E6    Starts conversion
NOP             CPU Halts
LDX    $93E0    Loads converted data to the index
                register
```

Polling Mode. Jumpers W24, 25 and 64 are removed. After a convert command is issued, the program does not read the board during the conversion time (60 or 175 microseconds). To assure that the conversion has been completed, the status bits should be interrogated. These instructions will read channel 4 at location 93E6:

```
STAA   $93E6 Starts Conversion
 •
 •     }      Other software for the conversion
 •     }      time
CC LDAA   $93E0 Load MSB of data (with status
                bit in D4) to accumulator
   BITA   #$10  Is status bit set?
   BEQ    CC
   LDX    $93E0 Yes. Load data word to index
                register
```

Interrupt Mode. Jumper W64 is removed and W24 or W25 installed (W24 for the maskable interrupt, $\overline{IRQ}$, and W25 for the non-maskable interrupt, $\overline{NMI}$). After a conversion is completed, an interrupt is generated. The interrupt line will go low and remain low until a board read is completed. The interrupt line may be tied to a vectored or nonvectored interrupt system. The interrupt line is optionally available as a data bit, $\overline{D5}$, and may be read by skip chain software to determine the interrupting device.

THEORY OF OPERATION

The combination of a valid address and write command triggers a one-shot which generates a delay pulse (25μsec for MP7608-I, 150μsec for MP7608). The low to high transition of this pulse latches the channel address. The delay allows the analog multiplexer and instrumentation amplifier time to settle to $\pm$0.01% before triggering the successive approximation A/D converter. The falling edge of the delay pulse triggers another one-shot that delivers a 1μs pulse. The rising edge of this pulse starts the A/D converter.

There are two control lines which may be connected to the bus: Halt and Interrupt.

The $\overline{HALT}$ control line goes low when the first one-shot is triggered and remains low until the conversion is completed. The $\overline{IRQ}$ or $\overline{NMI}$ interrupt line goes low when the conversion is completed and remains low until the board is read.

ADDRESS MODIFICATION

The base address of a board can be set to any value by changing the address selector jumpers on the input of eleven exclusive-or gates, the base address of these boards is set at the factory to $93E0_{16}$. Table IV shows the jumpers required for each address line.

Address Line	Factory Set	"0"	"1"
A15	1	W19	W20
A14	0	W21	W22
A13	0	W17	W18
A12	1	W15	W16
A11	0	W11	W12
A10	0	W13	W14
A9	1	W9	W10
A8	1	W7	W8
A7	1	W3	W4
A6	1	W5	W6
A5	1	W1	W2

TABLE IV. Address Selection Jumpers.

Address lines A8-A15 are set to 93_{16} by jumpers as shown in Table IV. Address lines A5-A7 are factory set to "1" by inserting both the "0" and the "1" jumpers in Table IV. This was done so that the base address of lines A5-A7 can be changed simply by removing jumpers. For instance, to change the A6 address to a "zero", jumper W6 must be removed. When changing A5, A6 or A7, one jumper for each line must be removed to prevent interaction. For instance, to make A7 = 1, A6 = 0, A5 = 1, jumpers W3, W6, and W1 must be removed. When changing other address lines, the jumper for the present address must be removed and the jumper for the desired address inserted.

MP7608-I DESCRIPTION

The MP7608-I is designed to accept 0-20mA current inputs on channels 0-7. Precision 250Ω ±0.01% resistors (R1-R8) are used to convert this current to 0-5 volts. These resistors are protected by 1/32 amp fuses (F1-F8). By clipping jumpers W27, 29, 31, 33, 35, 37, 39 and 41 the board can accommodate up to 8 channels of differential 0-5V input signals. By selectively clipping these jumpers the board can accept voltage or current inputs at the same time.

MP7608 DESCRIPTION

The MP7608 is an 8 channel differential voltage input unit. It is also capable of interfacing directly to sensors requiring bridge circuits such as RTD's (resistance temperature device) or strain gages.

MP7608 BRIDGE CIRCUITRY

Figure 1 shows the bridge circuit of the MP7608.

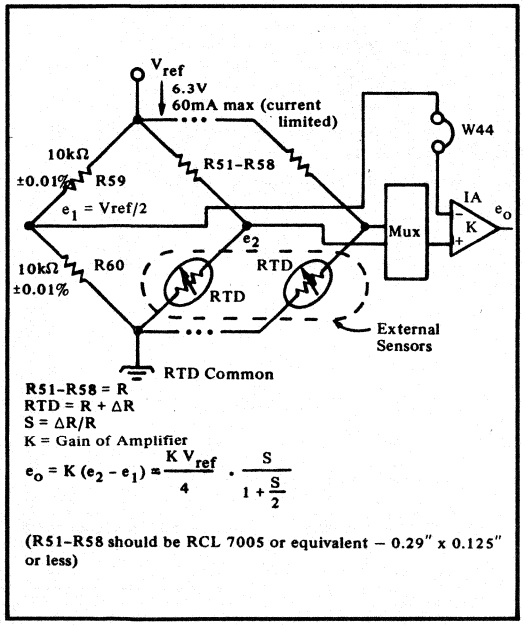


FIGURE 1. MP7608 Bridge Circuity.

Figure 2 shows interconnections for two and three wire RTD's.

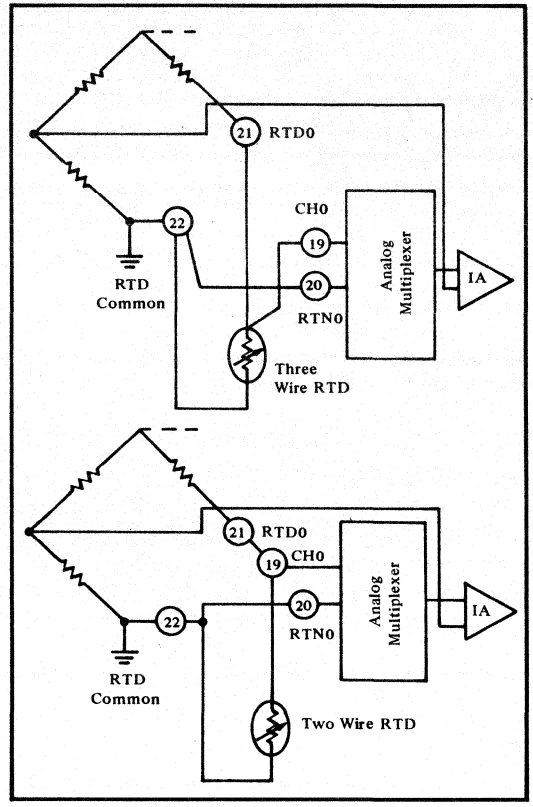


FIGURE 2. RTD Interconnection.

PIN CONNECTIONS (P2 CONNECTOR)

Channel	RTD Common	Bridge RTD0-RTD7	Multiplexer Input CH0-CH7	Multiplexer Input RTN0-RTN7
0	22	21	19	20
1	26	25	23	24
2	30	29	27	28
3	34	33	31	32
4	38	37	35	36
5	42	41	39	40
6	46	45	43	44
7	50	49	47	48

TABLE V. RTD Interconnections and Pin Out.

Up to 8 sensors can be connected to a single board. R51-R58 are precision resistors that are supplied by the user. They should match the "INITIAL" value of the sensor resistance for maximum sensitivity. RTD0-RTD7 should be connected to CH0-CH7 for two wire RTD input operation as shown in Figure 2 and Table V. W46 must be removed and W44 inserted to connect the bridge reference input to the instrument amplifier.

The voltage reference is generated on the MP7608 from the A/D converter reference voltage. The bridge

reference will therefore track the A/D converter gain drift, reducing overall system accuracy drift. V_{ref} is 6.3V ±5% at 60mA maximum with internal current limiting. The factory set gain of 5 is adjusted to compensate for the initial ±5% inaccuracy of V_{ref}. Therefore, if the gain of 5 is used with the bridge circuitry only minor gain and offset adjustments as described on pages 6-79 and 6-80 are required. A K V_{ref} product of exactly (5 x 6.3V) = 31.5V may be used in the bridge equation (see Figure 1).

Since the bridge reference is capable of supplying a maximum current of 60mA, the total bridge load cannot be less than 100Ω. For example, if the initial impedance of all sensors are equal and all 8 bridges are used, the impedance of each leg should be 800 ohms or more. Therefore, with 8 sensors per board, the sensor impedance should be 400 ohms or more. If fewer sensors are required, the impedance of each may be lower (50 ohms for one, 100 ohms for two, etc.).

INPUT RANGES

The on-board instrumentation amplifier of the MP7608/MP7608-I can be resistor programmed for gains from 1 to 500. The MP7608 is factory set for gains of 1, 5, and 100. It is shipped with a gain of 1 and a ±5V A/D converter range. Jumpers as shown in Table VI select gains of 5 and 100. The gain of 5 is approximate, see discussion above in Bridge Circuitry section. When using the MP7608 in gains of 5 and 100, the units should be calibrated with the on-board potentiometers as shown on pages 6-79 and 6-80.

As indicated in Table VI, a gain of 1 is intended for general purpose high level inputs, a gain of 5, for RTD-level signals and a gain of 100 for thermocouple-level signals. A user determined resistor (R62) can be placed on the board for other gains. W49 and W48 should then be open. R62 may be calculated by this formula:

$$\text{Gain} = 1 + 20k\Omega/R62.$$

The MP7608-I instrumentation amplifier is factory set for a gain of 1 with a 0-5V range on the A/D converter. It may be set for other A/D converter input ranges as shown in Table VII. The gain of the instrumentation amplifier may be set to any value between 1 and 500 as described in the previous paragraph. R65 and R66 in parallel (W48 inserted) or R63 and R64 in parallel (W49 inserted) or R62 may be used to set the gain.

As the gain of the instrumentation amplifier increases, the time required to settle increases. An on-board delay timer allows the amplifier and multiplexer to settle to rated accuracy after a channel is selected. This delay time is set for 25 microseconds in the MP7608-I. The delay timer is set for 150 microseconds in the MP7608 which is sufficient for gains of up to 10. By removing R35, the delay of the MP7608 goes to 500 microseconds which is sufficient for gains of up to 100. The delays required for other gains are shown in Figure 3. If 150 or 500 microsecond delays are not desired, R35 and R36** should be removed and replaced by a resistor calculated by the following formula:

$$R_{36} = \frac{(\text{Delay})(.00282)}{C9} \qquad C9 = .047\mu F \text{ (MP7608)},\ .0047\mu F \text{ (MP7608-I)}$$

where R_{36} is in kilohms, C9 is in microfarads and delay is in microseconds.

Example: MP7608-I Delay 100 microseconds

$$R = \frac{(100)(.00282)}{.0047} = 60k\Omega$$

The delay time may be measured at Pin 13 of IC10.

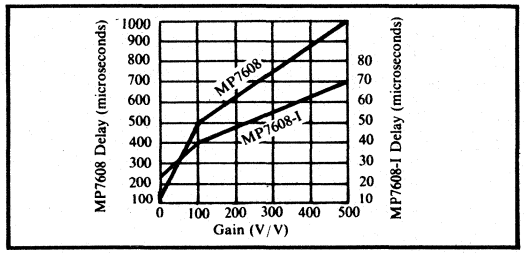


FIGURE 3. Delay vs Gain.

Gain	Jumper		Full Scale Value/Resolution for ADC			
	MP7608		±5V	±2.5V	0 to 10V*	0 to 5V
1	None	Range	±5V	±2.5V	0 to 10V	0 to 5V
		Resolution	2.44mV	1.22mV	2.44mV	1.22mV
≈5	W48	Range	±1V	±0.5V	0 to 2V	0 to 1V
		Voltage Resolution	≈488μV	≈244μV	≈488μV	≈244μV
		500Ω pt RTD Temp. Resolution	0.040°C	0.020°C	0.040°C	0.020°C
100	W49	Range	±50mV	±25mV	0 to 100mV	0 to 50mV
		Voltage Resolution	24.4μV	12.2μV	24.4μV	12.2μV
		Type J Thermocouple	0.46°C	0.24°C	0.46°C	0.24°C
		Type K Thermocouple	0.62°C	0.32°C	0.62°C	0.32°C
		Type T Thermocouple	0.46°C	0.24°C	0.46°C	0.24°C
		Type E Thermocouple	0.36°C	0.18°C	0.36°C	0.18°C
	MP7608-I					
1	W48 with 250Ω Input R	Range	N/A	N/A	N/A	0 to 20mA
		Resolution				4.88μA

* With ±12VDC supplies maximum input is 8 volts.

TABLE VI. Input Voltage Ranges.

** Refer to Figure 5 for location.

Range	Jumpers
±10V*	W55, W52
±5V	W56, W52
±2.5V	W54, W56, W52
0 to +10V*	W56, W53
0 to +5V	W54, W56, W53
* Requires external ±15VDC supply.	

TABLE VII. MP7608/MP7608-I Range Setting Jumpers.

INPUT OVERVOLTAGE PROTECTION/FILTERS

Each input channel is protected to 200V overvoltage. The circuitry is shown in Figure 4.

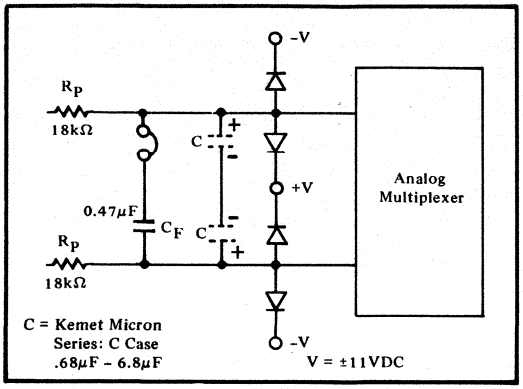


FIGURE 4. Input Overvoltage Protection and Filtering.

The input protection resistors (R_P) limit the current which flow through the protection diodes when overvoltages are applied to the inputs. The 18kΩ input protection resistors together with the 0.47μF capacitor in Figure 4 form the 10Hz input filter. Back to back polarized capacitors may be added in parallel with C_F as shown to lower the cutoff of the input filter. Each C_F has a jumper as shown so that the filter may be removed from the circuit on specific channels if desired, see Table VIII.

Channel	Filter Capacitor Jumper	Current Loop Resistor Jumper
0	W26	W27
1	W28	W29
2	W30	W31
3	W32	W33
4	W34	W35
5	W36	W37
6	W38	W39
7	W40	W41

TABLE VIII. Input Jumpers.

DIFFERENTIAL/SINGLE-ENDED SELECTION

These units are connected at the factory as 8 channel differential units. They may be connected by the user as 16 channels single-ended. In the single-ended mode, the filter capacitors must be removed from the circuit by removing the capacitor jumpers shown in Figure 4. Therefore, single-ended inputs will have no input filtering. Table IX shows the other required jumpers. When changing, first remove those jumpers indicated for the present mode and then insert the jumpers for the other mode.

Jumpers for differential input (std)	Jumpers for single-ended inputs
W42	W43
W46	W45
	W47

TABLE IX. Differential/Single-Ended Jumpers.

CALIBRATION

The MP7608 board can be calibrated with the following program.

```
                    ORG  $00FD
00FD                LSP  $037F      8E
                                    03
                                    7F
0100  START         LDAA #$64       86
                                    64
0102                STAA COUNT      B7
                                    01
                                    1B
0105                CLRA            4F    Clear Accumulators
0102                CLRB            5F
0107  CONV          STAA $93E0      B7    Begin Conversion
                                    93
                                    E0
010A                NOP             01
010B                LDX  $93E0      FE    Read Data
                                    93
                                    E0
010E                CPX  #$F800     8C    Is Data = Low Ref
                                    F8    Ref BTC Offset
                                    00
0111                BNE  AA         26    No
                                    01
0113                INCB            5C    Yes. Increment
                                          Count
0114  AA            DEC  COUNT      7A    Have Conversions
                                    01    reached 100?
                                    1B
0117                BNE  CONV       26    No. Do another
                                          Conversion
                                    EE
0119                BRA  START      20    Yes. Begin next run
                                    E5
011B  COUNT         RMB  1
                    END
```

This program assumes that the program is under control of the Motorola EXORciser EXbug monitor. If either the Mikbug or Microbug monitor is available, the following printout software may be added by using it to replace all codes starting from location 0119. In addition, the references to COUNT (1B) at 0104 and 0116 must be replaced with 2F.

```
                          Mikbug          Microbug
OUT2H                     EQU $E0BF ..... $FD98
OUTEEE                    EQU $E1D1 ..... $FD26

0119 F7                   STA B STR0
     01
     30
011C CE                   LDX   #STR0
     01
     30
011F BD                   JSR OUT2H  Print no. of true
                                     conversions.
     E0
     BF
0122 86                   LDA A #0D
     0D
0124 BD                   JSR OUTEEE
     E1
     D1
0127 86                   LDA A #0A
     0A
0129 BD                   JSR OUTEEE
     E1
     D1
     7E                   JMP START
     01
     00
012F       COUNT          RMB 1
0130       STR0           RMB 2
                          END
```

The reference values for Ref for straight binary coding are Offset Ref = 0000 and Gain Full Scale Ref = $FFFF_{16}$. For two's complement binary coding, Offset Ref = $F800_{16}$ and Gain Full Scale Ref = $07FF_{16}$.

The program assumes that the boards are set for channel zero located at $93E0_{16}$ and $93E1_{16}$. If the board has been reprogrammed for some other address this value should follow the program's LDX and STAA instruction at $010B_{16}$ and 0107_{16}.

If using EXORciser, after assembling and loading insert a breakpoint at location 119 via a 12C; V command to EXbug's MAID function. The program is started with a 00FD; G command.

If using Microbug or Mikbug, start program with G00FD.

Calibration is performed by connecting a precision voltage source capable of 0.005% accuracy to CH0. (This could also be a DC voltage source of less absolute accuracy whose output is monitored by a 0.005% DVM.)

The offset and gain adjustments are made while applying the voltages shown in Table X. For other ranges, the offset voltage adjustment is made at the most negative value of the range plus one half least significant bit (LSB). An LSB is equal to the span (full scale range) divided by 4096 for 12 bit resolution. The gain adjustment is made at the most positive value of the range less 1-1/2 LSB. Thus, for a range of ±100mV, an LSB is 200mV/4096 = 48.8μV. The offset adjustment is made at -100mV + 24.4μV = -99.976mV and the gain adjustment at +100mV -73.2μV = +99.927mV. Before making these adjustments, however, the unit should be allowed to reach thermal equilibrium (about 30 minutes under power).

The offset adjustment is made first by using the appropriate offset calibration voltage. With EXORciser the calibration program is then run and after 100 conversions will halt at the breakpoint. Control will return to the MAID function which will then print the contents of all of the program registers at the time of the breakpoint. The contents of accumulators A and B should be 32_{16}. If a difference of more than 10_{16} is present, slightly readjust the offset control and restart the program with a ;P command. Repeat this procedure until the accumulators' contents are within 10_{16} of each other. If using Microbug or Mikbug, after 100 conversions the B register will be printed and the next 100 conversions started. Printout should be 32 ±10_{16}. If not, adjust the offset control.

The gain adjustment is made in much the same manner. However, the data associated with the CPX instruction in the calibration program must be changed from $F800_{16}$ to $7FF_{16}$ (two's complement). The appropriate gain voltage is then applied and the calibation procedure performed as described for the offset adjustment.

Range	Offset	Gain
±10V*	-9.9976V	+9.9926V
±5V	-4.9988V	+4.9963V
±2.5V	-2.4994V	+2.4981V
0 to +10*	+1.22mV	+9.9953V
0 to +5	+0.61mV	+4.9981V
±1V	+0.99976V	+0.99927V
±0.5V	-0.49988V	+0.49963V
0 to +2V	+0.244mV	+1.9993V
0 to +1V	+0.122mV	+0.99953V
±50mV	-49.988mV	+49.963mV
±25mV	-24.994mV	+24.981mV
0 to 100mV	+12.2μV	+99.953mV
0 to 50mV	+6.1μV	+49.981mV
* With external ±15VDC supply.		

TABLE X. Calibration Values.

JUMPER SUMMARY

W1-W20 — Address selection jumpers, set at factory for $93E0_{16}$. If A5, A6 or A7 is changed, one jumper must be removed from each address line (A5, A6, A7). See page 6-76.

W26-W40 (even numbers) — These jumpers are installed at the factory. If clipped, they will remove 10Hz input filter. See page 6-79.

W27-W41 (odd numbers) — These jumpers are factory installed for MP7608-I. If clipped, they will remove the 250Ω input current loop resistor.

Jumper	Channel
W27	0
W29	1
W31	2
W33	3
W35	4
W37	5
W39	6
W41	7

TABLE XI. Input Current Loop Resistor Jumpers.

W42 — Jumper is inserted at factory to program multiplexer for 8 channel differential input operation. Remove jumper for 16 channel single-ended operation.

W43 — Insert jumper to program multiplexer for 16 channel single-ended input operation.

W44 — Insert jumper for 8 channel RTD input operation. This connects the inverting input of the instrumentation amplifier to Bridge REF ($=V_{REF}/2$). See Figure 1.

W45 — Insert jumper for 16 channel single-ended voltage input operation. This connects the instrumentation amplifier to REMOTE COMMON.

W46 — Jumper is inserted at the factory for 8 channel differential input operation. This connects the inverting input of the instrumentation amplifier to RET0-RET7.

W47 — Insert jumper for 16 channel single-ended voltage input operation. This connects the outputs of both 8 channel multiplexers to the non-inverting input of the instrumentation amplifier.

W24-W25 — Used to obtain a maskable or nonmaskable interrupt. W24 for $\overline{IRQ}$, W25 for $\overline{NMI}$. W24 and W25 are open as shipped from the factory.

W62-W63 — W62 is inserted for VMA input, W63 for VUA input. W62 is open and W63 inserted at the factory (VUA input). For VMA input, W62 is inserted and W63 open.

W64 — Jumper inserted at factory to allow for HALT mode of operation. W64 should be open for interrupt or polling operation. See page 6-76.

W80 — Inserted at factory for two's complements output coding.

W81 — W81 is installed and W80 removed for straight binary output coding.

W82 — Inserted at factory to connect REMOTE COMMON to system common. W82 connects the I.A. low input to system common for single-ended input operation. Remove for pseudo-differential input operation where REMOTE COMMON is connected to a separate external ground that is common to all inputs.

ANALOG CONNECTOR PINOUT

Component Side		Non Component Side	
+5V	1	2	+5V
+5V	3	4	+5V
+12V	5	6	+12V
GND	7	8	GND
GND	9	10	GND
(MP7608) V_{REF}	11	12	GND
REMOTE Com	13	14	GND
RTD Com	15	16	RTD Com
-12V	17	18	-12V
IN 0	19	20	RET0/IN 8
RTD 0	21	22	RTD Com
IN 1	23	24	RET1/IN 9
RTD 1	25	26	RTD Com
IN 2	27	28	RET2/IN 0
RTD 2	29	30	RTD Com
IN 3	31	32	RET3/IN11
RTD 3	33	34	RTD Com
IN 4	35	36	RET4/IN 12
RTD 4	37	38	RTD Com
IN 5	39	40	RET5/IN 13
RTD 5	41	42	RTD Com
IN 6	43	44	RET6/IN 14
RTD 6	45	46	RTD Com
IN 7	47	48	RET7/IN15
RTD 7	49	50	RTD Com

TABLE XII. Analog Connector Pin Out.

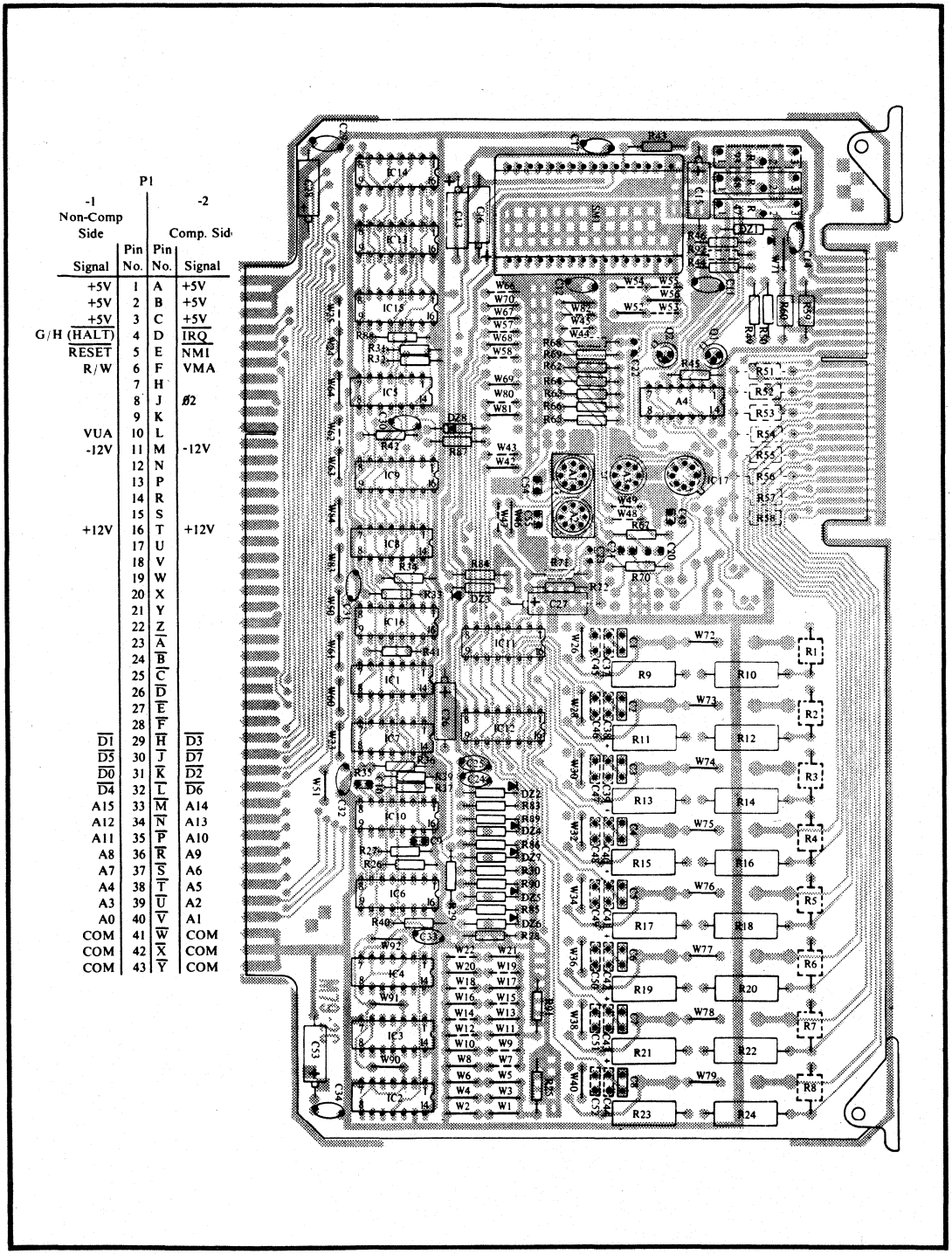


FIGURE 5. Analog Input System(MP7608)

THERMOCOUPLE TEMPERATURE ACQUISITION

Thermocouples are often used as temperature sensors for process control systems. Thermocouples are characterized by temperature coefficients of 10 to 70μV/°C and operating ranges of minus hundreds to plus thousands of degrees centrigrade. When the MP7608 is operated with an instrumentation amplifier gain of 100 or more, it may be connected directly to these devices (Figure 6). The wire runs from thermocouple to measuring device often pick up large common-mode noise signals of 60 Hz or higher frequencies.

The high common-mode rejection of the MP7608's instrument amplifier will reject common-mode noise. To minimize differential mode noise, the signal wire should be twisted and if possible shielded. As a rule, an unshielded twisted pair is better than a coax, and a shielded, twisted pair is still better.

The remote sensor should be earth grounded to prevent common-mode voltages from exceeding the ±5 volt range of the multiplexer.

To complete a thermocouple system it is necessary to terminate all thermocouple wire pairs at an isothermal box or connector strip of some type. An ordinary barrier strip may be monitored for temperature to allow the observed thermocouple emf to be cold junction compensated. Figure 7 shows an excellent circuit for this purpose. Its output is connected to one of the input channels to supply ambient temperature data to the system computer. Its output sensitivity is approximately 2mV/°C.

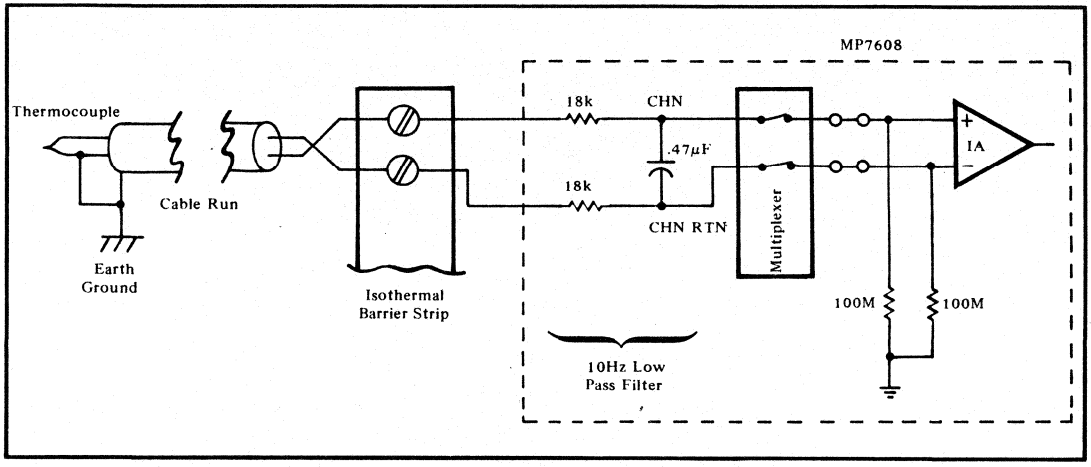


FIGURE 6. Thermocouple Input System

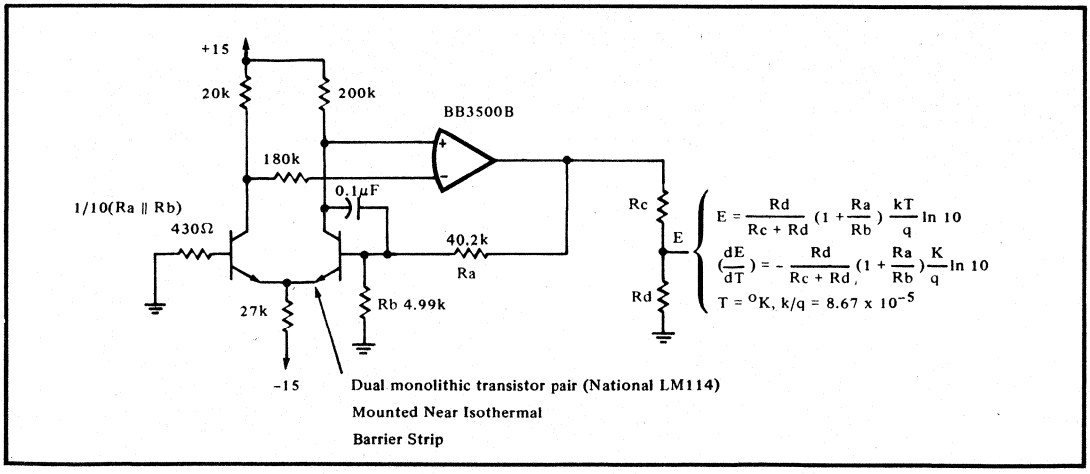
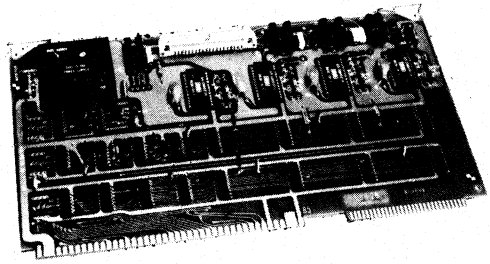


FIGURE 7. Ambient Temperature Sensor

BURR-BROWN



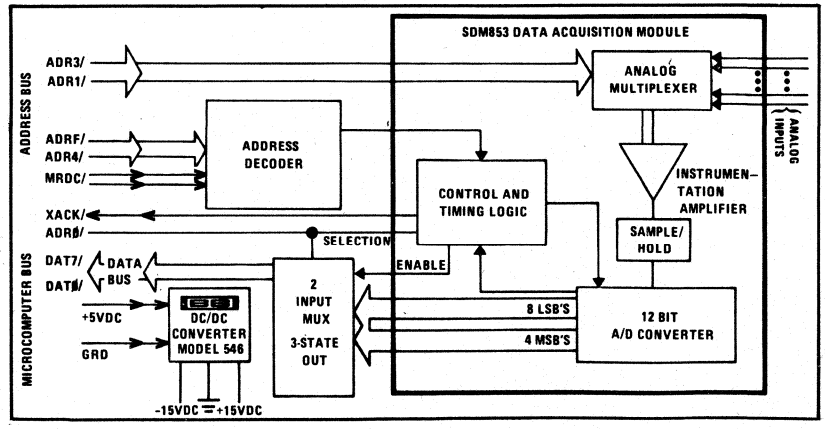
MP8304
MP8408
MP8416

MICROCOMPUTER ANALOG I/O SYSTEMS

INTEL - SBC80 and Intellec MDS Compatible
NATIONAL BLC80 Compatible
MP8304 - Analog Output System
MP8408 - Data Acquisition System
MP8416 - Data Acquisition System

FEATURES

- **EASY TO PROGRAM**
  Systems are treated as memory
- **REDUCES SYSTEM DEVELOPMENT TIME**
  System engineered and specified
  Operates from computer's +5VDC power supply if desired
- **EASY TO USE**
  All cabling and connectors are included



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PDS-353B
Printed in U.S.A. July, 1978

DESCRIPTION

These microcomputer peripherals provide two much needed functions that interface directly to Intel's SBC80/10 and Intellec MDS microcomputers. The functions are: 1) Analog Data Acquisition and 2) Analog Output. The devices are electrically and mechanically compatible with any SBC80/10 and Intellec MDS. Each analog system is contained on a single printed circuit board that is treated as memory input or output by the CPU. The cards will mate to any memory or I/O slot. They are compatible with the 0.6" spacing of the SBC80/10 or the 0.75" spacing of the Intellec MDS. The analog interface for each system is at a flat cable connector at the opposite edge of the board from the bus connector.

The Data Acquisition systems consist of the MP8408, an 8 channel differential input system; and the MP8416, a 16 channel single-ended input system. Burr-Brown's SDM853 modular data acquisition system is used to implement these systems. The data acquisition systems include an input multiplexer, high gain instrumentation amplifier, sample/hold and 12 bit A/D converter along with all the necessary timing, decoding and control logic. The model 546 DC/DC converter (+5V to ±15V) is also used so that only the computer's +5VDC power supply is required.

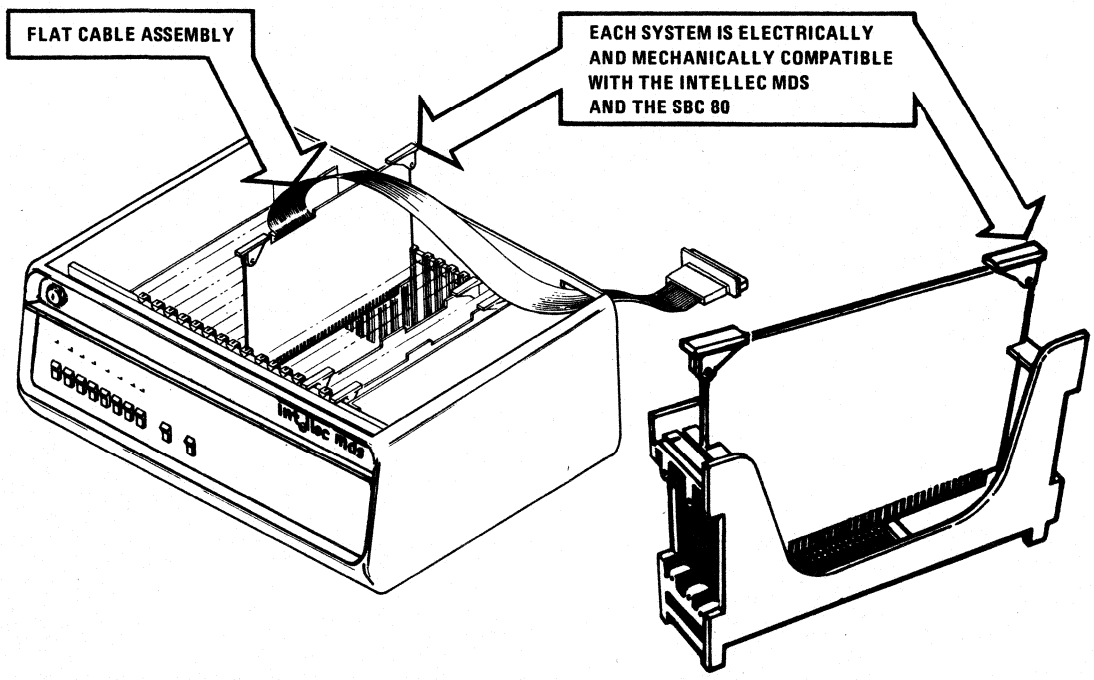
The MP8304, an analog output system, provides four analog output channels (using four of Burr-Brown's hybrid 12 bit DAC80 D/A converters). This board also contains the 546 DC/DC converter to assure operation on +5VDC power. The input of the D/A converters are double buffered so that a complete 12 bit word can be strobed into a D/A converter's input register to minimize output glitches. All of these systems are also offered in an OEM version without the DC/DC converter and cable.

THEORY OF OPERATION

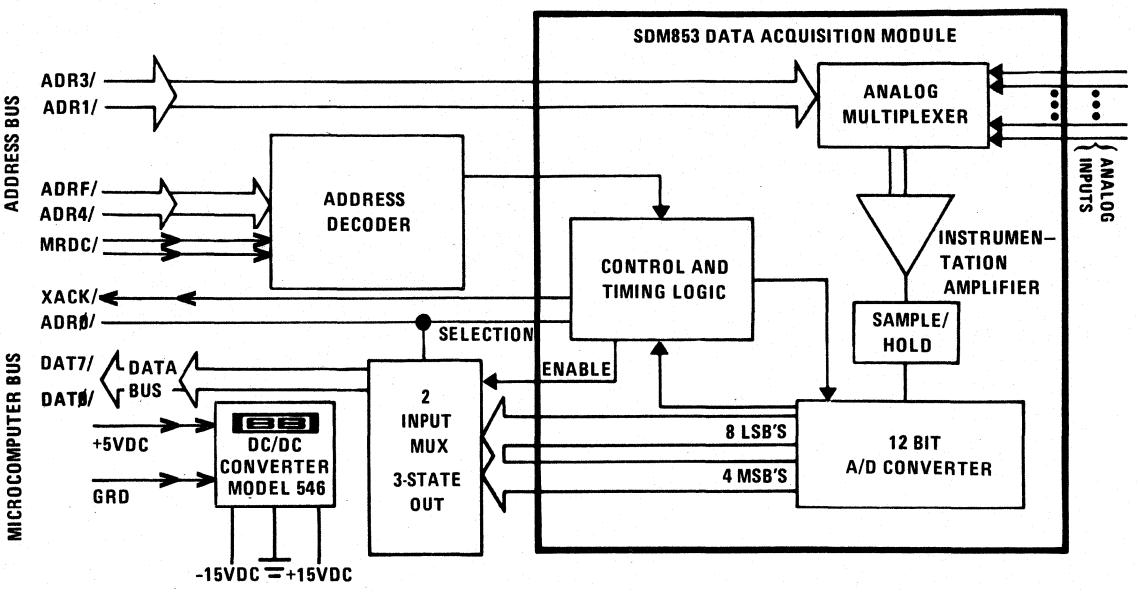
When programming with these peripherals, they are treated as memory locations. Both the A/D converter output and the D/A converter input are 12 bit words so two 8 bit memory locations are needed for each channel. But because the address block occupied by each peripheral is user selectable, it can be placed anywhere in memory. Existing memory can be overlapped since the peripherals inhibit all other memory that occupies the same memory locations.

Because these units are treated as memory, a single instruction is all that's needed to read an input channel or to set the input of a D/A converter. For instance, the LHLD (load) instruction followed by the proper address is used to read data from the MP8408 or MP8416. It will automatically select the desired channel, initiate conversion and when conversion is complete, transfer the A/D converter output for that channel to the 8080's H and L registers. The eight least significant bits are read first followed by the four most significant bits.

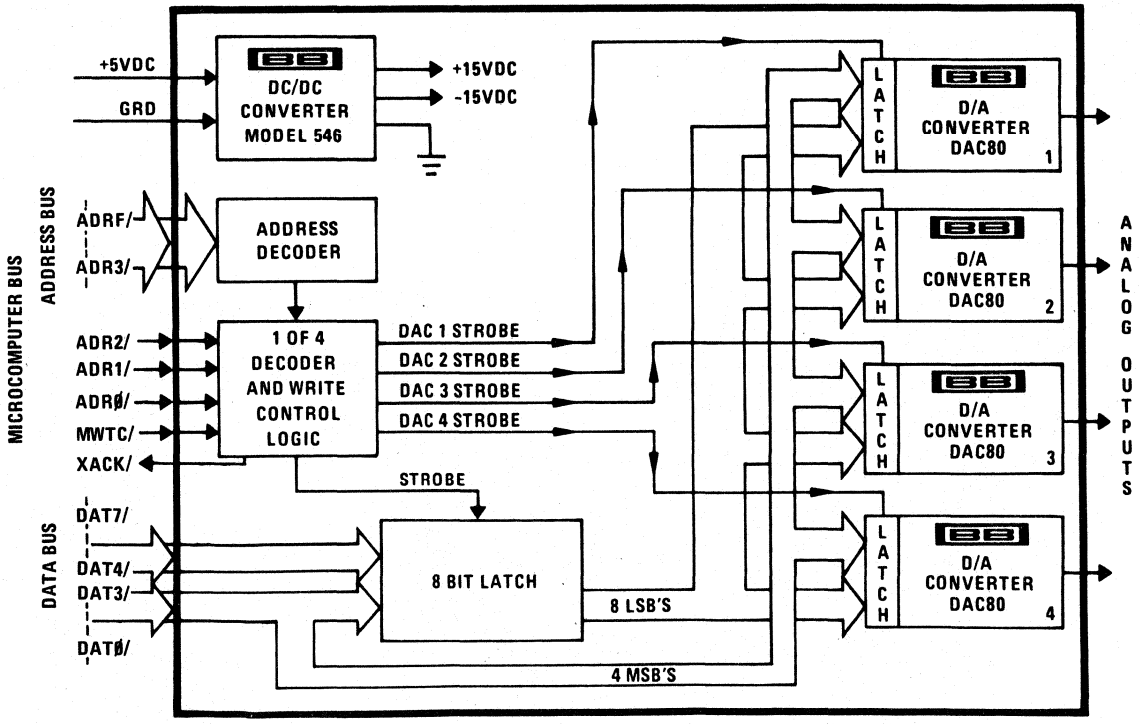
All of these systems are jumpered at the factory with the first channel at address $F720_{16}$. Each subsequent channel is two memory locations past the start of the last channel so that the second channel is at location $F722_{16}$.



ANALOG INPUT SYSTEM - MP8408/8416



ANALOG OUTPUT SYSTEM - MP8304



SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ANALOG INPUT SYSTEMS	MP8408/MP8416
ANALOG INPUT	
Number of analog inputs	
8 differential	MP8408
16 single-ended	MP8416
Input voltage range[1]	±10mV to ±10V
Input current loop ranges (resistor programmable)	4-20mA 10-50mA, etc.
ADC gain ranges (strap selectable)	±10V, 0 to 10V, 0 to 5V ±5V, ±2.5V
Amplifier gain range (resistor programmable)	1 to 1000 V/V
Amplifier gain equation	$G = 1 + 20\ k\Omega/R_{EXT}$ (resistor programmable)
Input overvoltage protection	±15V
Input impedance	100 megohms
Bias current	
25°C	20nA
0°C to 70°C	50nA
Amplifier output noise (Gain = 100 R_S = 500Ω)	1.2mV, rms; 7mV, p-p
Amplifier input offset voltage (max)[4]	400μV
Amplifier input offset voltage drift	$2 + \frac{20}{G}$ μV/°C
TRANSFER CHARACTERISTICS	
Resolution	12 bits binary
Throughput accuracy ±10V range (max)	±0.025% FSR[2]
±10mV range	±0.1% FSR
Temperature coefficient of accuracy	
±10V range (max)	±0.003% FSR/°C
±10mV range	±0.01% FSR/°C
Conversion time ±10V range	33 microseconds
±10mV range	100 microseconds
CMRR (for differential inputs)	74 dB (DC to 2000 Hz)
Sample/hold aperture time	30ns
DIGITAL INPUT/OUTPUT	
All signals are compatible with Microcomputer bus	
Output coding	Bipolar, Two's Complement; unipolar, straight binary
An analog input channel is selected by:	ADR1/ through ADR4/
The output data bits are read into:[3]	DAT0/ through DAT7/
POWER REQUIREMENTS	
MP8408, MP8416	+5VDC ±5% at 1 amp, 25mV ripple
MP8417-NS, MP8409-NS	+5VDC ±5% at +500mA, 25mV ripple +15VDC ±3% at +50mA, 5mV ripple -15VDC ±3% at -75mA, 5mV ripple
TEMPERATURE RANGE	
Temperature range	0°C to 70°C

ANALOG OUTPUT SYSTEMS	MP8304
ANALOG OUTPUT	
Number of analog outputs	4
Output voltage range[1]	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA (strap selectable)
Output impedance	1Ω
Output settling time	< 10 microseconds
TRANSFER CHARACTERISTICS	
Resolution	12 bits binary
Throughput accuracy (max)	±0.0125% FSR
Temperature coefficient of accuracy	
Unipolar	±0.003% FSR/°C
Bipolar	±0.0045% FSR/°C
DIGITAL INPUT/OUTPUT	
All signals are compatible with Microcomputer bus	
An analog output channel is selected by:	ADR1/ and ADR2/
The input data bits are read by:	DAT0/ through DAT7/
POWER REQUIREMENTS	
MP8304	+5VDC ±5% at +1 amp, 25mV ripple
MP8305-NS	+5VDC ±5% at +1 amp, 25mV ripple +15VDC ±3% at +100mA, 5mV ripple -15VDC ±3% at -100mA, 5mV ripple
TEMPERATURE RANGE	
Temperature range	0°C to 70°C

OPERATING INSTRUCTIONS

INSTALLATION

The MP8304, MP8408 and the MP8416 are shipped from the factory calibrated and ready for immediate use. Installation requires only plugging the card into any empty slot in the computer and routing the board's mating I/O cable. Cable placement is shown on page 6-85. The cable supplied with each board is shielded and, in the case of the MP8304, provided with the proper termination.

PROGRAMMING

Programming of these analog I/O boards is easily accomplished since all are treated as memory locations. The MP8304 uses a single SHLD instruction to load any of its four digital to analog converters from the H and L registers. In a similar manner a channel in the MP8408 or MP8416 is read by a single LHLD instruction.

The voltage data for these boards is represented by a 12 bit two's complement binary number. Each bit has a value of 4.88mV, with the polarity of the voltage indicated by the sign of the binary number. Since the H and L register pair is 16 bits long and the data word is 12 bits, the MP8408 and MP8416 set these unused bits to the same value as the most significant bit of the data. This assures proper representation of the data's sign.

Each board is set at the factory for a block of addresses beginning at F720. Any analog data channel requires two memory locations since the digital data is 12 bits. The least significant 8 bits of data are always located in an even location while the remaining 4 bits are located in the next higher location. Thus, the first analog channel is located at F720 and F721 while the second analog channel is located at F722 and F723. These boards can occupy the same address space as memory since they inhibit memory whenever they become active.

MECHANICAL CHARACTERISTICS

Compatible with Intellec MDS and SBC-604/614 card spacing.

Minimum card spacing: 12.7mm (0.5")

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers.

40 pin analog connector (3M - 3432) provided on board. Mating connector (for OEM versions) is 3M - 3417. Recommended cable also by 3M; 3476/40.

(1) Connected at the factory for ±10V range.
(2) FSR is Full Scale Range (i.e., 20V for ±10V range, 10V for 0 to +10V range).
(3) The 4 MSB's when conversion is complete, followed by the 8 LSB's.
(4) Adjustable to zero.

ADDRESS MODIFICATION

The base address of a board can be set to any value by properly jumpering its address selector. The most significant 8 bits of the address (ADR/8-F) are jumpered to read F7 by plated through connections on all boards. These addresses can be changed by first drilling out the hole that makes the connection (Figure 1) and then soldering an insulated wire jumper between the bit and logical zero or one. A 0.055" (#54) drill should be used for this purpose. Extreme caution must be exercised to prevent damage to the board and the scattering of metal particles over its surface.

The remaining lower ordered bits have been connected by wire jumpers at the factory. To change the sense of a bit simply reverse the connection of its jumper.

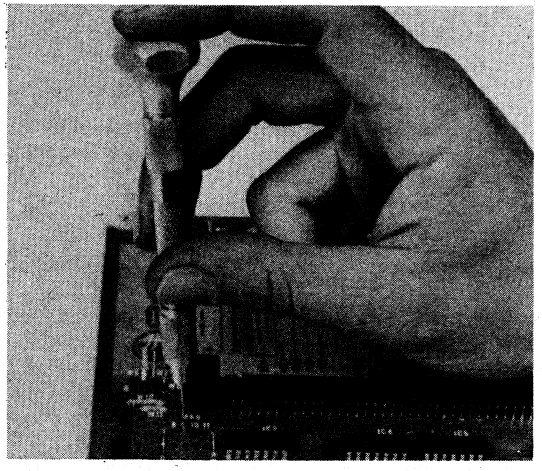
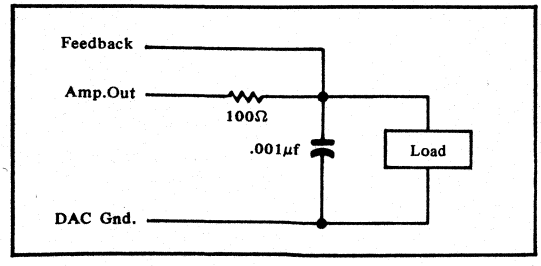


FIGURE 1. Drilling Out Plated Through Holes

MP8304 APPLICATION

The MP8304 system includes an MP8003-cable assembly that is required for proper operation. This is because the feedback for each DAC output amplifier is connected to the amplifier output through a low pass filter at the end of the cable. For those applications requiring a different cable, this feedback connection must be considered. Where increased noise may be tolerated, the feedback can be connected directly on the board via jumpers W6, W12, W18 and W50. However, if noise performance is to be optimized the feedback must be connected at the load through shielded cable and terminated as follows:



It is always necessary to recalibrate when the output cable is changed. For whatever feedback technique used, maximum accuracy and minimum noise requires the corresponding DAC ground to be used as the return from the load.

Test points at the top edge of the board make each DAC output (white) and analog common (black) available for easy reference. However, these points should never be used for calibration.

MP8408/8416 APPLICATION

The data acquisition module (Burr-Brown's SDM853) incorporated into the MP8408/8416 uses a fixed timing sequence between channel selection and the start of data conversion.

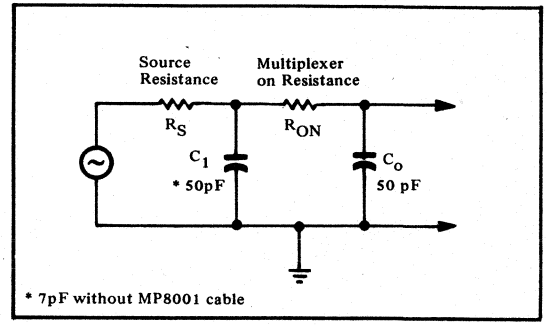


FIGURE 2. On Channel Multiplexer Circuit Model for Single-ended Operation

As normally supplied the time allowed for multiplexer settling is 9 μs which is sufficient for many applications. The only external factor which affects the multiplexer settling time is the output impedance (R_S) of the source connected to a channel. A circuit model of an "On" channel is shown in Figure 2. The input capacitance (C_1) of 50 pF does not affect the settling time since it is continuously connected to the source. The signal at the output of the multiplexer must be allowed to settle to ±0.01% (nine time constants) to maintain the full accuracy of the system. The multiplexer time constant can be calculated with the formula: $\Upsilon = (R_S + R_{on}) C_o$. For a source resistance of 1kΩ Υ = (1 + 1.8) kΩ x 50pF = 140ns. Thus, 1.26 μs is needed to settle to ±0.01%. This is well below the fixed 9 μs allowed for multiplexer settling so that the accuracy of the system is preserved.

If the source bandwith can be limited, high impedance sources may be accurately handled by placing a large capacitor across the multiplexer input. An analysis of such a circuit shows that a capacitor of 0.5 μF is sufficient. For such a capacitance the multiplexer time constant becomes 90ns. If this method cannot be used the time allowed for settling can be increased as described in the section on low level operation.

For switching of large signals it must be remembered that the on resistance is the channel resistance of a FET which is a nonlinear function of the applied voltages. As a result the previous calculations are only an approximation derived from a linearized model. Another factor not considered is the addressing delay of the multiplexer. This is typically 250ns and is additive to the above calculated times

For differential units the same considerations apply. Even though two input circuits are involved there is sufficient component matching within the multiplexer to prevent measurable differences in the transfer functions for each half of the signal. Therefore, the time constant for only one circuit can be considered the time constant for the entire channel. When operated in the differential mode, C_o in Figure 2 becomes 12.5 pF.

The analog inputs have reversed biased diode circuits which prevent damage from discharge of static electricity. However, it is still wise to take reasonable precautions against static discharge.

The MP8001 input cable provided with the MP8408 and MP8416 systems provides a shielded connection to the Intellec's rear panel. If a cable other than this is to be used, it should also be shielded for maximum noise immunity.

For a more complete discussion on the application of analog data acquisition systems, obtain a copy of Burr-Brown Application Note AN-79, and the SDM853 User's Manual, PDS-358.

MP8304 OUTPUT RANGE SELECTION

Each DAC is jumpered at the factory for ±10 volt operation (two's complement coding). However, it is possible to alter these jumpers as shown in Figure 3 for other output voltages. Jumpers indicated by an asterisk are plated through holes on the board and should be removed by drilling as described in the section on address modification. When making a change, first remove those jumpers indicated for the present range and replace them with those jumpers required for the desired range.

Range	DAC1	DAC2	DAC3	DAC4
±10	W1*, W2*	W7*, W8*	W13*, W14*	W19*,W20*
±5	W4, W2*	W10, W8*	W16, W14*	W22, W20*
±2.5	W4, W2*	W10, W8*	W16, W14*	W22, W20*
	W5	W11	W17	W23
0 to +10	W4, W3	W10, W9	W16, W15	W22, W21
0 to +5	W4, W3	W10, W9	W16, W15	W22, W21
	W5	W11	W17	W23

FIGURE 3. MP8304 Output Selection Jumpers

When converting from bipolar to unipolar operation W51* should be removed and W52 installed. This prevents the inversion of the most significant bit as required for two's complement operation. However, the data to all four DACs is affected by this change. If not all DACs are converted to unipolar operation, it will be necessary to perform this inversion in software for bipolar DACs.

BIPOLAR - TWO'S COMPLEMENT			
Digital Input/Output	±10V	±5V	±2.5V
0111 ... 11($7FF_{16}$)	+9.9951V	+4.9975V	+2.4988V
100 ... 00(800_{16})	-10.0000V	-5.0000V	-2.5000V
UNIPOLAR - STRAIGHT BINARY			
Digital Input/Output	0 to +10V	0 to +5	
111 ... 111(FFF_{16})	9.9975V	4.9988	
000 ... 00(000_{16})	0.0000V	0.0000V	

TABLE I. Analog Input and Analog Output Full Scale Range Values

MP8408/8416 INPUT RANGE SELECTION

The data acquisition module on these boards has been externally jumpered for ±10V operation. Other ranges are possible and can be selected as shown in Figure 4. Before adding new jumpers remove those indicated for the present range.

RANGE	JUMPERS
±10V	W6, W44
±5V	W4, W44
0 to +10V	W4, W45
0 to +5V	W4, W45, W48

FIGURE 4. MP8408/MP8416 Range Setting Jumpers

As configured at the factory, these boards are jumpered for two's complement operation (see Table I above) with jumper W14 inserted and W15 open. For operation in the straight binary mode (any range) jumper W14 is open and W15 is inserted. In addition, remove jumper W12 and insert a 1k, 1/4W resistor from the center pad (going to pin 11 of IC9) to +5V.

MP8408/8416 LOW LEVEL OPERATION

Terminals for external gain setting resistors (see Figure 6) have been provided so that the SDM853's instrumentation amplifier can be set for gains to 1000. The following formula can be used to calculate the value of the resistance: Gain = $1 + 20k\Omega/R_{ext}$.Where R_{ext} is the resistance between pins 26 and 27 of the SDM853. (R16, 17 in parallel form R_{ext} in Figure 6). The internal gain adjustment potentiometer in the SDM853 module will give an adjustment range of ±0.5%.

Very stable (10 ppm) wire wound resistors should be used in this application.

At high gains the instrumentation amplifier requires a longer settling time than that set internally. Pads have been provided (R26, R27,C6 in Figure 6) to allow the addition of external resistors and a capacitor to increase the delay time allotted for multiplexer and amplifier settling, see Figure 5. As normally shipped the amplifier gain is set for unity and the delay time set for 9μs. For a gain of 1000 this time should be set for 70μs. See Table II. The delay time may be measured at pin 18 or pin 59 of the SDM853 or with a high impedance oscilloscope probe on either side of C6.

Amplifier Gain V/V	System Accuracy	Delay Time (microseconds)	Total Conversion Time (microseconds)
1	±0.025% FSR	9	33
10	±0.03% FSR	18	40
100	±0.08% FSR	25	50
1000	±0.1% FSR	70	95

TABLE II. Typical System Performance

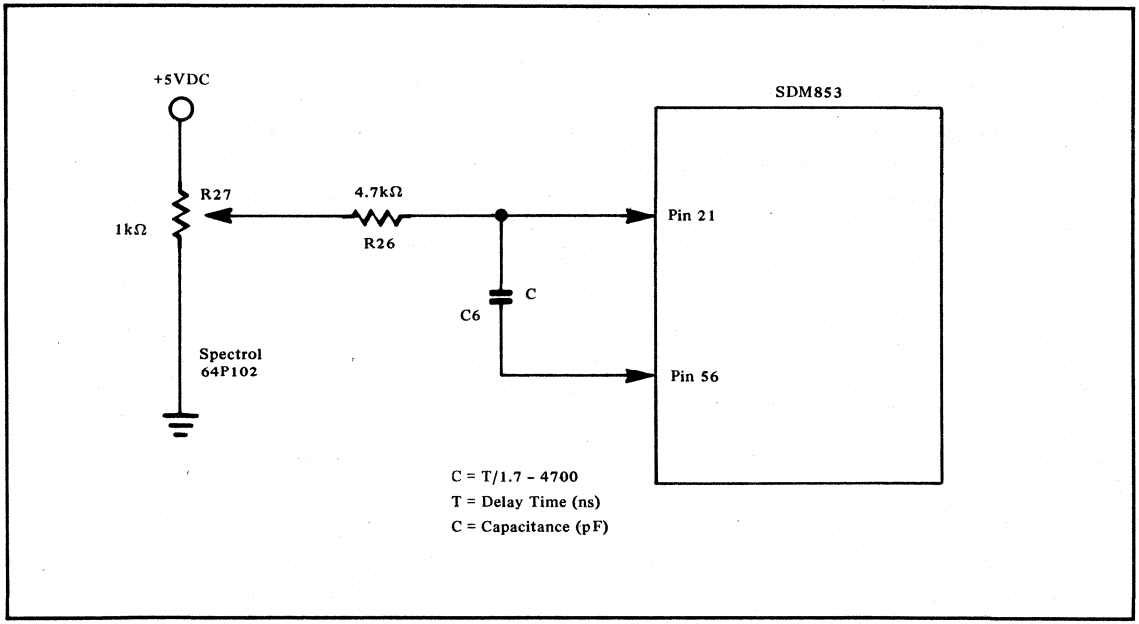


FIGURE 5. Delay Time Adjustment

At very high gains, the system offset may be so large as to be beyond the range of the SDM853's internal offset adjustment. When this occurs a 250k potentiometer (Spectrol 64P254) (R28 in Figure 6), a 1/10 watt, 50ppm, 51.1kΩ metal film resistor (R4 in Figure 6) and jumper W10 must be added. This control becomes the coarse offset adjustment that is used to extend the range of the module's fine adjustment.

When operating the amplifier at high gain the overall accuracy of the system declines. At a gain of 1000 accuracies of ±0.1% can be expected. This is due to increased noise and a loss in amplifier linearity (see Table II). For lowest system noise, the ADC range should be set on the ±10V or 0 to +10V ranges with the amplifier providing all the system gain.

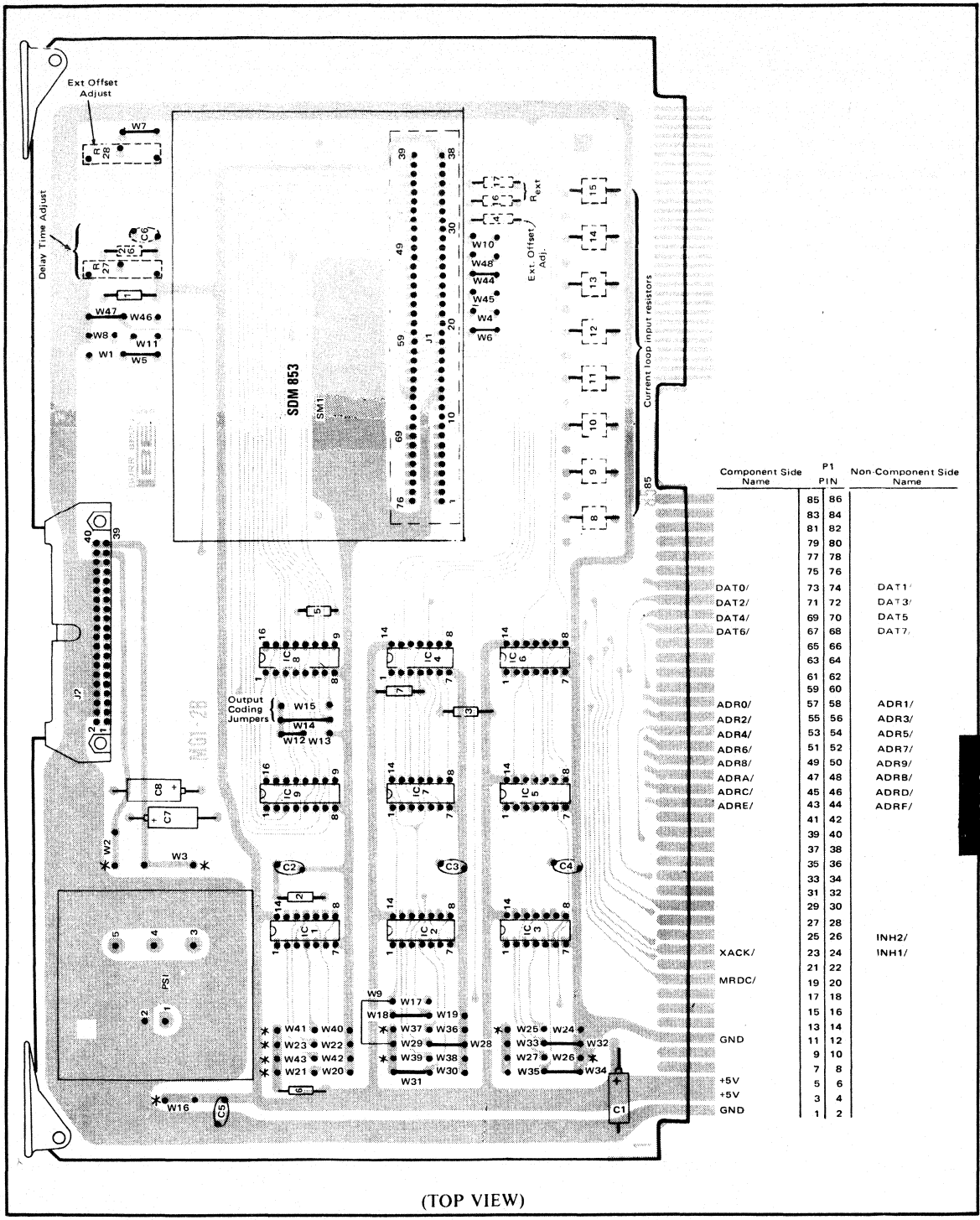


FIGURE 6. Analog Input System

MP8408 PROCESS CURRENT LOOP INPUT OPERATION

The MP8408 is designed to allow the user to easily add the dropping resistors (R8, -R15, Figure 6) needed to input process current loop signals such as 4-20mA and 10-50 mA. Figure 7 shows the resistor value and settings required.

Current Loop	Input Resistor	Amplifier Gain	ADC Range	Resolution
4-20mA	250Ω	1	0 to 5V	4.88μA
10-50mA	100Ω	1	0 to 5V	12.2μA

FIGURE 7. Current Loop Inputs.

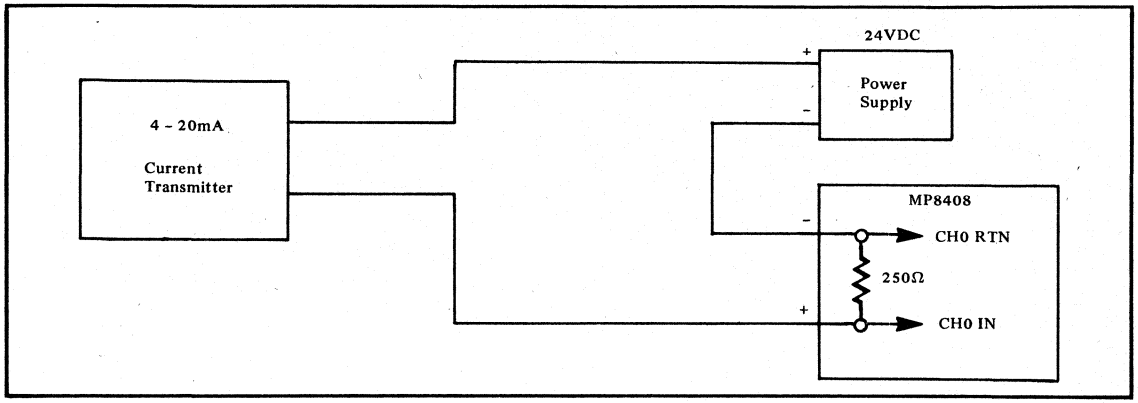


FIGURE 8. Typical Current Transmitter Interface

MP8408/8416 DIFFERENTIAL-SINGLE ENDED SELECTION

An input board can be converted from single-ended operation (MP8416) to differential operation (MP8408) or vice versa by simply changing several board jumpers. Figure 9 indicates those jumpers that must be present for a given mode of operation. To convert from one mode to the other remove those jumpers indicated for the present type of operation and install those necessary for the desired mode of operation.

MP8408 (Differential) required jumpers	MP8416 (Single ended) required jumpers
W5	
W9	W8, W11
W18	W17, W19
W28	W29, W46
W47	

FIGURE 9. Input Mode Selection Jumpers

ADDING EXTERNAL POWER SUPPLIES

The MP8408/8416/8304 boards require approximately 1 amp at 5V. In some applications it may be necessary to add an external power supply. This can be accomplished as follows:

±15 volts power can be supplied to each board through the board's analog connector. When this is done, the loading of the computer's 5 volt supply by the board is reduced by half. Before external power can be applied, the DC to DC converter must be disconnected. This is done on the MP8304 by removing plated through jumpers W53* - W55*, and jumpers W2*, W3*, W6* for the MP8408 and MP8416. These plated through jumpers are removed according to the technique described for address modification.

Of course, MP8409-NS/8417-NS/8305-NS are connected at the factory for use with an external ±15VDC power supply. Connect these supplies to the analog connector pins described on the last page.

MP8304 CALIBRATION

The MP8304 is calibrated through the use of the Intellec MDS and its monitor. With the board installed in the Intellec allow the system to reach thermal equilibrium (about 30 minutes under power) before starting the procedure.

Calibration is begun by loading DAC0 with data that will produce its most negative output. This is done via the monitor's S command since each DAC appears to the Intellec as two adjacent memory locations. For Two's Complement operation this data is 800_{16} and for straight binary the data is 0_{16}. The least significant 8 bits of the

data is transferred first into location $F720_{16}$ with the most significant 4 bits loaded next into location $F721_{16}$. The DAC should then be set by its offset control to the appropriate low voltage value as shown in Figure 5.

The gain control is adjusted in a similar manner, after setting the DAC to its most positive output. For a Two's complement DAC, the input data is $7FF_{16}$. For a straight binary unit the data is FFF_{16}. The Gain control is then used to set the DAC output to the high voltage value indicated in Figure 10.

The remaining DACs are calibrated in the same way. As shipped from the factory, the DACs occupy the following adjacent memory locations.

DAC 0 - F720, F721
DAC 1 - F722, F723
DAC 2 - F724, F725
DAC 3 - F726, F727

Range	Low	High	1 LSB
±10V	-10.000V	+9.9951V	4.8828mV
±5V	-5.000V	+4.9976V	2.4414mV
0 to +10V	0.0V	+9.9975V	2.4414mV
0 to +5V	0.0V	+4.9988V	1.2207mV

FIGURE 10. DAC Calibration Values

Calibration must always be made at the end of the cable that is normally used with the DAC and never at the board's test points. A five digit DVM which is capable of ±0.005% accuracy should be used.

MP8408/MP8416 CALIBRATION

The MP8408 and MP8416 boards are calibrated through the use of the following program:

```
        ORG     10H
AD:     LXI     B,0       ; Clear B and C Reg. Pair
AC:     LHLD    0F720H    ; Read Data from Board
        MOV     A, L      ; Is Data = Low Ref?
        SUI     0
        JZ      AA
        INR     C         ; No. Increment count
        JMP     AB
AA:     INR     B         ; Yes. Increment count
AB:     MOV     A, B      ; Have 100 conversion been
                            made
        ADD     C
        CPI     64H
        JNZ     AC
AE:     JMP     AD        ; Yes. Begin program again
        END
```

The program assumes that the boards are jumpered for channel zero located at F720. If the most significant bits of the address have been rejumpered, the address associated with the LHLD instruction at location AC must reflect this change.

After assembling and loading the program, set a breakpoint at AE. The program is then started by a G10 command to the Intellec monitor. After 100 conversions the breakpoint will be reached and control will return to the Intellec monitor. The B and C registers are then examined for an approximately equal count in each. Both the Offset and Gain adjustments require that this process be repeated until this condition is reached.

Range	Offset	Gain
±10V	-9.9976V	+9.9927V
±5V	-4.9987V	+4.9963V
0 to +10	+1.2207mV	+9.9963V
0 to +5	+0.61035mV	+4.9981V

FIGURE 11. Data Acquisition Calibration Values

Calibration is performed by connecting a precision voltage source capable of 0.005% accuracy to an input channel. (This could also be a DC voltage source of less absolute accuracy whose output is monitored by a 0.005% DVM.) The offset and gain adjustments on the SDM853 are made while applying the voltages shown in Figure 11. For other ranges, the offset voltage adjustment is made at the most negative value of the range less one half least significant bit (LSB). An LSB is equal to the span (full scale range) divided by 4096 for 12 bit resolution. The gain adjustment is made at the most positive value of the range less 1 1/2 LSB. Thus, for a range of ±50 mV, and LSB is 100 mV/4096 = 24.4μV. The offset adjustment is made at -50 mV + 12.2μV = -49.988 mV and the gain adjustment at +50 mV - 36.6μV = 49.963 mV. Before making these adjustments, however, the unit should be allowed to reach thermal equilibrium (about 30 minutes under power).

The offset adjustment is made first by using the appropriate offset calibration voltage. Run the calibration program and perform those offset control adjustments required to make the B and C registers approximately equal.

Before performing the Gain adjustment change the data associated with the SUI instruction in the calibration program from 0 to FF. Set the input voltage to the correct value as shown in Figure 11 and adjust the Gain control in the same manner as described for Offset.

TROUBLE SHOOTING

Trouble shooting typically requires that the board be continually operated. For the MP8304 this can be done by looping around a SHLD instruction and for the MP8408 and MP8416 a LHLD instruction. In this way all of the necessary Intellec signals are repetitively generated so that a scope or logic probe can be used for signal tracing. The interface portion of each board is straightforward and can easily be followed if all of the Intellec I/O signals and the board's function diagram are understood.

MP8304 BACKPANEL PINOUT

Pin No.			
Cable Shield GND	1	2	DAC1-FB
DAC1-OUT	3	4	DAC1-GND
-15V	5	6	N/C
N/C	7	8	GND
+15V	9	10	DAC2-FB
DAC2-OUT	11	12	DAC2-GND
DAC4-FB	13	14	DAC4-OUT
DAC4-GND	15	16	GND
DAC3-FB	17	18	DAC3-OUT
DAC3-GND	19	20	N/C
N/C	21	22	N/C
N/C	23	24	-15V
N/C	25	26	GND
+15V	27	28	N/C
N/C	29	30	N/C
N/C	31	32	N/C
N/C	33	34	N/C
N/C	35	36	N/C
N/C	37		

MP8408 BACKPANEL PINOUT

Pin No.			
Cable Shield GND	1	2	CH0 Return
CH0 IN	3	4	CH1 Return
CH1 IN	5	6	CH2 Return
CH2 IN	7	8	CH3 Return
CH3 IN	9	10	CH4 Return
CH4 IN	11	12	CH5 Return
CH5 IN	13	14	CH6 Return
CH6 IN	15	16	CH7 Return
CH7 IN	17	18	GND
-15V	19	20	N/C
GND	21	22	GND
GND	23	24	GND
GND	25	26	GND
GND	27	28	GND
GND	29	30	GND
GND	31	32	GND
GND	33	34	GND
GND	35	36	GND
+15V	37		

MP8416 BACKPANEL PINOUT

Pin No.			
Cable Shield GND	1	2	CH8 IN
CH0 IN	3	4	CH9 IN
CH1 IN	5	6	CH10 IN
CH2 IN	7	8	CH11 IN
CH3 IN	9	10	CH12 IN
CH4 IN	11	12	CH13 IN
CH5 IN	13	14	CH14 IN
CH6 IN	15	16	CH15 IN
CH7 IN	17	18	GND
-15V	19	20	Remote COM
CH8 COM	21	22	CH0 COM
CH9 COM	23	24	CH1 COM
CH10 COM	25	26	CH2 COM
CH11 COM	27	28	CH3 COM
CH12 COM	29	30	CH4 COM
CH13 COM	31	32	CH5 COM
CH14 COM	33	34	CH6 COM
CH15 COM	35	36	CH7 COM
+15V	37		

MP8304 or MP8305-NS BOARD
ANALOG CONNECTOR PINOUT

Pin No.			
GND	1	2	GND
GND	3	4	GND
DAC1-GND	5	6	DAC1-FB
DAC1-OUT	7	8	DAC1-GND
-15V	9	10	-15V
-15V	11	12	-15V
GND	13	14	+15V
GND	15	16	+15V
GND	17	18	+15V
DAC2-GND	19	20	DAC2-GND
DAC2-OUT	21	22	DAC2-OUT
DAC2-FB	23	24	DAC2-FB
DAC2-GND	25	26	DAC2-GND
DAC4-GND	27	28	DAC4-GND
DAC4-FBD	29	30	DAC4-FB
DAC4-OUT	31	32	DAC4-OUT
DAC4-GND	33	34	DAC4-GND
GND	35	36	GND
DAC3-GND	37	38	DAC3-FB
DAC3-OUT	39	40	DAC3-GND

MP8408 or MP8409–NS BOARD
ANALOG CONNECTOR PINOUT

Pin No.			
GND	1	2	Remote COM
RET	3	4	GND
IN0	5	6	GND
RET1	7	8	GND
IN1	9	10	GND
RET2	11	12	GND
IN2	13	14	GND
RET3	15	16	GND
IN3	17	18	GND
RET4	19	20	GND
IN4	21	22	GND
RET5	23	24	GND
IN5	25	26	GND
RET6	27	28	GND
IN6	29	30	GND
RET7	31	32	GND
IN7	33	34	GND
GND	35	36	GND
-15V	37	38	-15V
+15V	39	40	+15V

MP8416 or MP8417-NS BOARD
ANALOG CONNECTOR PINOUT

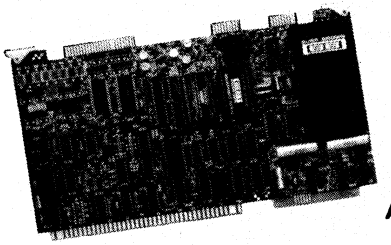
Pin No.			
GND	1	2	Remote COM
IN8	3	4	GND
IN0	5	6	GND
IN9	7	8	GND
IN1	9	10	GND
IN10	11	12	GND
IN2	13	14	GND
IN11	15	16	GND
IN3	17	18	GND
IN12	19	20	GND
IN4	21	22	GND
IN13	23	24	GND
IN5	25	26	GND
IN14	27	28	GND
IN6	29	30	GND
IN15	31	32	GND
IN7	33	34	GND
GND	35	36	GND
-15V	37	38	-15V
+15V	39	40	+15V

INPUT RANGE	ADC RANGE	AMPLIFIER GAIN
±10V	±10V	1
0 to 10V	0 to 10V	1
±5V	±5V	1
0 to 5V	0 to 5V	1
±1V	±10V	10
0 to 1V	0 to 10V	10
±100mV	±10V	100
0 to 100mV	0 to 10V	100
±50mV	±10V	200
0 to 50mV	0 to 10V	200
±10mV	±10V	1000
0 to 10mV	0 to 10V	1000

MP8001	Cable and Assembly included with MP8408 and MP8416
MP8002	Connector Kit included with 8304, MP8408, MP8416
MP8003	Cable and Assembly included with MP8304
MP8304	4 Channel DAC Output System (includes MP8002, MP8003, MP8305)
MP8305	4 Channel DAC Output Board
MP8305-NS	MP8305 without DC/DC converter (requires ±15VDC)
MP8408	8 Channel differential analog input system (includes MP8001, MP8002, MP8409)
MP8409	8 Channel differential analog input board
MP8409-NS	MP8409 without DC/DC converter (requires ±15VDC)
MP8416	16 Channel single-ended analog input system (includes MP8001, MP8002, MP8417)
MP8417	16 Channel single-ended analog input board
MP8417-NS	MP8417 without DC/DC converter (requires ±15VDC)

Each board interfaces to both the Intellec MDS and the SBC80.

BURR-BROWN



MP8418

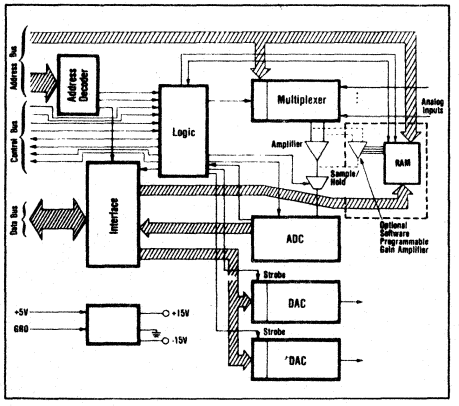
ADVANCE INFORMATION
Subject to Change

MICROCOMPUTER ANALOG I/O SYSTEMS

A 31 CHANNEL ANALOG INPUT, 2 CHANNEL OUTPUT SYSTEM COMPATIBLE WITH INTEL SBC80, INTELLEC® MDS AND NATIONAL BLC-80 MICROCOMPUTERS

FEATURES

- HIGH AND LOW LEVEL INPUTS
- SOFTWARE PROGRAMMABLE GAIN (1 to 1024) AMPLIFIER OPTION
- ANALOG INPUT AND OUTPUT ON ONE BOARD
- EASILY PROGRAMMED
- MEMORY MAPPED
- LOW COST



DESCRIPTION

The MP8418 series of analog I/O peripherals are electrically and mechanically compatible with and interface directly to Intel's SBC80 Multibus® and other microcomputers of similar configuration. These analog systems are treated as memory by the CPU.

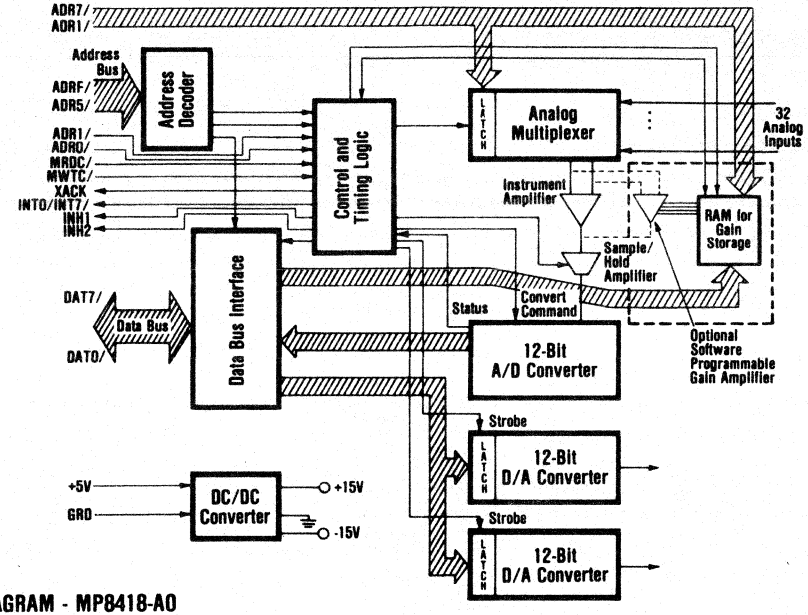
The analog input portion of the MP8418 includes: over-voltage protection to 26VDC; provision for up to eight 4-20mA inputs; an analog multiplexer; resistor programmed instrument amplifier or, a software programmable amplifier (gain of 1 to 1024); sample/hold amplifier and; a 12-bit A/D converter. An optional analog output system is included on the same board. It consists of two 12-bit D/A converters with double buffered inputs to minimize glitches, and control logic.

MP8418 is a 15 channel differential (user strappable as 31 channel single-ended) analog input system. With one expander board the system can be expanded to 63 differential channels (strappable as 127 single-ended channels). Another input channel is grounded on the board so that it may be used as ground reference for automatic calibration.

Gains of 1 to 1024 are software selectable for the programmable amplifiers and the gain for each channel (up to 127 channels) may be stored in an on-board RAM if desired. The proper gain for each channel is then selected automatically by the MP8418.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-401 Printed in U.S.A. July, 1978



BLOCK DIAGRAM - MP8418-A0

MECHANICAL SPECIFICATIONS

Compatible with Intellec MDS and SBC-604/614 card spacing.

Minimum card spacing: 15.2mm (0.6").

Microcomputer bus connected required: 86 pin PC edge connector with 0.156" contact centers.

50 pin analog edge connector on board for analog inputs.
Mating connector available from Burr-Brown: 2250MC. (Viking #3VH25/1JN5, solder tab); from 3M: 3415-0001 (Scotchflex).

20 pin analog edge connector on board for analog outputs and analog input expansion.
Mating connector available from Burr-Brown: 2220MC. (Viking #3VH10/1JN5).

OPERATING INSTRUCTIONS

INSTALLATION

MP8418 is shipped from the factory calibrated and ready to use. Installation requires only plugging the card into any empty slot in the computer and wiring the analog connector.

PROGRAMMING

This peripheral is programmed as a memory location and any memory reference instruction can be used. Both the A/D converter output and D/A converter input are 12-bit words, therefore, two memory locations are needed for each channel. The address block occupied by each MP8418 is user selectable and can be placed anywhere in memory.

Because these peripherals are treated as memory, a minimum of instructions are needed to read an input channel, or to set the input of a D/A converter. For example: when the MP8418 is connected in the HALT mode, the LHLD (load) instruction followed by the proper address can be used to read data from an analog input channel. It will automatically select the desired channel, initiate conversion and when conversion is complete, transfer the A/D converter output to the 8080's H and L registers. The eight least significant bits (LSB's) of the data word are transferred to the CPU first followed by the four most significant bits (MSB's). The four MSB's are in data bus positions 0 - 3. A single SHLD instruction can be used to write data to one analog output channel. The eight LSB's are written first, followed by the four MSB's (in D0-D3). When the four MSB's are written to the board, all twelve bits of the data word are transferred simultaneously to the D/A converter input.

DAC Bit Placement

	D7	D6	D5	D4	D3	D2	D1	D0
Low Byte	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
High Byte	X	X	X	X	B_{11}	B_{10}	B_9	B_8

On MP8418's, with the software programmable gain amplifier, an on-board random access memory (RAM) may be used to store the gain for each channel. In this

mode, (Control Register D4 = 1), the proper gain is automatically selected from the RAM when a channel is converted. If the RAM is not used (Control Register D4 = 0), the amplifier gain must be written to an on-board register (Control Register D0-D3).

All these systems are jumpered at the factory with a base address of $F700_{16}$. Each subsequent channel is two memory locations past the start of the last channel, consequently channel one is at location $F702_{16}$, channel two is at location $F704_{16}$, etc.

The input system operates in several modes:

INTERRUPT MODE: A read instruction to the board (ADR0 = 0) starts the conversion. An interrupt is generated at the end of the conversion. the interrupt can be connected to any of eight vector locations and may also be disabled in software. Control Register D6 = 1 enables interrupt for interrupt mode.

POLLING MODE: A read to the board starts the conversion. The interrupt is disabled by software and the CPU may then read the status word to determine when conversion is complete. Control Register D6 = 0 disables interrupt for polling mode.

HALT MODE: a read instruction to the board starts the conversion. The MP8418 halts the CPU until conversion is complete, at which point the data is transferred to the CPU. Only one instruction is needed to start conversion and to transfer data to the CPU (an LHLD or POP referenced to the channels LSB's can be used).

CONTINUOUS MODE: A read instruction to the board starts the conversion. The CPU is not halted, but reads the status of the MP8418 to determine when conversion is complete (Control Register D6 = 0) - or the CPU waits for an interrupt (Control Register D6 = 1). When the CPU has read the data at the end of conversion, a new conversion is started on the next required channel.

EXTERNAL TRIGGER: In this mode, an external edge starts the conversion. Interrupt is generated when conversion is complete (Control Register D6 = 1).

Typical at 25°C and rated power supplies unless otherwise noted.

ANALOG INPUT SECTION	
INPUT CHARACTERISTICS	
Number of Channels	31 single-ended/15 differential
ADC Gain Ranges (Jumper Selectable)[1]	0-5V, 0-10V, ±2.5V, ±5V, ±10V
Amplifier Gain Ranges	
Resistor Programmable[2]	1 to 1000
Software Programmable	1 to 1024
Maximum Input Voltage Without Damage	±26 volts
Input Impedance	100MΩ, 10pF OFF Channel 100MΩ, 100pF ON Channel
Bias Current (25°C)(max)	20nA
Bias Current (0-70°C)(max)	70nA
Differential Bias Current	20nA
Amplifier Input Offset Voltage	20μV
Amplifier Input Offset Voltage Drift	1μV/°C
TRANSFER CHARACTERISTICS	
Resolution	12 bits
Throughput Time (max) G = 1	
Resistor Programmable	38μsec
Software Programmable	350μsec
Throughput Time G = 1024	
Resistor Programmable	100μsec
Software Programmable	350μsec
ACCURACY	
System Accuracy at +25°C (max)[3] G = 1	±0.0325% FSR[4]
System Accuracy at +25°C (max) G = 1024	±0.45% FSR
Linearity	±1/2LSB
Differential Linearity	±1/2LSB
Quantizing Error	±1/2LSB
Gain Error	Adjustable to Zero[6]
Offset Error	Adjustable to Zero
Monotonicity[5]	Guaranteed 0°C to +70°C
STABILITY OVER TEMPERATURE (Bipolar)[7]	
System Accuracy Drift (max) G = 1	±45ppm of FSR/°C
System Accuracy Drift G = 1024	±100ppm of FSR/°C
DYNAMIC ACCURACY	
Sample/Hold Aperture Time	30ns
Aperture Time Uncertainity	±5ns
Differential Amplifier CMRR G = 1	74dB (DC to 1kHz)
Channel Crosstalk	80dB down at 1kHz, for OFF Channai to ON Channel
ANALOG OUTPUT SECTION	
OUTPUT CHARACTERISTICS	
Number of Channels	2
Output Voltage Ranges (Strap Selectable)	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA
Output Impedance	1Ω
Short Circuit Protection	Yes
TRANSFER CHARACTERISTICS	
Resolution	12 bits
Output Settling Time (max)	10μsec
ACCURACY	
Output Accuracy	±0.0125% FSR
Temperature Coefficient of Accuracy	±30ppm of FSR/°C
POWER REQUIREMENTS	
MP8418	+5V ±5% at 2.0 amp
ENVIRONMENTAL	
Operating Temperature	0°C to +70°C
Storage Temperature	-25°C to +85°C
Relative Humidity	95% noncondensing

TABLE I. Electrical Specifications

NOTES:
1. Factory set for ±10V range.
2. Factory set for Gain = 1.
3. Includes linearity errors with gain and offset errors adjusted to zero.
4. FSR means Full Scale Range.
5. No missing codes guaranteed.
6. When any one gain range is adjusted to zero gain error, the gain error for any other range is less than ±0.02% when using the software programmable amplifier.
7. Includes offset drift, gain drift and linearity drift.

FACTORY MODE CONNECTIONS	
MODEL	FACTORY SET MODE
MP8418	HALT
MP8418-AO	HALT
MP8418-PGA	POLLING/INTERRUPT*
MP8418-PGA-AO	POLLING/INTERRUPT*

Note: Any model can be connected in any mode.
*Int 1/ Factory Set

TABLE II. Programming Mode Connections

JUMPER REQUIRED	
Halt Mode	JP17, JP29, JP30
Polling and Interrupt Mode	JP17, JP29
Continuous Mode	JP17, JP31
External Trigger Mode	JP16, JP29

TABLE III. Mode Selection Jumpers

JUMPERS REQUIRED FOR INTERRUPT VECTOR	
INT0/	JP70
INT1/	JP71
INT2/	JP72
INT3/	JP73
INT4/	JP74
INT5/	JP75
INT6/	JP76
INT7/	JP77

TABLE IV. Interrupt Selection

MEMORY MAP

Factory Set	ADR7 ... ADR0		READ		WRITE
F700	0000 0000	CH0	8LSB's of offset		N/A / GAIN 0*
F701	0000 0001	IN	STATUS		CONTROL
F702	0000 0010	CH1	LSB		N/A / GAIN 1*
F703	0000 0011	IN	MSB		N/A
F704	0000 0100	CH2	LSB	CH0 OUT	LSB ..... / GAIN 2*
F705	0000 0101	IN	MSB	or GAIN	MSB
F706	0000 0110	CH3	LSB	CH1 OUT	LSB ..... / GAIN 3*
F707	0000 0111	IN	MSB	or GAIN	MSB
F708	0000 1000	CH4	LSB		N/A / GAIN 4*
F709	0000 1001	IN	MSB		N/A
			⋮		⋮
F71E	0001 1110	CH15	LSB		N/A / GAIN 15*
F71F	0001 1111	IN	MSB		N/A
F710	0001 0000	CH16	LSB		N/A / GAIN 16*
F711	0001 0001	IN	MSB		N/A

N/A - Not used.

STATUS REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
Convert Complete	Interrupt Enable	Write* Enable	RAM* Enable	--------	GAIN X*	----------	

*Used only on versions with software programmable amplifier.

Convert Complete - The bit is low during conversion. It goes high on completion of conversion and remains high until the MSB of a data word is read.

Interrupt enable: status of interrupt enable
Write enable: status of write enable
RAM enable: status of RAM enable
GAIN X: current value stored in PGA GAIN control register.

CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
Not Used	Interrupt Enable	Write* Enable	RAM* Enable	_ _ _ _ _	GAIN X*	_ _ _ _ _ _ _	

*Used only on versions with software programmable amplifier.

Interrupt enable: A "1" enables interrupt; A "0" disables interrupt

Write enable: A "1" enables the CPU to write the gain for each channel to the RAM. A "0" prevents the CPU from writing to the RAM.

RAM enable: A "0" disables the internal RAM and the CPU must write a gain into GAIN X. A "1" enables the RAM to supply gains as stored.

GAIN X: if the RAM is not used to store gain information, the gain may be written to GAIN X. The gain remains as written to GAIN X until a new value is written.

Channel zero is connected to the board's analog ground and may be used as a zero reference for auto calibration routine. To clear the board after channel zero data has been obtained, another channel's MSB must be read.

ADDRESS MODIFICATION

The base address of a board can be set to any value by properly jumpering its address selector. The base address set at the factory is F700. To change the sense of a bit simply reverse the connection of its jumper.

Address	Factory Set	Insert for a "0"	Insert for a "1"
ADR 5	0	JP34	JP40
ADR 6	0	JP32	JP38
ADR 7	0	JP35	JP41
ADR 8	1	JP58	JP50
ADR 9	1	JP59	JP51
ADR A	1	JP60	JP52
ADR B	0	JP61	JP53
ADR C	1	JP62	JP54
ADR D	1	JP63	JP55
ADR E	1	JP64	JP56
ADR F	1	JP65	JP57

TABLE V. Address Jumpers

ANALOG OUTPUT RANGE SELECTION

Each DAC, when included, is jumpered at the factory for ±10 volt operation (two's complement coding). It is possible, however, to alter jumpers on the board for other output voltages and coding. See Table VI. When making a change, just remove those jumpers indicated for the present range and replace them with the jumpers required for the desired range.

RANGE	DAC1	DAC2
±10	JP23, 25	JP19, 28
±5	JP23, 24	JP19, 27
±2.5	JP23, 24, 26	JP14, 20, 27
0 to +10	JP22, 24	JP18, 27
0 to +5	JP22, 24, 26	JP18, 20, 27
Coding		
Two's Complement	JP46	
Straight Binary	JP47	

TABLE VI. Analog Output Range Selection

Two's complement coding is typically used for bipolar ranges and straight binary for unipolar ranges, but either coding can be used for any range.

BIPOLAR - TWO'S COMPLEMENT			
Digital Input	±10V	±5V	±2.5V
(0000)* 0111 1111 1111/(0)*7FF$_{16}$	+9.9951V	+4.9976V	+2.4988V
(1111)* 1000 0000 0000/(F)*800$_{16}$	-10.000V	-5.000V	-2.500V
*The unused four most significant bits are tied to the most significant bit of the data word.			

UNIPOLAR - STRAIGHT BINARY		
Digital Input	0 to +10V	0 to +5V
(0000)* 1111 1111 1111/(0)*FFF$_{16}$	9.9775V	4.9988V
(0000) 0000 0000 0000/(0)*000$_{16}$	0.000V	0.000V
*The four most significant bits are tied to ground.		

TABLE VII. Analog Full Scale Range Values

ANALOG INPUT RANGE SELECTION

Software Programmable Amplifier (MP8418-PGA, MP8418-PGA-AO)

The analog input system as shipped from the factory can be software set for input ranges of ±10V to ±10mV. Table VIII gives the input ranges for each gain value.

Gain Setting	Amplifier Gain	Input Range*	LSB Value
0000	1	±10V	4.883mV
0001	2	±5V	2.441mV
0010	4	±2.5	1.221mV
0011	4	±2.5	
0100	4	±2.5	
0101	8	±1.25	610.4μV
0110	16	±625mV	305.2μV
0111	16	±625mV	
1000	32	±312.5mV	152.6μV
1001	64	±156.3mV	76.29μV
1010	128	±78.13mV	38.14μV
1011	128	±78.13mV	
1100	256	±39.06mV	19.07μV
1101	512	±19.53mV	9.537μV
1110	1024	±9.766mV	4.768μV
1111	1024	±9.766mV	4.768μV
*Assumes A/D converter input range of ±10V.			

TABLE VIII. Software Programmable Amplifier Input Ranges

Resistor Programmable Amplifier - (MP8418, MP8418-AO)

The analog input system can be set for any range between ±10V and 10mV. It is set for ±10V (two's complement coding) at the factory.

There are two gain determining elements in this system: the A/D converter and the instrumentation amplifier

(IA). The A/D converter is factory set for a ±10V range and the IA for a gain of 1. The A/D converter can be set for other ranges by simply changing jumpers as shown in Table IX. Before adding new jumpers, remove those indicated for the present range.

RANGE	JUMPERS
±10V	JP12, 14
±5V	JP11, 14
±2.5V	JP11, 13, 14
0 to +10V	JP11, 15
0 to +5V	JP11, 13, 15

TABLE IX. A/D Converter Range Setting Jumpers

MP8418 is factory jumpered for two's complement operation (see Table X) with jumper JP49 inserted and JP48 open. For operation in the straight binary mode (any range) jumper JP49 is open and JP48 is inserted.

TWO'S COMPLEMENT		
(0000)* 0111 1111 1111	$07FF_{16}$	Positive Full Scale
(0000) 0000 0000 0000	0000_{16}	Mid Scale
(1111) 1000 0000 0000	$F800_{16}$	Negative Full Scale
*Four most significant bits are tied to most significant bit of A/D converter.		
STRAIGHT BINARY		
(0000)* 1111 1111 1111	$0FFF_{16}$	Positive Full Scale
(0000)* 1000 0000 0000	0800_{16}	Mid Scale
(0000)* 0000 0000 0000	0000_{16}	Negative Full Scale
*Four most significant bits are tied to zero.		

TABLE X. Analog Input Codes

ANALOG INPUT LOW LEVEL OPERATION

Pads for external gain setting resistors are provided so that the instrumentation amplifier can be user set for gains to 1000. Use this formula to calculate the resistance value: Gain = 1 + 20kΩ/R_{EXT} where R_{EXT} is R13 in parallel with R14. The gain adjustment potentiometer on the board provides an adjustment range of ±1%. Therefore, if an R_{EXT} with an accuracy of ±0.5% is used, the on-board potentiometer will have sufficient range for adjustment. Stable (5ppm) resistors should be used in this application. As shipped from the factory, G = 1.

Settling time of the amplifier increases as gain increases. A delay time of 38 microseconds is set at the factory to allow for multiplexer and amplifier settling times. This delay time is sufficient for amplifier gains up to 50. For gains larger than 50, a longer delay time is required. A delay of 100 microseconds will be obtained by removing R36. This delay time is sufficient for gains up to 1000.

For lowest system noise, the ADC range should be set at the ±10V or 0 to 10V ranges with the amplifier providing all the system gain.

SINGLE-ENDED/DIFFERENTIAL OPERATION

MP8418's are connected at the factory for 15 channels differential. They can be converted to 31 channels single-ended by simply changing a few board jumpers. Table XI indicates those jumpers that must be present for a given mode of operation. To convert from one mode to the other, remove those jumpers indicated for the present type of operation and install those necessary for the operation.

Jumper Required for Differential	Jumpers Required for Single-Ended
15 channels JP3, JP4, JP7	31 channels JP2, JP5

TABLE XI. MP8418 Channel Conversion

In noisy environments the differential mode of operation is recommended for use with low level analog signals which are more prone to noise interference. The MP8418 can also operate in a pseudo-differential mode. In this mode, the system has 31 channels as in the single-ended mode, but the minus input of the IA is connected to a remote common rather than grounded on the board. This mode is useful if there is a remote common to all input signals. It combines the advantages of single-ended operation (maximum number of channels) with the increased noise rejection of differential operation.

ANALOG INPUT CALIBRATION

If the input range of the resistor programmable amplifier is to be changed, use the following program to adjust gain and offset. The gain and offset errors of the MP8418-PGA may be optimized for any one range by calibrating the unit on that range. The board is factory calibrated on the ±10V range.

```
                        ;*****************************************************
                        ;
                        ;INPUT CALIBRATION ROUTINE FOR MP8418
                        ;
                        ;*****************************************************
                        ;
0000  00 F8   REFH      EQU     0F8H        ;OFFSET REF=F800H, FULL SCALE REF=07FFH
0000  00 00   REFL      EQU     00
0000  F7 00   BADD      EQU     0F700H      ;BOARD BASE ADDRESS
0000  01 E8   CO        EQU     01E8H       ;MONITOR ROUTINES
0000  01 F3   CROUT     EQU     01F3H
0000  02 C2   NMOUT     EQU     02C2H
                        ;
                        ;       ORG     3C50H
                        ;
3C50  21 02 F7          LXI     H,BADD+2    ;INITIALIZE
3C53  31 FF 3F          LXI     SP,3FFFH
3C56  1E 10   BEG1      MVI     E,10H
3C58  06 00   BEG2      MVI     B,0
3C5A  0E 64             MVI     C,64H
3C5C  56        CLP     MOV     D,M         ;START CONVERTION
3C5D  3A 01 F7  SRL     LDA     BADD+1      ;CHECK STATUS
3C60  17                RAL
3C61  D2 5D 3C          JNC     SRL         ;JUMP IF CONVERSION NOT COMPLETE
3C64  56                MOV     D,M         ;READ LEAST SIGNIFICANT BYTE
3C65  23                INX     H
3C66  7E                MOV     A,M         ;READ MOST SIGNIFICANT BYTE
3C67  2B                DCX     H
3C68  D6 F8             SUI     REFH        ;INCREMENT DATA COUNT IF DATA=REF
3C6A  C2 74 3C          JNZ     NEQ
3C6D  7A                MOV     A,D
3C6E  D6 00             SUI     REFL
3C70  C2 74 3C          JNZ     NEQ
3C73  04                INR     B
3C74  0D                DCR     C           ;HAVE 100 CONVERSIONS BEEN MADE?
3C75  C2 5C 3C          JNZ     CLP
3C78  78                MOV     A,B         ;YES, PRINT DATA COUNT
3C79  CD C2 02          CALL    NMOUT
3C7C  0E 20             MVI     C,20H       ;PRINT A SPACE
3C7E  CD E8 01          CALL    CO
3C81  1D                DCR     E           ;FULL LINE BEEN PRINTED?
3C82  C2 58 3C          JNZ     BEG2
3C85  CD F3 01          CALL    CROUT       ;YES, PRINT CR & LF
3C88  C3 56 3C          JMP     BEG1
3C8B                    END
```

This program is written for polling mode operation. It will operate in the HALT mode. However, memory locations 3C5D to 3C64 may be deleted for HALT mode operation.

The program assumes that the system is under control of the SBC80/10 prototype package monitor (M 80P, version 1.0, March 1, 1976) and may be used for both offset and gain calibration. The system offset should be adjusted first, followed by the gain adjustment.

If the address of board base address has been changed from $F700_{16}$ then the value of the base address (BADD) should reflect that change.

A G3C50 monitor command will begin program execution. After 100 conversions have been made, the value (in hex) of the B register will be printed. This value represents the number of times the data read from the board was equal to "REF" (F800 for offset, 07FF for gain).

RANGE	OFFSET	GAIN
±10V	-9.9976	+9.9927
±5V	-4.9988	+4.9963
0 to +10	+1.221	+9.99634
0 to +5	+0.610	+4.9982

TABLE XII. Analog Input Calibration Values

Calibration is performed by connecting a voltage source capable of 0.002% accuracy to input channel zero (this could also be a DC voltage source of less absolute accuracy whose output is monitored by a 0.002% DVM).

Offset and gain adjustments are made while applying the voltage listed in Table XII.

For other ranges, offset voltage adjustment is made at the most negative value of the range, less one-half least significant bit (LSB). An LSB is equal to the span (full scale range) divided by 4096 for 12 bit resolution. Gain adjustment is made at the most positive value of the range less 1-1/2LSB. Thus, for a range of ±50mV, an LSB is 100mV/4096 = 24.4μV. The offset adjustment is made at -50mV + 12.2μV = -49.9878mV and the gain adjustment at +50mV -36.6μV = 49.963mV. Before making these adjustments, however, allow the MP8418 to reach thermal equilibrium (about 30 minutes under power).

The offset adjustment is made first by using the appropriate offset calibration voltage. Run the calibration program and adjust the on-board offset potentiometer until B register contains a value between $1E_{16}$ and 46_{16} (30_{10} and 70_{10}).

To perform the gain adjustment, change the data labeled "REFH" in the calibration program from F8 to 07, the data labeled "REFL" from 00 to FF, set the input voltage to the value shown in Table XII, and adjust the on-board gain potentiometer in the same manner described for offset, above. If the SBC monitor is available, the substitute (S) command can be used to interrogate an input channel.

ANALOG OUTPUT CHECKOUT

It is simple to perform static checks of the two analog outputs. Load the H and L register pair with the output data word. An SHLD instruction can then be used to transfer data to a DAC. The base addresses of the analog outputs are factory set to values of $F704_{16}$ and $F706_{16}$. The ideal values for plus and minus full scale are shown in Table XIII.

DATA WORD	RANGE				
	±2.5V	±5.0V	±10V	0 to +5V	0 to +10V
$F800_{16}$	-2.5000V	-5.000V	-10.000V		
$07FF_{16}$	+2.4988V	+4.9976V	+9.9951V		
0000_{16}				0.0000V	0.0000V
$0FFF_{16}$				+4.9988V	+9.9976V

TABLE XIII. DAC Full Scale Values

Two's complement coding is shown for bipolar ranges; straight binary for unipolar ranges. If the SBC80 monitor is available, Insert (I) and Substitute (S) commands can also be used to accomplish an output write.

To check the dynamic characteristics of the analog outputs use the following program.

```
                ;*****************************************************
                ; 84DDCK.I80     MP8418-A0 & MP8418-PGA-A0 DYNAMIC DAC
                ;                                              CHECK
                ;*****************************************************
0000  F7 00     BADD    EQU     0F700H  ;BASE ADDRESS
                ;
                        ORG     3C40H
                ;
3C40  21 FF 07          LXI     H,07FFH ;SET DATA VALUE
3C43  22 04 F7  LOOP    SHLD    BADD+4  ;SET DAC 1
3C46  22 06 F7          SHLD    BADD+6  ;SET DAC 2
3C49  7C                MOV     A,H     ;COMPLIMENT DATA VALUE
3C4A  2F                CMA
3C4B  67                MOV     H,A
3C4C  7D                MOV     A,L
3C4D  2F                CMA
3C4E  6F                MOV     L,A
3C4F  C3 43 3C          JMP     LOOP
3C52                    END
```

A 14kHz square-wave will be present on both DAC outputs.

ANALOG OUTPUT CALIBRATION

Analog outputs can be calibrated through the use of the SBC80 and its monitor. With the board installed, allow the system to reach thermal equilibrium (about 30 minutes under power) before starting the procedure.

Start calibration by loading DAC1 with data that will produce its most negative output. This is done via the monitor's S command since each DAC appears as two adjacent memory locations. For two's complement operation this data is $F800_{16}$ and for straight binary the data is 0000_{16}. The least significant 8 bits of data is transferred first into location $F704_{16}$ with the most significant 4 bits loaded next into location $F705_{16}$. The DAC should then be set by its offset control to the appropriate low voltage value shown in Table XIV. The gain control is adjusted in a similar manner, after setting the DAC to its most positive output. For a two's complement DAC, the input data is $07FF_{16}$. For a straight binary unit, the data is $0FFF_{16}$. The gain control is used to set the DAC output to the high voltage value indicated in Table XIV. The remaining DAC is calibrated in the same way. As shipped from the factory, the DAC's occupy these adjacent memory locations:

DAC1 - F704, F705
DAC2 - F706, F707

RANGE	LOW	HIGH	ILSB
±10V	-10.000V	+9.9951V	4.88mV
±5V	-5.000V	+4.9976V	2.44mV
±2.5V	-2.500V	+2.4988V	1.22mV
0 to +10V	0.0V	+9.9975V	2.44mV
0 to +5V	0.0V	+4.9988V	1.22mV

TABLE XIV. DAC Calibration Values

OPERATION SUMMARY

MP8418 boards are shipped from the factory ready for immediate use. However, they do have a number of user selectable options. These options, which have already

been described, are summarized below:

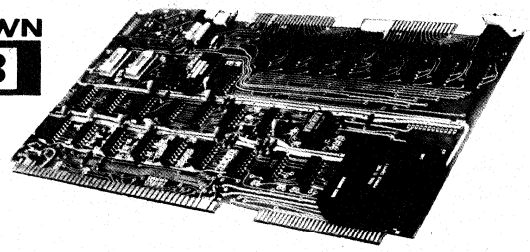
1. Programming Mode. Units are factory set to either the HALT or INTERRUPT Mode (Table II). They may be user connected for HALT, INTERRUPT, POLLING, CONTINUOUS or in EXTERNAL TRIGGER modes as described previously. Table IV describes the selection of one of eight interrupt vectors.

2. Address. These units are memory mapped and factory set for a base address of $F700_{16}$. Table V describes the jumpers which allow the user to configure these units for any address.

3. Analog Input Range. Two input amplifier systems are available with these units: resistor programmable amplifier or a software programmable amplifier. In both cases, the A/D converter may be any of five input ranges (Table VII). The resistor programmable amplifier is factory set for a gain of 1. It may be user set for gains between 1 and 1000 as described previously. The gain of the software programmable amplifier may be stored in an on-board RAM for each channel with gains of 1 to 1024 (Table VIII). These units are factory connected as 15 channel differential, and may be user connected for 31 channels, single-ended operation as shown in Table XI.

4. Analog Output Range. For units with Analog Output options, the on-board D/A Converters are factory set for the ±10V range. The D/A Converters may be set for other ranges as shown in Table VI.

BURR-BROWN

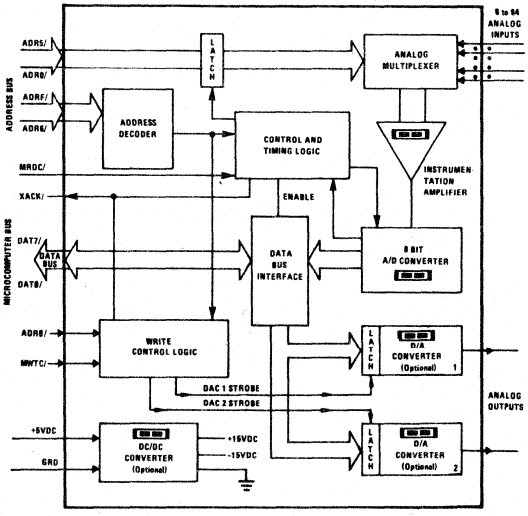


MP8608
MP8616
MP8632

MICROCOMPUTER ANALOG I/O SYSTEMS

FEATURES

- INTEL-SBC80 and INTELLEC MDS COMPATIBLE
- NATIONAL-BLC80 COMPATIBLE
- LOW COST
- 70°C BURN-IN
- EASY TO PROGRAM
  Systems are treated as memory
- REDUCES SYSTEM DEVELOPMENT TIME
  System engineered and specified
  Operates from computer's +5VDC
  power supply if desired
- EASY TO USE
  8 to 64 input channels on one board
  Analog input and output on one board



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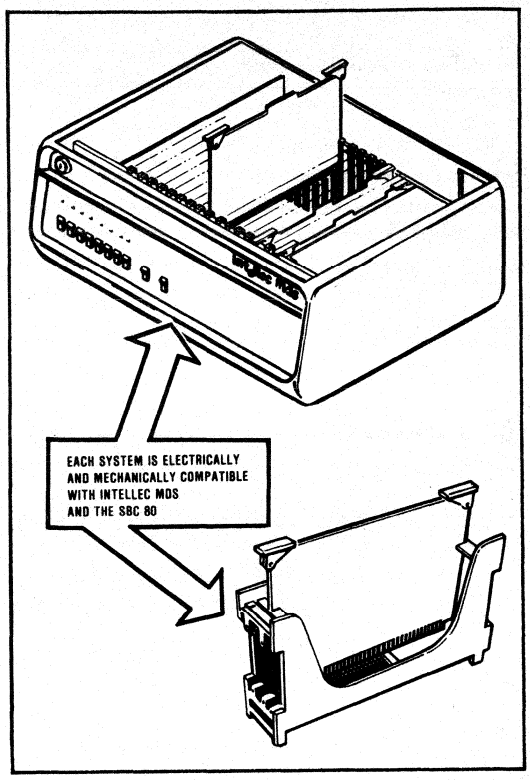
PDS-368A

Printed in U.S.A. July, 1978

DESCRIPTION

These microcomputer peripherals provide two functions that interface directly to Intel's SBC80 and Intellec MDS microcomputers. The functions are: (1) Analog Data Acquisition and (2) Analog Output. The devices are electrically and mechanically compatible with any SBC80 and Intellec MDS. Both analog input and output systems are contained on a single printed circuit board that is treated as memory input or output by the CPU. The cards will mate to any memory or I/O slot. They are compatible with the 0.6" spacing of the SBC80 or the 0.75" spacing of the Intellec MDS. The analog interface for each system is a connector at the opposite edge of the board from the bus connector.

The Data Acquisition system is available with up to 64 channels single-ended on one board. It includes an input multiplexer, high gain instrumentation amplifier, 8-bit A/D converter along with all the necessary timing, decoding and control logic. A DC/DC converter (+5V to ±15V) is also available so that only the computer's power supply is required. The Data Acquisition System is available with two optional 8-bit D/A converters to provide analog input and output on the same board.



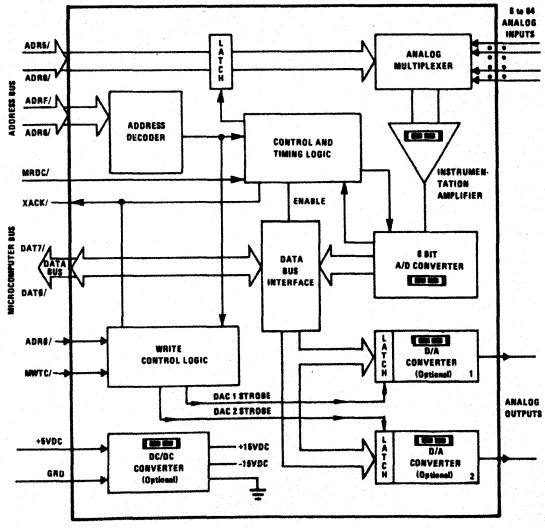
THEORY OF OPERATION

When programming with these peripherals, they are treated as memory locations. Any memory reference instruction can be used. Both the A/D converter output and the D/A converter input are 8-bit words so one memory location is needed for each channel. Because the address block occupied by each peripheral is user selectable, it can be placed anywhere in memory.

Because these units are treated as memory, a minimum of instructions are needed to read an input channel or to set the input of a D/A converter. For instance, the LHLD (load) instruction followed by the proper address can be used to read data from two successive analog input channels. It will automatically select the desired channel, initiate conversion and when conversion is complete, transfer the A/D converter output for the first channel to the 8080's L register and the second channel to the H register. Likewise a single LDA instruction can be used to read one analog input channel.

All of these systems are jumpered at the factory with the first channel at address $F700_{16}$. Each subsequent channel is one memory location past the start of the last channel so that the second channel is at location $F701_{16}$.

ANALOG INPUT/ OUTPUT SYSTEM



SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ANALOG INPUT/OUTPUT SYSTEM

ANALOG INPUT

Number of analog inputs	
8 differential	MP8608
16 single-ended	MP8616
32 differential or 64 single-ended [5]	MP8632
Input voltage range[1]	±10mV to ±5V
ADC gain ranges[1]	±10V, 0 to 10V, 0 to 5V
(strap selectable)	±5V, ±2.5V
Amplifier gain range[1]	1 to 1000 V/V
(resistor programmable)	
Amplifier gain equation	$G = 100k\Omega/R_{EXT}$
Input overvoltage protection	±15V
Input impedance	100 megohms
Bias current	
25°C (max)	+300nA
0°C to 70°C	-2nA/°C
Amplifier input offset voltage	±2mV
Amplifier input offset voltage drift	$\pm(5 + \frac{1000}{G})$ μV/°C

ANALOG INPUT TRANSFER CHARACTERISTICS

Resolution	8 bit binary
Throughput accuracy ±5V range (max)	±0.4% FSR[2]
±10mV range	±0.5% FSR
Temperature coefficient of accuracy	
±5V range (max)	±0.02% FSR/°C
±10mV range	±0.07% FSR/°C
Conversion time ±5V range	44 microseconds
±10mV range	84 microseconds
CMRR (for differential inputs)[3]	66 dB (Gain = 2)
	86 dB (Gain = 100)

ANALOG OUTPUT

Number of analog outputs	2
Output voltage range[4]	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA (strap selectable)
Output impedance	1Ω
Output settling time (max)	< 5 microseconds

ANALOG OUTPUT TRANSFER CHARACTERISTICS

Resolution	8 bits binary
Throughput accuracy (max)	±0.4% FSR
Temperature coefficient of accuracy	
Unipolar	±0.005% FSR/°C
Bipolar	±0.01% FSR/°C

DIGITAL INPUT/OUTPUT

All signals are compatible with Microcomputer Bus	
Output coding	Bipolar, two's complement; Unipolar, straight binary
An analog input channel is selected by:	ADR0/ through ADR5/
An analog output channel is selected by:	ADR0/
The input/output data bits are read through:	DAT0/ through DAT 7/

POWER REQUIREMENTS

MP8608, MP8616, MP8632,	+5VDC ±5% at 1 amp, 25mV ripple
MP8608-NS, MP8616-NS, MP8632-NS	+5VDC ±5% at 500mA, 25mV ripple +15VDC ±3% at 40mA, 5mV ripple -15VDC ±3% at 40mA, 5mV ripple
With analog output	
MP8608-AO, MP8616-AO, MP8632-AO	+5VDC ±5% at 2 amp, 25mV ripple
MP8608-NS-AO, MP8616-NS-AO, MP8632-NS-AO,	+5VDC ±5% at 500mA, 25mV ripple +15VDC ±3% at 100mA, 5mV ripple -15VDC ±3% at 100mA, 5mV ripple

TEMPERATURE RANGE

0°C to 70°C

OPERATING INSTRUCTIONS

INSTALLATION

These units are shipped from the factory calibrated and ready for immediate use. Installation requires only plugging the card into any empty slot in the computer and wiring the analog connector.

PROGRAMMING

Programming of this analog I/O board is easily accomplished since all channels are treated as memory locations. Any memory reference instruction can be used. A single STA instruction may be used to load the accumulator contents to one of the D/A converters. Likewise a single LDA instruction can be used to read an analog input channel.

Single instructions can also be used to set the inputs of both D/A converters and read two adjacent analog input channels. An SHLD instruction referenced to DAC 1 will load the contents of the L register into DAC 1 and the contents of the H register into DAC 2. An LHLD instruction will read the channel addressed and the next higher channel. The channel addressed will be transferred to the L register and the next higher channel to the H register. Of course, any MOV instruction may also be used if direct addressing is not desired.

The normal operation of this board halts the CPU during the conversion time of the analog input system. This is because the software in this mode is simpler than in any other (i.e., only one instruction required!). If the halt feature is not desirable, it may be disabled. Figure 1 shows the jumpers required. The jumpers shown with an asterisk are plated-through holes and must be drilled out before installation of the other jumpers. A 0.055" (No. 54) drill should be used for this purpose. Caution must be exercised to prevent damage to the board (see Figure 2).

MECHANICAL CHARACTERISTICS

Compatible with Intellec MDS and SBC-604/614 card spacing.

Minimum card spacing: 12.7mm (0.5").

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers.

50 pin analog edge connector on board.

Mating connector available from Burr-Brown: 2250MC (Viking # 3VH25/1JN5, solder tab); from 3M: 3415-0001 (Scotchflex).

(1) Connected at the factory for ±5V range (ADC range = ±10V, Gain = 2).
(2) FSR is Full Scale Range (i.e., 10V for ±5V range).
(3) DC to 60Hz with 1kΩ source unbalance.
(4) Connected at the factory for ±10V range.
(5) Connected at the factory as 32 differential.

OPERATION WITH HALT. JUMPERS REQUIRED	OPERATION WITHOUT HALT. JUMPERS REQUIRED
W55*, W56*, W57*	W53, W54, W58

FIGURE 1. Halt Selection Jumpers

For operation without halting the CPU, the conversion should be started by using a single channel memory reference instruction (LDA or MOV). Then the CPU should execute a routine which will take longer than the conversion time (44 to 84 microseconds). When the CPU now uses an LDA or MOV referenced to the same memory location, the converted data will be transferred to the CPU.

The voltage data for these boards is represented by an 8-bit two's complement binary number. With a ±5V range, each bit has a value of 39.1mV, with the polarity of the voltage indicated by the sign of the binary number.

Each board is set at the factory for a block of addresses beginning at F700. Any analog data channel requires one memory location. Thus the first analog channel is located at F700 while the second analog channel is located at F701.

ADDRESS MODIFICATION

The base address of a board can be set to any value by properly jumpering its address selector. The most significant 8 bits of the address (ADR/8-F) are jumpered to read F7 by plated through connections on all boards. These addresses can be changed by first drilling out the hole that makes the connection (Figure 2) and then soldering a wire jumper between the bit and logical zero or one. A 0.055" (No. 54) drill should be used for this purpose. Caution must be exercised to prevent damage to the board and the scattering of metal particles over its surface.

The remaining lower ordered bits have been connected by wire jumpers at the factory. To change the sense of a bit simply reverse the connection of its jumper.

ADDRESS	HIGH	LOW
4	W37	W38
5	W35	W36
6	W33	W34
7	W31	W32
8	W29*	W30
9	W27*	W28
A	W25*	W26
B	W23	W24*
C	W21*	W22
D	W19*	W20
E	W17*	W18
F	W15*	W16

* Plated through jumpers

ADDRESS JUMPERS

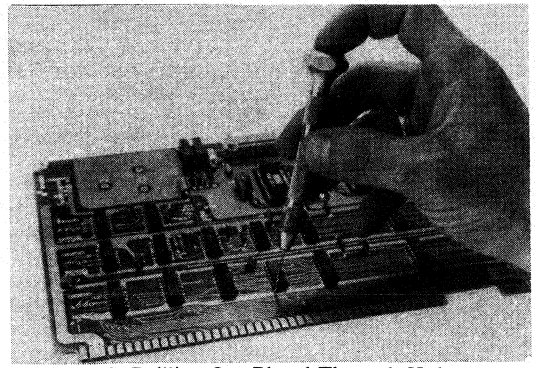


FIGURE 2. Drilling Out Plated Through Holes

ANALOG OUTPUT RANGE SELECTION

When included, each DAC is jumpered at the factory for ±10 volt operation (two's complement coding). However, it is possible to alter these jumpers as shown in Figure 3 for other output voltages and coding. Jumpers indicated by an asterisk are plated through holes on the board and should be removed by drilling as described in the section on address modification. When making a change, first remove those jumpers indicated for the present range and replace them with those jumpers required for the desired range.

Range	DAC 1	DAC 2
±10	W66*, W67*	W70*, W72*
±5	W65, W67*	W69, W72*
±2.5	W65, W67*, W74	W69, W72*, W73
0 to +10	W65	W69
0 to +5	W65, W74	W69, W73
Coding		
Two's Complement	W61*	W63*
Straight Binary	W62	W64

FIGURE 3. Analog Output Range Selection

Two's complement coding is typically used for bipolar ranges and straight binary for unipolar ranges, but either coding can be used for any range.

BIPOLAR - TWO'S COMPLEMENT			
Digital Input/Output	±10V	±5V	±2.5V
01111111 ($7F_{16}$)	+9.922V	+4.961V	+2.480V
10000000 (80_{16})	-10.000V	-5.000V	-2.500V
UNIPOLAR - STRAIGHT BINARY			
Digital	Input/Output	0 to +10V	
11111111 (FF_{16})	9.961V	4.980V	
00000000 (00_{16})	0.000V	0.000V	

TABLE I. Analog Full Scale Range Values.

ANALOG INPUT RANGE SELECTION

The analog input system can be set for any range between ±5V and ±2.5mV. It is set for ±5V (two's complement

coding) from the factory. There are two gain determining elements in this system: the A/D converter and the instrumentation amplifier (IA). The A/D converter is set for a ±10V range and the IA for a gain of 2 at the factory. The A/D converter can be set for other ranges simply by changing jumpers as shown in Figure 4. Before adding new jumpers, remove those indicated for the present range. The input voltage presented to the analog multiplexer must not exceed 5.25VDC for proper operation.

RANGE	JUMPERS
±10V	W1*, W2*
±5V	W2*, W4
±2.5V	W2*, W4, W5
0 to +10V	W3, W4
0 to +5V	W3, W4, W5

*Plated through jumpers

FIGURE 4. A/D Converter Range Setting Jumpers

As configured at the factory, this board is jumpered for two's complement operation (see Table I above) with jumper W59* inserted and W60 open. For operation in the straight binary mode (any range) jumper W59* is open and W60 is inserted.

ANALOG INPUT LOW LEVEL OPERATION

Pads for external gain setting resistors (see Figure 7) have been provided so that the instrumentation amplifier can be user set for gains to 1000. The following formula can be used to calculate the value of the resistance: Gain = 100 kΩ/R_{EXT}, where R_{EXT} is the resistance between pins 1 and 12 of the IA (R15, 94 in parallel form R_{EXT} in Figure 7). The gain adjustment potentiometer on the board will give an adjustment range of ±1%. Therefore, if an R_{EXT} with an accuracy of ±0.5% is used, the on-board potentiometer will have sufficient range for adjustment. Stable (50ppm) resistors should be used in this application. As shipped from the factory, R15 = 49.9kΩ. The settling time of the amplifier increases as the gain increases. A delay time of 41 microseconds is set at the factory to allow for multiplexer and amplifier settling times. This delay time is sufficient for amplifier gains of up to 50. For gains larger than 50, a longer delay time is required. A delay time of 81 microseconds will be obtained by removing R17. This delay time is sufficient for gains of up to 1000.

For lowest system noise, the ADC range should be set on the ±10V or 0 to 10V ranges with the amplifier providing all the system gain.

A 64/32 channel input board can be converted from single-ended operation to differential operation or vice versa by simply changing a few board jumpers (MP8632 from/to MP8664). Figure 5 indicates those jumpers that must be present for a given mode of operation. To convert from one mode to the other remove those jumpers indicated for the present type of operation and install those necessary for the desired mode of operation.

Required Jumpers for Differential	Required Jumpers for Single-ended
32 Channels	64 Channels
W8	W6
W9	W7
	W10

FIGURE 5. MP8632 Channel Conversion

The differential mode of operation should be used for analog signals in noisy environments. The differential mode is particularly useful for low level signals since they are more prone to noise than high level signals. This board can also operate in a pseudo-differential mode. In this mode, the system has the number of channels of the single-ended mode, but the minus input of the IA is connected to a remote common rather than grounded on the board. This mode of operation is useful if there is a remote ground common to all the input signals. In this way the advantages of single-ended operation (maximum number of channels) and differential operation (better noise rejection) are combined. Jumpers W10 and W52 are installed and W7 is removed for this mode of operation.

ANALOG OUTPUT CHECKOUT

A static check of the two analog outputs is very simple. Load the L register with the output 1 data word and the H register with the output 2 data word. An SHLD instruction can then be used to transfer the data to the DAC's. The addresses of the analog outputs are set at the factory to values of $F700_{16}$ and $F701_{16}$. The ideal values for plus and minus full scale are shown in Figure 6.

DATA WORD	RANGE				
	±2.5V	±5.0V	±10V	0 to +5V	0 to +10
80_{16}	-2.500	-5.000	-10.000		
$7F_{16}$	+2.480	+4.961	+9.922		
00_{16}				0.000	0.000
FF_{16}				+4.980	+9.961

FIGURE 6. DAC Full Scale Values.

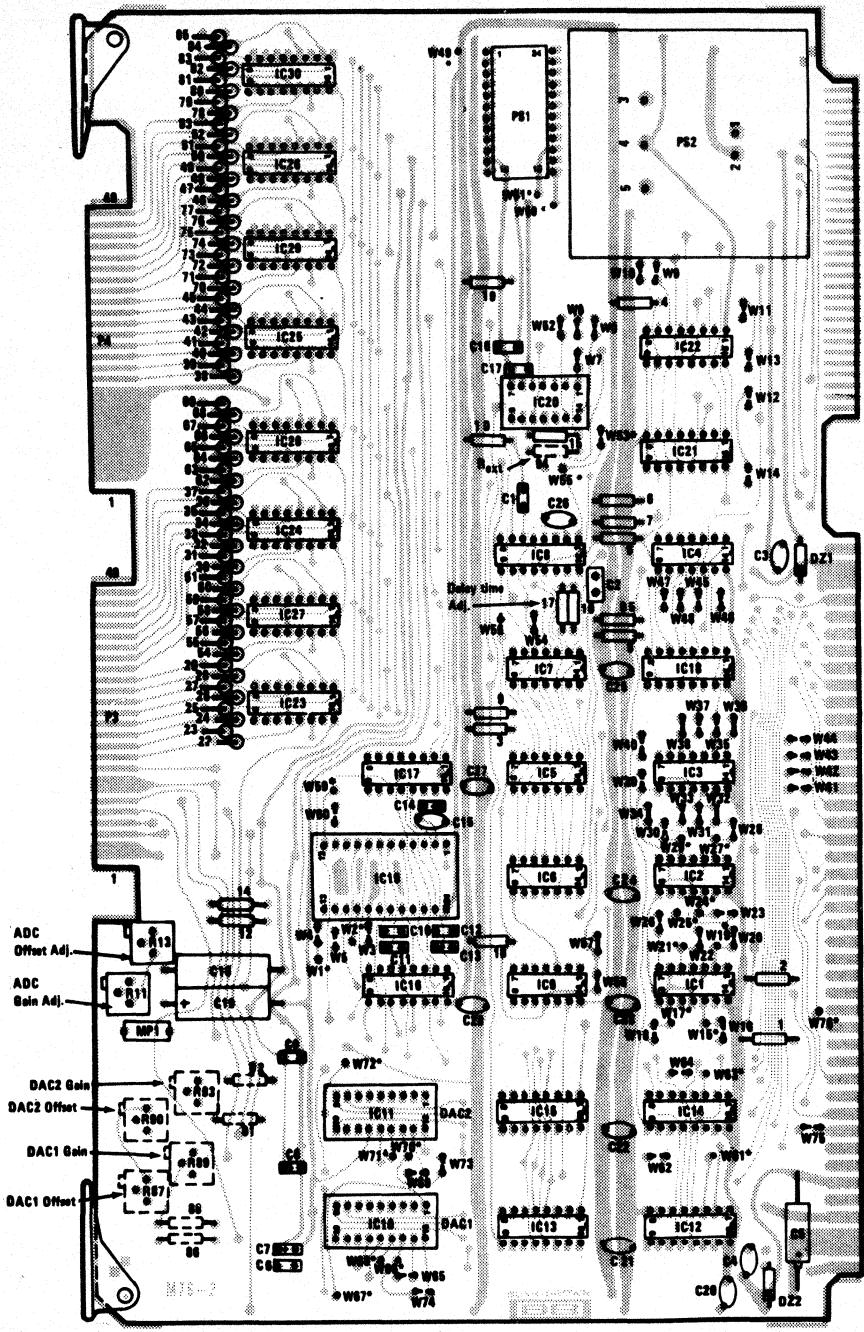
Two's complement coding is shown for bipolar ranges; straight binary for unipolar ranges.

If the SBC80/10 monitor is available, the Insert (I) and Substitute (S) commands can also be used to accomplish an output write.

To check the dynamic characteristics of the analog outputs the following program can be used.

```
        ORG   3C40H
        LXI   H, 0F700H ; Set H & L to DAC 1 Address
        MVI   A, 7FH    ;Initialize Data Word
LOOP:   MOV   M,A       ;Load DAC 1
        INX   H
        MOV   M, A      ;Load DAC 2
        DCX   H
        CMA             ;Compliment Data Word
        JMP   LOOP
        END
```

A 27 kHz square-wave will be present on both DAC outputs.



MP8600 SERIES BOARD LAYOUT
(TOP VIEW)

FIGURE 7.

ANALOG INPUT CALIBRATION

These systems are set at the factory for a ±5V input range. If the input system range is to be changed, the following program may be used to adjust gain and offset.

```
REF     EQU   80H          ;Offset Ref = 80H, Full Scale Ref = 07FH
CO      EQU   01E8H        ;Monitor routines
CROUT   EQU   01F3H
NMOUT   EQU   02C2H
        ;
        ORG   3C50H
        ;
        LXI   H, 0F700H ;Initialize
        LXI   SP, 3FFFH
BEG1:   MVI   E, 10H
BEG2:   LXI   B, 0
CLP:    MOV   A, M         ;Read data from board
        SUI   REF          ;Increment data count if data = REF
        JNZ   NEQ
        INR   B
NEQ:    INR   C            ;Have 100 conversions been made?
        MVI   A, 64H
        SUB   C
        JNZ   CLP
        MOV   A, B         ;Yes, Print data count
        CALL  NMOUT
        MVI   C, 20H       ;Print a space
        CALL  CO
        DCR   E            ;Full line been printed?
        JNZ   BEG2
        CALL  CROUT        ;Yes, Print CR & LF
        JMP   BEG1
        END
```

The program assumes that the system is under the control of the SBC80/10 prototype package monitor (M80P, version 1.0, March 1, 1976). It may be used for both offset and gain calibration. The system offset should be adjusted first, followed by the gain adjustment.

If the address of channel zero on the board has been changed from $F700_{16}$ then the LXI H instruction should reflect that change.

A G3C50 monitor command will begin program execution. After 100 conversions have been made, the value (in hex) of the B register will be printed. This value represents the number of times the data read from the board was equal to "REF" (80 for offset; 7F for gain).

RANGE	OFFSET	GAIN
±5V	-4.980	+4.941
0 to +10	+19.53mV	+9.941
0 to +5	+9.766mV	+4.971

FIGURE 8. Analog Input Calibration Values

Calibration is performed by connecting a voltage source capable of 0.01% accuracy to input channel zero (this could also be a DC voltage source of less absolute accuracy whose output is monitored by a 0.01% DVM).

The offset and gain adjustments are made while applying the voltage shown in Figure 8. For other ranges, the offset voltage adjustment is made at the most negative value of the range less one half least significant bit (LSB). An LSB is equal to the span (full scale range) divided by 256 for 8 bit resolution. The gain adjustment is made at the most positive value of the range less 1 1/2 LSB. Thus for a range of ±50mV, an LSB is 100mV/256 = 391μV. The offset adjustment is made at -50mV + 195μV = -49.80mV and the gain adjustment at +50mV - 586μV = 49.41mV. Before making these adjustments, however, the unit should be allowed to reach thermal equilibrium (about 30 minutes under power).

The offset adjustment is made first by using the appropriate offset calibration voltage. Run the calibration program and adjust the on board offset potentiometer until the B register contains a value between $1E_{16}$ and 46_{16} (30_{10} and 70_{10}).

To perform the gain adjustment change the data labeled "REF" in the calibration program from 80 to 7F, set the input voltage to the correct value as shown in Figure 8 and adjust the on board gain potentiometer in the same manner as described for offset.

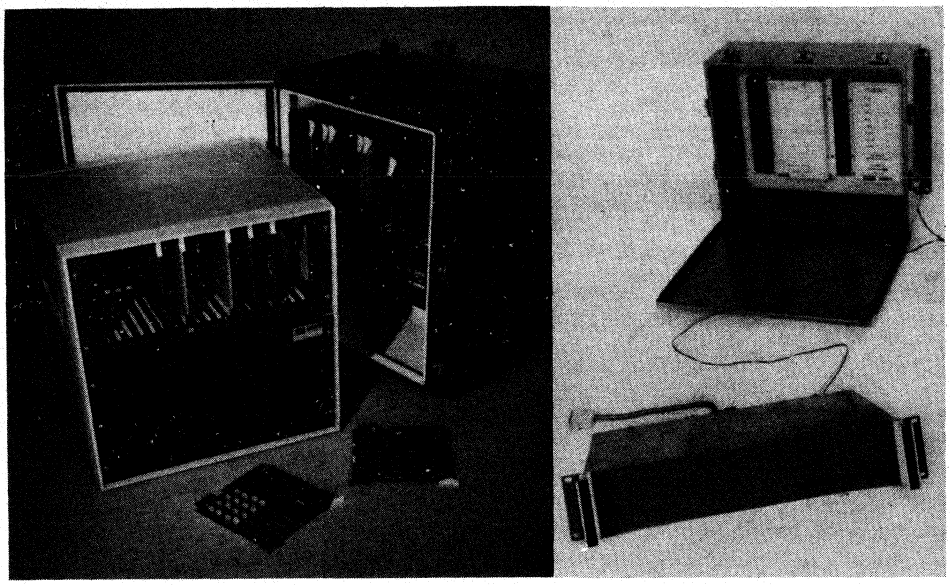
If the SBC80 monitor is available, the substitute (S) command can be used to interrogate an input channel.

CONNECTOR PINOUT

P-3 ANALOG CONNECTOR PINOUT Pin No.				P-4 ANALOG CONNECTOR PINOUT Pin No.			
GND	1	2	GND		1	2	
GND	3	4	GND		3	4	
-15VDC	5	6	-15VDC		5	6	
+15VDC	7	8	+15VDC		7	8	
AO RET 1	9	10	AO RET 2	GND	9	10	GND
Analog Out 1	11	12	Analog Out 2		11	12	
GND	13	14	GND		13	14	
GND	15	16	GND		15	16	
Remote Common	17	18	GND		17	18	
IN0	19	20	IN32/RET0	IN16	19	20	IN48/RET16
IN1	21	22	IN33/RET1	IN17	21	22	IN49/RET17
IN2	23	24	IN34/RET2	IN18	23	24	IN50/RET18
IN3	25	26	IN35/RET3	IN19	25	26	IN51/RET19
IN4	27	28	IN36/RET4	IN20	27	28	IN52/RET20
IN5	29	30	IN37/RET5	IN21	29	30	IN53/RET21
IN6	31	32	IN38/RET6	IN22	31	32	IN54/RET22
IN7	33	34	IN39/RET7	IN23	33	34	IN55/RET23
IN8	35	36	IN40/RET8	IN24	35	36	IN56/RET24
IN9	37	38	IN41/RET9	IN25	37	38	IN57/RET25
IN10	39	40	IN42/RET10	IN26	39	40	IN58/RET26
IN11	41	42	IN43/RET11	IN27	41	42	IN59/RET27
IN12	43	44	IN44/RET12	IN28	43	44	IN60/RET28
IN13	45	46	IN45/RET13	IN29	45	46	IN61/RET29
IN14	47	48	IN46/RET14	IN30	47	48	IN62/RET30
IN15	49	50	IN47/RET15	IN31	49	50	IN63/RET31

MP8608	8-channel differential analog input system	
MP8608-AO	MP8608 with two channel analog output	
MP8608-NS	MP8608 without DC/DC converter	
MP8608-NS-AO	MP8608-NS with two channel analog output	
MP8616	16-channel single-ended analog input system	
MP8616-AO	MP8616 with two channel analog output	
MP8616-NS	MP8616 without DC/DC converter	
MP8616-NS-AO	MP8616-NS with two channel analog output	
MP8632	32-channel differential analog input system (may be connected as 64-channel single-ended system)	
MP8632-AO	MP8632 with two channel analog output	
MP8632-NS	MP8632 without DC/DC converter	
MP8632-NS-AO	MP8632-NS with two channel analog output	
2350MC	Analog connector, one required for 8, 16 channel units two required for 32/64 channel units	

7. INDUSTRIAL MEASUREMENT AND CONTROL PRODUCTS

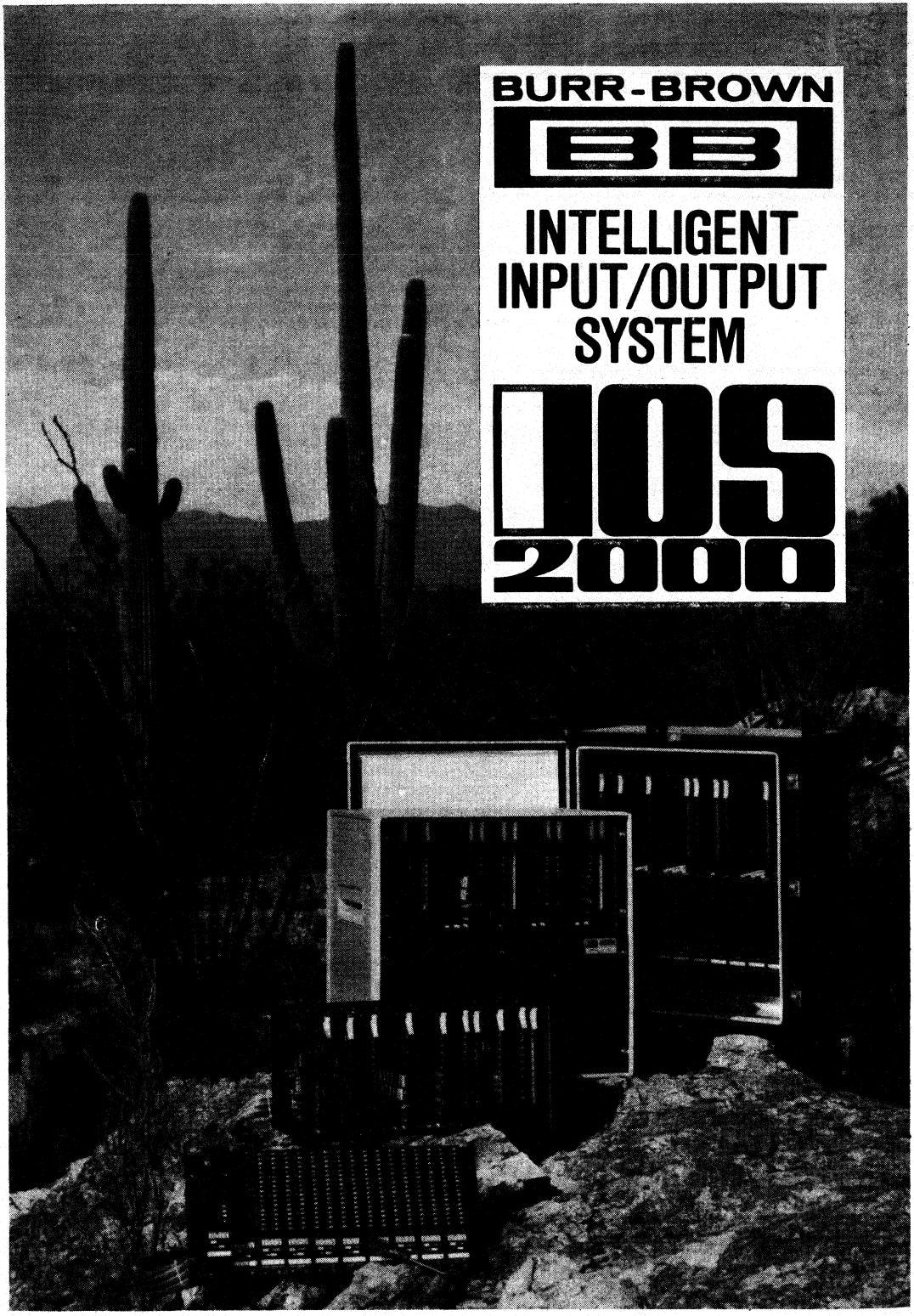


Vertical integration is a continuing force in Burr-Brown's product design philosophy. From simple op amps our line has grown to include complex hybrid data acquisition devices such as the MP22 described in section 5 and the uC-compatible analog and digital input/output microperipheral products described in section 6.

What more could Burr-Brown do to help customers design their systems and produce products even more effectively and profitably?

INTEGRATE THE INTEGRATED PRODUCTS ... put them into sensor-based subsystems such as MICROMUX - then go further and create microprocessor controlled systems such as the IOS2000.

The Industrial Measurement and Control Products group was established to design and market systems for industrial process control and measurement operations that take place in the real world ... to provide solutions in an environment where problems, language and tools are different from "data based" operations. You will find this group oriented to your specific and unique needs in the application of modern techniques for Industrial Measurement and Control.



DISTRIBUTED INTELLIGENCE FOR MEASUREMENT AND CONTROL

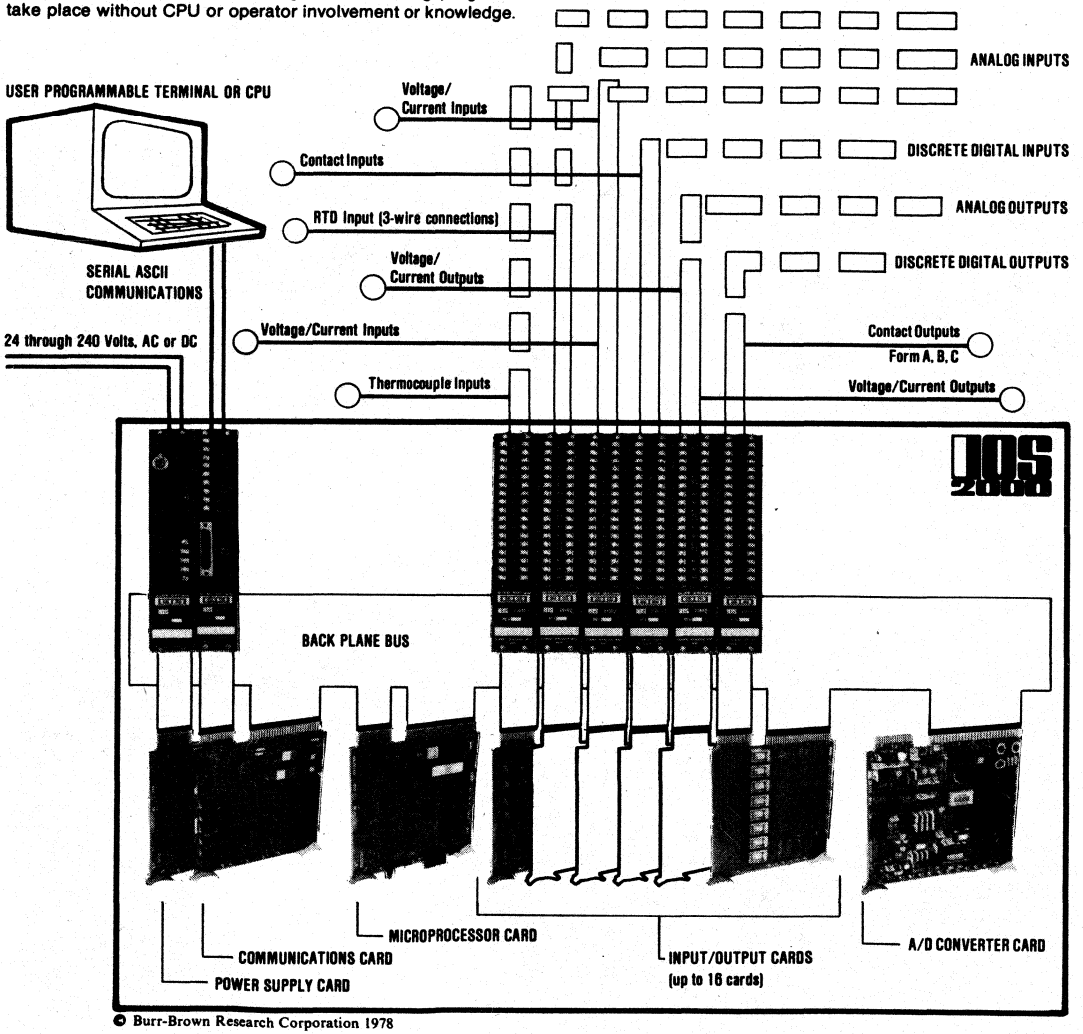
IOS2000 A DISTRIBUTED INPUT/OUTPUT SYSTEM FOR MEASUREMENT AND CONTROL

IOS2000 introduces dynamic new concepts for distributed input/output (I/O) systems. Utilizing its preprogrammed microprocessor, it functions as the sensory center of your measurement and process control system. Flexible ... fully expandable ... totally transparent to CPU and operator, IOS2000 sharply reduces system design and installation costs while providing a burdenless interface with your software/CPU team.

Remotely located, this intelligent front-end handles all forms of inputs and outputs. It collects and conditions sensor inputs - sends them to your CPU already digitized and preprocessed. When operating in a closed loop installation, IOS2000 responds to CPU commands and generates contact closure outputs to turn on lights, motors...generates analog output voltages and currents to modulate valves, establish set points and similar functions. Routine sensor signal conditioning and monitoring programs take place without CPU or operator involvement or knowledge.

Up to fifteen IOS2000 systems can connect to one ASCII serial asynchronous communications line. IOS2000 is also available in stand-alone configurations which include user terminals programmable in FORTRAN IV and BASIC.

IOS2000 presents dramatic new designs in dynamic configuration control. Plug-in modules let you add more sensors, more outputs, more power in the field as your measurement and control requirements demand. Rack mounted card files, remote termination panels (screwdriver compatible), NEMA-4 enclosures and a wide variety of I/O options let you match the IOS2000 exactly to your control system's needs.



IOS 2000 BENEFITS SIMPLIFY YOUR I/O SYSTEM DESIGN, INSTALLATION, OPERATION

PROGRAMMED INTELLIGENCE UNBURDENS CPU/SOFTWARE

IOS2000 uses its factory programmed intelligence to make non-processing related decisions and perform functions usually made by the operator or by the CPU and its software. Major functions include:

A/D converter card that performs:
- Automatic zero
- Automatic ranging
- System calibration
- Baseline offset at operator request

I/O cards with on-card PROM instructions tailored for each type of sensor input:
- T/C and RTD linearization
- Units conversion

Dynamic system configuration control allows you to plug in and remove any I/O card at any time in any slot position without affecting system operation. Factory installed indentifiers on I/O cards are automatically read to identify the card type; therefore, addressing is to a slot position thus eliminating complex card address decoding schemes.

Self-diagnostic programs check every operation. A detailed diagnostic analysis is available to identify impending problems.

THESE FEATURES REDUCE YOUR SYSTEM EXPANSION AND OPERATING COSTS

MODULAR PACKAGE FLEXIBILITY
Rack mounted card cages and NEMA-4 enclosures in various sizes meet initial and system growth needs.

FIELD TERMINATIONS
Screwdriver compatible. Card removal/replacement does not involve field termination connections.

SYSTEM MICROPROCESSOR and MEMORY
Factory programmed to control IOS2000's internal functions - transparent to your terminal.

DISTRIBUTED MEMORY
I/O and function memory, as needed, is located on each card. Adding cards for system growth adds the correct memory.

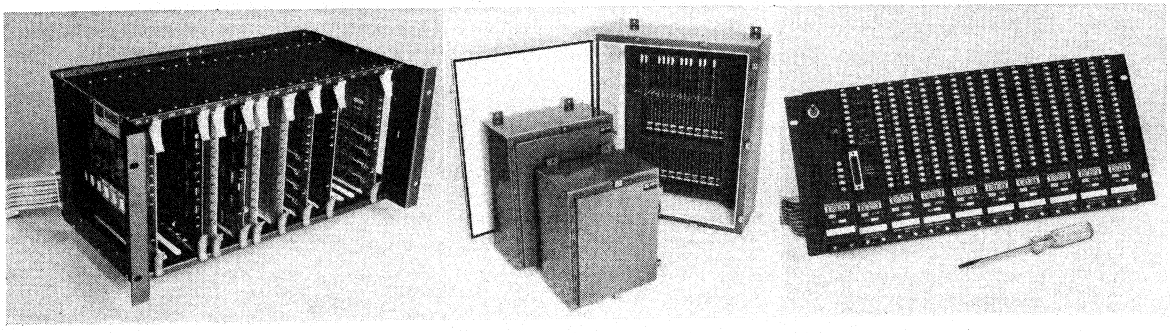
COMMUNICATIONS
Interface cards for popular ASCII, 20mA current loop and RS232 are standard. Transactions are secured by using word parity, message check sum, and echo techniques.

MINIMUM POWER CONSUMPTION
Add modular, plug-in power supplies to support I/O demands. As supply modules are added, total load is redistributed automatically over all supplies. CMOS design further reduces power demand.

REDUCED NOISE EFFECT
Noise generation is minimized and noise immunity enhanced by using CMOS circuits. In addition, synchronizing the switching power supply and A/D converter with the processor clock further reduces the effects of noise.

POWER FAILURE PROTECTION
IOS2000 powers up without human involvement.

OPERATING ENVIRONMENT
Operating temperature range of -40°C to +85°C permits installation in remote, inhospitable environments.



MORE IMPORTANT FACTS ABOUT IOS2000:

Full capacity of the largest NEMA-4 enclosure (36"H x 30"W x 10"D) is 256 digital points or 128 analog channels - or a mix.

To expand a rack mounted configuration, up to three card files can be clustered to operate from a single processor, communication and ADC card set. Capacity of this card set is 48 I/O card slots(768 digital points or 384 analog channels or mix).

When inputting digital data, channel scan speeds greater than 1000 points per second are possible. Analog channel scan speeds range from 10 to more than 100 channels per second, depending on application.

Throughput error is 0.02% FS in the ±10V range; 0.05% FS in the ±10mV range over operating temperature.

Accuracy of thermocouple measurement throughput is approximately 0.5°C over the typical thermocouple range - more accurate than the thermocouple itself.

Accuracy of temperature measurements from RTD inputs will be approximately 0.1°C, depending on application.

For locations beyond one mile, modems are available.

IOS2000 can operate from any power source between 24V and 240V, AC or DC.

IOS 2000

REDUCES SYSTEM COSTS

Your total system costs are reduced using IOS2000...less sensor oriented software and greatly simplified, less costly cabling requirements.

Simplified maintenance and designed-in diagnostic routines keep IOS2000 on line, trouble free. Symptoms of potential problems are detected-reported, early, before they become serious. Plug-in modularity cuts downtime to minutes with replacement cards.

RELIABILITY DESIGNED IN

To assure trouble-free performance, IOS2000 features high reliability design, 100% burn-in of sub-systems and thorough performance checks of complete systems prior to shipment.

Should problems arise in the field, they are detected by the IOS2000's diagnostic programs. Quick plug-in replacement of the suspect module with a spare part will keep downtime to an acceptable minimum. Factory service is available with one to two week turn-around for module repairs. All Burr-Brown parts and assemblies are warranted for one year with extended warranties available. Special training sessions at the factory can also be arranged.

HOW TO USE IOS2000

IOS2000 is fully compatible with virtually any intelligent, programmable terminal equipped with a serial ASCII port. The preprogrammed capability of the IOS2000 is utilized by "talking" to it with straightforward languages such as BASIC or FORTRAN. Of course, assembly language can also be used.

Because of its factory preprogrammed personality some of the IOS2000 functions you can request or define include:

- Request random access
- Request sequential scans
- Define functions to be performed by IOS2000 before formatting data
- Pre-define scan patterns for later request
- Define spans, limits, etc.
- Queue outputs prior to activation
- Activate outputs
- Request extended "state-of-health" status

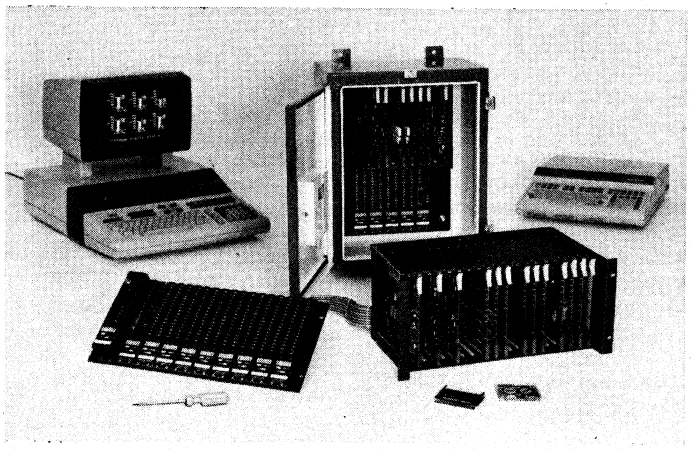
STAND-ALONE IOS2000

If you don't have a terminal or CPU, or if they're fully dedicated, you can specify a stand-alone IOS2000. Burr-Brown can provide a compatible desk top computer such as Hewlett-Packard System 9845 or 9825 to function as an IOS2000 controller. This system is complete with a software application package to handle communications and is ready to operate.

All function commands for IOS2000 are stored on a preprogrammed magnetic tape provided with the stand-alone system. This program can be used in two ways.

One method allows direct operator interaction with the IOS2000 through the Hewlett-Packard terminal's keyboard. The program functions, loaded into the H-P memory, are activated by pressing the desired function key. You communicate with the IOS2000 by manually pressing function keys and observing the display.

Should you wish to operate the system automatically, you can load the IOS2000 utility programs, and call them up with your master or executive program using the H-P equipment.



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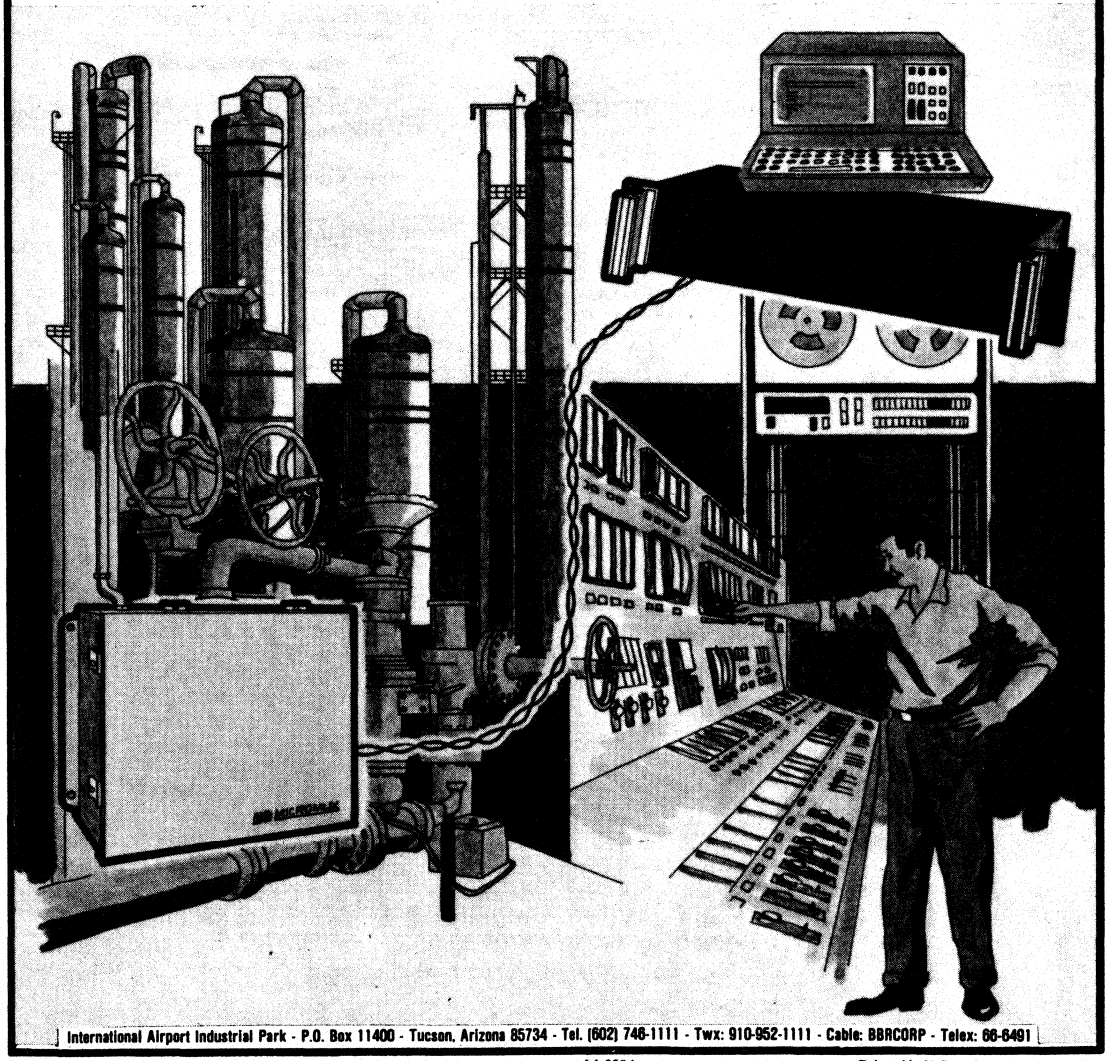
A TWO-WIRE DATA ACQUISITION SYSTEM - WITH ASCII COMPUTER INTERFACE - DESIGNED FOR TOUGH ENVIRONMENTS!



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LI-228A

Printed in U.S.A. July, 1978

MICROMUX™

REMOTE DATA ACQUISITION

ADD TO EXISTING SYSTEMS . . . USE IN NEW DESIGNS TO MONITOR FEW OR DISPERSED OPERATIONS

What happens when your data acquisition network is fully utilized - and you have to add more inputs?

How do you monitor a new 100 point system when sensors and transmitters will be scattered all over the plant, and the yard?

It can be an expensive problem, but there's a practical solution: MICROMUX™!

This modern remote data acquisition system uses a simple two-wire interconnection from field to computer that reduces wiring and installation costs. It also provides computer interface to reduce costs in the computer room.

If you're adding to an existing system it's easy to run in a twisted wire pair. And if your pickup points are few and far between, MICROMUX' two-wire feature will save you substantial costs while insuring data integrity in runs of a mile or more. MICROMUX also uses the same wire pair to provide power for the remote transmitters - you avoid another major installation cost!

HOW MICROMUX WORKS

MICROMUX Remote Transmitters are located near monitoring points. As many as 16 analog or digital inputs are connected to each unit. Inputs include thermocouples, voltage and current signals and contact closures. The remote transmitter converts these inputs to multiplexed digital signals which are transmitted - not by 32 wires, but by a single wire pair to the receiver.

The MICROMUX Receiver is located near the computer. It receives incoming signals from remote transmitters and converts them to three digit binary coded decimal (BCD) format. This continuously updated information is stored in the receiver's memory.

Each remote transmitter scans 16 channels of data every 4.3 seconds. MICROMUX receivers accept inputs from up to four remote transmitters - a maximum of 64 channels. The computer reads data from the receiver at a maximum of 80 channels per second.

ENVIRONMENTAL ADVANTAGES

Install MICROMUX Remote Transmitters close to sensors - on stacks, boilers, on rolling mill floors - indoors or outdoors. They're designed for heavy industrial applications and their tough, steel enclosures are environmentally sealed. Internal circuitry is also coated to provide an extra measure of protection.

INTRINSICALLY SAFE REMOTE TRANSMITTERS

If you must monitor operations in an explosive atmosphere, MICROMUX is "intrinsically safe" when you install approved safety barriers. In this condition the remote transmitters cannot release enough energy to ignite hazardous gases and are providing a new, safe method for supervising difficult processes. Intrinsic safety certification has been obtained for thermocouple inputs. Certification for other low energy inputs may be obtained.

PROTECTING DATA ACCURACY

Data relayed from sensors to computer by conventional methods is subjected to electrical noise interference in industrial plants. MICROMUX is designed expressly to protect data accuracy all the way. A major factor in this data integrity is MICROMUX' conversion of analog sensor data to digital right at the remote transmitters. Transmitted MICROMUX digital signals are far less affected by electrical noise than are analog signals.

A number of other digital verification steps are performed by MICROMUX to protect data and insure its accuracy enroute to the computer.

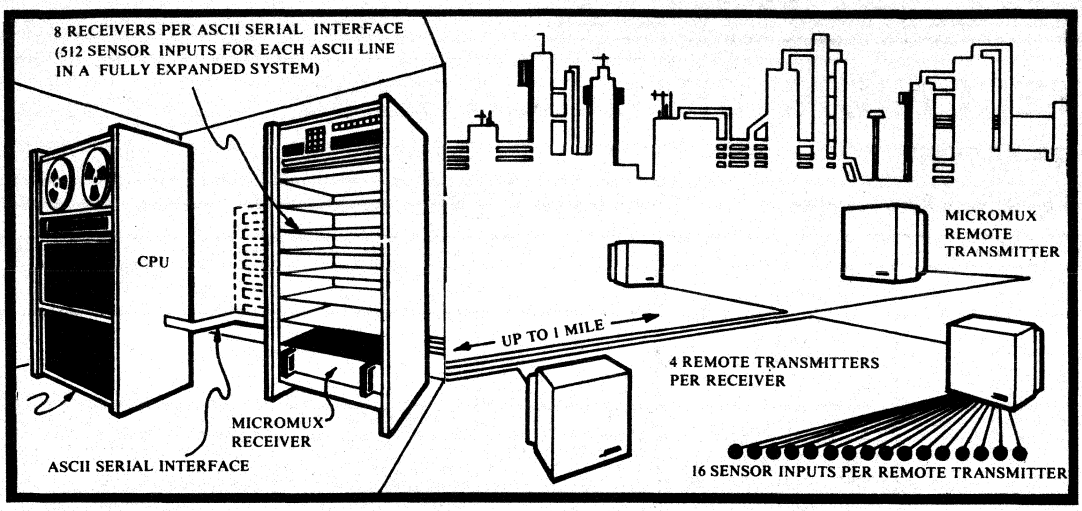
COMPUTER INTERFACE

An ASCII compatible, 20mA current loop (2400 baud) serial interface is built into every MICROMUX Receiver. An RS-232C interface with switch selectable rates of 110, 150, 300, 600, 1200 and 2400 baud is an option.

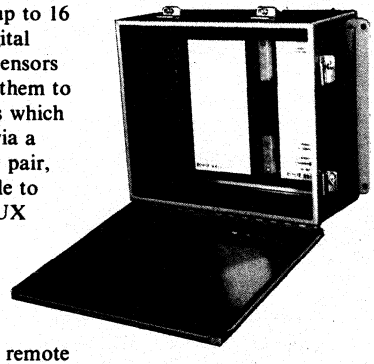
As many as eight MICROMUX Receivers (accommodating up to 512 channels of sensor inputs) can be connected to a single serial communications port on the computer. Programming to control MICROMUX is very similar to that used for most ASCII peripheral devices.

RELIABILITY - SERVICE

Carefully engineered solid state logic design, plus thorough pre-shipment burn-in and testing assure trouble-free field operation of MICROMUX systems. Should a failure occur, modular design permits fast plug-in replacement with spare boards and, therefore, minimum downtime. Factory service is available with one to two week turn around for module repairs. Burr-Brown warrants parts and labor in MICROMUX for one year.



REMOTE TRANSMITTER



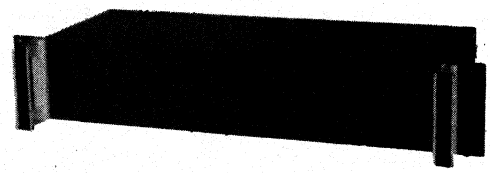
Multiplexes up to 16 analog or digital inputs from sensors . . . converts them to digital signals which are relayed, via a single twisted pair, up to one mile to a MICROMUX receiver.

Rugged, weatherproof remote transmitter is mounted right at the sensors, in any environment - even explosive. Doesn't require AC or battery supply.

FEATURES

Mounts anywhere - environmentally protected
Intrinsically safe (when used with appropriate safety barriers for thermocouple inputs)
2-wire hook-up powered by receiver unit
High electrical noise immunity
Converts inputs to multiplexed digital signals
16 sensor inputs per remote unit
Accepts high and low level voltage signals
Accepts current and contact closure signals
Ambient temp sensor for thermocouple compensation
Scans 16 channels every 4.3 seconds

RECEIVER



Converts and stores the continuous flow of sensor signals sent from each remote transmitter to a three digit BCD format. When instructed by a computer, the receiver transmits the latest data held in memory.

Standard ASCII serial interfaces are built into the receiver which is located near the control computer.

FEATURES

20mA current loop, 2400 baud interface standard
Selectable baud rate RS232C interface optional
Accommodates four remote transmitters
Provides power for remote transmitters
Two-wire connection to remote transmitters
Memory continuously updated
Data accuracy checked by receiver logic
Open circuit detection
Special noise isolation/rejection techniques
Basic 16 channel system expandable to 64 channels
Mounts in 19" rack

MICROMUX™

TECHNICAL SPECIFICATIONS

REMOTE TRANSMITTER

Number of Inputs:	16 per remote unit
Input Type:	1) Thermocouples 2) 4-20mA, 10-50mA 3) Voltage - ±12.5mV to +10V 4) Contact Closures (on some ranges)
Input Filtering:	Single pole 1Hz filter
Common-mode Voltage:	600VDC/240VAC remote unit to earth ground, 7VDC/5VAC channel to channel
Input Protection:	310VDC/220VAC channel to channel
Common-mode Rejection:	> 140dB at DC > 100dB at 50 or 60Hz
Normal Mode Rejection:	> 34dB at 50 or 60Hz
Remote to Receiver Distance:	1500M/5000 ft.
Data Rate to Receiver:	Varies from 119 channels per second for a 512 channel system to 3.7 channels per second for 16 channel system
Temperature Range:	-25°C to +85°C (-12°F to +185°F)
Enclosure:	NEMA-4 - 407mm x 350mm x 152mm (16" x 14" x 6")
Weight:	55kg (25 pounds)
Field Termination:	Barrier Strip (# 6 screw)

RECEIVER

	Standard	With Selectable Baud Rate RS232C Option*
Input:	From 1 to 4 remote units each connected with wire pair	
Data Rate to Computer:	80 channels per second	Selectable 3.6, 5, 10, 20, 40, 80 channels per second
Output:	2400 baud, ASCII, 20mA digital current loop. Even, odd or no parity with one stop bit	Selectable EIA or 20mA digital current loop ASCII 110, 150, 300, 600, 1200, 2400 baud. Even, odd or no parity with one stop bit
Output Interface:	Multidrop, up to 8 receivers per computer communications interface	Multidrop, up to 8 receivers per computer interface. At 2400 baud only one receiver requires EIA option. Others are standard.
Power Requirements:	105 - 124VAC/210 - 250 VAC/90 - 110VAC, 47 - 440Hz, 50 watts	105 - 125VAC/210 - 250 VAC/90 - 110VAC 47 - 440Hz, 60 watts
Temperature Range:	0 - 40°C (+32°F to +104°F)	
Enclosure:	483mm (19") rack mount, 89mm (3.5") panel, 178mm (7.0") deep	483mm (19") rack mount 89mm (3.5") panel, 305mm (12") deep
Weight:	5.7kg (12.5 pounds)	6.8kg (15 pounds)

MICROMUX ACCURACY

Throughput Accuracy:	±0.2% of span
Accuracy Stability (vs. temperature of remote unit)	±0.01% of span/°C (±0.005%/°F) [±0.015% of span/°C (±0.008%/°F) for low level ranges]

PRICES

MICROMUX' minimum systems consist of one remote transmitter (16 channels) and the receiver with its computer interface. Field expansion requires purchase of additional remote transmitters and plug-in printed circuit boards (which plug into the receiver) for each remote transmitter added.

Volume end user and OEM discounts available.

System prices with single receiver*

16 channel system	$1990
32 channel system	3380
48 channel system	4770
64 channel system	6160

Selectable Baud Rate RS232C Option: Add $500 to system price.

* for 25mV range input

8. MODULAR POWER SUPPLIES

Well-regulated DC power is usually required to power modern electronic circuits. Over the years electronic circuits have changed in terms of size and performance. Packaged in small integrated circuit packages or in hybrid modules, more and more electronic circuits now provide significantly improved performance. Burr-Brown encapsulated power supplies have kept up with changing times. We provide a broad line of reliable, self-contained, ready to use power supplies, at low cost, to meet OEM and design engineers' power supply requirements.

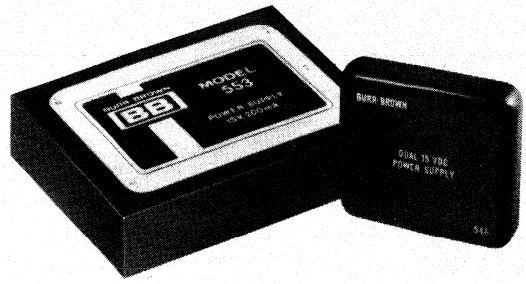
Burr-Brown standard series AC/DC power supplies and DC/DC converters provide maximum flexibility in systems design. They are particularly useful for powering analog interface circuitry involving operational amplifiers, A/D and D/A converters, instrumentation and isolation amplifiers, analog circuit functions, and so forth, in digital and analog systems. A wide range of output voltage and current ratings are available; international input voltage ratings are also available.

The AC/DC supplies are available in both the PC board-mountable and chassis-mountable verisons. The chassis mount type provides the same reliable performance as the PC board mount type, but the input and output connections are made on a terminal strip via screw terminals rather than pins. They are useful in applications where use of PC boards or sockets is either undesirable or impractical.

The DC/DC converters are available in small encapsulated PC board-mountable packages. They provide high input-output isolation, making them suitable in computer interface applications where, if necessary, the analog circuitry can be "floated" completely independent of digital ground. Specially designed DC/DC converters are available for use with optically-coupled isolation amplifiers and for applications where isolation voltage ratings of 3000 volts and more are required.

All Burr-Brown power supplies are extensively tested before and after encapsulation to ensure reliable operation. Computerized automatic testing equipment is used to implement stringent quality control. Years of linear and digital engineering expertise have gone into the design and manufacture of Burr-Brown products. Most of these power supplies are available from stock in both small and large quantities.

BURR-BROWN



MODULAR AC/DC AND DC/DC POWER SUPPLIES

FEATURES

- PC BOARD COMPATIBLE
- CHASSIS MOUNTABLE
- HIGH RELIABILITY, FULLY TESTED
- LOW INSTALLED COST
- COMPLETELY SELF-CONTAINED

DESCRIPTION

Burr-Brown standard series power supplies and DC/DC converters provide maximum flexibility in systems design. They are particularly useful for powering analog interface circuitry in digital and analog systems and have a wide range of output voltage and current ratings. They are completely self-contained, ready to use encapsulated units. For most OEM users they eliminate engineering start-up/documentation costs and manufacturing delays at prices generally far below internal manufacturing costs.

The AC/DC power supplies have a current limiting circuit in the output stage, designed to withstand output short-circuit-to-common or substantial overload conditions for long periods of time, without causing damage to the power supply.

In applications where isolation between input and output is an essential requirement (such as powering isolation amplifier input and output stages) the Burr-Brown isolated DC/DC converters provide up to 1500VDC of isolation protection.

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PDS-337B

Printed in U.S.A. July, 1978

MODULAR AC/DC POWER SUPPLIES

- PC BOARD/CHASSIS MOUNT TYPE
- ±15VDC DUAL OUTPUTS, +5VDC SINGLE OUTPUT
- 25mA TO 1000mA CURRENT CAPABILITY
- CURRENT-LIMITED OUTPUTS FOR SHORT CIRCUIT PROTECTION
- INTERNATIONAL AC INPUT VOLTAGE OPTIONS AVAILABLE

SPECIFICATIONS COMMON TO ALL AC/DC POWER SUPPLIES

Input Voltage: 105VAC to 125VAC, 50Hz to 400Hz. For international AC input voltages see options E, F, and H.

Input Isolation: 50MΩ

Breakdown Voltage: 500V, min.

Output Voltage: Error, ±1%; temperature coefficient, ±0.02%/°C

Output Protection: Current limiting protection for output to withstand overloads and direct short circuits to ground to prevent excessive temperature within the unit.

Rated Operating Temperature: -25°C to +71°C. May be operated at higher temperatures with proper derating.

Storage Temperature: -25°C to +85°C.

DC/DC CONVERTERS, ±15VDC OUTPUT

- REGULATED ±15VDC FROM UNREGULATED DC INPUT
- DIFFERENT DC INPUT VOLTAGE RANGES AVAILABLE
- HIGH CURRENT CAPABILITY WITH CURRENT LIMIT PROTECTION
- ISOLATED DC/DC CONVERTERS, 75% EFFICIENCY AT FULL LOAD
- LOW COUPLING CAPACITANCE (8pF)
- HIGH ISOLATION VOLTAGE (1500VDC)
- LOW EMI, SHIELDED AND UNSHIELDED UNITS
- UP TO FOUR FULLY ISOLATED OUTPUT CHANNELS (Model 710)
- SMALL SIZE

AC/DC CONVERTERS

	Dual ±15VDC Supplies							5VDC Logic Supplies		
	PC Board Mount					Chassis Mount		PC Board Mount		
Model	550	551	552	553	554	556	558	560	561	562
RATED OUTPUT										
Voltage (nom)	±15V	±15V	±15V	±15V	±15V	±15V	±15V	5V[1]	5V[1][2]	5V[1][2]
Current (max)	±25mA	±50mA	±100mA	±200mA	±350mA	±200mA	±500mA	250mA	500mA	1000mA
RATED INPUT										
Voltage	105 - 125VAC, 50 - 400Hz					105 - 125VAC 50 - 400Hz		105 - 125VAC, 50 - 400Hz		
Options[3]	E, F, H					E, F, H		E, F, H		
REGULATION										
No load to full load (max)	±0.1%	±0.05%	±0.05%	±0.05%	±0.02%	±0.05%	±0.05%	±0.1%	±0.1%	±0.1%
Over rated line voltage (max)	±0.05%	±0.05%	±0.05%	±0.05%	±0.02%	±0.05%	±0.05%	±0.05%	±0.05%	±0.05%
OUTPUT RIPPLE AND NOISE										
At full load, rms (max)	2mV	0.5mV	0.5mV	0.5mV	0.5mV	1mV	1mV	1mV	1mV	1mV

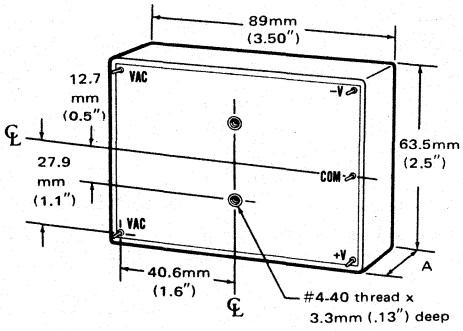
DC/DC CONVERTERS ±15VDC Output

	Low Profile	Isolated	
MODEL	546	700/700U[4]	710[5]
RATED INPUT			
Voltage	4.5VDC to 5.5VDC	10VDC to 18VDC	10VDC to 18VDC
Current, Quiescent	400mA, max	20mA at ±3mA load	40mA at total output of 24mA
Current, full load	1.8A, max	89mA max at ±30mA load	100mA at total output of 76mA
RATED OUTPUT			
Voltage (no load)	15V	$\pm V_{IN}$ w/1V tolerance	4 sets of $\pm V_{IN}$ w/1V tolerance
Current	120mA, max	total 60mA, max	total 76mA max; any single output -60mA, max
Short circuit current	180mA, max	120mA, max	120mA, max
REGULATION			
Line at full load	0.1%, max	—	—
Load, zero to full load	0.02% typ, 0.1% max	35mV/mA	75mV/mA
OUTPUT VOLTAGE TEMP. COEFFICIENT	±3mV/°C	—	—
OUTPUT RIPPLE	10mV peak, typ; 20mV peak, max; 0.8mV, rms max	±15mV peak at ±3mA load; ±80mV peak, max, at ±30mA load	±25mV peak at ±3mA load; ±80mV peak; max, at ±9.5mA load
INPUT-OUTPUT ISOLATION			
Test voltage, 5sec at 60Hz	—	4200Vp/5000Vp	2200V, rms
Voltage, continuous, derated	300VDC	1500Vp/2000Vp	600V, rms, 1000Vp
Impedance	$10^{10}\Omega$ || 50pF	$10^{10}\Omega$ || 5pF/$10^{10}\Omega$ || 3pF	$10^{10}\Omega$ || 8pF
Leakage current at 240V/60Hz, tested	—	1μA, max	1μA, max
TEMPERATURE RANGE			
Operating	0°C to 71°C	-25°C to +85°C	-25°C to +85°C
Storage	-55°C to +100°C	-55°C to +125°C	-55°C to +110°C

1. The output may be connected as +5V or -5V.
2. These 5V supplies have over-voltage protection which limits the output voltage to 7V (max) in a fault condition.
3. International input voltage rating available. Specify: E option - 205VAC to 240VAC, 50Hz to 400Hz.
   F option - 90VAC to 110VAC, 50Hz to 400Hz.
   H option - 220VAC to 260VAC, 50Hz to 400Hz.
4. Models 700 and 700M have separate internal input and output shields. Models 700U and 700UM have no internal shields. Model 700M and 700UM are similar to Models 700/700U but, in addition, they are 100% screened to patient connected circuit requirements for the leakage current (par. 27.5) and dielectric withstand voltage (par. 31.11) of UL544. Additional $2.00/unit charge for 700M or 700UM. See Product Data Sheet for complete specifications.
5. Model 710 provides 4 channels (sets) of isolated outputs. See Product Data Sheet for complete specifications.

PACKAGE DRAWINGS

DRAWING NO. 1



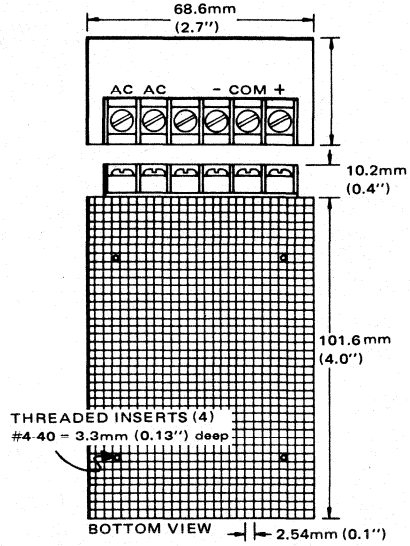
Pin Diameter 1.02mm (0.04")
* No Connection for Models 560, 561, 562.

For Models 550, 551, 560 – A = 22.2mm (0.875")
Weight: 340 grams (12 oz)

For Models 552, 553, 561, 562 – A = 32mm (1.25")
Weight: 425 grams (15 oz)

For Model 554 – A = 4.1cm (1.62")
Weight: 750 grams (26 oz)

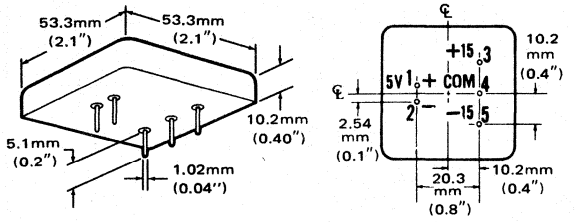
DRAWING NO. 2



For Model 556 – A = 36.6mm (1.44")

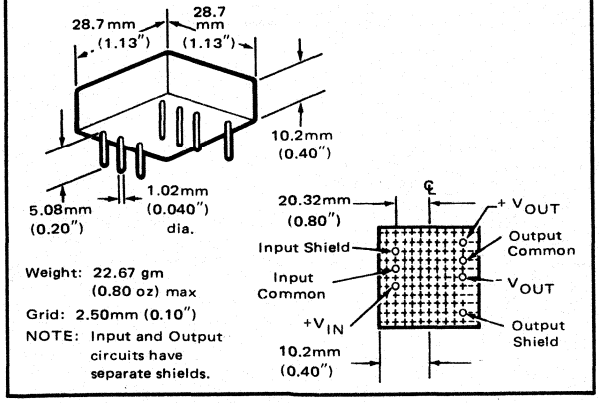
For Model 558 – A = 50.8mm (2.00")

DRAWING NO. 3 Model 546



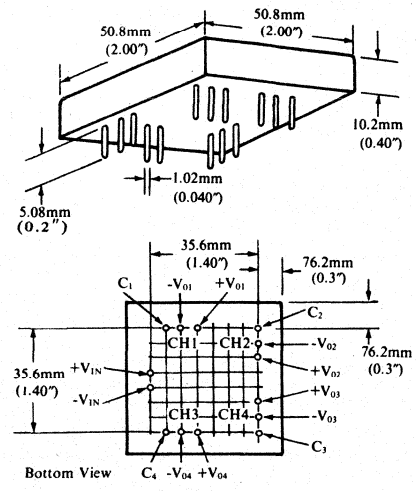
WEIGHT - 50 grams (1.7 oz)

DRAWING NO. 4 Model 700



Weight: 22.67 gm
(0.80 oz) max
Grid: 2.50mm (0.10")
NOTE: Input and Output
circuits have
separate shields.

DRAWING NO. 5 Model 710



Weight: 25 grams (0.9 oz.)
Grid: 5.08mm (.20")

BURR-BROWN

700/700U

ISOLATED DC-TO-DC CONVERTER

FEATURES

- HIGH BREAKDOWN VOLTAGE 5000V PEAK
- LOW LEAKAGE CAPACITANCE ≅3pF
- SHIELDED AND UNSHIELDED UNITS
- COMPLETELY SPECIFIED

BENEFITS

- HIGH VOLTAGE RATING PROTECTS EXPENSIVE INSTRUMENTATION
- LOW LEAKAGE CURRENT PROTECTS HUMAN LIFE
- EXCELLENT ISOLATION CMR IMPROVES SYSTEM PERFORMANCE
- SHIELDING PREVENTS ELECTROSTATIC AND EMI PROBLEMS

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- MEDICAL INSTRUMENTATION
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS

DESCRIPTION

The Model 700 converts a 10VDC to 18VDC input to a dual output of the same value as the input voltage. The internal hybrid integrated circuit reduces size and cost. A self-contained frequency stable 130kHz oscillator drives switching circuitry which is designed to minimize the common problem of spiking due to transformer saturation. Regulation and short circuit protection, if desired, can easily be added (see Figure 3). Models 700 and 700M have separate internal input and output shields. Models 700U and 700UM have no internal shields.

PWR. SUP.

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PDS-328C
Printed in U.S.A. July, 1978

SPECIFICATIONS

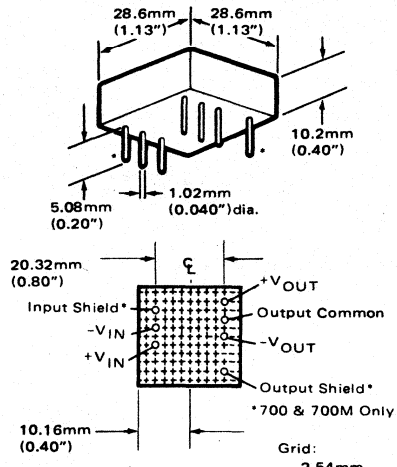
(Typical at 25°C with 15V supply unless otherwise noted.)

ELECTRICAL

MODEL	700/700M	700U/700UM
INPUT		
Voltage Range(1)	10V to 18V	
Current @ ±3 mA Load	20 mA	
Current @ ±30 mA Load	89 mA, max.	
Ripple Current @ ±3 mA Load	±3 mA, peak	
Ripple Current @ ±30 mA Load	±25 mA, peak	
ISOLATION(2)		
Voltage, Test, 5 sec. @ 60 Hz	4200Vp	5000Vp
Voltage, Continuous, derated	1500Vp	2000Vp
Impedance	10G Ω‖5 pF	10G Ω‖3 pF
Leakage Current @ 240V/60 Hz	1 μA, max.	1 μA, max.
OUTPUT		
V_{out} @ ±3 to ±30 mA Load	$\pm V_{in}$ with ±1V tolerance	
Operating Current total of both outputs	60 mA max.	
Safe Nondestructive Current at 25°C	120 mA max.	
Sensitivity to Input Voltage	1.08V/V	
Load Regulation	35 mV/mA	
Ripple Voltage @ ±3 mA Load	±15 mV, peak	
Ripple Voltage @ ±30 mA Load	±80 mV, peak max.	
Balance of +V and -V @ +I = -I	±20 mV	
TEMPERATURE RANGE		
Operating	-25°C to +85°C	
Storage	-55°C to +125°C	

NOTES: 1. Derate to 16V max between $+V_{in}$ and $-V_{in}$ above 70°C.
2. A medical grade unit is available which is 100% screened to Patient Connected Circuit requirements for the leakage current (par. 27.5) and dielectric withstand voltage (par. 31.11) of UL544. Specify 700M or 700UM.

MECHANICAL



Material: Black Epoxy
Weight: 22.67 gm (0.80 oz.) max
Grid: 2.50mm (0.10")
Pin: Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

NOTE: Input and Output circuits have separate shields.

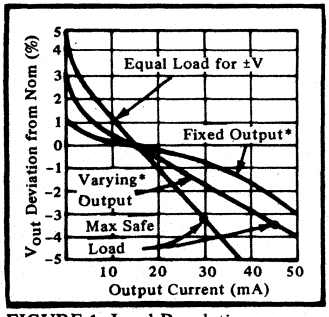


FIGURE 1. Load Regulation.

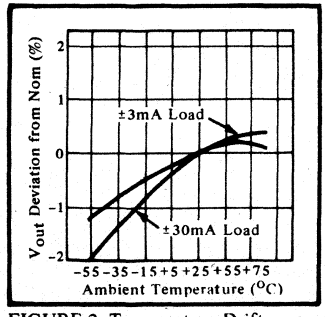


FIGURE 2. Temperature Drift.

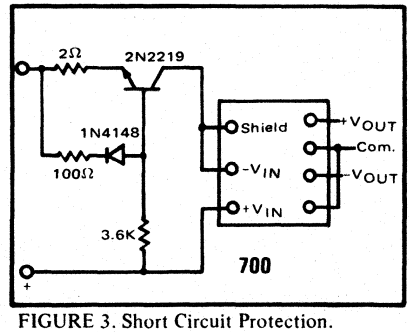


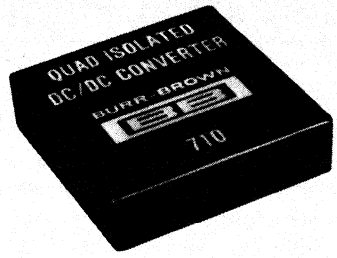
FIGURE 3. Short Circuit Protection.

*For one output with constant 15 mA load and varying current on other output.
(A minimum load of 3mA is recommended for each output).

Use with Isolation Amplifiers:

When the Model 700/700U is used with isolation amplifiers such as the Burr-Brown 3650 and 3652 special attention should be given to current ratings to avoid over designing. Since the isolation amplifiers do not draw max. current simultaneously from the +V and -V Model 700/700U terminals, it is possible to drive more isolation amplifiers per Model 700/700U than one might initially expect. The Model 700/700U is capable of providing a total output current of 60 mA balanced or unbalanced between the two outputs. A minimum load of 3 mA is recommended for each output.

BURR-BROWN



710

QUAD-ISOLATED DC-TO-DC CONVERTER

FEATURES

- FOUR ISOLATED ±10VDC to ±18VDC OUTPUTS
- DRIVES FOUR 3650/3652 ISOLATION AMPS
- HIGH BREAKDOWN VOLTAGE, 2200VDC TEST
- LOW LEAKAGE CAPACITANCE, 8pF
- LOW LEAKAGE CURRENT, 1μA @ 240V/60Hz
- LOW COST PER ISOLATED CHANNEL

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS

DESCRIPTION

The Model 710 converts a single 10VDC to 18VDC input into four dual isolated outputs of the same value as the input voltage. The converter is capable of providing a total of 76mA at rated output voltage accuracy and can provide isolated power to four independently isolated 3650/3652 optically coupled isolation amplifiers with the entire assembly mounted on one 5" x 7" card.

Extensive use is made of hybrid integrated circuits to reduce size and cost. A self-contained frequency stable 130 kHz oscillator drives switching circuitry which is designed to minimize the common problem of spiking due to transformer saturation.

PWR SUP

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PDS-367A Printed in U.S.A. July, 1978

DESCRIPTION

OUTPUT CURRENT RATINGS

The Model 710 is capable of providing a total of 76mA of output current divided among its eight outputs. The maximum current available from any one output is shown in Figure 9. A minimum average current of 3mA is recommended for each output in order to maintain output voltage accuracy. Thus, the current may be balanced (such as +9.5mA and -9.5mA) or unbalanced (such as +16mA and -3mA). The best output voltage accuracy will be obtained under balanced conditions.

Channels may be connected in series or parallel for higher voltage or current. For parallel operation connection of channel 1 to 2 or channel 3 to 4 will result in lowest ripple.

In some cases the 710 may drive larger loads than would be apparent from a cursory examination of the specifications. For example, see Figures 1 and 2. The most total current drawn from the pair of $+V_o$ and $-V_o$ output is $I_{max} + I_Q$ (not 2 x I_{max}). For the 3650 this is a maximum of 12mA +1.2mA = 13.2mA (instead of 24mA).

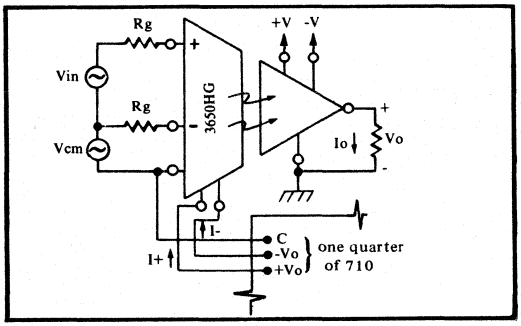


FIGURE 1. Typical Connection

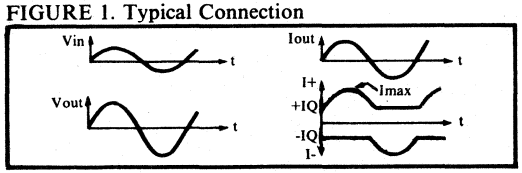


FIGURE 2. Waveforms

ISOLATION VOLTAGE RATINGS

It is important that the user understand the significance of the continuous derated isolation voltage specification and its relationship to the actual test voltage applied to the unit. Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration) it is generally accepted practice to perform a production test at a higher voltage (i.e., higher than the continuous rating) for some shorter length of time.

The important consideration is then "what is the relationship between actual test conditions and the continuous derated minimum specification?" There are several rules of thumb used throughout the industry to establish this relationship. Burr-Brown has chosen a very conservative one: $V_{test} = (2 \times V_{continuous\ rating}) + 1000$ V. This relationship is appropriate for conditions where the system transient voltages are not well defined.* Where the real voltages are well defined or where the isolation voltage is not continuous the user may choose to use a less conservative derating to establish a specification from the test voltage.

* Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS I-109 and ICS I-111.

SHORT CIRCUIT PROTECTION

The circuit in Figure 3 may be added to the input of the 710 in order to protect it from damage in situations where too much current is demanded from the outputs – such as a short circuit from an output to its common. The circuit limits the input current to approximately 100 mA for an input voltage of 15 VDC (for β of 2N2219 of 50).

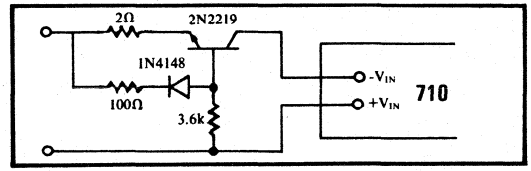


FIGURE 3. Short Circuit Protection

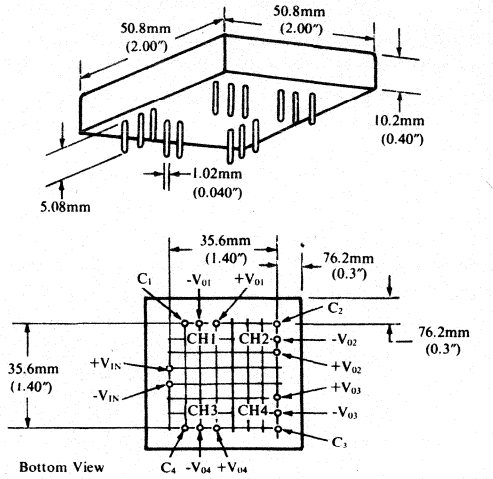
SPECIFICATIONS

(Typical at 25°C with 15V supply unless otherwise noted.)

ELECTRICAL

MODEL	710
INPUT	
Voltage Range (1)(2)	10V to 18V
Current at Total Output Current of 24mA	40mA
Current at Total Output Current of 76mA	100mA, max.
Ripple at Total Output Current of 24mA	15mA, peak
Ripple at Total Output Current of 76mA	40mA, peak
ISOLATION (3)	
Voltage, Test, 5 sec. (4)	2200V rms at 60Hz
Voltage, Continuous, derated, minimum (4)	600V rms AC, 1000VDC
Impedance	10 G Ω ‖ 8 pF
Leakage Current at 240V/60 Hz	1 μA, max.
OUTPUT	
Voltage Accuracy (5)	See Figure 8
Current for Rated Accuracy: Total of all currents	76mA max
: Any one output	60mA max
Total Safe Nondestructive Current at 25°C	120mA max
Sensitivity to Input Voltage	1.08V/V
Load Regulation (6)	75mV/mA
Ripple Voltage at ±3mA Load	±25mV, peak
Ripple Voltage at ±9.5mA Load	±80mV, peak max
Balance of +V and -V at +I = -I	±20mV
ΔV_{out} vs Temperature -25°C to +85°C	3.0%
TEMPERATURE RANGE	
Operating	-25°C to +85°C
Storage	-55°C to +110°C

MECHANICAL



Material: Black Epoxy
Weight: 25 grams (0.9 oz.)
Grid: 5.08mm (.20")
Pin: Material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

NOTES:
1. Derate to 16V max between $+V_{IN}$ and $-V_{IN}$ above 70°C.
2. Operation down to 5V is possible with reduced output current and accuracy.
3. Isolation specifications are applicable to input to output isolation as well as channel to channel isolation.
4. See discussion on page 8-10; 2200V rms ≈ 3000V peak.
5. A minimum output current of ±3mA per channel is recommended to maintain output voltage accuracy.
6. Load regulation for one channel with other channels at ±9.5mA load.

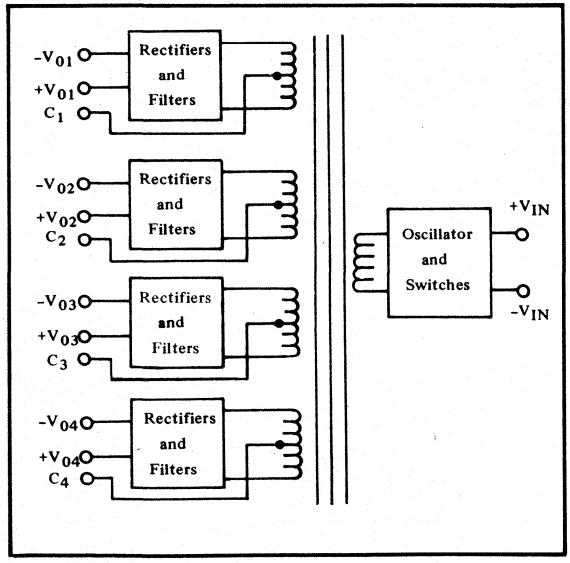


FIGURE 4. Functional Diagram

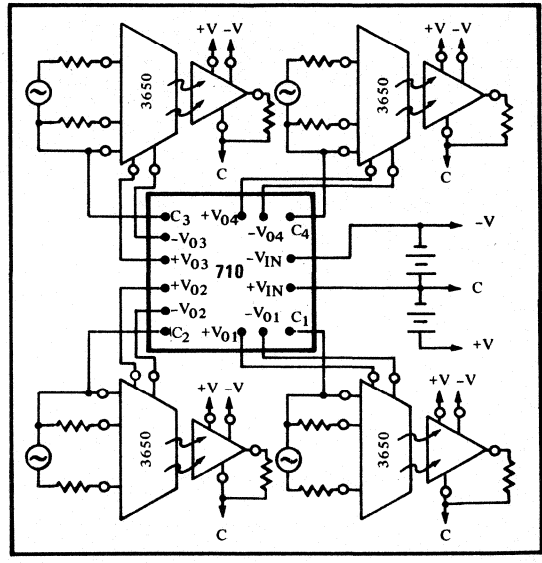


FIGURE 5. Typical Connection with four 3650 Isolation Amplifiers.

PWR. SUP.

TYPICAL PERFORMANCE CURVES

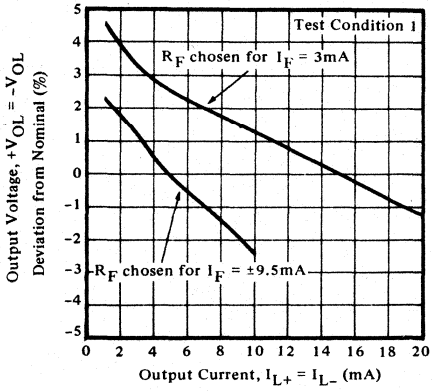


FIGURE 6. LOAD REGULATION - balanced load

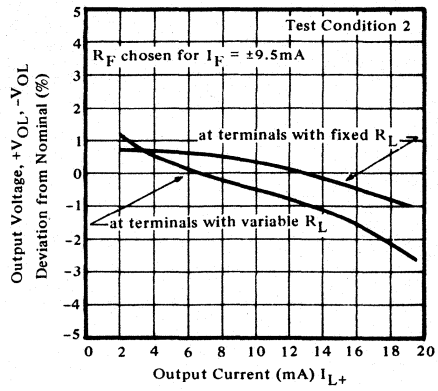


FIGURE 7. LOAD REGULATION - unbalanced load

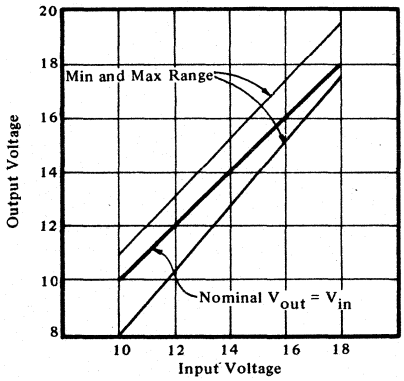


FIGURE 8. OUTPUT VOLTAGE ACCURACY VS INPUT VOLTAGE

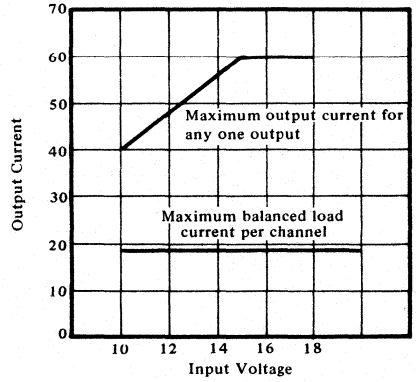


FIGURE 9. OUTPUT CURRENT RATINGS TO MAINTAIN OUTPUT VOLTAGE TOLERANCE

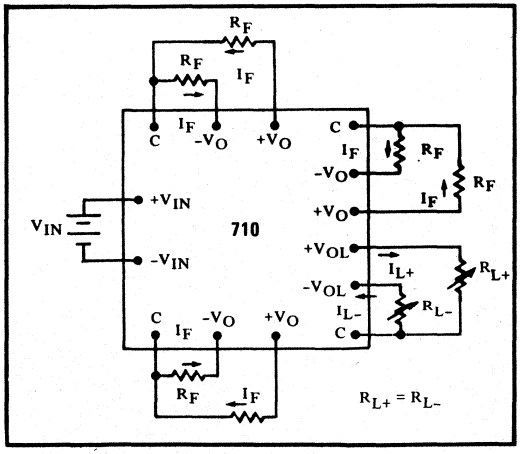


FIGURE 10. Test Condition 1: Balanced Load

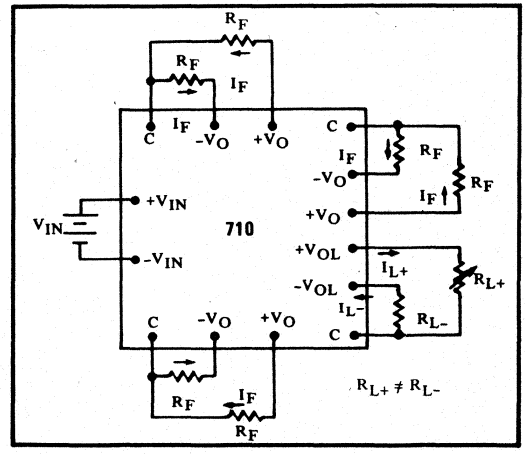
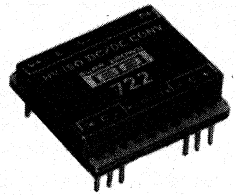


FIGURE 11. Test Condition 2: Unbalanced Load

BURR-BROWN

722



ADVANCE INFORMATION
Subject to Change

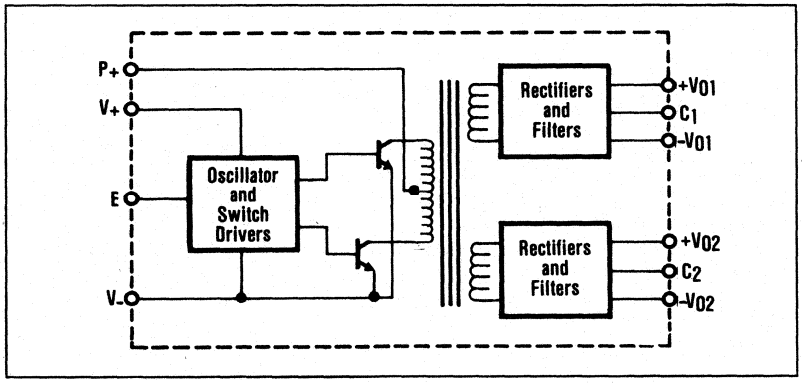
DUAL ISOLATED DC/DC CONVERTER

FEATURES

- DUAL ISOLATED ±5 TO ±16V OUTPUTS
- HIGH BREAKDOWN VOLTAGE, 8000V TEST
- LOW LEAKAGE CURRENT, <1μA AT 240V/60Hz
- LOW COST PER ISOLATED CHANNEL
- SMALL SIZE, 27.9mm x 27.9mm x 7.6mm (1.1" x 1.1" x 0.3")

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS
- NUCLEAR INSTRUMENTATION



DESCRIPTION

The 722 converts a single 5VDC to 16VDC input into a pair of bipolar output voltages of the same value as the input voltage. The converter is capable of providing a total output current of 64mA at rated voltage accuracy and up to 250mA without damage.

The two output channels are isolated from the input and from each other. They may be connected independently, in series for higher output voltage or in parallel for higher output current, as a single channel isolated DC/DC converter.

Integrated circuit construction of the 722 reduces size and cost. High isolation breakdown voltages and low leakage currents are assured by special design and construction which includes use of a high dielectric strength, low leakage coating used on the internal assembly.

A self-contained 900kHz oscillator drives switching circuitry which is designed to eliminate the common problem of input current spiking due to transformer saturation.

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PDS-398

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DISCUSSION

OUTPUT CURRENT RATINGS

At rated output voltage accuracy, the 722 is capable of providing 64mA divided among its four outputs[1]. A minimum average output current of 3mA is recommended at each output to maintain voltage accuracy.

Output channels[2] may be connected in series or parallel for higher output voltage or current.

ISOLATION CONFIGURATIONS

The fact that the two outputs of the 722 are isolated from the input and from each other allows both two-port and three-port isolation connections.

Figure 1 shows Burr-Brown's 3650 Optically Coupled Isolation Amplifier connected in three-port configuration. One of the 722 channels provides power to the 3650's input. The other channel supplies power to the 3650's output. The amplifier's input and output are isolated from each other and the system's power supply common. In this configuration the 722's channel-to-channel isolation specification applies to the amplifier input-to-output voltage.

Figure 3 illustrates how the 722 may provide isolated input power to the input stage of two 3650's connected in the two-port configuration. Power for the output stage is provided by the system +15V and -15V supplies. Input stages are isolated from each other and from the system supply. In this situation the 722's input-to-output isolation specification applies to the amplifiers' input-to-output voltages while the channel-to-channel 722 specification applies to the voltage existing between "I/P Com # 1" and "I/P Com # 2."

(1) "output" denotes a single output terminal (+V or -V) and its associated common
(2) "channel" denotes a pair of outputs (+V and -V) and their associated common

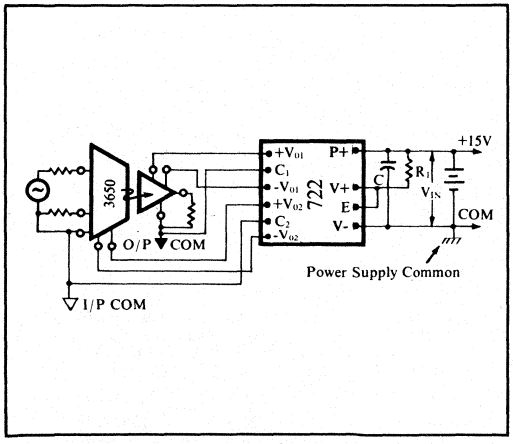


FIGURE 1. Three-Port Isolation

ISOLATION VOLTAGE RATINGS

Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration) it is generally accepted practice to perform a production test at a higher voltage (i.e., higher than the continuous rating) for some shorter length of time.

The important consideration is then "what is the relationship between actual test conditions and the continuous derated maximum specification?" There are several rules of thumb used throughout the industry to establish this relationship. Burr-Brown has chosen a very conservative one: $V_{test} = (2 \times V_{continuous\ rating}) + 1000V$. This relationship is appropriate for conditions where the system transient voltages are not well defined.[3] Where the real voltages are well defined or where the isolation voltage is not continuous the user may choose to use a less conservative derating to establish a specification from the test voltage.

(3) Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS 1-109 and ICS 1-111

SHORT CIRCUIT PROTECTION

The circuit in Figure 2 may be added to the input of the 722 to protect it from damage in situations where too much current is demanded from the outputs - such as a short circuit from an output to its common. The circuit limits input current to approximately 150mA for an input voltage of 15VDC (for β of 2N2219 of 50).

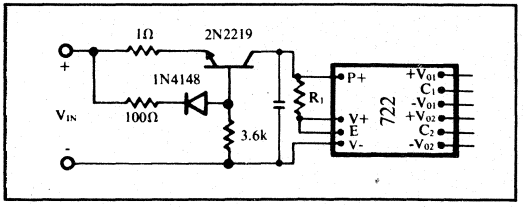


FIGURE 2. Short Circuit Protection

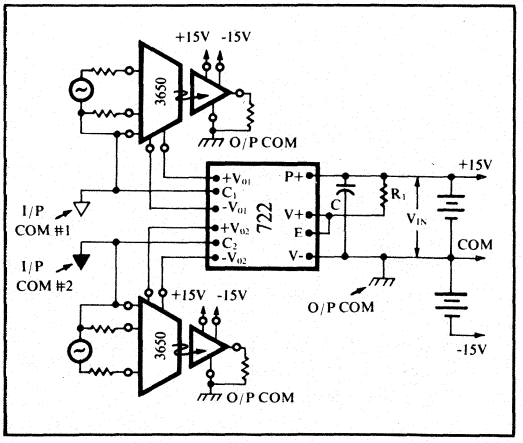


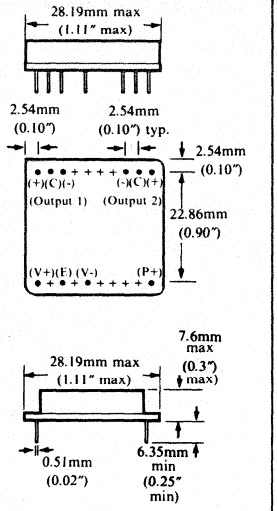
FIGURE 3. Two-Port Isolation with two 3650's.

ELECTRICAL SPECIFICATIONS

At 25°C with V_{IN} = 15V, R_1 = 1.3kΩ, C = 0.47μF unless noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT					
Input Voltage		±5	±15	±16	VDC
Input Current	Σ I_{OUT} = 12mA		50		mA
	Σ I_{OUT} = 64mA, 25°C		105	120	mA
	Σ I_{OUT} = 64mA, 85°C		120		mA
Input Ripple[4]	Σ I_{OUT} = 12mA, C = 0.47μF		10		mApk
	Σ I_{OUT} = 64mA, C = 0.47μF			25	mApk
ISOLATION					
Test Voltage[1]	Input-to-output, 5sec min			8000	Vpk
	Channel-to-channel, 5sec min			5000	Vpk
Rated Voltage[1]	Input-to-output, continuous			3500	V
	Channel-to-channel, continuous			2000	V
Isolation Impedance	Input-to-output		10 ‖ 6		GΩ ‖ pF
Leakage Current	Input-to-output, 240V/60Hz			1.0	μA
OUTPUT					
Voltage Accuracy[2]	I_L = 3mA	15.4		16.0	V
	I_L = 16mA	14.6		15.4	V
Current for Rated Voltage Accuracy	Total of all outputs			64	mA
	Any one output[3]	3			mA
Total Safe Non-destructive Current	Total of all outputs			250	mA
	Any one output			125	mA
Load Regulation			Note 2		
Ripple Voltage	I_L = 3mA		15		mVpk
	I_L = 16mA			100	mVpk
Difference of $+V_0$ and $-V_0$	$+I_L = -I_L$		±30		mV
Sensitivity to Input Voltage Change			1.13		V/V
Output Voltage over Temperature	-25°C to +85°C		2		%
TEMPERATURE RANGE					
Operating		-25		+85	°C
Storage		-55		+125	°C

MECHANICAL



PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2). CASE: Ceramic
WEIGHT: 11 grams (0.4 oz.).

TABLE I. Electrical Specifications

NOTES:
1. See "ISOLATION VOLTAGE RATINGS" on preceding page.
2. See "TYPICAL PERFORMANCE CURVES."
3. A minimum output current of 3mA at each output is recommended to maintain output voltage accuracy.
4. External capacitor across "P+" to "V-" pins and 12" of # 24 wire to V_{IN}.
5. For ambient temperature above 70°C the input voltage is 12.5V max. The input voltage remains 16V max. If case temperature is kept below 85°C.

INSTALLATION AND OPERATING INSTRUCTIONS

Typical application connections for the 722 are shown in Figures 1 and 3. Primary power (V_{IN}) is applied at the "P+" and "V-" terminals. The common or ground for V_{IN} may be connected to either "P+" or "V-"; the only requirement is that "P+" and "V+" must be positive with respect to "V-."

Power for the internal oscillator and switch drivers is derived from the primary power by a voltage dropping resistor R_1. The value of R_1 as a function of V_{IN} is shown in the TYPICAL PERFORMANCE CURVES section. Alternately, voltage for the "V+" terminal may be obtained from a separate source. "V+" should be +5V to +7.5V positive with respect to "V-". If a separate source is used, the V+ input must be applied before the "P+" input to avoid possible damage to the unit. P+ and V+ must remain positive with respect to V- at all times (including transients). If necessary, diode clamps should be put across these inputs.

The "E" pin enables the oscillator when connected to "V+" and disables it when connected to "V-."

An external capacitor, "C", (0.47μF ceramic) is used to reduce input ripple. It should be connected as close to the "P+" and "V-" pins as practical. Input leads to these terminals should also be kept as short as possible. Since the 722 is not internally shielded, external shielding may be appropriate in some applications if RFI at the 900kHz nominal oscillator frequency is a problem. A shield, model 100MS, is available.

Each output is filtered with an internal 0.22μF capacitor. Output ripple voltage can be reduced below the specified value by adding external capacitors up to 10μF between each output and its common.

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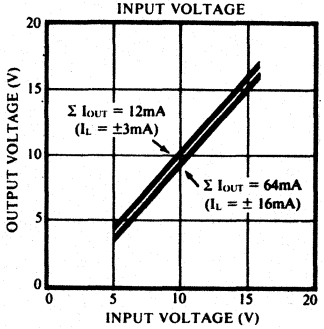
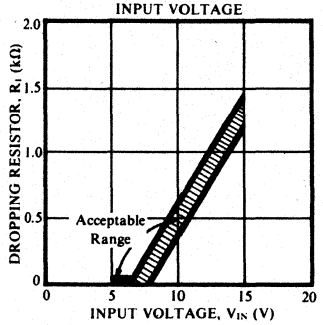
TYPICAL PERFORMANCE CURVES

All specifications typical at 25°C unless otherwise noted.

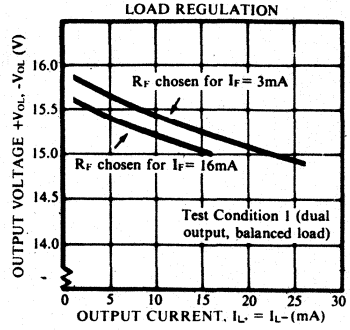
OUTPUT VOLTAGE VS INPUT VOLTAGE



DROPPING RESISTOR VS INPUT VOLTAGE



LOAD REGULATION



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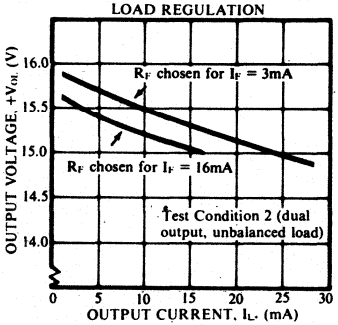
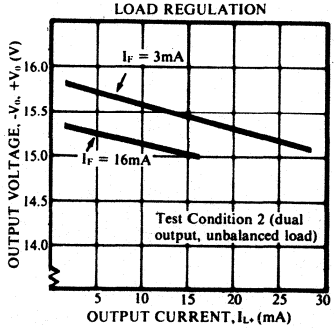


LOAD REGULATION



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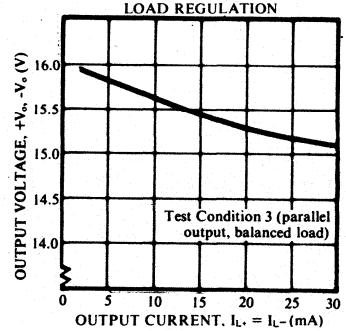

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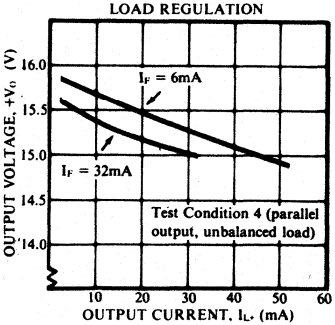

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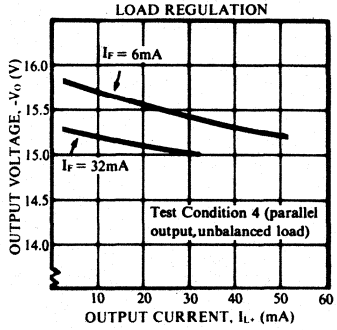
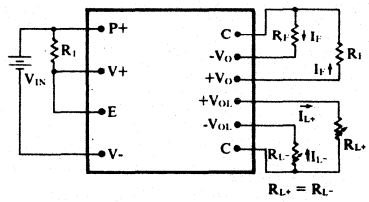
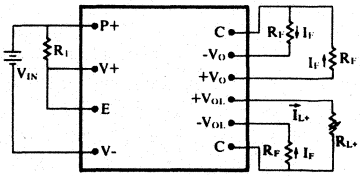


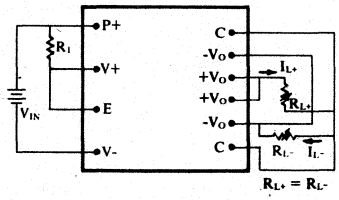
TEST CONDITION 1
(Balanced Load)



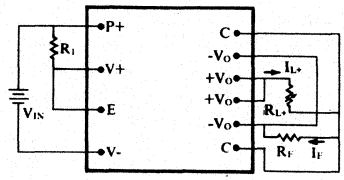
TEST CONDITION 2
(Unbalanced Load)



TEST CONDITION 3
(Parallel Output)



TEST CONDITION 4
(Parallel Output)

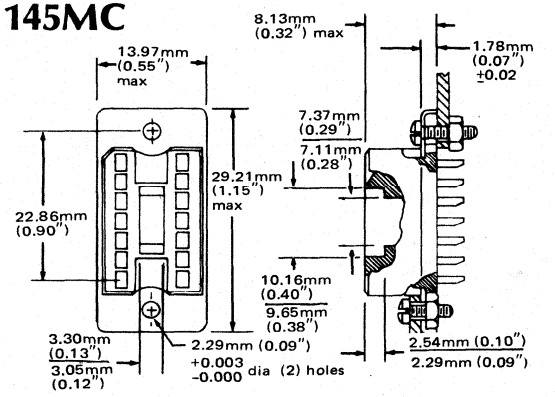


9. ACCESSORIES

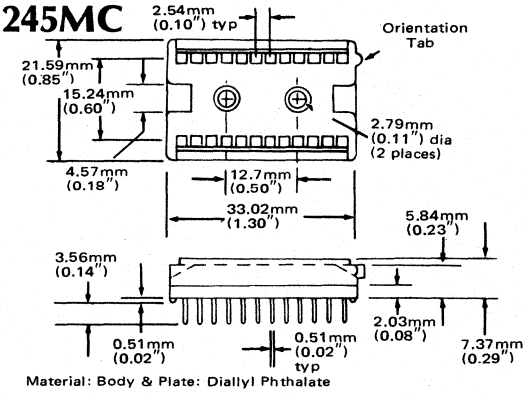
This section contains illustrations and information on the mating connectors and heat sinks available for use with various Burr-Brown products. The type of connector and/or heat sink required by the product is specified within the product data sheet. Prices are available from your nearest Burr-Brown representative.

MATING CONNECTORS

145MC

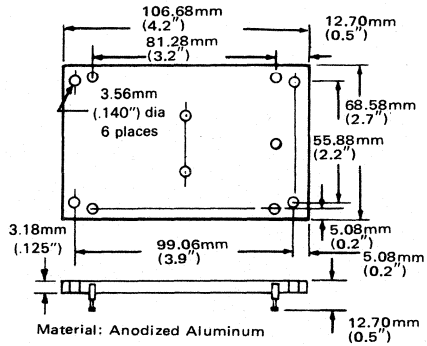


245MC



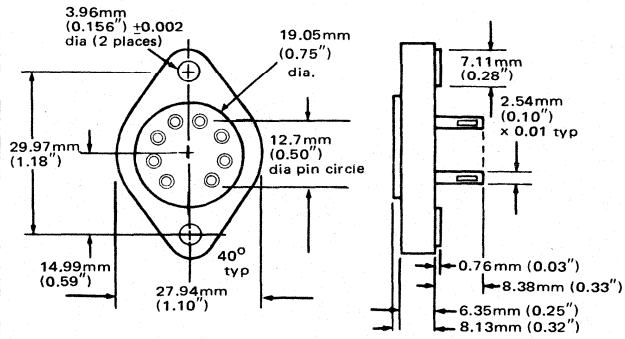
Material: Body & Plate: Diallyl Phthalate

548MC

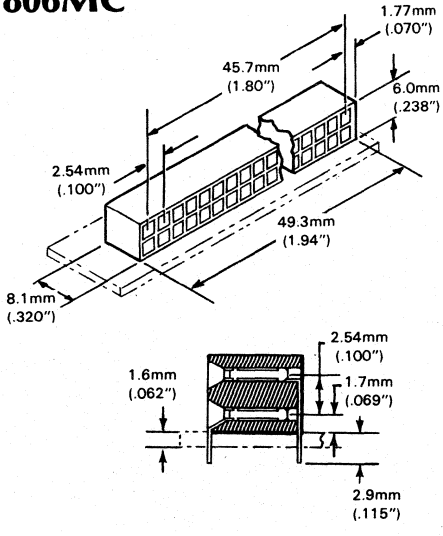


Material: Anodized Aluminum

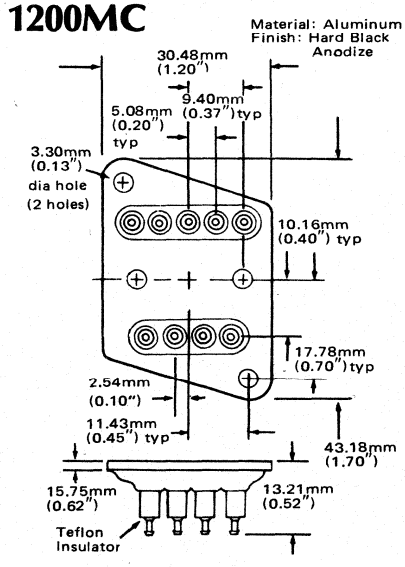
803MC



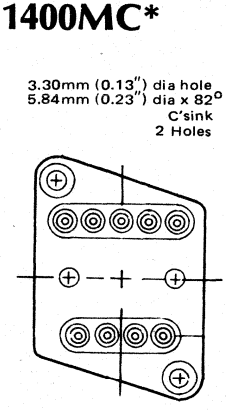
806MC



1200MC



1400MC*



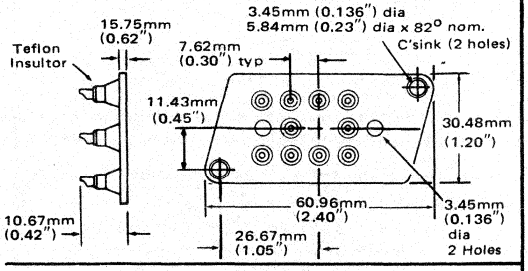
Material: Aluminum
Finish: Hard Black Anodize

* Identical to 1200MC except for mounting holes.

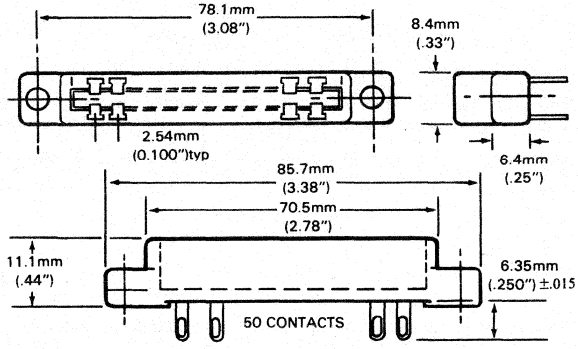
MATING CONNECTORS

1500MC

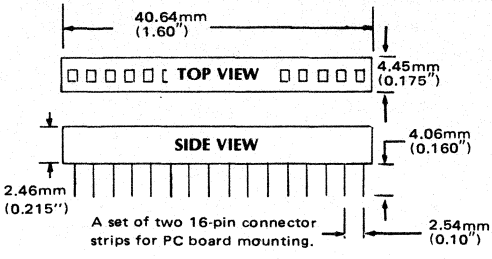
Material: Aluminum
Finish: Hard Black Anodize



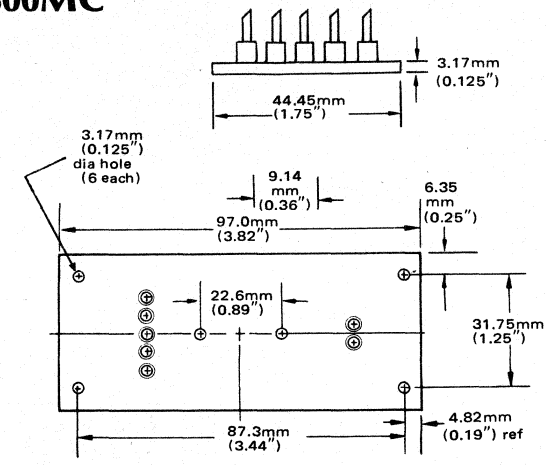
2250MC



2302MC



2800MC

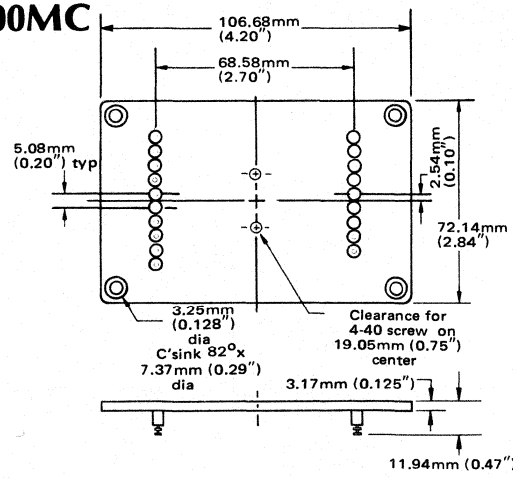


2401MC

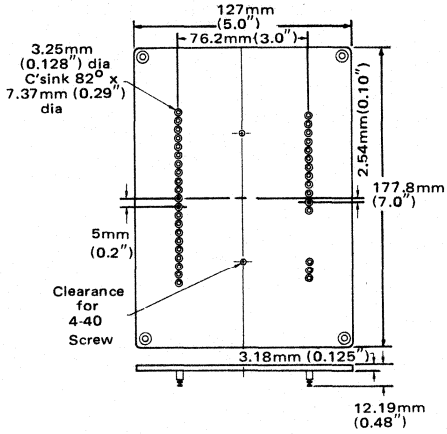
Identical to 2302MC except each connector strip length is 45.72mm (1.80")

A set of four 18-pin connector strips for PC board mounting.

4400MC

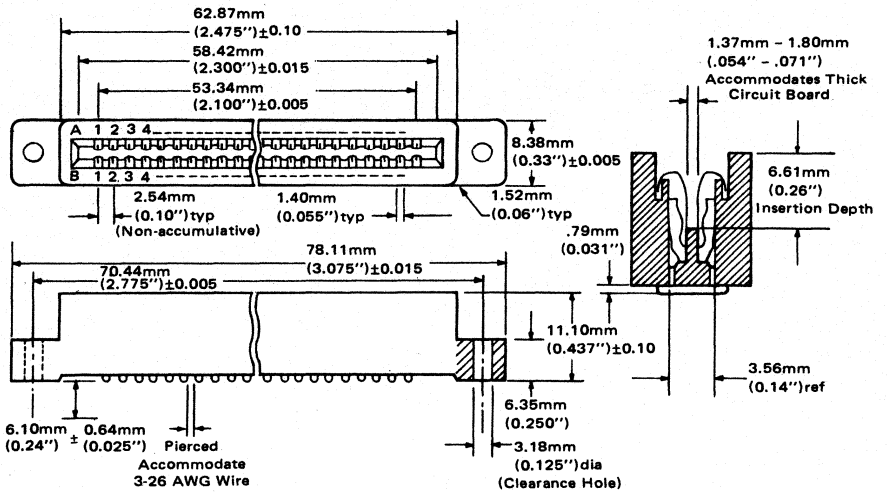


4800MC

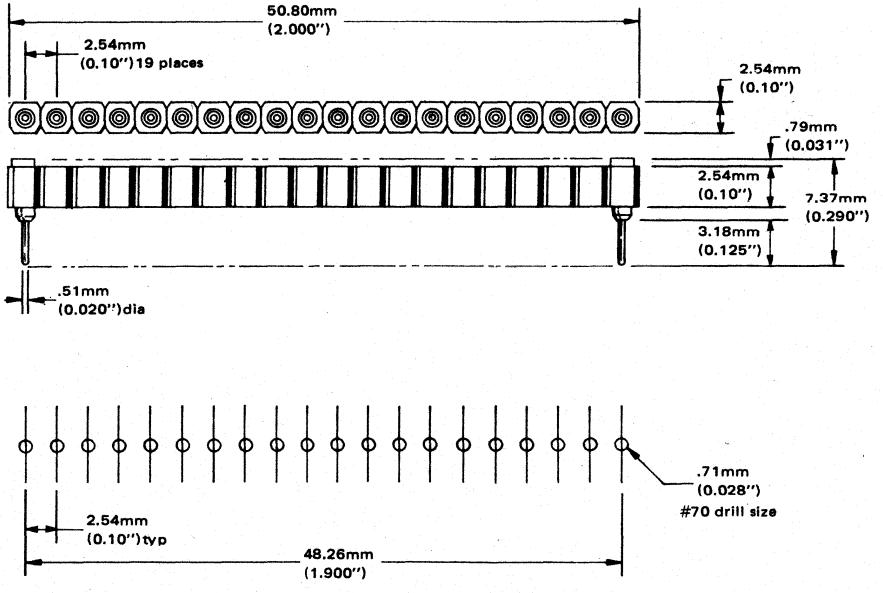


MATING CONNECTORS

2201MC

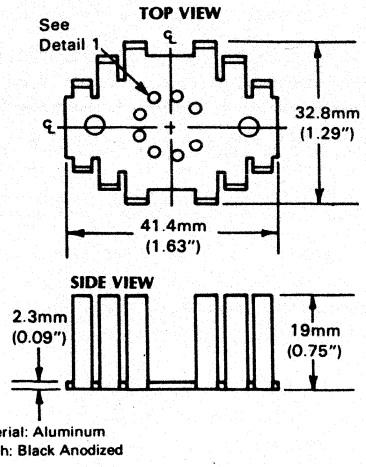


2350MC



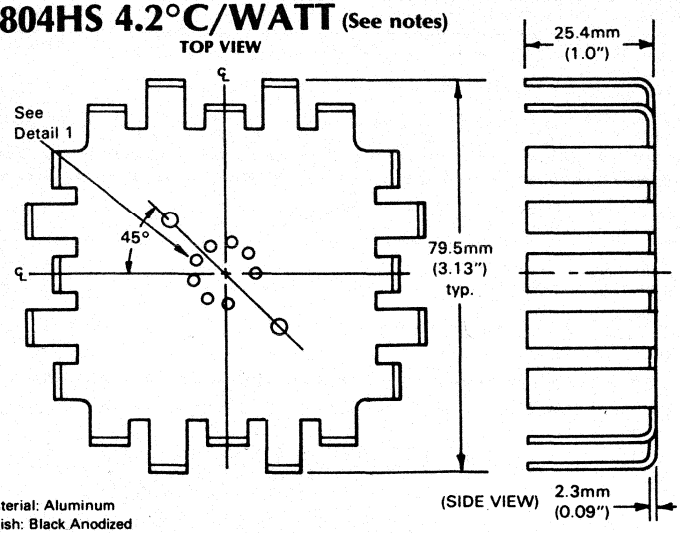
0803HS 12°C/WATT

(See notes)



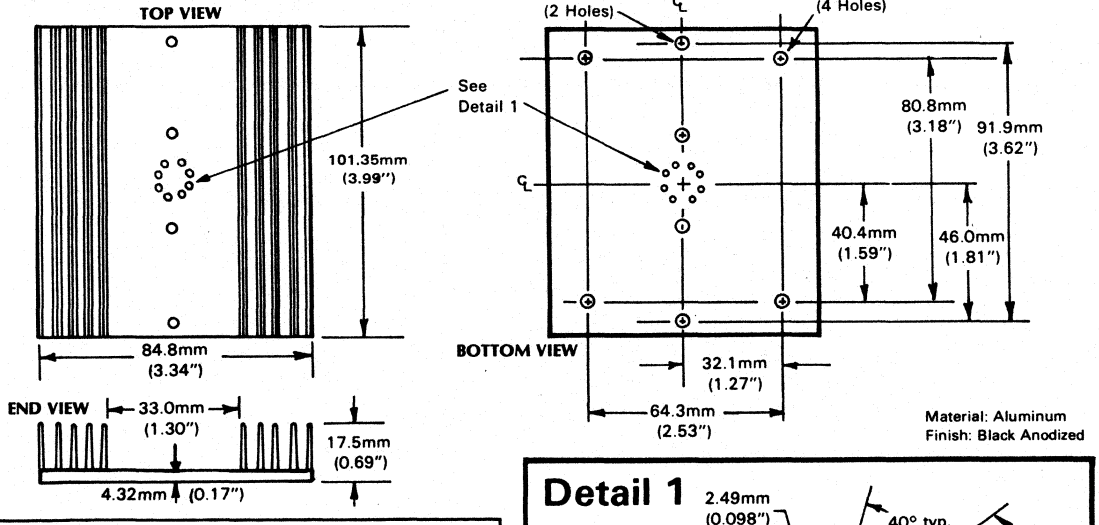
Material: Aluminum
Finish: Black Anodized

0804HS 4.2°C/WATT (See notes)



Material: Aluminum
Finish: Black Anodized

0805HS 3°C/WATT

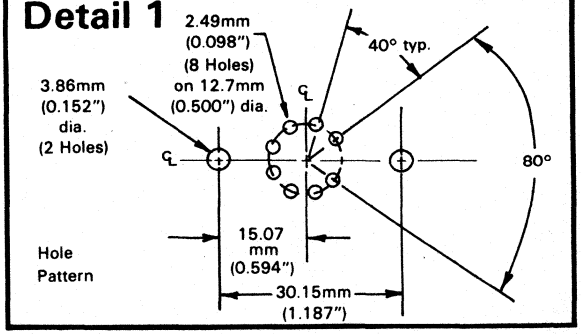


Material: Aluminum
Finish: Black Anodized

***NOTES**

1. Thermal resistance specified are for natural connection. Heatsinks 0803HS and 0804HS are mounted on 6" x 6" x 1/16" G-10 PC board.
2. A thin-film of heatsink compound (Dow Corning 340 or equivalent) between the heatsink and the TO-3 device is recommended.

Detail 1



PEAK DETECTOR
LOG AMPLIFIER